

## SUD50N02-06P

**Vishay Siliconix** 

## N-Channel 20 V (D-S) 175 °C MOSFET

PRODUCT SUMMARY				
V <sub>DS</sub> (V)	<b>R<sub>DS(on)</sub> (</b> Ω <b>)</b>	I <sub>D</sub> (A) <sup>a</sup>		
20	0.0060 at V <sub>GS</sub> = 10 V	26		
	0.0095 at $V_{GS}$ = 4.5 V	21		

Drain Connected to Tab

TO-252

G D s

Top View

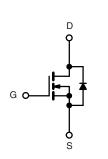
Ordering Information: SUD50N02-06P-E3 (Lead (Pb) free)



- TrenchFET<sup>®</sup> Power MOSFET
- 175 °C Junction Temperature
- PWM Optimized for High Efficiency
- 100 % R<sub>q</sub> Tested
- Compliant to RoHS Directive 2002/95/EC

#### **APPLICATIONS**

- Synchronous Buck DC/DC Conversion
  - Desktop
  - Server



N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS (T	$_{\rm A}$ = 25 °C, unless othe	rwise noted)		
Parameter	Symbol	Limit	Unit	
Drain-Source Voltage	V <sub>DS</sub>	20	v	
Gate-Source Voltage	V <sub>GS</sub>	± 20	v	
	T <sub>A</sub> = 25 °C		26 <sup>a</sup>	
Continuous Drain Current <sup>a</sup>	T <sub>C</sub> = 25 °C		50 <sup>b</sup>	
Pulsed Drain Current	I <sub>DM</sub>	100	А	
Continuous Source Current (Diode Conduction) <sup>a</sup>	۱ <sub>S</sub>	26		
Avalanche Current	L = 0.1 mH	I <sub>AS</sub>	45	
Single Pulse Avalanche Energy	L = 0.1 IIIH	E <sub>AS</sub>	101	mJ
Maximum Power Dissipation	T <sub>A</sub> = 25 °C	P <sub>D</sub>	6.8 <sup>a</sup>	w
Maximum rower Dissipation	T <sub>C</sub> = 25 °C		65	vv
Operating Junction and Storage Temperature Range	T <sub>J</sub> , T <sub>stg</sub>	- 55 to 175	°C	

THERMAL RESISTANCE RATINGS							
Parameter		Symbol	Typical	Maximum	Unit		
Maximum hundling to Angleingtâ	t ≤ 10 s	R <sub>thJA</sub>	18	22	°C/W		
Maximum Junction-to-Ambient <sup>a</sup>	Steady State		40	50			
Maximum Junction-to-Case		R <sub>thJC</sub>	1.9	2.3			

Notes:

a. Surface mounted on FR4 board, t  $\leq$  10 s.

b. Limited by package.



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## SUD50N02-06P

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Parameter	Symbol	Test Conditions	Min.	Typ. <sup>a</sup>	Max.	Unit	
Static	1 -		I.	,,,	I I		
Drain-Source Breakdown Voltage	V <sub>DS</sub>	V <sub>GS</sub> = 0 V, I <sub>D</sub> = 250 μA	20			v	
Gate Threshold Voltage	V <sub>GS(th)</sub>	$V_{DS} = V_{GS}, I_{D} = 250 \ \mu A$	0.8		3	V	
Gate-Body Leakage	I <sub>GSS</sub>	$V_{DS} = 0 V, V_{GS} = \pm 20 V$			± 100	nA	
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> = 20 V, V <sub>GS</sub> = 0 V V <sub>DS</sub> = 20 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 125 °C			1	μA	
On-State Drain Current <sup>b</sup>	I <sub>D(on)</sub>	$v_{DS} = 20 \text{ v}, v_{GS} = 0 \text{ v}, T_{J} = 125 \text{ C}$ $V_{DS} = 5 \text{ V}, V_{GS} = 10 \text{ V}$	50		50	A	
	D(01)	$V_{GS} = 10 \text{ V}, \text{ I}_{D} = 20 \text{ A}$		0.0046	0.006		
Drain-Source On-State Resistance <sup>b</sup>	r <sub>DS(on)</sub>	$V_{GS} = 10 \text{ V}, \text{ I}_{D} = 20 \text{ A}, \text{ T}_{J} = 125 \text{ °C}$			0.0084	Ω	
		V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 20 A		0.0073	0.0095		
Forward Transconductance <sup>b</sup>	9 <sub>fs</sub>	V <sub>DS</sub> = 15 V, I <sub>D</sub> = 20 A	15			S	
Dynamic <sup>a</sup>			•	•			
Input Capacitance	C <sub>iss</sub>			2550		pF	
Output Capacitance	C <sub>oss</sub>	V <sub>GS</sub> = 0 V, V <sub>DS</sub> = 10 V, f = 1 MHz		900			
Reverse Transfer Capacitance	C <sub>rss</sub>			415			
Total Gate Charge <sup>c</sup>	Qg			19	30	nC	
Gate-Source Charge <sup>c</sup>	Q <sub>gs</sub>	$V_{DS}$ = 10 V, $V_{GS}$ = 4.5 V, $I_{D}$ = 50 A		7.5			
Gate-Drain Charge <sup>c</sup>	Q <sub>gd</sub>			6		1	
Gate Resistance	R <sub>g</sub>		0.5	1.5	2.4	Ω	
Turn-On Delay Time <sup>c</sup>	t <sub>d(on)</sub>			11	20		
Rise Time <sup>c</sup>	t <sub>r</sub>	$V_{DD}$ = 10 V, $R_L$ = 0.2 $\Omega$		10	15	ns	
Turn-Off Delay Time <sup>c</sup>	t <sub>d(off)</sub>	$\text{I}_\text{D}{\cong}50$ A, $\text{V}_\text{GEN}$ = 10 V, $\text{R}_\text{G}$ = 2.5 $\Omega$		24	35		
Fall Time <sup>c</sup>	t <sub>f</sub>			9	15		
Source-Drain Diode Ratings and Cha	racteristic (T	<sub>C</sub> = 25 °C)					
Pulsed Current	I <sub>SM</sub>				100	А	
Diode Forward Voltage <sup>b</sup>	V <sub>SD</sub>	I <sub>F</sub> = 50 A, V <sub>GS</sub> = 0 V		1.2	1.5	V	
Source-Drain Reverse Recovery Time	t <sub>rr</sub>	I <sub>F</sub> = 50 A, dl/dt = 100 A/μs		35	70	ns	

Notes:

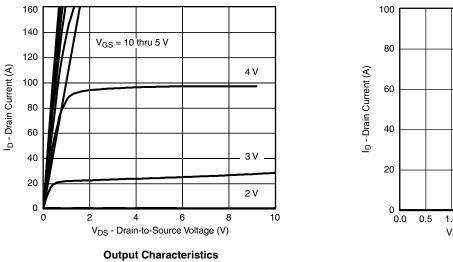
a. Guaranteed by design, not subject to production testing.

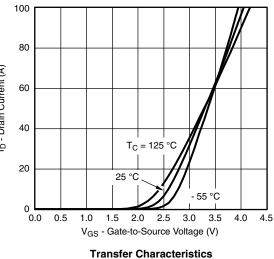
b. Pulse test; pulse width  $\leq$  300 µs, duty cycle  $\leq$  2 %.

c. Independent of operating temperature.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

#### TYPICAL CHARACTERISTICS (25 °C unless noted)





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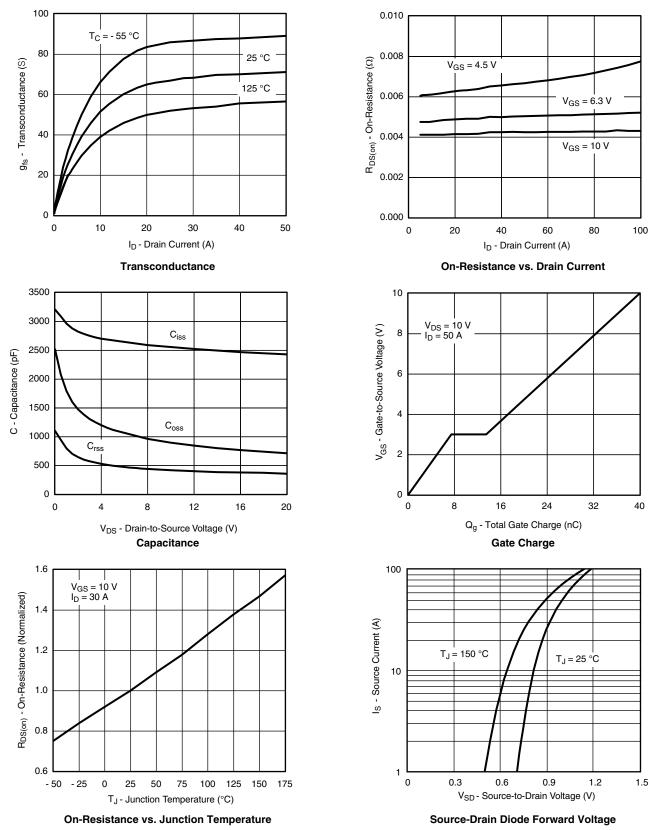
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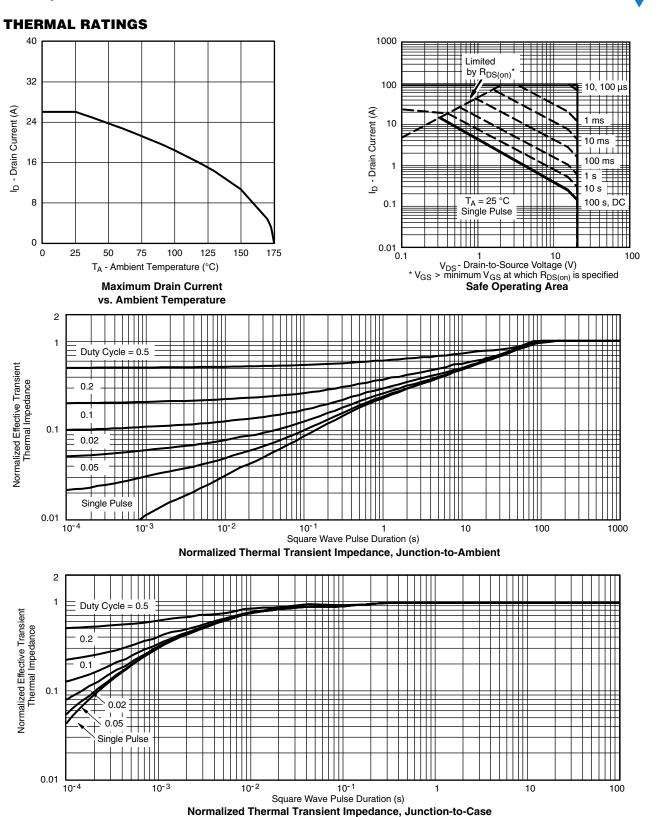
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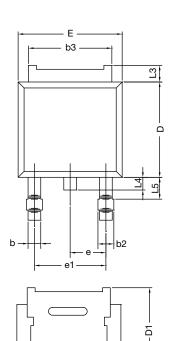
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**TO-252AA** Case Outline

	MILLIN	<b>IETERS</b>	INCHES		
DIM.	MIN.	MAX.	MIN.	MAX.	
А	2.18	2.38	0.086	0.094	
A1	-	0.127	-	0.005	
b	0.64	0.88	0.025	0.035	
b2	0.76	1.14	0.030	0.045	
b3	4.95	5.46	0.195	0.215	
С	0.46	0.61	0.018	0.024	
C2	0.46	0.89	0.018	0.035	
D	5.97	6.22	0.235	0.245	
D1	4.10	-	0.161	-	
E	6.35	6.73	0.250	0.265	
E1	4.32	-	0.170	-	
Н	9.40	10.41	0.370	0.410	
е	2.28	BSC	0.090 BSC		
e1	4.56	BSC	0.180 BSC		
L	1.40	1.78	0.055	0.070	
L3	0.89	1.27	0.035	0.050	
L4	-	1.02	-	0.040	
L5	1.01	1.52	0.040	0.060	
ECN: T13-0359-Rev. O, 03-Jun-13 DWG: 5347					

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Notes

• Dimension L3 is for reference only.

• Xi'an, Mingxin, and GEM SH actual photo.



Revision: 03-Jun-13

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#### **RECOMMENDED MINIMUM PADS FOR DPAK (TO-252)**



Recommended Minimum Pads Dimensions in Inches/(mm)

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