

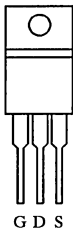
N-Channel Enhancement-Mode Transistor

175°C Maximum Junction Temperature

Product Summary

$V_{(BR)DSS}$ (V)	$r_{DS(on)}$ (Ω)	I_D (A)
60	0.018	48

TO-220AB

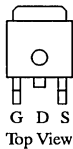


Top View

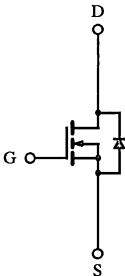
SUP50N06-18

DRAIN connected to TAB

TO-263



SUB50N06-18



N-Channel MOSFET

Absolute Maximum Ratings ($T_C = 25^\circ\text{C}$ Unless Otherwise Noted)

Parameter		Symbol	Limit	Unit
Drain-Source Voltage		V_{DS}	60	V
Gate-Source Voltage		V_{GS}	± 20	
Continuous Drain Current ($T_J = 175^\circ\text{C}$)	$T_C = 25^\circ\text{C}$	I_D	48	A
	$T_C = 100^\circ\text{C}$		34	
Pulsed Drain Current		I_{DM}	240	
Avalanche Current		I_{AR}	60	
Repetitive Avalanche Energy ^a		E_{AR}	90	mJ
Power Dissipation	$T_C = 25^\circ\text{C}$ (TO-220AB and TO-263)	P_D	83	W
	$T_A = 25^\circ\text{C}$ (TO-263) ^b		3.7	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	-55 to 175	$^\circ\text{C}$

Thermal Resistance Ratings

Parameter		Symbol	Limit	Unit
Junction-to-Ambient	PCB Mount (TO-263) ^b	R_{thJA}	40	$^\circ\text{C/W}$
	Free Air (TO-220AB)		80	
Junction-to-Case		R_{thJC}	1.8	

Notes:

a. Duty cycle $\leq 1\%$.

b. When mounted on 1" square PCB (FR-4 material).

Specifications ($T_J = 25^\circ\text{C}$ Unless Otherwise Noted)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Static						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$	60			V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_{DS} = 1\text{ mA}$	2.0	3.0	4.0	
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0\text{ V}, V_{GS} = \pm 20\text{ V}$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 48\text{ V}, V_{GS} = 0\text{ V}$			25	μA
		$V_{DS} = 48\text{ V}, V_{GS} = 0\text{ V}, T_J = 125^\circ\text{C}$			250	
		$V_{DS} = 48\text{ V}, V_{GS} = 0\text{ V}, T_J = 175^\circ\text{C}$			500	
On-State Drain Current ^b	$I_{D(on)}$	$V_{DS} = 5\text{ V}, V_{GS} = 10\text{ V}$	48			A
Drain-Source On-State Resistance ^b	$r_{DS(on)}$	$V_{GS} = 10\text{ V}, I_D = 30\text{ A}$			0.018	Ω
		$V_{GS} = 10\text{ V}, I_D = 30\text{ A}, T_J = 125^\circ\text{C}$			0.030	
		$V_{GS} = 10\text{ V}, I_D = 30\text{ A}, T_J = 175^\circ\text{C}$			0.036	
Forward Transconductance ^b	g_{fs}	$V_{DS} = 15\text{ V}, I_D = 30\text{ A}$				S
Dynamic ^a						
Input Capacitance	C_{iss}	$V_{GS} = 0\text{ V}, V_{DS} = 25\text{ V}, f = 1\text{ MHz}$				pF
Output Capacitance	C_{oss}					
Reversen Transfer Capacitance	C_{rss}					
Total Gate Charge ^c	Q_g	$V_{DS} = 30\text{ V}, V_{GS} = 10\text{ V}, I_D = 48\text{ A}$			100	nC
Gate-Source Charge ^c	Q_{gs}				20	
Gate-Drain Charge ^c	Q_{gd}				50	
Turn-On Delay Time ^c	$t_{d(on)}$	$V_{DD} = 30\text{ V}, R_L = 1\text{ }\Omega$ $I_D \approx 48\text{ A}, V_{GEN} = 10\text{ V}, R_G = 2.5\text{ }\Omega$			30	ns
Rise Time ^c	t_r				35	
Turn-Off Delay Time ^c	$t_{d(off)}$				65	
Fall Time ^c	t_f				30	
Source-Drain Diode Ratings and Characteristics ($T_C = 25^\circ\text{C}$) ^a						
Continuous Current	I_s				48	A
Pulsed Current	I_{SM}				200	
Forward Voltage ^b	V_{SD}	$I_F = 48\text{ A}, V_{GS} = 0\text{ V}$			2.0	V
Reverse Recovery Time	t_{rr}	$I_F = 48\text{ A}, di/dt = 100\text{ A}/\mu\text{s}$				ns
Peak Reverse Recovery Current	$I_{RM(REC)}$					A
Reverse Recovery Charge	Q_{rr}					μC

Notes:

- Guaranteed by design, not subject to production testing.
- Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.
- Independent of operating temperature.