

Automotive N-channel 60 V, 2.3 mΩ typ., 180 A STripFET™ F6 Power MOSFET in a TO-247 package

Datasheet - preliminary data

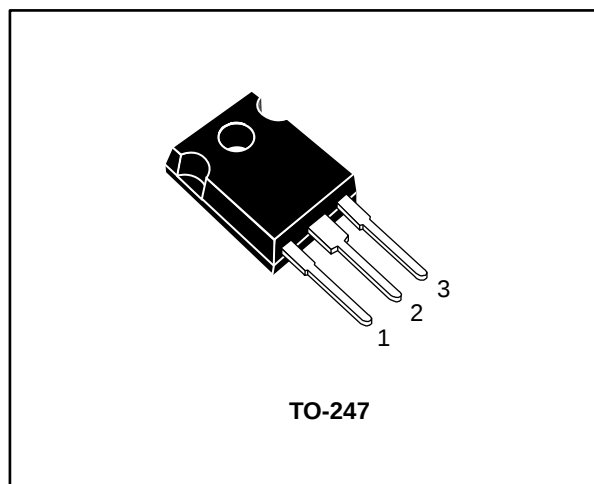
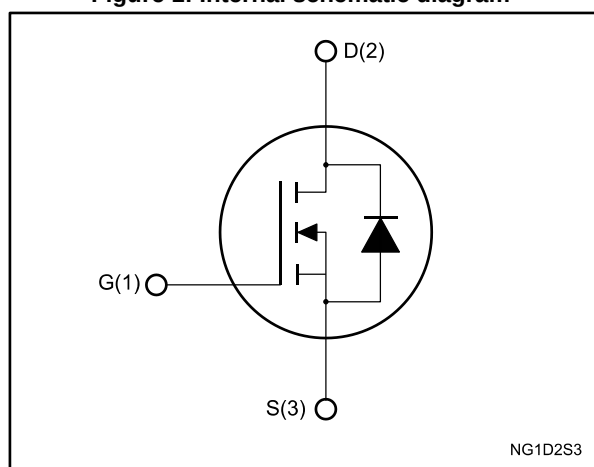


Figure 1: Internal schematic diagram



Features

Order code	V _{DS}	R _{DS(on)} max	I _D
STW265N6F6AG	60 V	2.85 mΩ	180 A

- Designed for automotive applications
- Very low on-resistance
- Very low gate charge
- High avalanche ruggedness
- Low gate drive power loss

Applications

- Switching applications

Description

This device is an N-channel Power MOSFET developed using the STripFET™ F6 technology with a new trench gate structure. The resulting Power MOSFET exhibits very low R_{DS(on)} in all packages.

Table 1: Device summary

Order code	Marking	Package	Packing
STW265N6F6AG	265N6F6	TO-247	Tube

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1 Electrical ratings

Table 2: Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	60	V
V_{GS}	Gate-source voltage	± 20	V
$I_D^{(1)}$	Drain current (continuous) at $T_C = 25\text{ }^{\circ}\text{C}$	180	A
I_D	Drain current (continuous) at $T_C = 100\text{ }^{\circ}\text{C}$	180	A
$I_{DM}^{(2)}$	Drain current (pulsed)	720	A
P_{TOT}	Total dissipation at $T_C = 25\text{ }^{\circ}\text{C}$	300	W
E_{AS}	Single pulse avalanche energy (Starting $T_J = 25\text{ }^{\circ}\text{C}$, $I_D = 80\text{ A}$)	720	mJ
T_{stg}	Storage temperature range	- 55 to 175	$^{\circ}\text{C}$
T_J	Operating junction temperature range		

Notes:

⁽¹⁾Current limited by package.

⁽²⁾ Pulse width limited by safe operating area.

Table 3: Thermal data

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case max	0.5	$^{\circ}\text{C/W}$
$R_{thj-amb}$	Thermal resistance junction-amb max	50	$^{\circ}\text{C/W}$

2 Electrical characteristics

(T_{CASE} = 25 °C unless otherwise specified)

Table 4: On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V _{(BR)DSS}	Drain-source breakdown voltage	I _D = 250 μA, V _{GS} = 0 V	60			V
I _{DSS}	Zero gate voltage drain current	V _{DS} = 60 V, V _{GS} = 0 V			1	μA
		V _{DS} = 60 V, T _C = 125 °C ⁽¹⁾ V _{GS} = 0 V			100	μA
I _{GSS}	Gate-body leakage current	V _{GS} = ± 20 V, V _{DS} = 0 V			± 100	nA
V _{GS(th)}	Gate threshold voltage	V _{DS} = V _{GS} , I _D = 250 μA	2		4	V
R _{DS(on)}	Static drain-source on-resistance	V _{GS} = 10 V, I _D = 60 A		2.3	2.85	mΩ

Notes:

⁽¹⁾Defined by design, not subject to production test.

Table 5: Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C _{iss}	Input capacitance	V _{DS} = 25 V, f = 1 MHz, V _{GS} = 0 V	-	11800	-	pF
C _{oss}	Output capacitance		-	1235	-	pF
C _{rss}	Reverse transfer capacitance		-	488	-	pF
Q _g	Total gate charge	V _{DD} = 30 V, I _D = 120 A, V _{GS} = 10 V (see Figure 14: "Test circuit for gate charge behavior")	-	183	-	nC
Q _{gs}	Gate-source charge		-	53	-	nC
Q _{gd}	Gate-drain charge		-	41	-	nC

Table 6: Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
t _{d(on)}	Turn-on delay time	V _{DD} = 30 V, I _D = 60 A R _G = 4.7 Ω, V _{GS} = 10 V (see Figure 13: "Test circuit for resistive load switching times" and Figure 18: "Switching time waveform")	-	31	-	ns
t _r	Rise time		-	165	-	ns
t _{d(off)}	Turn-off-delay time		-	144	-	ns
t _f	Fall time		-	63	-	ns

Table 7: Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current				180	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)				720	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 180\text{ A}$, $V_{GS} = 0\text{ V}$			1.1	V
t_{rr}	Reverse recovery time	$I_{SD} = 120\text{ A}$, $V_{DD} = 48\text{ V}$ $di/dt = 100\text{ A}/\mu\text{s}$, $T_J = 150\text{ }^\circ\text{C}$ (see Figure 15: "Test circuit for inductive load switching and diode recovery times")	-	56	-	ns
Q_{rr}	Reverse recovery charge		-	116	-	nC
I_{RRM}	Reverse recovery current		-	3.8	-	A

Notes:

⁽¹⁾ Pulse width limited by safe operating area.

⁽²⁾ Pulsed: pulse duration = 300 μs , duty cycle 1.5%.

2.1 Electrical characteristics (curves)

Figure 2: Safe operating area

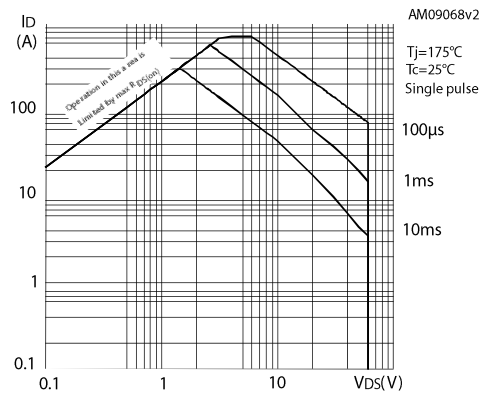


Figure 3: Thermal impedance

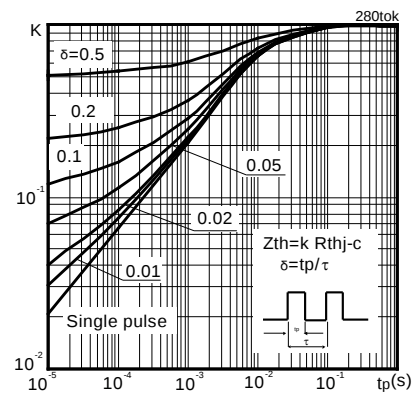


Figure 4: Output characteristics

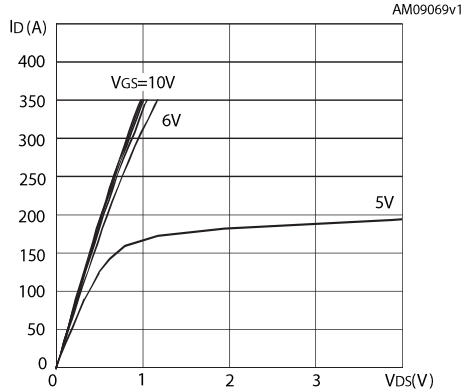


Figure 5: Transfer characteristics

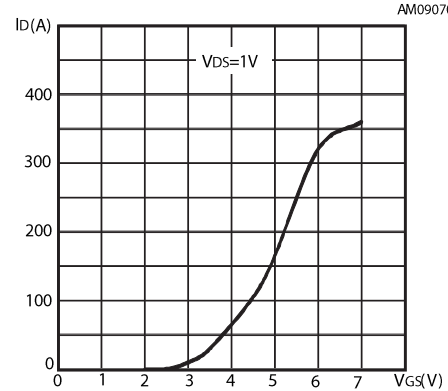
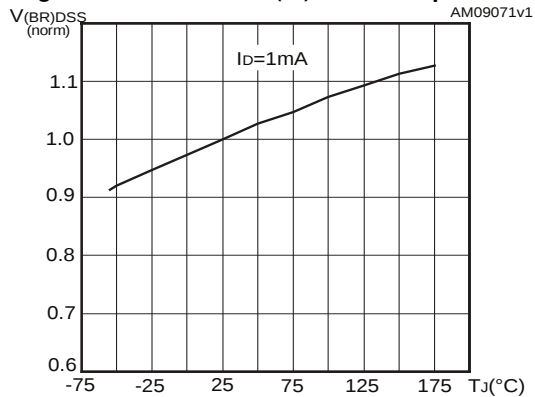
Figure 6: Normalized $V_{(BR)DSS}$ vs. temperature

Figure 7: Static drain-source on-resistance

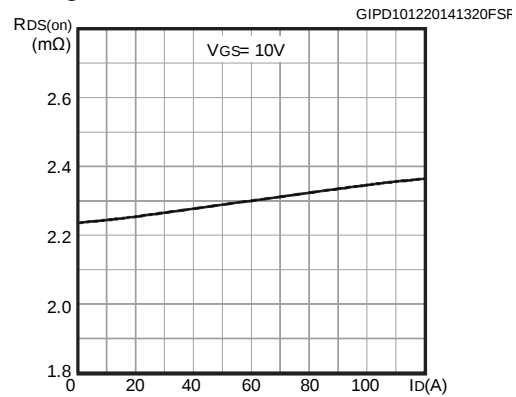


Figure 8: Gate charge vs. gate-source voltage

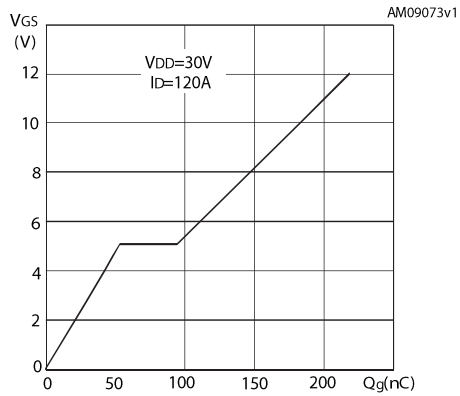


Figure 9: Capacitance variations

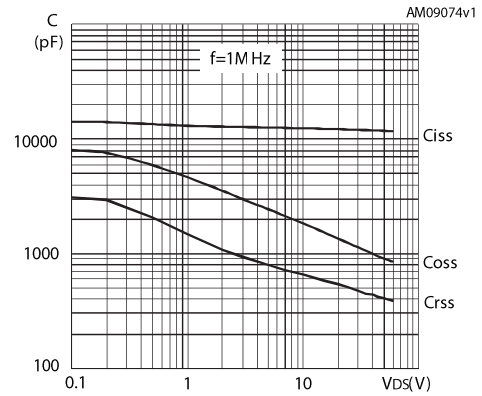


Figure 10: Normalized gate threshold voltage vs. temperature

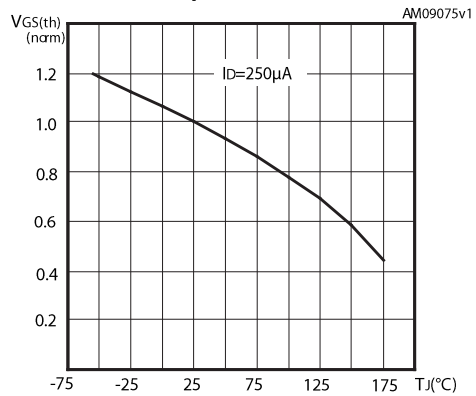


Figure 11: Normalized on resistance vs. temperature

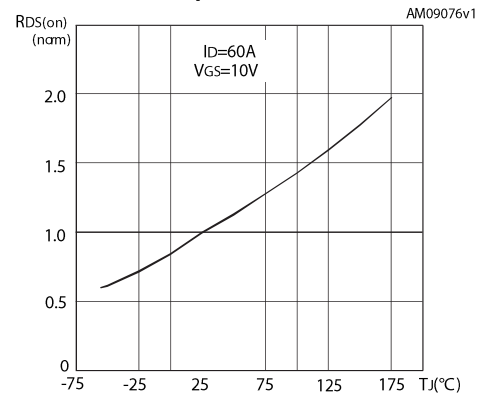
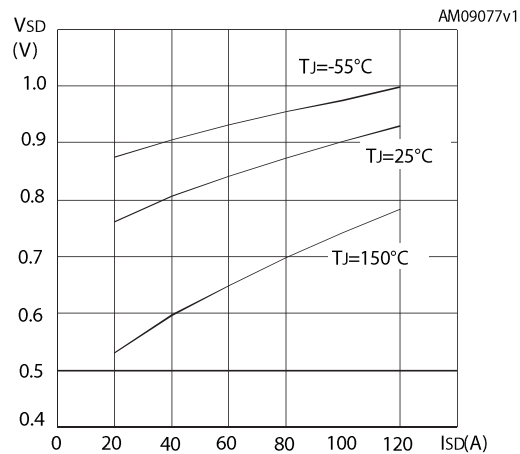
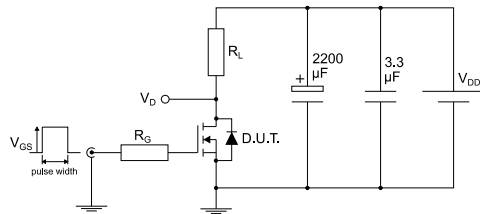


Figure 12: Source-drain diode forward characteristics



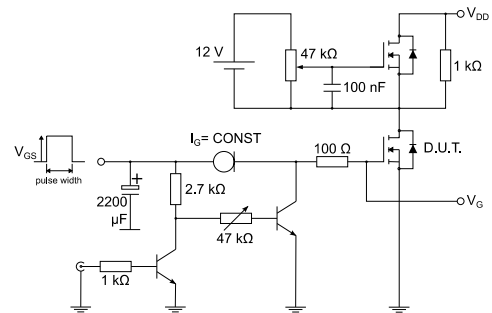
3 Test circuits

Figure 13: Test circuit for resistive load switching times



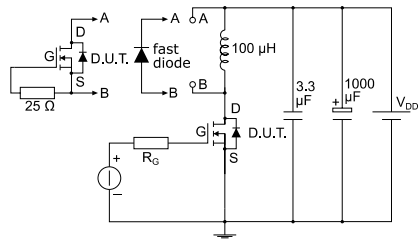
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Figure 14: Test circuit for gate charge behavior



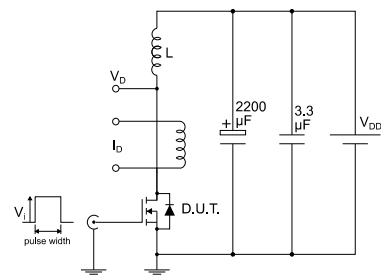
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Figure 15: Test circuit for inductive load switching and diode recovery times



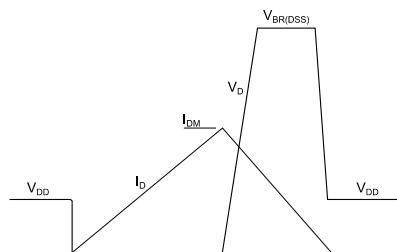
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Figure 16: Unclamped inductive load test circuit



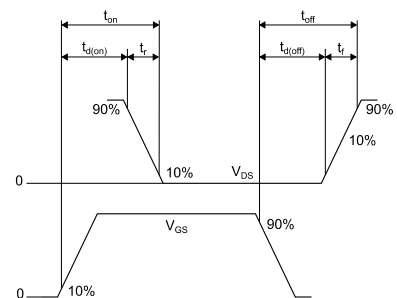
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Figure 17: Unclamped inductive waveform



AM01472v1

Figure 18: Switching time waveform



AM01473v1

4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

4.1 TO-247 package information

Figure 19: TO-247 package outline

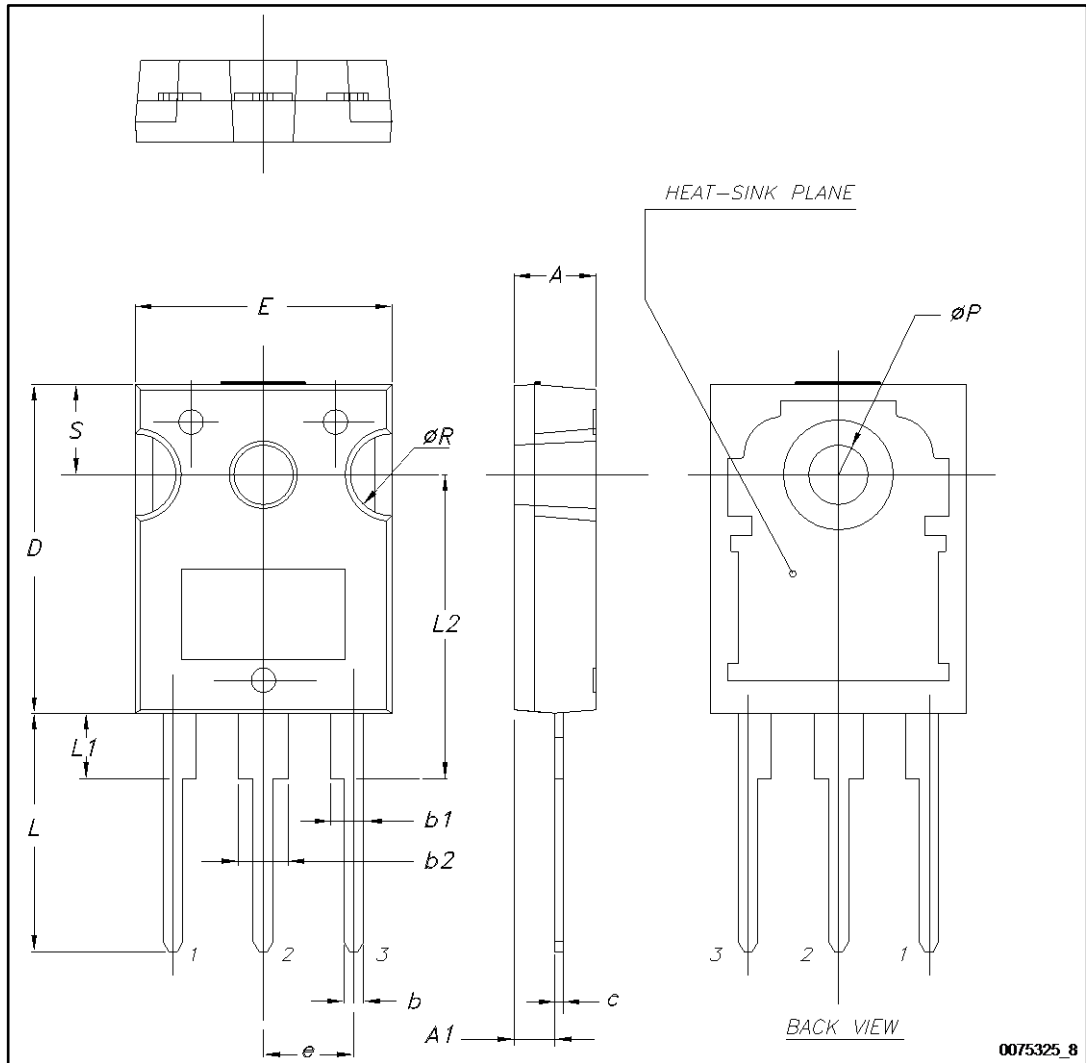


Table 8: TO-247 package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.85		5.15
A1	2.20		2.60
b	1.0		1.40
b1	2.0		2.40
b2	3.0		3.40
c	0.40		0.80
D	19.85		20.15
E	15.45		15.75
e	5.30	5.45	5.60
L	14.20		14.80
L1	3.70		4.30
L2		18.50	
ØP	3.55		3.65
ØR	4.50		5.50
S	5.30	5.50	5.70

5 Revision history

Table 9: Document revision history

Date	Revision	Changes
16-Nov-2016	1	First release

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