



**STV5348**

## MONOCHIP TELETEXT AND VPS DECODER WITH 8 INTEGRATED PAGES

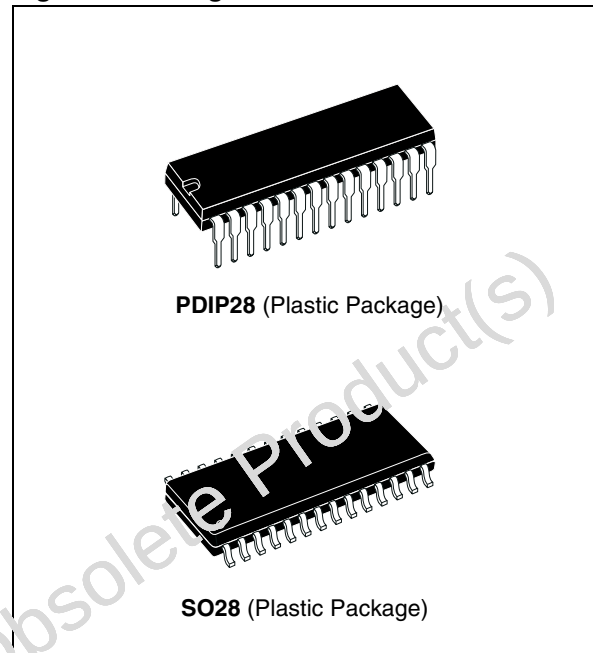
### FEATURES SUMMARY

- COMPLETE TELETEXT AND VPS DECODER INCLUDING AN 8 PAGE MEMORY ON A SINGLE CHIP
- UPWARD SOFTWARE COMPATIBLE WITH PREVIOUS ST's MULTICHIP SOLUTIONS (SAA5231, SDA5243, STV5345)
- PERFORM PDC SYSTEM A (VPS) AND PDC SYSTEM B (8/30/2) DATA STORAGE SEPARATELY
- DEDICATED "ERROR FREE" OUTPUT FOR VALID PDC DATA
- INDICATION OF LINE 23 FOR EXTERNAL USE
- SINGLE +5V SUPPLY VOLTAGE
- SINGLE 13.875MHz CRYSTAL
- REDUCED SET OF EXTERNAL COMPONENTS, NO EXTERNAL ADJUSTMENT
- OPTIMIZED NUMBER OF DIGITAL SIGNALS REDUCING EMC RADIATION
- HIGH DENSITY CMOS TECHNOLOGY
- DIGITAL DATA SLICER AND DISPLAY CLOCK PHASE LOCK LOOP
- 28 PIN DIP & SO PACKAGE

### DESCRIPTION

The STV5348 decoder is a computer-controlled teletext device including an 8 page internal memory. Data slicing and capturing extracts the teletext information embedded in the composite video signal. Control is accomplished via a two wire serial I<sup>2</sup>C bus®. Chip address is 22h. Internal ROM provides a character set suitable to display text using up to seven national languages. Hardware and software features allow selectable master/slave synchronization configurations. The STV5348 also supports facilities for reception and display of current level protocol data.

**Figure 1. Package**



**Figure 2. Pin Connections**

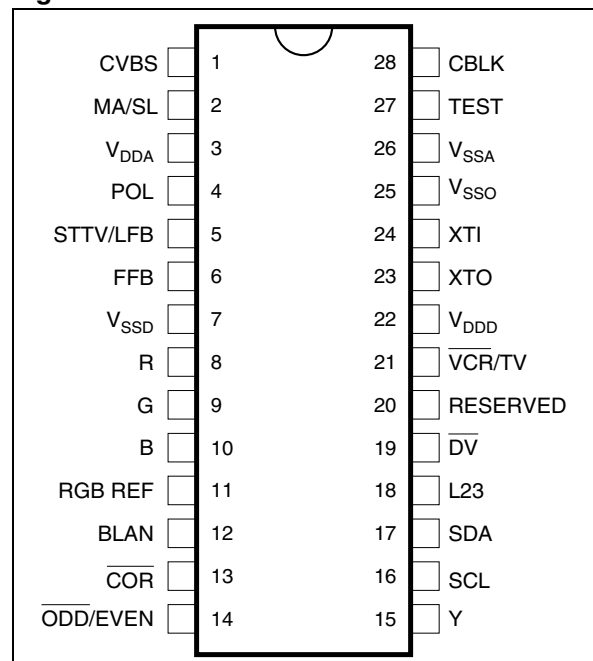


Table 1. Pin Description

| Pin No | Symbol                        | Function       | Description                                               | Figure |
|--------|-------------------------------|----------------|-----------------------------------------------------------|--------|
| 1      | CVBS                          | Input          | Composite Video Signal Input through Coupling Capacitor   | 12     |
| 2      | MA/SL                         | Input          | Master/Slave Selection Mode                               | 14     |
| 3      | V <sub>DDA</sub>              | Analog Supply  | +5V                                                       | -      |
| 4      | POL                           | Input          | STTV / LFB / FFB Polarity Selection                       | 15     |
| 5      | STTV/LFB                      | Output / Input | Composite Sync Output, Line Flyback Input                 | 18     |
| 6      | FFB                           | Input          | Field Flyback Input                                       | 15     |
| 7      | VSSD                          | Ground         | Digital Ground                                            | -      |
| 8      | R                             | Output         | Video Red Signal                                          | 16     |
| 9      | G                             | Output         | Video Green Signal                                        | 16     |
| 10     | B                             | Output         | Video Blue Signal                                         | 16     |
| 11     | RGBREF                        | Supply         | DC Voltage to define RGB High Level                       | 16     |
| 12     | BLAN                          | Output         | Fast Blanking Output TTL Level                            | 18     |
| 13     | COR                           | Output         | Open Drain Contrast Reduction Output                      | 18     |
| 14     | $\overline{\text{ODD}}$ /EVEN | Output         | 25Hz Output Field synchronized for non-interlaced display | 18     |
| 15     | Y                             | Output         | Open Drain Foreground Information Output                  | 18     |
| 16     | SCL                           | Input          | Serial Clock Input                                        | 19     |
| 17     | SDA                           | Input/ Output  | Serial Data Input/Output                                  | 20     |
| 18     | L23                           | Output         | Line 23 Identification                                    | 18     |
| 19     | DV                            | Output         | VPS Data Valid                                            | 18     |
| 20     | RESERVED                      | Test           | To be connected to VSSD through a resistor                | 18     |
| 21     | VCR/TV                        | Input          | PLL Time Constant Selection                               | 18     |
| 22     | V <sub>DD</sub> D             | Digital Supply | +5V                                                       | -      |
| 23     | XTO                           | Crystal Output | Oscillator Output 13.875MHz                               | 17     |
| 24     | XTI                           | Crystal Input  | Oscillator Input 13.875MHz                                | 17     |
| 25     | VSSO                          | Ground         | Oscillator Ground                                         | -      |
| 26     | V <sub>SSA</sub>              | Ground         | Analog Ground                                             | -      |
| 27     | TEST                          | Test           | Grounded to V <sub>SSA</sub>                              | 14     |
| 28     | CBLK                          | Input / Output | To connect Black Level Storage Capacitor                  | 13     |

Figure 3. Block Diagram

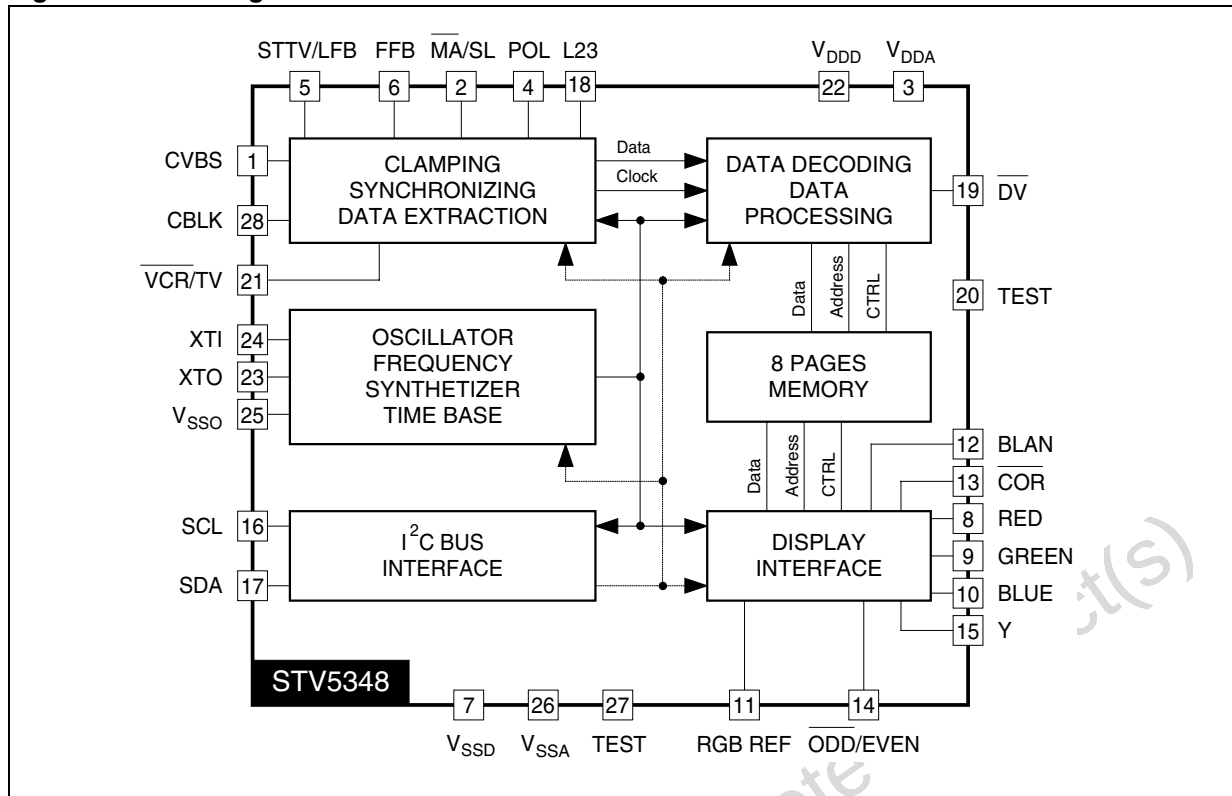


Table 2. Absolute Maximum Ratings

| Symbol            | Parameter                                                       | Value                       | Unit |
|-------------------|-----------------------------------------------------------------|-----------------------------|------|
| V <sub>DD</sub>   | Positive Supply Voltage on V <sub>DD</sub> and V <sub>DDA</sub> | -0.3, 6.0                   | V    |
| V <sub>I</sub>    | Input Voltage (any input)                                       | -0.3, V <sub>DD</sub> + 0.5 | V    |
| V <sub>O</sub>    | Output Voltage (any output)                                     | -0.3, V <sub>DD</sub> + 0.5 | V    |
| ΔV <sub>DD</sub>  | Difference between V <sub>DD</sub> , V <sub>DDA</sub>           | 0.25                        | V    |
| T <sub>oper</sub> | Operating Ambient Temperature                                   | 0, +70                      | °C   |
| T <sub>stg</sub>  | Storage Temperature                                             | -40, +150                   | °C   |

**ELECTRICAL CHARACTERISTICS**(V<sub>DD</sub> = 5V, V<sub>SS</sub> = 0V, T<sub>A</sub> = 25°C)**Table 3. Supplies**

| Symbol           | Parameter                           | Min. | Typ. | Max. | Unit |
|------------------|-------------------------------------|------|------|------|------|
| V <sub>DD</sub>  | Supply Voltage                      | 4.75 | 5.0  | 5.25 | V    |
| I <sub>DDD</sub> | V <sub>DDD</sub> Pin Supply Current |      | 30   |      | mA   |
| I <sub>DDA</sub> | V <sub>DDA</sub> Pin Supply Current |      | 5    |      | mA   |

**Table 4. Inputs**

| Symbol                          | Parameter                                                       | Min.                  | Typ.            | Max.                  | Unit |
|---------------------------------|-----------------------------------------------------------------|-----------------------|-----------------|-----------------------|------|
| CBLK                            |                                                                 |                       |                 |                       |      |
| I <sub>BLKO</sub>               | Source Current (V <sub>CBLK</sub> = 2V, V <sub>CVBS</sub> = 0V) | 4.75                  | 5.0             | 5.25                  | V    |
| I <sub>BLKI</sub>               | Sink Current (V <sub>CBLK</sub> = 2V, V <sub>CVBS</sub> = 1V)   |                       | 30              |                       | mA   |
| CVBS                            |                                                                 |                       |                 |                       |      |
| CVBSI                           | Video Input Amplitude (peak to peak)                            |                       | 1               |                       | V    |
| CVBSC                           | Input Capacitance                                               |                       |                 | 10                    | pF   |
| t <sub>SYNC</sub>               | Delay from CVBS to TCS Output from STTV Pin                     |                       | 200             |                       | ns   |
| V <sub>CLAMP</sub>              | Clamping Level at Synchro Pulse                                 |                       | 0               |                       | mV   |
| I <sub>CLPH</sub>               | High Level Clamp Current (CVBS = V <sub>CLAMP</sub> + 1V)       |                       | 5               |                       | μA   |
| I <sub>CLPL</sub>               | Low Level Clamp Current (CVBS = V <sub>CLAMP</sub> - 0.3V)      |                       | -400            |                       | μA   |
| MA/SL, POL, LFB, FFB, VCR/TV    |                                                                 |                       |                 |                       |      |
| V <sub>IL</sub>                 | Input Voltage Low Level                                         | -0.3                  |                 | +0.8                  | V    |
| V <sub>IH</sub>                 | Input Voltage High Level                                        | 2                     |                 | V <sub>DD</sub>       | V    |
| I <sub>IL</sub>                 | Input Leakage Current (V <sub>I</sub> = 0 to V <sub>DD</sub> )  | -10                   |                 | +10                   | μA   |
| C <sub>I</sub>                  | Input Capacitance                                               |                       |                 | 10                    | pF   |
| SCL, SDA                        |                                                                 |                       |                 |                       |      |
| V <sub>IL</sub>                 | Input Voltage Low Level                                         | -0.3                  |                 | +1.5                  | V    |
| V <sub>IH</sub>                 | Input Voltage High Level                                        | 3                     |                 | V <sub>DD</sub>       | V    |
| I <sub>IL</sub>                 | Input Leakage Current (V <sub>I</sub> = 0 to V <sub>DD</sub> )  | -10                   |                 | +10                   | μA   |
| f <sub>SCL</sub>                | Clock Frequency (SCL)                                           |                       |                 | 100                   | kHz  |
| t <sub>R</sub> , t <sub>F</sub> | Input Rise and Fall Time (10 to 90%)                            |                       |                 | 2                     | μs   |
| C <sub>I</sub>                  | Input Capacitance                                               |                       |                 | 10                    | pF   |
| RGB REF                         |                                                                 |                       |                 |                       |      |
| V <sub>I</sub>                  | Input Voltage                                                   | V <sub>DD</sub> -0.5V | V <sub>DD</sub> | V <sub>DD</sub> +0.3V | V    |
| I <sub>I</sub>                  | Input Current                                                   |                       |                 | 50                    | mA   |

Table 5. Outputs

| Symbol                                                     | Parameter                                                                         | Min.           | Typ. | Max.     | Unit          |
|------------------------------------------------------------|-----------------------------------------------------------------------------------|----------------|------|----------|---------------|
| RGB                                                        |                                                                                   |                |      |          |               |
| $V_{OL}$                                                   | Output Low Voltage ( $I_{OL} = 2\text{mA}$ )                                      |                |      | 0.4      | V             |
| $V_{OH}$                                                   | Output High Voltage ( $I_{OH} = -2\text{mA}$ , RGB REF = $V_{DD}/2$ )             | RGB REF – 0.5  |      | RGB REF  | V             |
| $C_L$                                                      | Load Capacitance                                                                  |                |      | 50       | pF            |
| $t_R, t_F$                                                 | Rise and Fall Time (10 to 90%)                                                    |                |      | 20       | ns            |
| BLAN                                                       |                                                                                   |                |      |          |               |
| $V_{OL}$                                                   | Output Low Voltage ( $I_{OL} = 2\text{mA}$ )                                      | 0              |      | 0.4      | V             |
| $V_{OH}$                                                   | Output High Voltage ( $I_{OH} = -0.2\text{mA}$ )                                  | $V_{DD} - 0.5$ |      |          | V             |
| $C_L$                                                      | Load Capacitance                                                                  |                |      | 50       | pF            |
| $t_R, t_F$                                                 | Rise and Fall Time (10 to 90%)                                                    |                |      | 20       | ns            |
| $\overline{ODD}/\text{EVEN}$ , STTV, L23, $\overline{DV}$  |                                                                                   |                |      |          |               |
| $V_{OL}$                                                   | Output Low Voltage ( $I_{OL} = 2\text{mA}$ )                                      | 0              |      | 0.5      | V             |
| $V_{OH}$                                                   | Output High Voltage ( $I_{OH} = -0.2\text{mA}$ )                                  | $V_{DD} - 0.8$ |      | $V_{DD}$ | V             |
| $C_L$                                                      | Load Capacitance                                                                  |                |      | 50       | pF            |
| $t_R, t_F$                                                 | Rise and Fall Time (10 to 90%)                                                    |                |      | 20       | ns            |
| $\overline{COR}$ AND COR AND Y (with Pull up to $V_{DD}$ ) |                                                                                   |                |      |          |               |
| $V_{OL}$                                                   | Output Low Voltage ( $I_{OL} = 2\text{mA}$ )                                      | 0              |      | 0.5      | V             |
| $C_L$                                                      | Load Capacitance                                                                  |                |      | 25       | V             |
| $t_F$                                                      | Fall Time ( $R_L = 1.2\text{k}\Omega$ , $V_{DD} - 0.5\text{V}$ to $1.5\text{V}$ ) |                |      | 50       | ns            |
| $I_{OLL}$                                                  | Output Leakage Current                                                            | -10            |      | +10      | $\mu\text{s}$ |
| SDA                                                        |                                                                                   |                |      |          |               |
| $V_{OL}$                                                   | Output Low Voltage ( $I_{OL} = 3\text{mA}$ )                                      | 0              |      | 0.5      | V             |
| $t_F$                                                      | Fall Time (3.0 to 1.0V)                                                           |                |      | 200      | ns            |
| $C_L$                                                      | Load Capacitance                                                                  |                |      | 400      | pF            |

Table 6. Crystal Oscillator

| Symbol     | Parameter                | Min. | Typ.   | Max. | Unit      |
|------------|--------------------------|------|--------|------|-----------|
| $f_{XTAL}$ | Crystal Frequency        |      | 13.875 |      | MHz       |
| $R_{BIAS}$ | Internal Bias Resistance | 0.4  | 1      | 3    | $M\Omega$ |
| $C_I$      | Input Capacitance        |      |        | 7    | pF        |

Table 7. Timing

| Symbol                                                    | Parameter                                                | Min. | Typ. | Max. | Unit    |
|-----------------------------------------------------------|----------------------------------------------------------|------|------|------|---------|
| SERIAL BUS (referred to $V_{IH} = 3V$ , $V_{IL} = 1.5V$ ) |                                                          |      |      |      |         |
| $t_{LOW}$                                                 | Clock:                                                   | 4    |      |      | $\mu s$ |
| $t_{HIGH}$                                                | ● Low Period<br>● High Period                            | 4    |      |      | $\mu s$ |
| $t_{SU, DAT}$                                             | Data Set-up Time                                         | 250  |      |      | ns      |
| $t_{HD, DAT}$                                             | Data Hold Time                                           | 170  |      |      | ns      |
| $t_{SU, STO}$                                             | Stop Set-up Time from Clock High                         | 4    |      |      | $\mu s$ |
| $t_{BUF}$                                                 | Start Set-up Time following a Stop                       | 4    |      |      | $\mu s$ |
| $t_{HD, STA}$                                             | Start Hold Time                                          | 4    |      |      | $\mu s$ |
| $t_{SU, STA}$                                             | Start Set-up Time following Clock Low to High Transition | 4    |      |      | $\mu s$ |

Figure 4. Display Output Timing

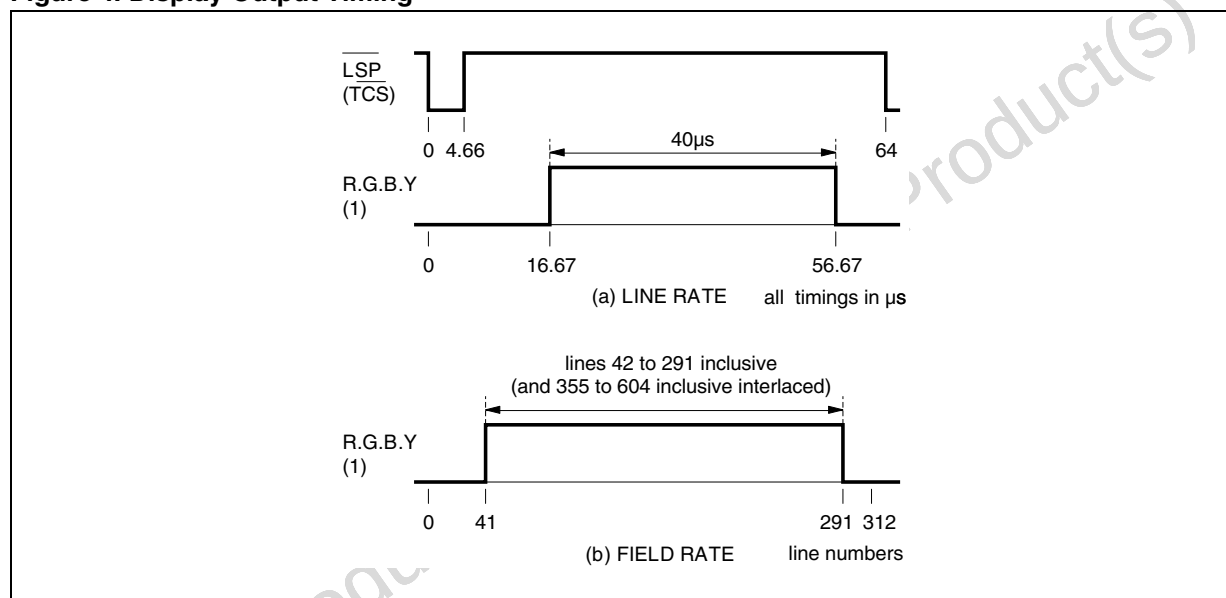


Figure 5. Serial Bus Timing

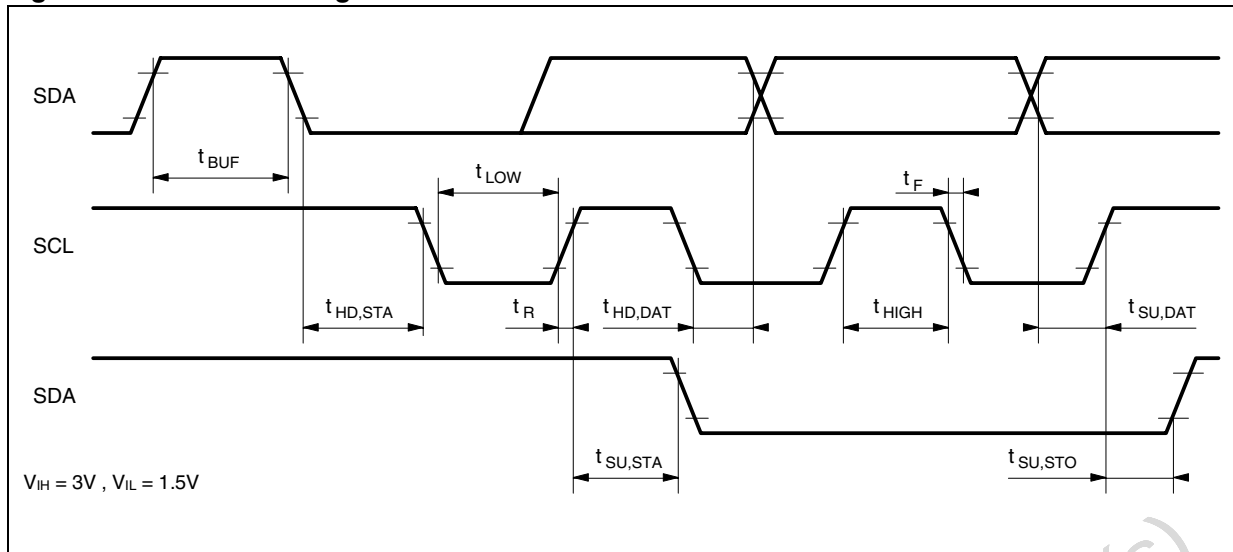


Figure 6. Master Synchronization Mode - Hardware Configuration

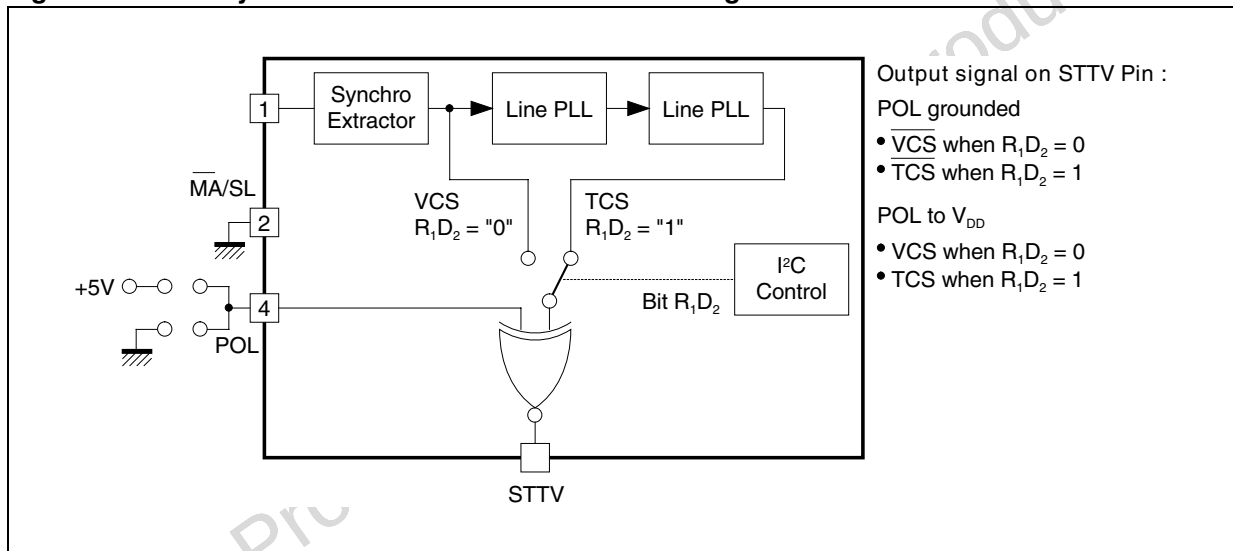


Figure 7. Master Synchronization Mode - Delivered Composite Synchronization Signal

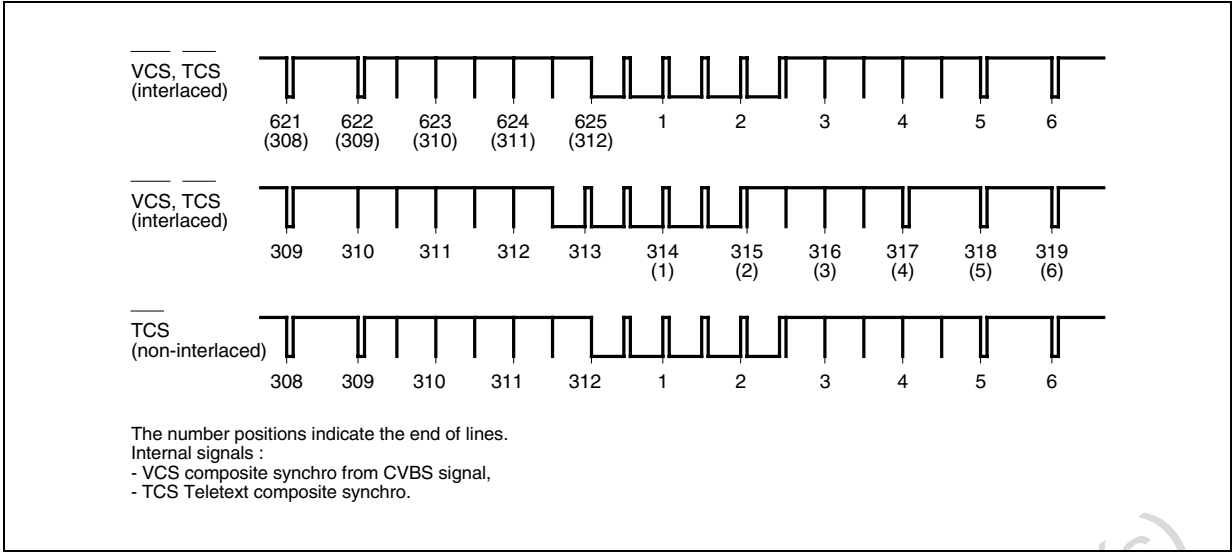


Figure 8. Slave Synchronization Mode

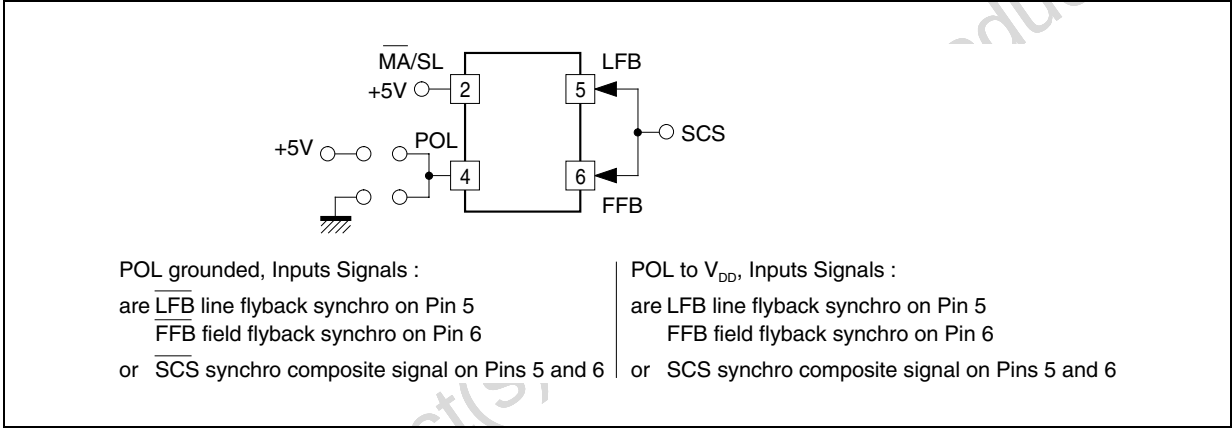
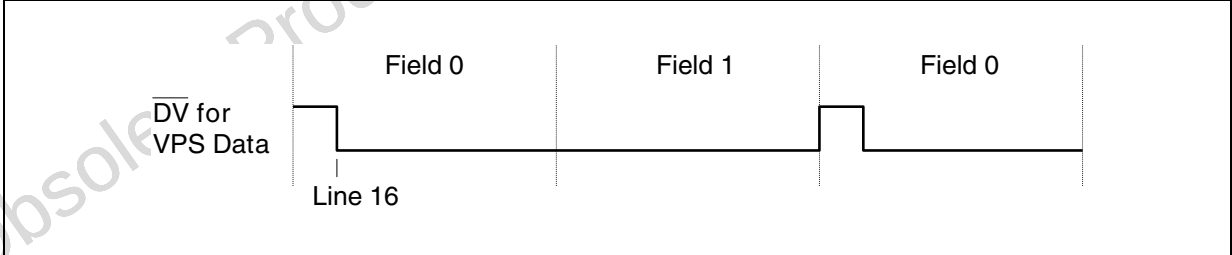


Figure 9. Data Valid Timing (DV)





## FUNCTIONAL DESCRIPTION

### Displayable Page Memory Map

The organization of a page memory is shown in Figure 10.

The display area consists of 25 rows of 40 characters per row.

The organization is as follows:

- Row zero contains the page header:
  - The first seven characters (0 - 6) are used for messages regarding the operational status.
  - The eighth character is an alphanumeric control character either "white" or "green" defining the "search" status of the page. When it is "white" the operational state is normal and the header appears white; when it is "green" the operational state corresponds
- to the "search mode" and the header appears green.
- The following twenty-four characters give the header of the requested page when the system is in search mode.
- The last eight characters display the time of day.
- Row number twenty-four is used by the microprocessor for the display of information, or used to display X/24 colored key data according to R0D7 bit.
- Row twenty-five comprises ten bytes of control data concerning the received page (see Table 9) and fourteen free bytes which can be used by the microprocessor.

**Figure 10. Page Memory Organization**

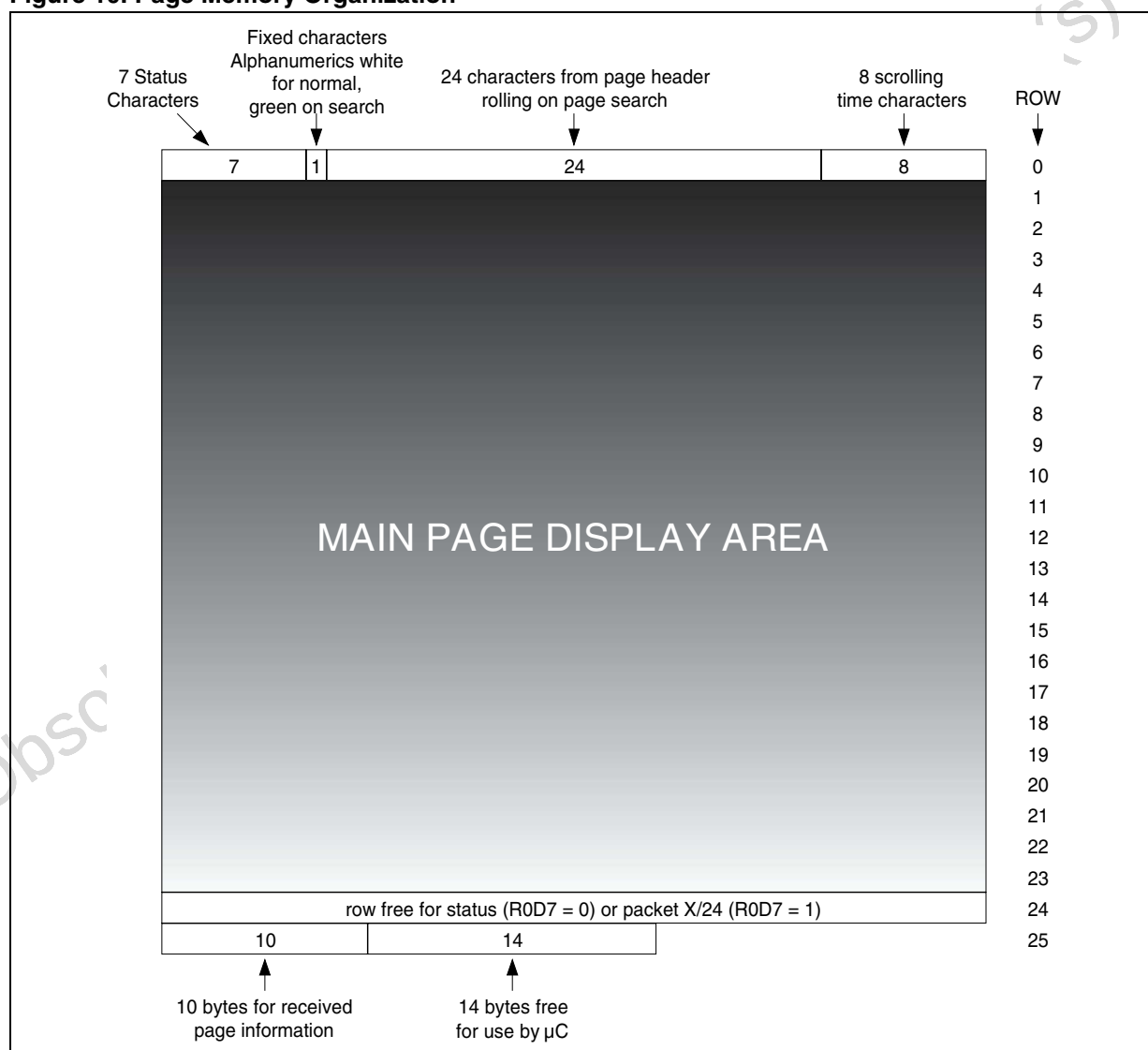


Table 8. Ghost Row Storage Organization

| Row Address of Stored Data | Designation Code | Row (Packet) Number   | Function                                        |
|----------------------------|------------------|-----------------------|-------------------------------------------------|
| 0                          | 0 0 0 0          | X / 26                | Enhanced display facilities                     |
| 1                          | 0 0 0 1          |                       |                                                 |
| 2                          | 0 0 1 0          |                       |                                                 |
| 3                          | 0 0 1 1          |                       |                                                 |
| 4                          | 0 1 0 0          |                       |                                                 |
| 5                          | 0 1 0 1          |                       |                                                 |
| 6                          | 0 1 1 0          |                       |                                                 |
| 7                          | 0 1 1 1          |                       |                                                 |
| 8                          | 1 0 0 0          |                       |                                                 |
| 9                          | 1 0 0 1          |                       |                                                 |
| 10                         | 1 0 1 0          |                       |                                                 |
| 11                         | 1 0 1 1          |                       |                                                 |
| 12                         | 1 1 0 0          |                       |                                                 |
| 13                         | 1 1 0 1          |                       |                                                 |
| 14                         | 1 1 1 0          |                       |                                                 |
| 15                         | 0 0 1 0          | X / 28                | Conditional access                              |
| 16                         | 0 0 0 0          | X / 27                | Editorial                                       |
| 17                         | 0 0 0 1          |                       | Linked pages                                    |
| 18                         | 0 1 0 0          |                       |                                                 |
| 19                         | 0 1 0 1          |                       | Composition                                     |
| 20                         |                  | X / 24                | Page extension stored here if R0D7 = 0          |
| 21                         |                  | X / 25                | Page extension                                  |
| 22                         | 0 0 0 0          | X / 28                | Color definition                                |
| 23                         | X X X X          | 8 / 30 <sup>(1)</sup> | <sup>(1)</sup> Broadcasting service data packet |
| 24                         | 0 0 0 1          | X/28                  | Character set designation                       |
| 25 <sup>(2)</sup>          | Not used         |                       |                                                 |

Page related data stored in chapter corresponding to level 1 data, i.e. For 0 goes in 4

" 1 " " 5  
" 2 " " 6  
" 3 " " 7

Note: 1. Packet 8/30 storage: 8/30/0,1: chapter 4, row23  
8/30/2,3: chapter 5, row23  
8/30/4 to 15: chapter 6, row23

2. See Table 10 for VPS data storage.

**Table 9. Row 25 Received Page Control Data Format**

|        |     |     |     |     |     |     |     |     |       |      |
|--------|-----|-----|-----|-----|-----|-----|-----|-----|-------|------|
| D0     | PU0 | PT0 | MU0 | MT0 | HU0 | HT0 | C7  | C11 | MAG0  | 0    |
| D1     | PU1 | PT1 | MU1 | MT1 | HU1 | HT1 | C8  | C12 | MAG1  | 0    |
| D2     | PU2 | PT2 | MU2 | MT2 | HU2 | C5  | C9  | C13 | MAG2  | 0    |
| D3     | PU3 | PT3 | MU3 | C4  | HU3 | C6  | C10 | C14 | 0     | 0    |
| D4     | HAM | HAM | HAM | HAM | HAM | HAM | HAM | HAM | FOUND | 0    |
| D5     | 0   | 0   | 0   | 0   | 0   | 0   | 0   | 0   | 0     | PBLF |
| D6     | 0   | 0   | 0   | 0   | 0   | 0   | 0   | 0   | 0     | 0    |
| D7     | 0   | 0   | 0   | 0   | 0   | 0   | 0   | 0   | 0     | 0    |
| COLUMN | 0   | 1   | 2   | 3   | 4   | 5   | 6   | 7   | 8     | 9    |

Page number : - MAG = magazine, PU = page units, PT = page tens.

Page sub-code : - MU = minutes units, MT = minutes tens, HU = hours units, HT = hours tens.

PBLF = page being looked for, FOUND = low for page found, HAM = hamming error in byte, C4-14 = control bits.

### VPS DATA (see Table 10)

VPS data are stored in row 25 chapter 5 as shown in Table 10 when VPS enable bit (D4 of R8 register) is set. VPS data bits are decoded and stored in a received area with biphas error bit.

8/30/2 data are stored as received (without hamming decoding) in Row 23 chapter 5 according to Table 10.

8/30 packet and VPS data decoding is the responsibility of the control software. The decoder simply stores transmitted data.

### I<sup>2</sup>C Bus Register Map (see Table 11)

Registers R0 to R10 are write only whilst R11A is a read/write and R11B is read only.

The automatic succession on a byte by byte basis is indicated by the arrows in Table 10.

In the normal operating mode TB should be set to logic level 0.

After power-up the contents of the registers are as follows: all bits in registers R0 to R11A are cleared to zero with the exception of bits D0 and D1 in registers R5 and R6 which are set to logical one.

After power-up all the memory bytes are preset to hexadecimal value 20H (space) with the exception of the byte corresponding to row 0 of column 7 of chapter 0 which is set to the value corresponding to "alpha white" hexadecimal value 07H.

**Table 10. PDC Data Storage**

|                 |                           |              |   |   |   |   |   |     |     |     |     |     |     |     |     |     |     |     |     |     |
|-----------------|---------------------------|--------------|---|---|---|---|---|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| Column          | 0                         | 1            | 2 | 3 | 4 | 5 | 6 | 7   | 8   | 9   | 10  | 11  | 12  | 13  | 14  | 15  | 16  | 17  | 18  | 19  |
| 8/30/2 (Row 23) | D                         | Initial Page |   |   |   |   |   | b13 | b14 | b15 | b16 | b17 | b18 | b19 | b20 | b21 | b22 | b23 | b24 | b25 |
| VPS (Row 25)    | Received Page Information |              |   |   |   |   |   |     |     |     | B11 |     | B12 |     | B13 |     | B14 |     | B15 |     |

|                 |                |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
|-----------------|----------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Column          | 20             | 21 | 22 | 23 | 24 | 25 | 26 | 27 | 28 | 29 | 30 | 31 | 32 | 33 | 34 | 35 | 36 | 37 | 38 | 39 |
| 8/30/2 (Row 23) | Status Display |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| VPS (Row 25)    | B4             |    | B5 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |

Table 11. Register Specification

| D7                 | D6                         | D5              | D4                     | D3                            | D2               | D1               | D0                   |                                           |
|--------------------|----------------------------|-----------------|------------------------|-------------------------------|------------------|------------------|----------------------|-------------------------------------------|
| X24 POSITION       | FREE RUNNING PLL           | 0               | DISABLE ROLLING HEADER | (1)                           | EVEN OFF         | (1)              | SEL 11B              | R0 Mode 0                                 |
| (1)                | $7 + \overline{P}$ / 8 BIT | ACQ. ON/OFF     | GHOST ROW ENABLE       | $\overline{DEW}$ / FULL FIELD | TCS ON           | T1               | T0                   | R1 Mode 1                                 |
| (1)                | BANK SELECT A2             | ACQ. CCT A1     | ACQ. CCT A0            | TB                            | START COLUMN SC2 | START COLUMN SC1 | START COLUMN SC0     | R2 Page request address                   |
| (1)                | (1)                        | (1)             | PRD4                   | PRD3                          | PRD2             | PRD1             | PRD0                 | R3 Page request data                      |
| (1)                | (1)                        | (1)             | (1)                    | (1)                           | A2               | A1               | A0                   | R4 Display chapter                        |
| BKGND OUT          | BKGND IN                   | COR OUT         | COR IN                 | TEXT OUT                      | TEXT IN          | PON OUT          | PON IN               | R5 Display control (normal)               |
| BKGND OUT          | BKGND IN                   | COR OUT         | COR IN                 | TEXT OUT                      | TEXT IN          | PON OUT          | PON IN               | R6 Display control (newsflash / subtitle) |
| STATUS ROW BTM/TOP | CURSOR ON/OFF              | CONCEAL/ REVEAL | TOP/ BOTTOM            | SINGLE/ DOUBLE HEIGHT         | BOX ON 24        | BOX ON 1-23      | BOX ON 0             | R7 Display mode                           |
| (1)                | (1)                        | (1)             | VPS ENABLE             | CLEAR MEM.                    | A2               | A1               | A0                   | R8 Active chapter                         |
| (1)                | (1)                        | (1)             | R4                     | R3                            | R2               | R1               | R0                   | R9 Active row                             |
| (1)                | (1)                        | C5              | C4                     | C3                            | C2               | C1               | C0                   | R10 Active column                         |
| D7 (R/W)           | D6 (R/W)                   | D5 (R/W)        | D4 (R/W)               | D3 (R/W)                      | D2 (R/W)         | D1 (R/W)         | D0 (R/W)             | R11A Active data                          |
| 60Hz               | 0                          | 0               | 0                      | 0                             | 0                | DATA QUAL        | V <sub>CS</sub> QUAL | R11B Status                               |

Note (1). Reserved register bits: must be set to 0.

Table 12. Registers Functions

| Register             | Function                                                 | Bit(s)                                           | Description                                                                                                                                                                                                                                                          |
|----------------------|----------------------------------------------------------|--------------------------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| R0<br>Address<br>00H | R11 addressing and<br>pin functions control              | SEL 11B (D0)                                     | Selection of register 11B (D0 = 1) or 11A (D0 = 0)                                                                                                                                                                                                                   |
|                      |                                                          | EVEN OFF (D2)                                    | Control of $\overline{\text{ODD}}$ /EVEN pin: EVEN signal output (D2 = 0) or grounded (D2 = 1)                                                                                                                                                                       |
|                      |                                                          | DISABLE ROLLING<br>HEADER                        | D4 = 1, Disable rolling header<br>D4 = 0, Normal operation                                                                                                                                                                                                           |
|                      |                                                          | FREE RUNNING<br>PLL (D6)                         | D6 = 0, PLL locks on line frequency<br>D6 = 1, to force free running mode                                                                                                                                                                                            |
|                      |                                                          | X/24 POSITION (D7)                               | D7 = 0, packet X/24 stored to chapter 4 to 7/row 20<br>D7 = 1, packet X/24 stored to chapter 0 to 3/row 24                                                                                                                                                           |
| R1<br>Address<br>01H | Operating mode<br>controls                               | T1 (D1) T0 (D0)<br>0 0<br>0 1<br>1 0<br>1 1      | Character display line control:<br>312.5/312.5 line MIX - mode with interlace<br>312/313 line TEXT - mode without interlace<br>312/312 line Terminal mode without interlace<br>External synchronization. SCS mode (scan field<br>synchro)                            |
|                      |                                                          | TCS ON (D2)                                      | Master Mode ( $\overline{\text{MA}}/\text{SL}$ Pin 2 = 0)<br>case POL Pin 4 = 0<br>D2 = 0, Pin 5 = $\overline{\text{VCS}}$<br>D2 = 1, Pin 5 = $\overline{\text{TCS}}$<br>Slave Mode ( $\overline{\text{MA}}/\text{SL}$ Pin 2 = $\text{V}_{\text{DD}}$ )<br>No effect |
|                      |                                                          | $\overline{\text{DEW}}$ / FULLFIELD<br>(D3)      | Selection of field flyback mode or full channel mode<br>(D3 = 1) for recovering of Teletext data.                                                                                                                                                                    |
|                      |                                                          | GHOST ROW<br>ENABLE (D4)                         | Selection of ghost row mode (D4 = 1)                                                                                                                                                                                                                                 |
|                      |                                                          | ACQUISITION<br>ON / OFF (D5)                     | Control of acquisition operation (D5 = 0 enables<br>acquisition)                                                                                                                                                                                                     |
|                      |                                                          | 7 bits + parity or 8 bits<br>without parity (D6) | Selection of received data format either 7 bits with<br>parity (D6 = 0) or 8 bits without parity (D6 = 1).                                                                                                                                                           |
| R2<br>Address<br>02H | Addressing<br>information for<br>a page request          | SC0, SC1, SC2<br>(D0, D1, D2)                    | Address the first column of the on chip page request<br>RAM to be written.                                                                                                                                                                                           |
|                      |                                                          | TB (D3)                                          | Test bit equal to "0" in the normal working mode.                                                                                                                                                                                                                    |
|                      |                                                          | A0, A1 (D4, D5)                                  | Address a group of four consecutive pages currently<br>used for data acquisition.                                                                                                                                                                                    |
|                      |                                                          | A2 (D6)                                          | Address of one of the two groups of four pages for<br>acquisition in normal mode.                                                                                                                                                                                    |
| R3<br>Address<br>03H | Data relative to the<br>requested page<br>(see Table 10) | PRD0 - PRD4<br>(D0 - D4)                         | Written data in the page request RAM, starting with<br>the columns addressed by SC0, SC1, SC2.                                                                                                                                                                       |
| R4<br>Address<br>04H | Selection of one of<br>eight pages to<br>display         | A0, A1, A2<br>(D0, D1, D2)                       | Chapter selection.                                                                                                                                                                                                                                                   |

| Register                                           | Function                                                                                                                                                | Bit(s)                                                          | Description                                                                             |
|----------------------------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------------------------------------------------------|-----------------------------------------------------------------------------------------|
| R5<br>Address<br>05H                               | Display control for normal operation                                                                                                                    | PON (D0, D1)                                                    | Picture on (IN: D0, OUT: D1)                                                            |
|                                                    |                                                                                                                                                         | TEXT (D2, D3)                                                   | Text on (IN: D2, OUT: D3)                                                               |
|                                                    |                                                                                                                                                         | $\overline{\text{COR}}$ (D4, D5)                                | Contrast reduction on (IN: D4, OUT: D5)                                                 |
|                                                    |                                                                                                                                                         | BKGND (D6, D7)                                                  | Background color on (IN: D6, OUT: D7)                                                   |
|                                                    |                                                                                                                                                         | IN / OUT                                                        | Enable inside/outside the box                                                           |
| R6<br>Address<br>06H                               | Display control for news-flash subtitle generation                                                                                                      | See R5                                                          | See R5                                                                                  |
| R7<br>Address<br>07H                               | Display mode                                                                                                                                            | BOX ON 0, 1-23,24 (D0, D1, D2)                                  | The "boxing" function is enabled on row 0,1-23 and 24 by D0, D1 and D2 set to one.      |
|                                                    |                                                                                                                                                         | $\overline{\text{TOP}}$ / BOTTOM Single / Double Height (D4/D3) | X0 = Normal<br>01 = double height Rows 0 to 11<br>11 = double height Rows 12 to 23      |
|                                                    |                                                                                                                                                         | $\overline{\text{Conceal}}$ / Reveal (D5)                       | Conceal Reveal Function                                                                 |
|                                                    |                                                                                                                                                         | Cursor ON/ $\overline{\text{OFF}}$ (D6)                         | Cursor position given by row/column value of R9/R10                                     |
|                                                    |                                                                                                                                                         | $\overline{\text{STATUS ROW BTM}}$ / TOP (D7)                   | The row 24 is displayed before the "Main text Area" (lines 0-23) or after (D7 = 0).     |
| R8                                                 | Memory access                                                                                                                                           | VPS Enable (D4)                                                 | D4 = 1 Enable VPS acquisition and DV signal output.                                     |
|                                                    |                                                                                                                                                         | Clear Memory (D3)                                               | D4 = 1 Clear memory.<br>Chapter selected with A2A1A0 (D2, D1, D0) R4.                   |
|                                                    |                                                                                                                                                         | Chapter Address (D2, D1, D0)                                    | Chapter selection                                                                       |
| R9 to R11A<br>Address<br>08H to 0BH <sup>(1)</sup> | Active row address (R9), active column address (R10).<br>Data contained in R11A read (written) from (to) memory by microprocessor via I <sup>2</sup> C. |                                                                 |                                                                                         |
| R11B<br>Address<br>0BH <sup>(1)</sup>              | Status                                                                                                                                                  | VCS QUAL (D0)                                                   | Good VCS quality signal detected (D0 = 1).<br>Bad VCS quality signal detected (D0 = 0). |
|                                                    |                                                                                                                                                         | DATA QUAL (D1)                                                  | Good TELETEXT signal (D1 = 1).<br>Bad TELETEXT signal (D1 = 0).                         |
|                                                    |                                                                                                                                                         | 50/60Hz (D7)                                                    | If D1 = 0 frame frequency is 50Hz<br>(only valid with good VCS)                         |

Note: 1. Reading of R11A or R11B is determined by register 0, bit D0. However, write operation is always performed on R11A register.

**Table 13. Register R3**

| START COLUMN | PRD4                  | PRD3                     | PRD2 | PRD1 | PRD0 |
|--------------|-----------------------|--------------------------|------|------|------|
| 0            | Do care magazine      | $\overline{\text{HOLD}}$ | MAG2 | MAG1 | MAG0 |
| 1            | Do care page tens     | PT3                      | PT2  | PT1  | PT0  |
| 2            | Do care page units    | PU3                      | PU2  | PU1  | PU0  |
| 3            | Do care hours tens    | X                        | X    | HT1  | HT0  |
| 4            | Do care hours units   | HU3                      | HU2  | HU1  | HU0  |
| 5            | Do care minutes tens  | X                        | MT2  | MT1  | MT0  |
| 6            | Do care minutes units | MU3                      | MU2  | MU1  | MU0  |

The abbreviations have the same significance as in Table 9 with the exception of the "DO CARE" entries. It is only when this bit is "1" that the corresponding digit is taken into consideration on page request. For example, a page defined as "normal" or one defined as "timed" may be selected.

If " $\overline{\text{HOLD}}$ " is low the page is held. The addressing of successive bytes via the I<sup>2</sup>C is automatic.

### Character Sets

The complete character set with 8-bit decoding is given in Table 12.

Characters in columns 0 and 1 are normally displayed as blanks. Black dots represent the character shape whereas white dots represent the background.

Each character can be identified by a pair of corresponding row and column integers: for example the character "3" may be indicated by 3/3.

A rectangle may be represented as follows .

The characters 8/6, 8/7, 9/5, 9/7 are used as special characters, always in conjunction with 8/5.

The 13 national characters are placed in columns with bit 8 = 0.

Table 14. STV5348 Complete Character Set (with 8 bit codes) - West European Languages

| B<br>T<br>S | b <sub>9</sub><br>b <sub>7</sub><br>b <sub>6</sub><br>b <sub>5</sub> | b <sub>4</sub><br>b <sub>3</sub><br>b <sub>2</sub><br>b <sub>1</sub> | column |   |   |   |   |   |   |    |   |    |   |   |    |    |    |   | 15 |   |
|-------------|----------------------------------------------------------------------|----------------------------------------------------------------------|--------|---|---|---|---|---|---|----|---|----|---|---|----|----|----|---|----|---|
|             |                                                                      |                                                                      | 0      | 1 | 2 | 3 | 4 | 5 | 6 | 6a | 7 | 7a | 8 | 9 | 12 | 13 | 14 |   |    |   |
| 0 0 0 0     | 0                                                                    | 0                                                                    | 0      | 0 | 0 | 0 | 0 | 0 | 0 | 0  | 0 | 0  | 0 | 0 | 0  | 0  | 0  | 0 | 0  | 1 |
| 0 0 0 1     | 1                                                                    | 0                                                                    | 0      | 0 | 0 | 0 | 0 | 0 | 0 | 0  | 0 | 0  | 0 | 0 | 0  | 0  | 0  | 0 | 0  | 1 |
| 0 0 1 0     | 2                                                                    | 0                                                                    | 0      | 0 | 0 | 0 | 0 | 0 | 0 | 0  | 0 | 0  | 0 | 0 | 0  | 0  | 0  | 0 | 0  | 1 |
| 0 0 1 1     | 3                                                                    | 0                                                                    | 0      | 0 | 0 | 0 | 0 | 0 | 0 | 0  | 0 | 0  | 0 | 0 | 0  | 0  | 0  | 0 | 0  | 1 |
| 0 1 0 0     | 4                                                                    | 0                                                                    | 0      | 0 | 0 | 0 | 0 | 0 | 0 | 0  | 0 | 0  | 0 | 0 | 0  | 0  | 0  | 0 | 0  | 1 |
| 0 1 0 1     | 5                                                                    | 0                                                                    | 0      | 0 | 0 | 0 | 0 | 0 | 0 | 0  | 0 | 0  | 0 | 0 | 0  | 0  | 0  | 0 | 0  | 1 |
| 0 1 1 0     | 6                                                                    | 0                                                                    | 0      | 0 | 0 | 0 | 0 | 0 | 0 | 0  | 0 | 0  | 0 | 0 | 0  | 0  | 0  | 0 | 0  | 1 |
| 0 1 1 1     | 7                                                                    | 0                                                                    | 0      | 0 | 0 | 0 | 0 | 0 | 0 | 0  | 0 | 0  | 0 | 0 | 0  | 0  | 0  | 0 | 0  | 1 |
| 1 0 0 0     | 8                                                                    | 0                                                                    | 0      | 0 | 0 | 0 | 0 | 0 | 0 | 0  | 0 | 0  | 0 | 0 | 0  | 0  | 0  | 0 | 0  | 1 |
| 1 0 0 1     | 9                                                                    | 0                                                                    | 0      | 0 | 0 | 0 | 0 | 0 | 0 | 0  | 0 | 0  | 0 | 0 | 0  | 0  | 0  | 0 | 0  | 1 |
| 1 0 1 0     | 10                                                                   | 0                                                                    | 0      | 0 | 0 | 0 | 0 | 0 | 0 | 0  | 0 | 0  | 0 | 0 | 0  | 0  | 0  | 0 | 0  | 1 |
| 1 0 1 1     | 11                                                                   | 0                                                                    | 0      | 0 | 0 | 0 | 0 | 0 | 0 | 0  | 0 | 0  | 0 | 0 | 0  | 0  | 0  | 0 | 0  | 1 |
| 1 1 0 0     | 12                                                                   | 0                                                                    | 0      | 0 | 0 | 0 | 0 | 0 | 0 | 0  | 0 | 0  | 0 | 0 | 0  | 0  | 0  | 0 | 0  | 1 |
| 1 1 0 1     | 13                                                                   | 0                                                                    | 0      | 0 | 0 | 0 | 0 | 0 | 0 | 0  | 0 | 0  | 0 | 0 | 0  | 0  | 0  | 0 | 0  | 1 |
| 1 1 1 0     | 14                                                                   | 0                                                                    | 0      | 0 | 0 | 0 | 0 | 0 | 0 | 0  | 0 | 0  | 0 | 0 | 0  | 0  | 0  | 0 | 0  | 1 |
| 1 1 1 1     | 15                                                                   | 0                                                                    | 0      | 0 | 0 | 0 | 0 | 0 | 0 | 0  | 0 | 0  | 0 | 0 | 0  | 0  | 0  | 0 | 0  | 1 |

Case using C12 C13 C14 = 001 (German Set)

\* These control characters are reserved for compatibility with other data codes.  
\*\* These control characters are presumed before each row begins







**Table 16. STV5348/T Complete Character Set (with 8 bit codes) - Turkish European Languages**

[illegible]

Case using C12 C13 C14 = 001 (German Set)

\* These control characters are reserved for compatibility with other data codes.  
 \*\* These control characters are presumed before each row begins

The basic set of the 96 characters is shown in Table 17. The location of the 13 national characters

are shown in Table 17 whilst full national character sets are depicted in Table 18, 19 and 20.

**Table 17. Basic character set.**

|      |                    |      |  |      |                    |      |                    |      |                    |      |                    |
|------|--------------------|------|--|------|--------------------|------|--------------------|------|--------------------|------|--------------------|
| 2/0  |                    | 3/0  |  | 4/0  | National Character | 5/0  |                    | 6/0  | National Character | 7/0  |                    |
| 2/1  |                    | 3/1  |  | 4/1  |                    | 5/1  |                    | 6/1  |                    | 7/1  |                    |
| 2/2  |                    | 3/2  |  | 4/2  |                    | 5/2  |                    | 6/2  |                    | 7/2  |                    |
| 2/3  | National Character | 3/3  |  | 4/3  |                    | 5/3  |                    | 6/3  |                    | 7/3  |                    |
| 2/4  | National Character | 3/4  |  | 4/4  |                    | 5/4  |                    | 6/4  |                    | 7/4  |                    |
| 2/5  |                    | 3/5  |  | 4/5  |                    | 5/5  |                    | 6/5  |                    | 7/5  |                    |
| 2/6  |                    | 3/6  |  | 4/6  |                    | 5/6  |                    | 6/6  |                    | 7/6  |                    |
| 2/7  |                    | 3/7  |  | 4/7  |                    | 5/7  |                    | 6/7  |                    | 7/7  |                    |
| 2/8  |                    | 3/8  |  | 4/8  |                    | 5/8  |                    | 6/8  |                    | 7/8  |                    |
| 2/9  |                    | 3/9  |  | 4/9  |                    | 5/9  |                    | 6/9  |                    | 7/9  |                    |
| 2/10 |                    | 3/10 |  | 4/10 |                    | 5/10 |                    | 6/10 |                    | 7/10 |                    |
| 2/11 |                    | 3/11 |  | 4/11 |                    | 5/11 | National Character | 6/11 |                    | 7/11 | National Character |
| 2/12 |                    | 3/12 |  | 4/12 |                    | 5/12 | National Character | 6/12 |                    | 7/12 | National Character |
| 2/13 |                    | 3/13 |  | 4/13 |                    | 5/13 | National Character | 6/13 |                    | 7/13 | National Character |
| 2/14 |                    | 3/14 |  | 4/14 |                    | 5/14 | National Character | 6/14 |                    | 7/14 | National Character |
| 2/15 |                    | 3/15 |  | 4/15 |                    | 5/15 | National Character | 6/15 |                    | 7/15 |                    |

Table 18. STV5348 Character Set - West European Languages

| LANGUAGE | PHCB (1) |     |     | CHARACTER POSITION (COLUMN/ROW) |     |     |      |      |      |      |      |     |      |      |      |      |
|----------|----------|-----|-----|---------------------------------|-----|-----|------|------|------|------|------|-----|------|------|------|------|
|          | C12      | C13 | C14 | 2/3                             | 2/4 | 4/0 | 5/11 | 5/12 | 5/13 | 5/14 | 5/15 | 6/0 | 7/11 | 7/12 | 7/13 | 7/14 |
|          |          |     |     |                                 |     |     |      |      |      |      |      |     |      |      |      |      |
| ENGLISH  | 0        | 0   | 0   |                                 |     |     |      |      |      |      |      |     |      |      |      |      |
| GERMAN   | 0        | 0   | 1   |                                 |     |     |      |      |      |      |      |     |      |      |      |      |
| SWEDISH  | 0        | 1   | 0   |                                 |     |     |      |      |      |      |      |     |      |      |      |      |
| ITALIAN  | 0        | 1   | 1   |                                 |     |     |      |      |      |      |      |     |      |      |      |      |
| FRENCH   | 1        | 0   | 0   |                                 |     |     |      |      |      |      |      |     |      |      |      |      |
| SPANISH  | 1        | 0   | 1   |                                 |     |     |      |      |      |      |      |     |      |      |      |      |

Note: 1. Where PHCB are the Page Header Control bits. Other Combinations default to English. Only the above characters change with the PHCB. All others characters in the basic set are shown in Table 14.

Table 19. STV5348/H Character Set - East European Languages

| LANGUAGE     | PHCB (1) |     |     | CHARACTER POSITION (COLUMN/ROW) |     |     |      |      |      |      |      |     |      |      |      |      |
|--------------|----------|-----|-----|---------------------------------|-----|-----|------|------|------|------|------|-----|------|------|------|------|
|              | C12      | C13 | C14 | 2/3                             | 2/4 | 4/0 | 5/11 | 5/12 | 5/13 | 5/14 | 5/15 | 6/0 | 7/11 | 7/12 | 7/13 | 7/14 |
|              |          |     |     |                                 |     |     |      |      |      |      |      |     |      |      |      |      |
| POLISH       | 0        | 0   | 0   |                                 |     |     |      |      |      |      |      |     |      |      |      |      |
| GERMAN       | 0        | 0   | 1   |                                 |     |     |      |      |      |      |      |     |      |      |      |      |
| SWEDISH      | 0        | 1   | 0   |                                 |     |     |      |      |      |      |      |     |      |      |      |      |
| SERBO-CROAT  | 1        | 0   | 1   |                                 |     |     |      |      |      |      |      |     |      |      |      |      |
| CZECHOSLOVAK | 1        | 1   | 0   |                                 |     |     |      |      |      |      |      |     |      |      |      |      |
| RUMANIAN     | 1        | 1   | 1   |                                 |     |     |      |      |      |      |      |     |      |      |      |      |

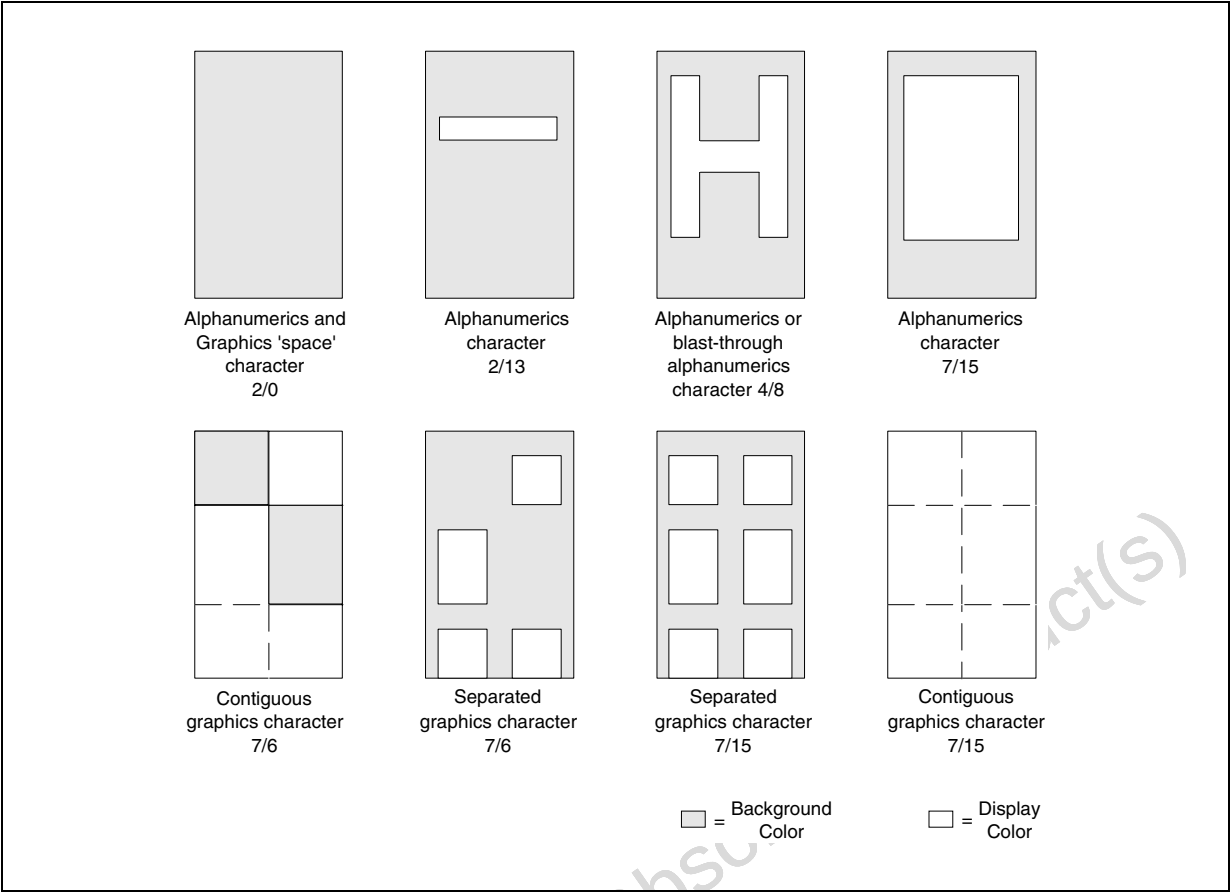
Note: 1. Where PHCB are the Page Header Control bits. Other Combinations default to German. Only the above characters change with the PHCB. All others characters in the basic set are shown in Table 16.

Table 20. STV5348/T Character Set - Turkish European Languages

| LANGUAGE | PHCB (1) |     |     | CHARACTER POSITION (COLUMN/ROW)                                                       |                                                                                       |                                                                                       |                                                                                       |                                                                                       |                                                                                      |                                                                                     |                                                                                     |                                                                                     |                                                                                     |                                                                                     |                                                                                     |                                                                                     |
|----------|----------|-----|-----|---------------------------------------------------------------------------------------|---------------------------------------------------------------------------------------|---------------------------------------------------------------------------------------|---------------------------------------------------------------------------------------|---------------------------------------------------------------------------------------|--------------------------------------------------------------------------------------|-------------------------------------------------------------------------------------|-------------------------------------------------------------------------------------|-------------------------------------------------------------------------------------|-------------------------------------------------------------------------------------|-------------------------------------------------------------------------------------|-------------------------------------------------------------------------------------|-------------------------------------------------------------------------------------|
|          | C12      | C13 | C14 | 2/3                                                                                   | 2/4                                                                                   | 4/0                                                                                   | 5/11                                                                                  | 5/12                                                                                  | 5/13                                                                                 | 5/14                                                                                | 5/15                                                                                | 6/0                                                                                 | 7/11                                                                                | 7/12                                                                                | 7/13                                                                                | 7/14                                                                                |
|          |          |     |     |                                                                                       |                                                                                       |                                                                                       |                                                                                       |                                                                                       |                                                                                      |                                                                                     |                                                                                     |                                                                                     |                                                                                     |                                                                                     |                                                                                     |                                                                                     |
| ENGLISH  | 0        | 0   | 0   |    |    |    |    |    |    |    |    |    |    |    |    |    |
| GERMAN   | 0        | 0   | 1   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| TURKISH  | 1        | 1   | 0   |  |  |  |  |  |  |  |  |  |  |  |  |  |
| ITALIAN  | 0        | 1   | 1   |  |  |  |  |  |  |  |  |  |  |  |  |  |
| FRENCH   | 1        | 0   | 0   |  |  |  |  |  |  |  |  |  |  |  |  |  |
| SPANISH  | 1        | 0   | 1   |  |  |  |  |  |  |  |  |  |  |  |  |  |

Note: 1. Where PHCB are the Page Header Control bits. Other Combinations default to Turkish. Only the above characters change with the PHCB. All others characters in the basic set are shown in Table 16.

Figure 11. Character Format



## I/O PIN ELECTRICAL SCHEMATICS

Figure 12. Analog 1 (CVBS)

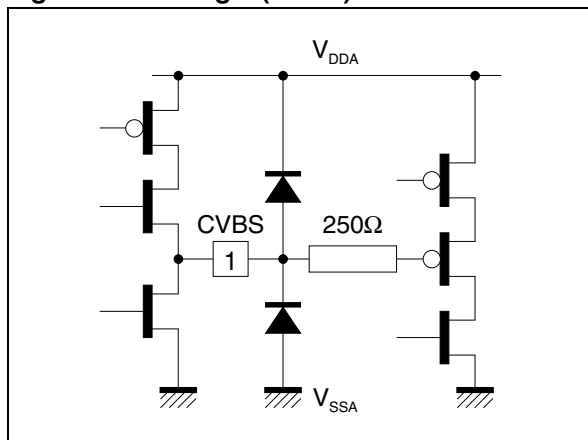


Figure 15. Input D

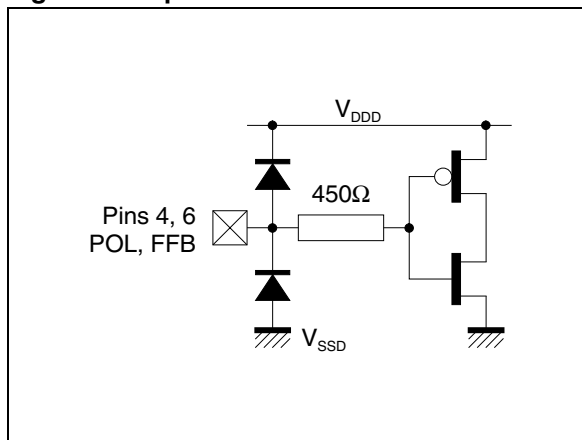


Figure 13. Analog 2 (CBLK)

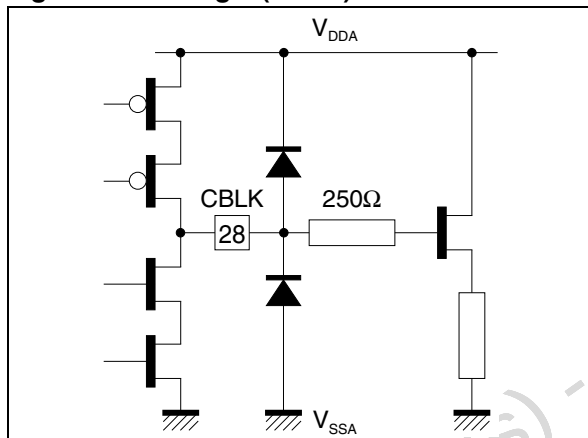


Figure 16. PRGB

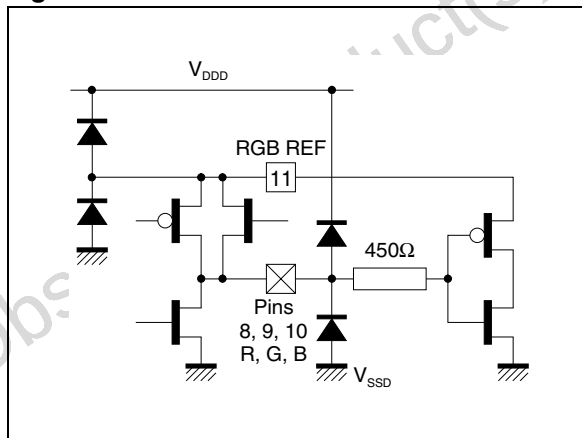


Figure 14. Input A

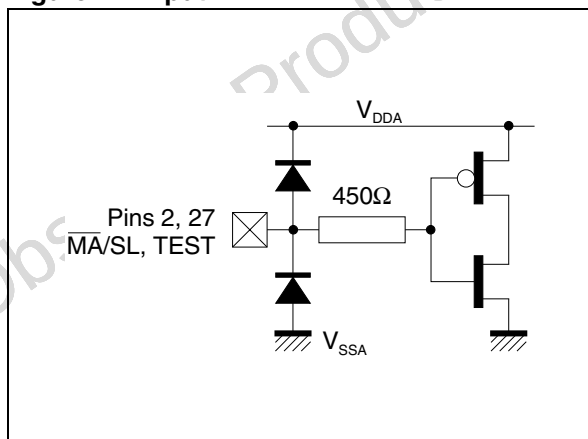


Figure 17.

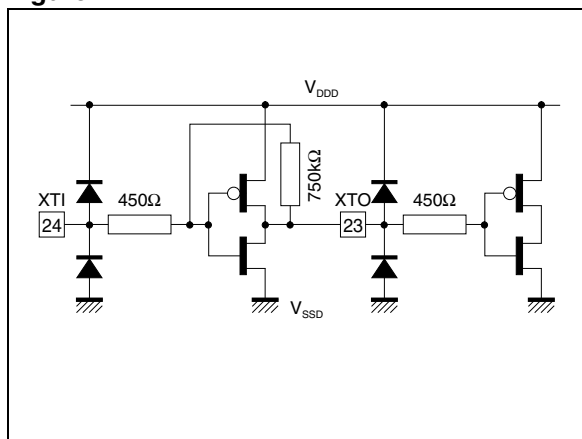


Figure 18. INOUT

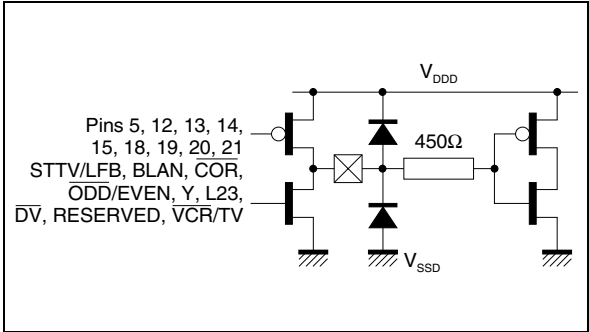


Figure 20. PSDA

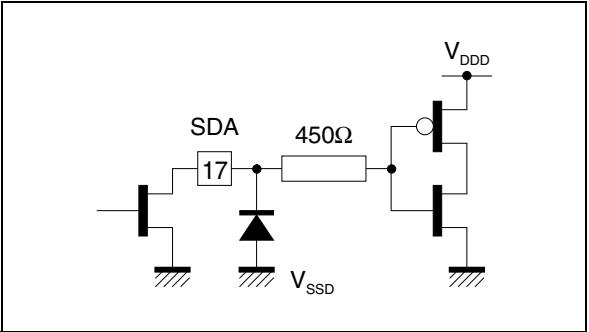


Figure 19. PSCL

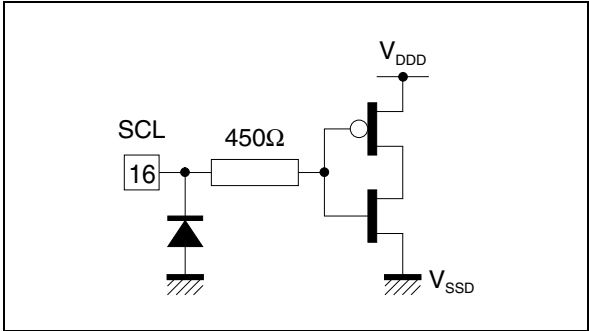
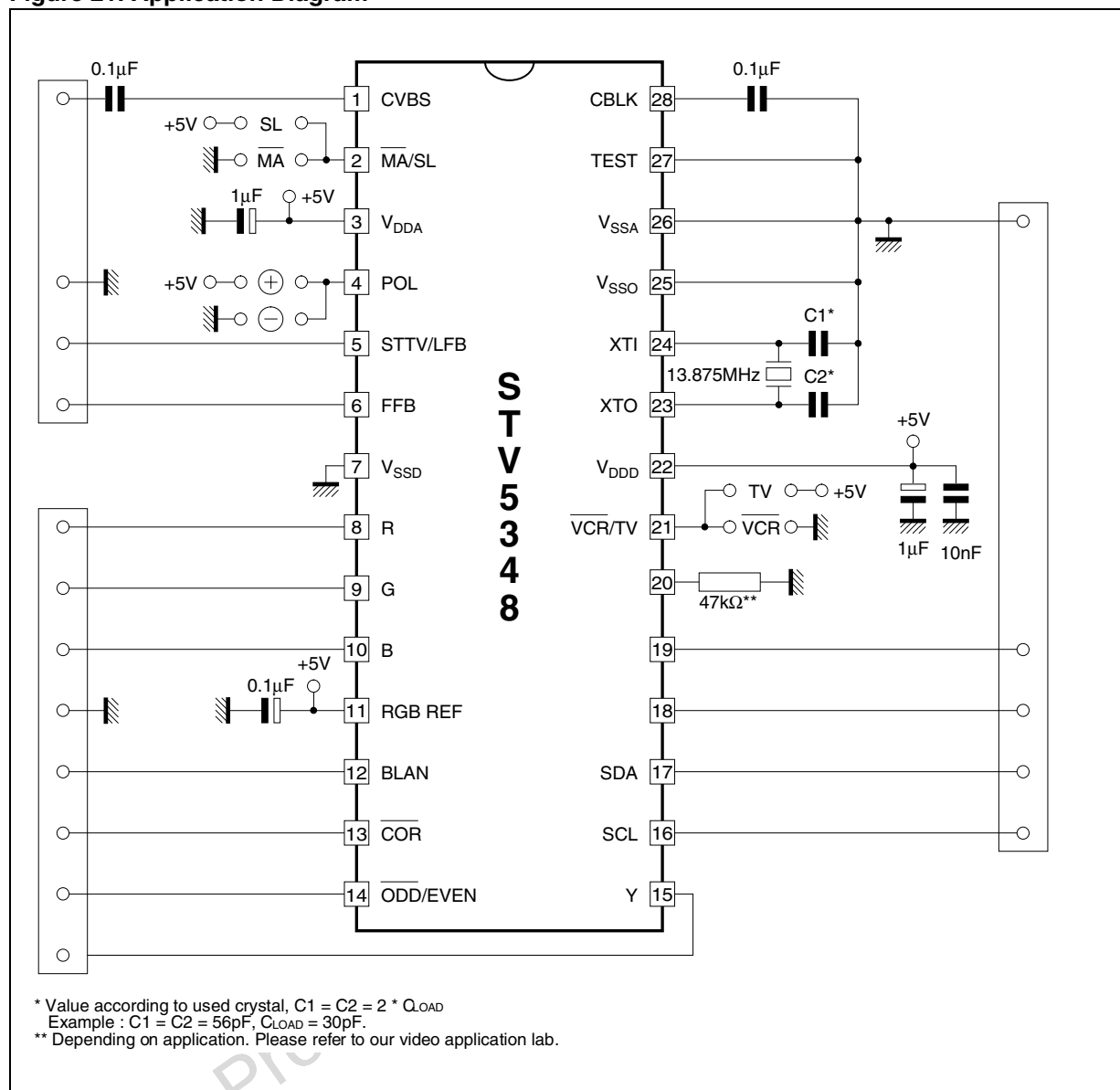




Figure 21. Application Diagram



**Remark:** all the power supply inputs must be switched on at the same time (connected to the same source).

## STV5348

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### PART NUMBERING

**Table 21. Order Codes**

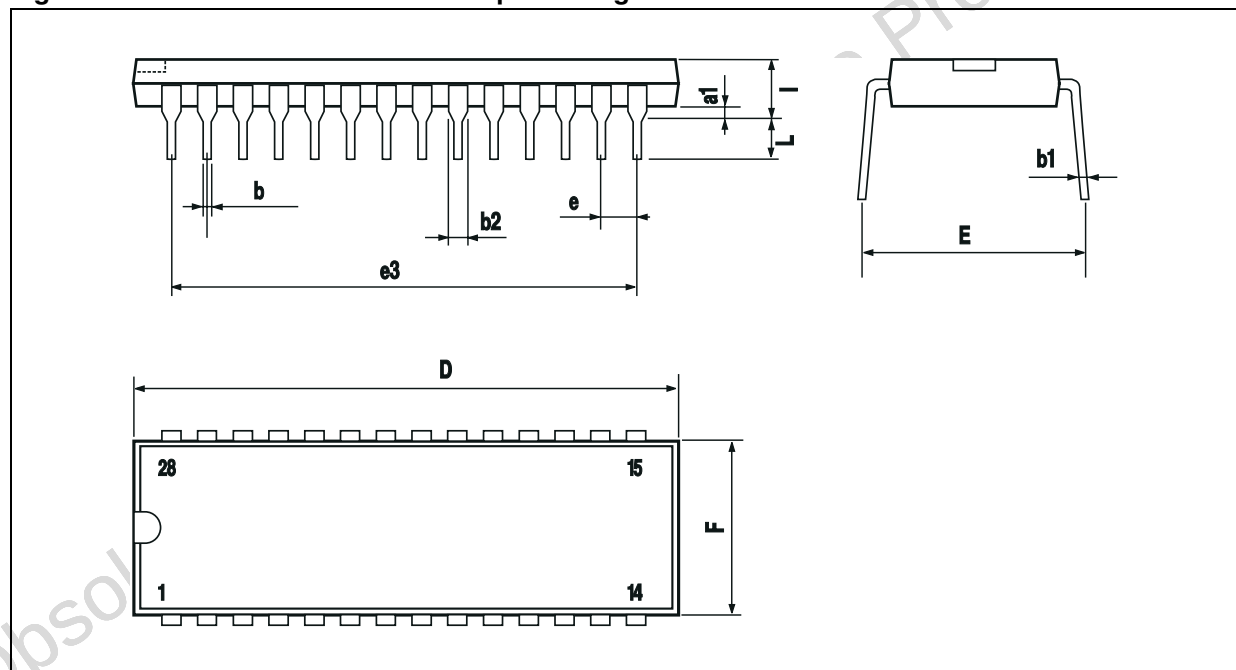
| Part Number | Package |                      | Temperature Range |
|-------------|---------|----------------------|-------------------|
| STV5438     | PDIP28  | West European        | 0 to 70 °C        |
| STV5438/H   | PDIP28  | East European        | 0 to 70 °C        |
| STV5348/T   | PDIP28  | Turkish and European | 0 to 70 °C        |
| STV5348D    | SO28    | West European        | 0 to 70 °C        |
| STV5348D/T  | SO28    | Turkish and European | 0 to 70 °C        |

## PACKAGE MECHANICAL

Table 22. PDIP28 - 28 Pins - Plastic Dip - Mechanical Data

| Symbol | millimeters |       |       | inches |       |       |
|--------|-------------|-------|-------|--------|-------|-------|
|        | Min         | Typ   | Max   | Min    | Typ   | Max   |
| a1     |             | 0.63  |       |        | 0.025 |       |
| b      |             | 0.45  |       |        | 0.018 |       |
| b1     | 0.23        |       | 0.31  | 0.009  |       | 0.012 |
| b2     |             | 1.27  |       |        | 0.050 |       |
| D      |             |       | 37.4  |        |       | 1.470 |
| E      | 15.2        |       | 16.68 | 0.598  |       | 0.657 |
| e      |             | 2.54  |       |        | 0.100 |       |
| e3     |             | 33.02 |       |        | 1.300 |       |
| F      |             |       | 14.1  |        |       | 0.555 |
| l      |             | 4.445 |       |        | 0.175 |       |
| L      |             | 3.3   |       |        | 0.130 |       |

Figure 22. PDIP28 - 28 Pins - Plastic Dip - Package Dimensions

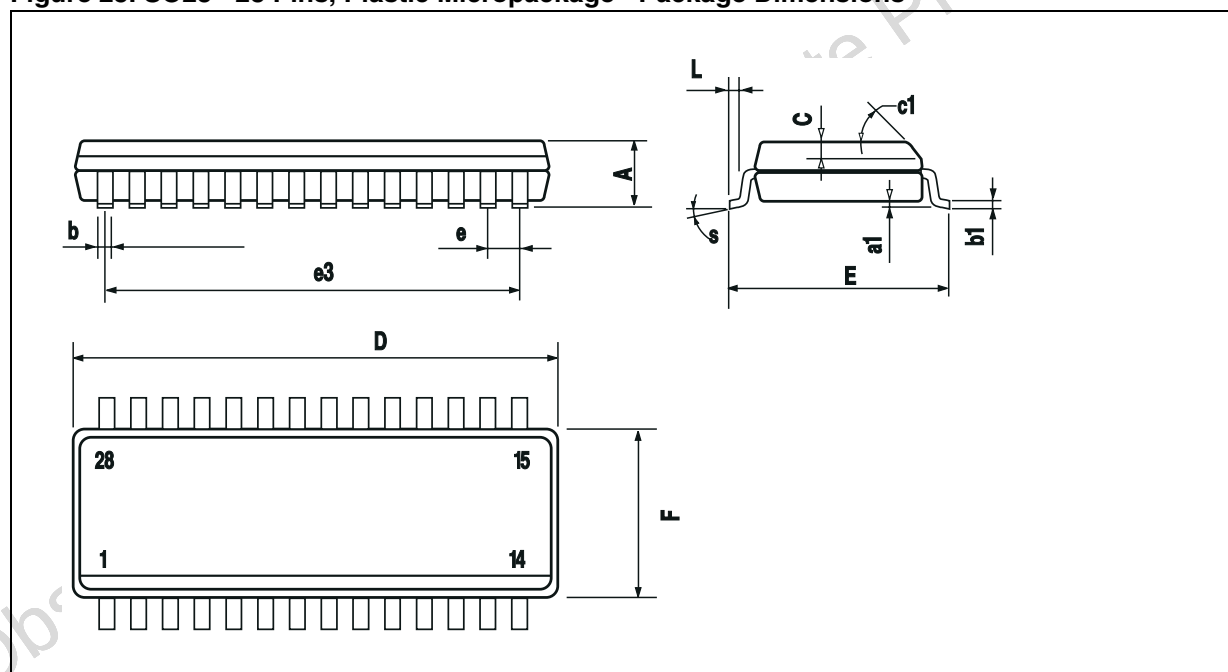


Note: Drawing is not to scale

Table 23. SO28 - 28 Pins, Plastic Micropackage - Mechanical Data

| Symbol | millimeters |       |       | inches |       |       |
|--------|-------------|-------|-------|--------|-------|-------|
|        | Min         | Typ   | Max   | Min    | Typ   | Max   |
| A      |             |       | 2.65  |        |       | 0.104 |
| a1     | 0.1         |       | 0.3   | 0.004  |       | 0.012 |
| b      | 0.35        |       | 0.49  | 0.014  |       | 0.019 |
| b1     | 0.23        |       | 0.32  | 0.009  |       | 0.013 |
| C      |             | 0.5   |       |        | 0.020 |       |
| c1     | 45° (Typ)   |       |       |        |       |       |
| D      | 17.7        |       | 18.1  | 0.697  |       | 0.713 |
| E      | 10          |       | 10.65 | 0.394  |       | 0.419 |
| e      |             | 1.27  |       |        | 0.050 |       |
| e3     |             | 16.51 |       |        | 0.65  |       |
| F      | 7.4         |       | 7.6   | 0.291  |       | 0.299 |
| L      | 0.4         |       | 1.27  | 0.016  |       | 0.050 |
| S      | 8° (Max)    |       |       |        |       |       |

Figure 23. SO28 - 28 Pins, Plastic Micropackage - Package Dimensions



Note: Drawing is not to scale

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**REVISION HISTORY****Table 24. Revision History**

| Date           | Revision | Description of Changes                |
|----------------|----------|---------------------------------------|
| September-1998 | 1        | First Issue                           |
| 28-May-2004    | 2        | Stylesheet update. No content change. |

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