

STV4614C

SWITCH MODE POWER SUPPLY CONTROLLER

ADVANCE DATA

- FLYBACK CONVERTER POWER SUPPLY
- CURRENT MODE CONTROLLED SMPS
- LOW POWER CONSUMPTION
- PRIMARY AND SECONDARY REGULATION
- CONTROL OF CONDUCTION TIME AND OF SWITCHING FREQUENCY
- REVERSE CURRENT CONCEPT
- SOFTSTART
- ADJUSTABLE OVERCURRENT DETECTOR
- SECURITY FUNCTION FOR SHORT-CIRCUIT

DESCRIPTION

The STV4614C is an IC designed to drive the bipolar switching transistor in a Switch Mode Power Supply.

The STV4614C can be used in a flyback converter structure in a primary regulation or in secondary regulation with the reverse current concept.

This concept allows a secondary regulation without need of optocoupler or dedicated transformer to send a regulating signal from secondary to primary side. The regulating signal is sent through the main transformer during a dead time, after the energy have been transfered from primary to secondary side.



PIN CONNECTIONS



This is advance information on a new product now in development or undergoing evaluation. Details are subject to change without notice.

PIN DESCRIPTION

Pin N°	Symbol	Description
1	OVER	Threshold for OVERLOAD at Pin ISENS.
2	FMIN	An external resistor on this pin fixes the minimum switch frequency, reached for min load.
3	PRESEC	Input for the primary and secondary regulation information.
4	REG T	Output of the transconductance error amplifier which is internal by connected to the input of the PWM generator. The external RC network is responsible for the accuracy, dynamic and stability of the regulation loop.
5	IREF	External resistor generating a temperature independent internal current.
6	GND	Ground.
7	P GND	Power ground internally connected to the power elements.
8	REG F	Input of the frequency regulation. The information of the Pin REG T is transferred through a RC network to Pin REG F. This external RC network is responsible for the range and stability of the frequency regulation.
9	OUT L	The current at this pin has the task to collect quickly the charge carriers in the base region of the saturated switch transistor.
10	OUT H	The current at this pin is the base current of the switch transistor.
11	Vcc	Positive power supply.
12	ISENS	Detection of the collector current of the switch transistor to control the conduction time. To avoid damage from the IC and the application, this pin delivers a current of 200mA if the voltage becomes lower than -9.1V (security function).
13	SET DELAY	Time delay for the detection of the secondary regulation information.
14	FMAX	The threshold voltage at FMAX adjusts the output power at which the maximum frequency is reached.

BLOCK DIAGRAM



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CIRCUIT DESCRIPTION

In free running flyback-converters, the STV4614C assumes the control of the bipolar switching transistor and all necessary regulations and monitoring functions.

It consists of seven blocks (see block diagram).

The DC Reference Generator

This blocks generates a reference voltage (Pin IREF). Via an external resistor ($15k\Omega$) a temperature independent current is generated.

The Vcc Monitoring and Protection Block

By monitoring the V_{CC} voltage, the IC determines the mode in which the circuit is working.

Five phases are monitored : start-up, initialisation, softstart, normal mode and switch off.

Also this block identifies dangerous operation conditions. E. g. if V_{CC} is too low, the IC switches off (VIREF goes to zero).

The Sampling Block

This block detects the regulation information coming from a winding of the transformer and generates the sample voltage.

The IC can operate in primary or secondary regulation. By using the secondary regulation, the secondary information (V_{SEC}) has to be larger than the primary information (V_{PR}). Otherwise the SMPS is in primary regulation. This relation is fixed by external elements at Pin PRSEC.

The primary regulation information is sampled during the conduction time of the secondary diodes (secondary conduction time).

The secondary regulation information is included in the amplitude of the first ringing after the secondary conduction time. The amplitude of this ringing is processed by a circuit on the secondary side ("reverse current"). If a failure of the secondary regulation loop occurs, the IC takes over the primary regulation to limit the output voltages.

The sampling block identifies the end of the secondary conduction time. Then it generates a PREP signal for the oscillator block.

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The PREP pulse is generated if following condition is valid :

Tx x $V_{SEC} \ge 2.10^{-7}$ (Volts.Second) (see Figure 1) Otherwise the PREP pulse is forced after a specified time.

The Error Amplifier

This block transforms the sample voltage into the regulation voltage (REG T, REG F). See Figures 5 and 6.

The REGT voltage determines the conduction time of the switching transistor. This REG T voltage is transmitted by an external RC network to the pin REG F, which is responsible for the switching frequency.

In case of overload or underload, the IC switches off. In normal mode, the REGT voltage is proportional to the output power.

The Oscillator

This block generates a SET signal which starts the conduction of the switching transistor. The voltages at REG F, FMAX and SET DELAY and the current generated by the resistor at FMIN determine the time T_B between the PREP pulse and the SET pulse (see normal mode).

The PWM Generator Block

This block detects the collector current of the switching transistor at pin ISENS and generates a RESET signal if this current exceeds the allowed maximum current which is proportional to the REGT voltage. This RESET starts the switch off of the switching transistor.

This block contains some safety functions : if the collector current rises too fast, OVERLOAD is activated. In case of fatal error (ISENS voltage < -9V) ISENS delivers a current which destroyes an external fuse resistor to prevent further damage from the SMPS.

The Output Stage

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This block drives the switching transistor. It has two seperate outputs : OUT H for the conducting time and OUT L for an active switch off (collection of base charge carriers).

FUNCTIONAL DESCRIPTION

Startup Phase

Mains charges an external capacitor at Pin $V_{CC}.$ No current is consumed by the IC.

Initialisation Phase (see Figure 2)

If V_{CC} exceeds V_{INITON} the IC starts the initialisation. When V_{CC} reaches V_{ON}, the IC switches on. The reference voltage at I_{REF} is then 3.5V. The current consumption exceeds the current which is delivered by the mains. This current must be delivered from the V_{CC} capacitor. As a result the V_{CC} voltage decreases. This initialisation ends when the V_{CC} voltage decreases below the V_{ENDIN} voltage. Note : during the initialisation phase no output pulses are generated.

Softstart

When the V_{CC} voltage is lower than V_{ENDIN} voltage, the IC delivers pulses to drive the switching transistor. The power transmission is increased slowly. The velocity of the softstart is fixed internally.

The stored energy in the V_{CC} capacitor supplies the IC during softstart. Afterwards the IC is supplied by a transformer winding.

Normal Mode Phase

If the output voltages of the SMPS have reached their nominal values, the IC enters the normal mode operation.

Timing diagram

A typical waveform of PRSEC signal is shown in Figure 1. The cycle time T consists of four parts :

- T_{ON} time (V_{PRSEC} low) : the switching transistor is on and the current flows into the transformer.
- T_P time (V_{PRSEC} high): the switching transistor is off and the current flows out of the transformer through the secondary diodes.
- T_D time (V_{PRSEC} around zero): the transformer is free oscillating. This time includes a fixed time delay and an adjustable delay (Pin SET DELAY). This T_D time defines the earliest start of a new cycle. This ensures an energy free transformer and a proper detection of the secondary regulation information.
- T_R time (still free oscillating of the transformer) : this time results of the frequency regulation. Its value is defined by the following formula :

WWW.Data TR = 5.10"4 x RFMIN x (VFMAX + 0.7V - VREGF)

with T_R in μ s, R_{FMIN} in Ω and V in Volt. This equation is only valid for V_{REGF} > 0.9V and T_R > 0. Otherwise T_R = 0.

Figure 1 : VPRSEC Voltage Waveform



Frequency and TON Regulation

At low load the switching frequency and ToN is proportional to the output power. If REG T and REG F voltage is equal to the voltage of V_{FMAX} + 0.7V, the switching frequency is maximum. The further increase of output power ($V_{REG T}$, $V_{REG F}$ larger than V_{FMAX} + 0.7V) is reached by only increasing the conduction time which reduces slightly the frequency. In this mode losses in snubber network and switching transistors are low.

The secondary information is manipulated by a circuit on the secondary side. This circuit compares the output voltage with a reference voltage and transmits a "reverse current" during the free oscillating time from the secondary to the primary side of the transformer. This "reverse current" manipulates the amplitude of the ringing, which can be sampled at the PRSEC input.

Switch Off (see Figure 3)

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If the V_{CC} voltage falls under V_{OFF} or another OVERLOAD function is triggered the voltage reference (I_{REF}) and the external switch transistor are switched off. An internal current source is switched on, which discharge the external V_{CC} capacitor below V_{LOW} to ensure a new startup. Therefore the supply current delivered by the mains must be lower than this internal current (I_{LOWOFF}).

If V_{CC} voltage reaches V_{LOW}, the internal current is switched off (no current consumption) and a new startup begins.

This is a safety feature which ensures in case of failure, that the power parts cannot be overloaded, because they are off for a long time (during switch off and startup).

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ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
Vcc	Supply Voltage	20	V
Ti	Junction Temperature	125	°C
T _{stg}	Storage Temperature	-40, +150	•C
Toper	Operating Temperature	0, +70	°C

NORMAL OPERATING CONDITIONS

Pin N°	Symbol	Min.	Тур.	Max.	Unit
1	OVER	0		3.65	۷
2	FMIN	2.65		2.95	٧
3	PRSEC	-4.5		4.5	٧
4	REG T	0.7		4.25	V
8	REG F	0.7		4.25	V
9	OUT L	0		8	V
10	OUTH	-5		8	ν.
11	Vcc	6.3	9	17.5	V
12	ISENS	-11		0	V
13	SET DELAY	0.5		3	V
14	FMAX	0		3.65	V
4	IREGT		±100		μA
3	T _{PRSEC} : Pulse Duration for Reading the Primary or Secondary Information.	500			ns
10	Minimal SET Reaction Time (VSET DELAY = 0.5V)			900	ns

THERMAL DATA

Symbol Parameter Value Unit Bread Junction Ambient Thermal Besistance 90 °C/W				
Symbol	Parameter	Value	Unit	18
	Junction Ambient Thermal Resistance	90	°C/W	46140

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ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C)

Symbol	nbol Parameter Test Conditions		Min.	Тур.	Max.	Unit
PROTECTI	ON					
VPISENS	Protection Current	If the voltage at Pin ISENS is VPISENS, a 100mA current flows out of Pin ISENS	-11	-10	-8	V
IISENS	Protection Current	Maximum current flowing out the Pin ISENS	200			mA
OVER	Voltage at Pin ISENS	IC switchs off (OVERLOAD) because ISENS voltage reaches threshold, fixed by OVER voltage	-3.0		-0.5	V

DC CHARACTERISTICS

IREF	Reference Voltage	Bandgap is activated	3.35	3.5	3.65	V
VINIT/ON	V _{CC} Voltage		15		17	V
INIT/ON	Icc Current				700	μA
Von	Vcc Voltage	If V _{CC} exceeds V _{ON} the bandgap is activated	15.5	16.5	17.5	٧
ION	Current Consumption	Startup mode : V _{CC} > V _{INIT} : bandgap on	13	21.5	28	mA
VENDIN	V _{CC} Voltage	End of initialization (normal mode) : V _{CC} < V _{ENDIN}			17	V
IENDIN	Current Consumption	End of initialisation : V _{CC} < V _{ENDIN}			10	mΑ
Р	Power Consumption	Period time T = 7μ s, T _{ON} = 3μ s Base discharge time T _B = 1μ s			0.6	W
If Vcc bec ILOWOFF is	switched on.	ase (Figure 3) reference voltage (IREF) is switched off and an interna internal current source ILOWOFF is switched off. A new				
VOFF	Vcc Voltage	V _{CC} < V _{OFF} : voltage reference is switched off	6.3	6.7	7.1	V
LOWOFF	Current Consumption	VLOW < VCC < VOFF	6		11	mA
VLOW	Vcc Voltage	V _{CC} < V _{LOW} : the whole IC is switched off	2.5	3	4	V
DVONOF	V _{CC} Range in Normal	DVONOF = VON - VOFF.	8.8	9.5		V

Figure 2 : IC from OFF to ON and Normal Mode



Figure 3 : IC from ON to OFF



6/10

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Symbol	Parameter	Test Conditions	Min.	Тур.	Max.	Unit
PERIODIC Vcc = 9V, R _{FMIN} = 18k	FUNCTIONS - OUTPUT CHARACTE Vover = 3V, Vregt = Vregf = 3V, Vfn (Ω)	ERISTICS (Figure 4) MAX = 1V, VSET DELAY = 0.5V, IOUTH	= 200mA,	Ioutl = 2	00mA,	
VDROPH	Voltage Drop at OUT H	I _{OUTH} = 200mA		1.8	2.2	V
Іоитн	Output H Current				+200	mA
VDROPL	Voltage Drop at OUT L	Ιουτι = -800mA		1.5	2.3	٧
IOUTL	Output L Current		-800		+200	mA
ROUTH	Rising Time of OUT H Signal				150	ns
FOUTH	Falling Time of OUT H Signal				150	ns
ROUTL	Rising Time of OUT L Signal				200	ns
FOUTL	Falling Time of OUT L Signal			<u> </u>	200	ns
TDHL	Time Delay Between the Falling Times of OUT H and OUT L		90		150	ns
V _{zen}	Maximum Voltage on Pins OUT H and OUT L	V _{CC} = 10V to 13V	6.9	7.4	8	V
T _{SET}	Forced SET Time		24	31	43	μs
TSETMAX	Maximum SET Delay	VSET DELAY = 3V		1.3		μs
FMINAB	∆(1/Fmin)	For R = $10k\Omega$ (Ra) and R = $18k\Omega$ (Rc)		9		μs
FMINBC	∆(1/Fmin)	For R = $18k\Omega$ (Rb) and R = $33k\Omega$ (Rc)		16		μs
Δεμαχ	۵(1/Fmax)			14		μs
MINCT	Minimal Conduction Time		350	450	600	ns
Control Ch	naracteristics for Primary Regulation (Figure 5)			• • • • • • • •	
∆V _{REG1}	ΔV _{REG}	At $V_{PR} = 0.5V$ and 2.5V	1.9	1.96	2.1	V
V _{REGPR1}	V _{REG} in Primary Regulation	At V _{PR} = 3V	3.9	4.1	4.3	V
ΔV_{REG2}	ΔV _{REG}	At VPR = 3.3V and 3.6V	1.1	1.35	1.6	V
VPROFF	VPR which Switches the IC Off		4.5			V
Control Ch	aracteristics for Secondary Regulation	on (Figure 6)		• • • • • • • • • • • • • • • • • • • •		
ΔV _{RS1}	ΔV _{REG}	At VSEC = -1.2V and -2.5V	1.1	1.32	1.5	V
VRS28	VREG	At VSEC = -2.8V	3.75	4	4.25	V
∆V _{RS2}	ΔV _{REG}	At V _{SEC} = -3.2V and -3.5V		1.25		V
VSECOFF	VSEC which Switches the IC Off				-4.5	v

Figure 4



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Figure 5



Figure 6



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APPLICATION DIAGRAM

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PACKAGE MECHANICAL DATA 14 PINS - PLASTIC PACKAGE



Dimensions							
	Min.	Тур.	Max.	Min.	Тур.	Max.	
a1	0.51			0.020			
В	1.39		1.65	0.055		0.065	
b		0.5			0.020		
b1		0.25			0.010		٦
D			20			0.787	
E		8.5			0.335		
е		2.54			0.100		
e3		15.24			0.600		
F			7.1			0.280	
i			5.1			0.201	
L		3.3			0.130		Ē
Z	1.27		2.54	0.050		0.100	

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10/10



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