



STSJ100NH3LL

N-CHANNEL 30 V - 0.0032 Ω - 25 A PowerSO-8™ STripFET™ III MOSFET FOR DC-DC CONVERSION

Table 1: General Features

TYPE	V _{DSS}	R _{DS(on)}	I _D
STSJ100NH3LL	30V	< 0.0035 Ω	25A

- TYPICAL R_{DS(on)} = 0.0032 Ω @ 10V
- OPTIMAL R_{DS(on)} x Q_g TRADE-OFF @ 4.5V
- SWITCHING LOSSES REDUCED
- LOW THRESHOLD DEVICE
- IMPROVED JUNCTION-CASE THERMAL RESISTANCE

DESCRIPTION

The **STSJ100NH3LL** utilizes the latest advanced design rules of ST's proprietary STripFET™ technology. This process coupled to unique metallization techniques realizes the most advanced low voltage MOSFET in SO-8 ever produced. The exposed slug reduces the R_{thj-c} improving the current capability.

APPLICATIONS

- SPECIFICALLY DESIGNED AND OPTIMISED FOR HIGH EFFICIENCY CPU CORE DC/DC CONVERTERS FOR MOBILE PCs

Figure 1: Package

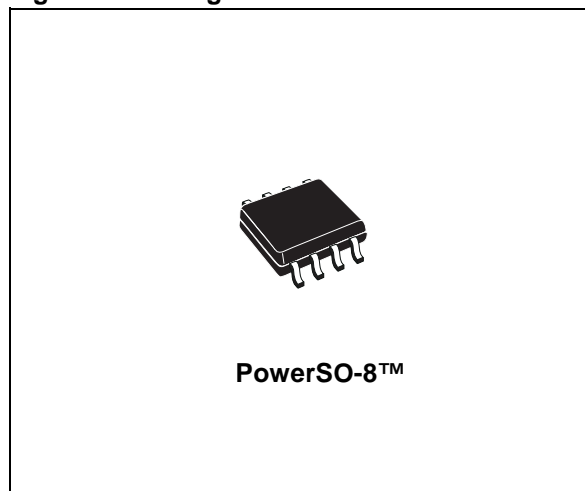


Figure 2: Internal Schematic Diagram

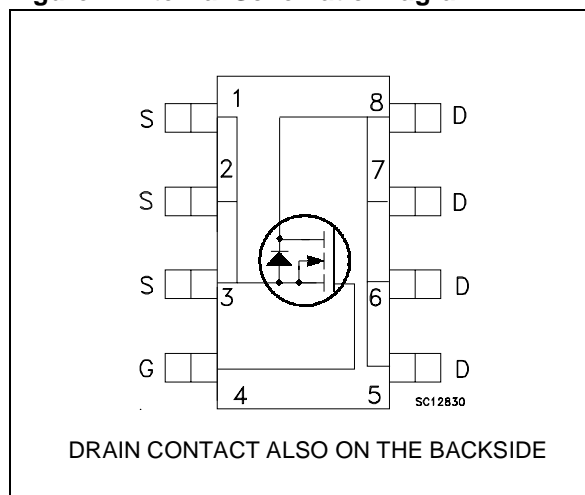


Table 2: Order Codes

SALES TYPE	MARKING	PACKAGE	PACKAGING
STSJ100NH3LL	100H3LL-	PowerSO-8	TAPE & REEL

Table 3: Absolute Maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source Voltage ($V_{GS} = 0$)	30	V
V_{GS}	Gate- source Voltage	± 16	V
$I_{D(2)}$	Drain Current (continuous) at $T_C = 25^\circ\text{C}$	100	A
$I_{D(1)}$	Drain Current (continuous) at $T_C = 25^\circ\text{C}$	25	A
I_D	Drain Current (continuous) at $T_C = 100^\circ\text{C}$	15.6	A
$I_{DM(3)}$	Drain Current (pulsed)	100	A
$P_{tot(2)}$	Total Dissipation at $T_C = 25^\circ\text{C}$	70	W
$P_{tot(1)}$	Total Dissipation at $T_C = 25^\circ\text{C}$	3	W

Table 4: Thermal Data

R_{thj-c}	Thermal Resistance Junction-case	Max	1.8	$^\circ\text{C/W}$
$R_{thj-pcb(4)}$	Thermal Resistance Junction-ambient	Max	42	$^\circ\text{C/W}$
T_j	Maximum Operating Junction Temperature		150	$^\circ\text{C}$
T_{stg}	Storage Temperature		-55 to 150	$^\circ\text{C}$

Table 5: Avalanche Characteristics

Symbol	Parameter	Max Value	Unit
I_{AV}	Not-Repetitive Avalanche Current (pulse width limited by T_j max)	12.5	A
E_{AS}	Single Pulse Avalanche Energy (starting $T_j = 25^\circ\text{C}$, $I_D = I_{AV}$, $V_{DD} = 24\text{ V}$)	1.3	J

ELECTRICAL CHARACTERISTICS ($T_{CASE} = 25^\circ\text{C}$ UNLESS OTHERWISE SPECIFIED)**Table 6: On /Off**

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source Breakdown Voltage	$I_D = 250\mu\text{A}$, $V_{GS} = 0$	30			V
I_{DSS}	Zero Gate Voltage Drain Current ($V_{GS} = 0$)	$V_{DS} = \text{Max Rating}$ $V_{DS} = \text{Max Rating}$, $T_C = 125^\circ\text{C}$			1 10	μA μA
I_{GSS}	Gate-body Leakage Current ($V_{DS} = 0$)	$V_{GS} = \pm 16\text{ V}$			± 100	nA
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}$, $I_D = 250\mu\text{A}$	1			V
$R_{DS(on)}$	Static Drain-source On Resistance	$V_{GS} = 10\text{ V}$, $I_D = 12.5\text{ A}$ $V_{GS} = 4.5\text{ V}$, $I_D = 12.5\text{ A}$		0.0032 0.004	0.0035 0.005	Ω Ω

ELECTRICAL CHARACTERISTICS (CONTINUED)**Table 7: Dynamic**

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
g_{fs} (5)	Forward Transconductance	$V_{DS}=10V, I_D = 12.5A$		30		S
C_{iss} C_{oss} C_{rss}	Input Capacitance Output Capacitance Reverse Transfer Capacitance	$V_{DS} = 25V, f = 1 \text{ MHz}, V_{GS} = 0$		4450 655 50		pF pF pF
R_G	Gate Input Resistance	$f=1\text{MHz}$ Gate DC Bias = 0 Test Signal Level = 20mV Open Drain	1	2	3	Ω

Table 8: Switching On

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$ t_r	Turn-on Delay Time Rise Time	$V_{DD} = 15V, I_D = 12.5A$ $R_G = 4.7\Omega, V_{GS} = 10V$ (see Figure 15)		18 50		ns ns
Q_g Q_{gs} Q_{gd}	Total Gate Charge Gate-Source Charge Gate-Drain Charge	$V_{DD}=15V, I_D=25A$ $V_{GS}=4.5V$ (see Figure 17)		30 12.5 10	40	nC nC nC

Table 9: Switching Off

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(off)}$ t_f	Turn-off Delay Time Fall Time	$V_{DD} = 15V, I_D = 12.5A$ $R_G = 4.7\Omega, V_{GS} = 10V$ (see Figure 15)		75 8		ns ns

Table 10: Source Drain Diode

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{SD} I_{SDM}	Source-drain Current Source-drain Current (pulsed)				25 100	A A
$V_{SD(5)}$	Forward On Voltage	$I_{SD} = 25A, V_{GS} = 0$			1.3	V
t_{rr} Q_{rr} I_{RRM}	Reverse Recovery Time Reverse Recovery Charge Reverse Recovery Current	$I_{SD} = 25A, di/dt = 100A/\mu s$ $V_{DD} = 25V, T_j = 150^\circ C$ (see Figure 16)		32 34 2.1		ns nC A

Notes

1. This value is noted according to $R_{thj-pcb}$
2. This value is noted according to R_{thj-c}
3. Pulse width limited by safe operating area
4. When Mounted on 1 inch² FR-4 board, 2 oz Cu ($t \leq 10 \text{ sec.}$)
5. Pulsed: pulse duration=300 μs , duty cycle 1.5%

Figure 3: Safe Operating Area

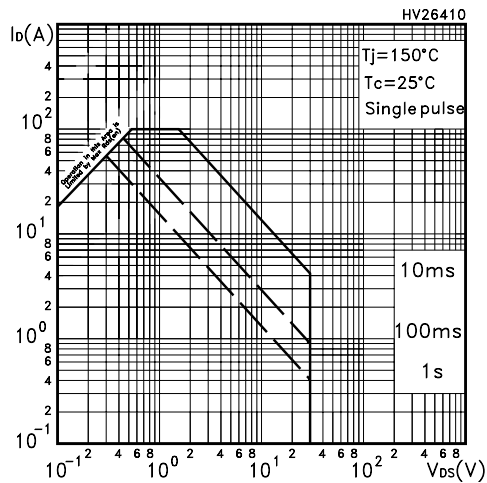


Figure 4: Output Characteristics

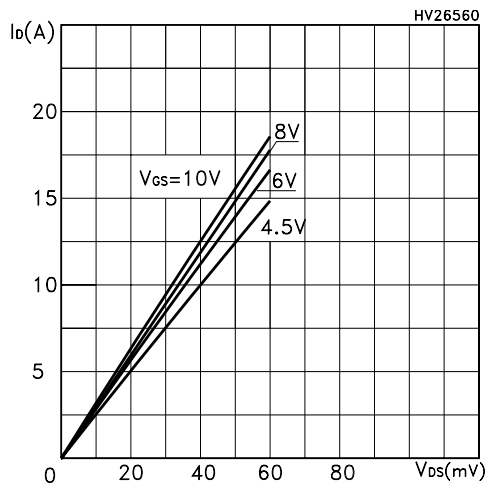


Figure 5: Transconductance

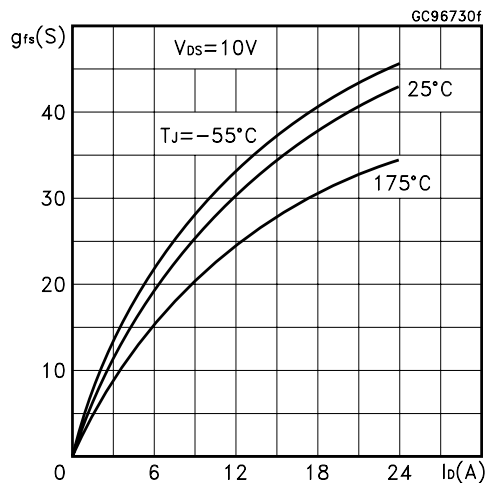


Figure 6: Thermal Impedance

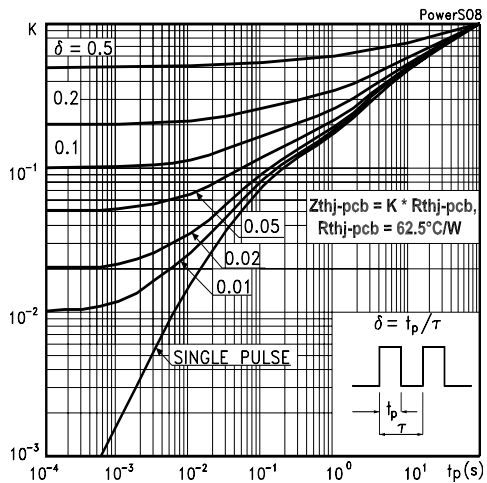


Figure 7: Transfer Characteristics

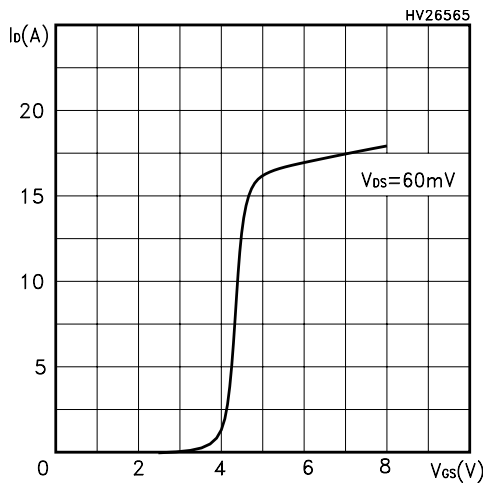


Figure 8: Static Drain-source On Resistance

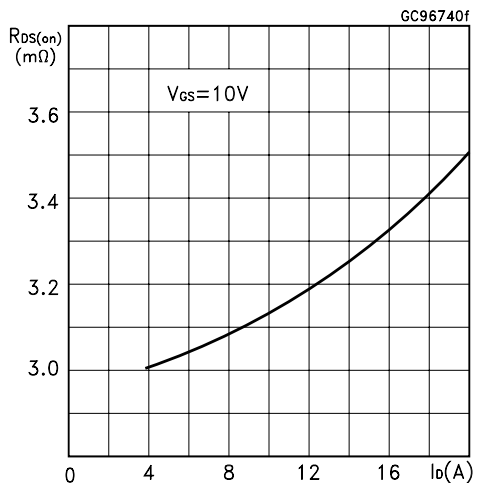


Figure 9: Gate Charge vs Gate-source Voltage

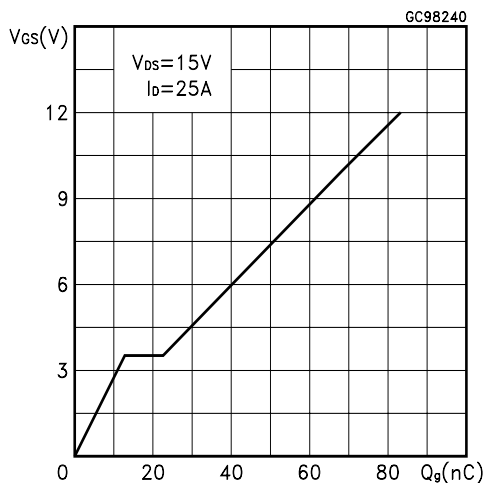


Figure 10: Normalized Gate Threshold Voltage vs Temperature

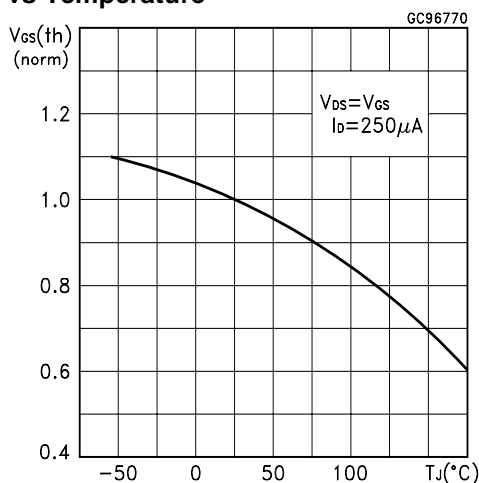


Figure 11: Normalized On Resistance vs Temperature

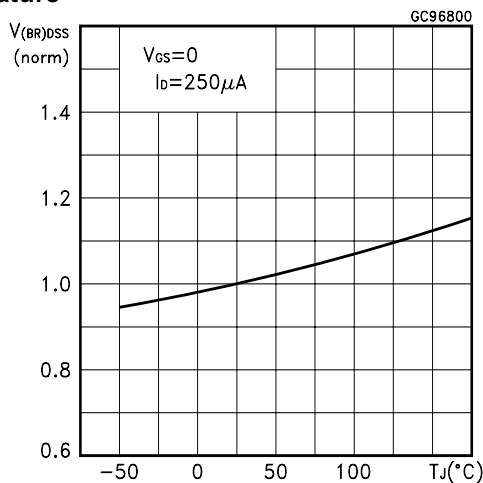


Figure 12: Capacitance Variations

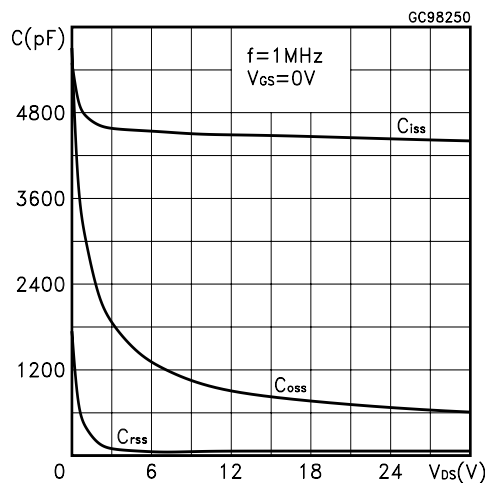


Figure 13: Normalized BVDSS vs Temperature

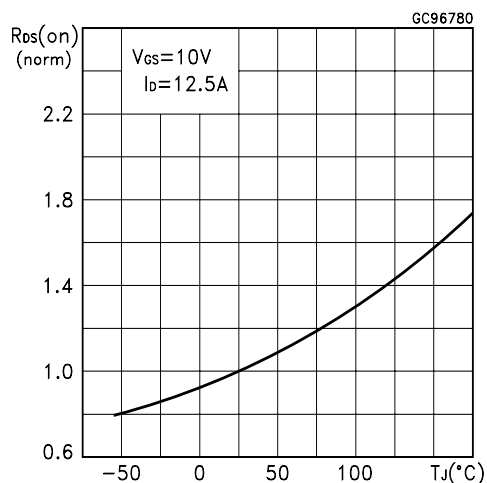


Figure 14: Source-Drain Diode Forward Characteristics

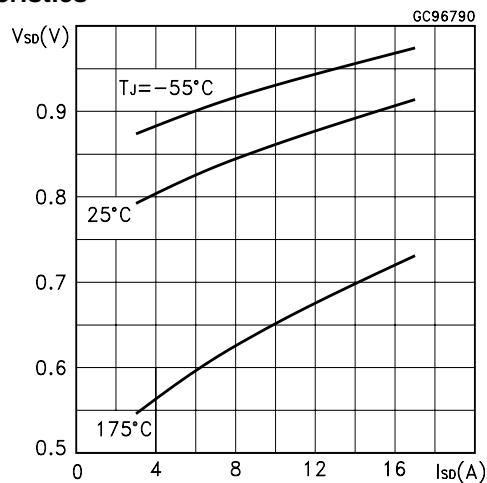
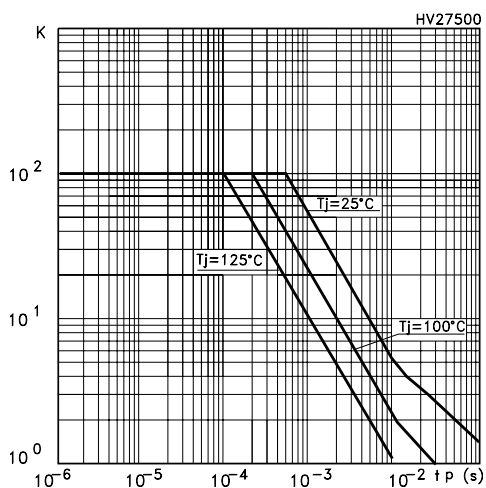


Table 11: Allowable I_{AV} vs. Time in Avalanche



The previous curve gives the single pulse safe operating area for unclamped inductive loads, under the following conditions:

$$P_{D(AVE)} = 0.5 \cdot (1.3 \cdot BV_{DSS} \cdot I_{AV})$$

$$E_{AS(AR)} = P_{D(AVE)} \cdot t_{AV}$$

Where:

I_{AV} is the Allowable Current in Avalanche

$P_{D(AVE)}$ is the Average Power Dissipation in Avalanche (Single Pulse)

t_{AV} is the Time in Avalanche

Figure 15: Switching Times Test Circuit For Resistive Load

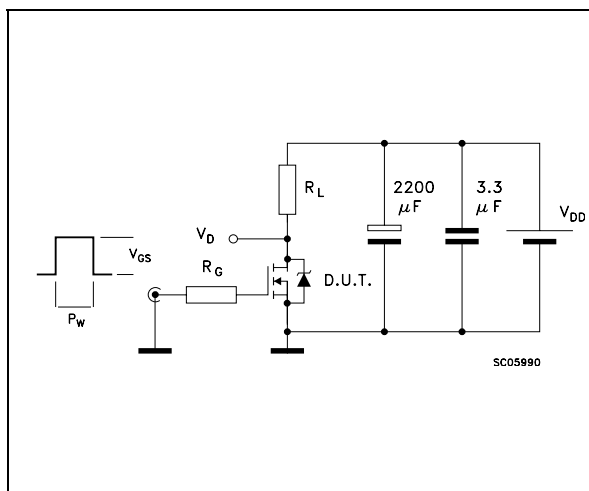


Figure 16: Test Circuit For Diode Recovery Times

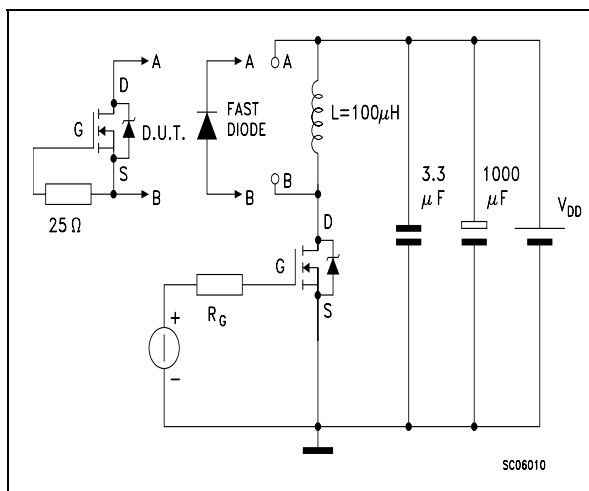
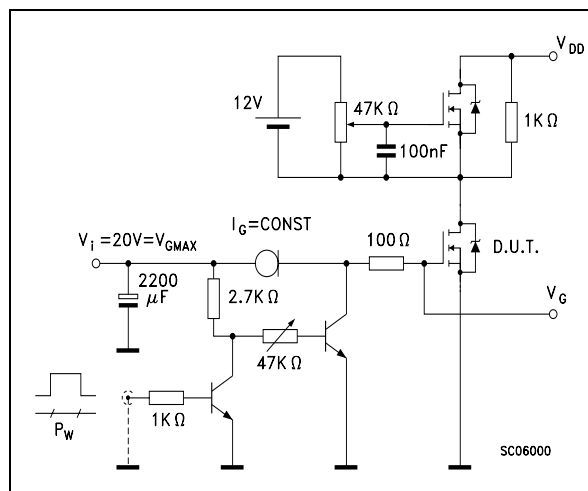


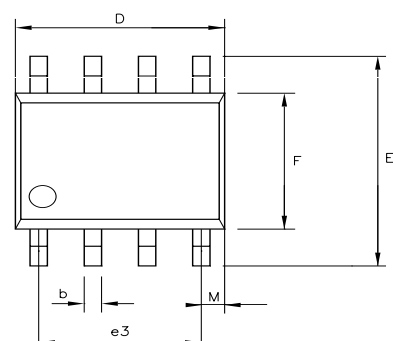
Figure 17: Gate Charge Test Circuit



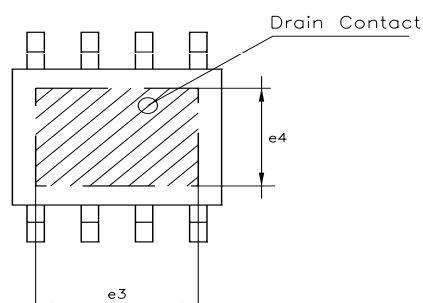
In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect . The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com

PowerSO-8™ MECHANICAL DATA

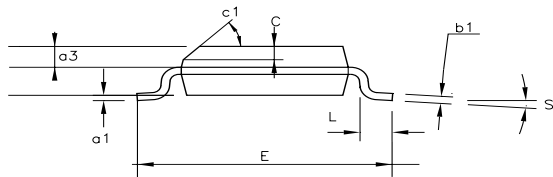
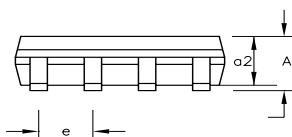
DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			1.75			0.068
a1	0.1		0.25	0.003		0.009
a2			1.65			0.064
a3	0.65		0.85	0.025		0.033
b	0.35		0.48	0.013		0.018
b1	0.19		0.25	0.007		0.010
C	0.25		0.5	0.010		0.019
c1	45° (typ.)					
D	4.8		5.0	0.188		0.196
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		3.81			0.150	
e4		2.79			0.110	
F	3.8		4.0	0.14		0.157
L	0.4		1.27	0.015		0.050
M			0.6			0.023
S	8° (max.)					



(Top View)



(Bottom View)



PowerSO-8

Table 12: Revision History

Date	Revision	Description of Changes
14-Sep-2004	2	Preliminary Data.
23-May-2005	3	New values on table 5
29-Jun-2005	4	New R_G value on table 6
16-Nov-2005	5	Complete version

Information furnished is believed to be accurate and reliable. However, STMicroelectronics assumes no responsibility for the consequences of use of such information nor for any infringement of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of STMicroelectronics. Specifications mentioned in this publication are subject to change without notice. This publication supersedes and replaces all information previously supplied. STMicroelectronics products are not authorized for use as critical components in life support devices or systems without express written approval of STMicroelectronics.

The ST logo is a registered trademark of STMicroelectronics

All other names are the property of their respective owners

© 2005 STMicroelectronics - All Rights Reserved

STMicroelectronics group of companies

Australia - Belgium - Brazil - Canada - China - Czech Republic - Finland - France - Germany - Hong Kong - India - Israel - Italy - Japan - Malaysia - Malta - Morocco - Singapore - Spain - Sweden - Switzerland - United Kingdom - United States of America