



SGS-THOMSON
MICROELECTRONICS

STP4N40
STP4N40FI

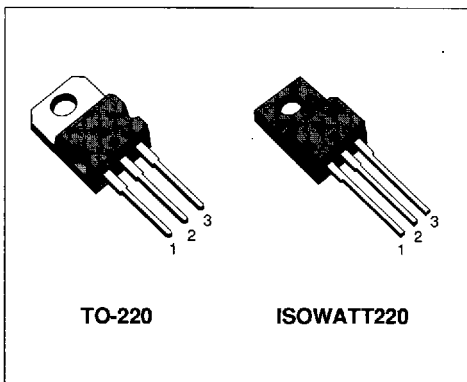
N - CHANNEL ENHANCEMENT MODE POWER MOS TRANSISTOR

TYPE	V _{DSS}	R _{DS(on)}	I _D
STP4N40	400 V	< 2.1 Ω	4 A
STP4N40FI	400 V	< 2.1 Ω	3 A

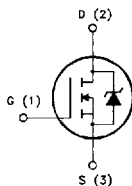
- TYPICAL R_{DS(on)} = 1.65 Ω
- AVALANCHE RUGGED TECHNOLOGY
- 100% AVALANCHE TESTED
- REPETITIVE AVALANCHE DATA AT 100°C
- APPLICATION ORIENTED CHARACTERIZATION

APPLICATIONS

- HIGH CURRENT, HIGH SPEED SWITCHING
- SWITCH MODE POWER SUPPLIES (SMPS)
- CHOPPER REGULATORS, CONVERTERS, MOTOR CONTROL, LIGHTING FOR INDUSTRIAL AND CONSUMER ENVIRONMENT



INTERNAL SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value		Unit
		STP4N40	STP4N40FI	
V _{DS}	Drain-source Voltage (V _{GS} = 0)	400		V
V _{DGR}	Drain- gate Voltage (R _{GS} = 20 k Ω)	400		V
V _{GS}	Gate-source Voltage	± 20		V
I _D	Drain Current (continuous) at T _c = 25 °C	4	3	A
I _D	Drain Current (continuous) at T _c = 100 °C	2.5	1.9	A
I _{DM} (*)	Drain Current (pulsed)	16	16	A
P _{tot}	Total Dissipation at T _c = 25 °C	75	35	W
	Derating Factor	0.6	0.28	W/°C
V _{ISO}	Insulation Withstand Voltage (DC)	—	2000	V
T _{stg}	Storage Temperature	-65 to 150		°C
T _j	Max. Operating Junction Temperature	150		°C

(*) Pulse width limited by safe operating area

THERMAL DATA

		TO-220	ISOWATT220	
$R_{thj-case}$	Thermal Resistance Junction-case Max	1.67	3.57	$^{\circ}\text{C/W}$
$R_{thj-amb}$	Thermal Resistance Junction-ambient Max		62.5	$^{\circ}\text{C/W}$
$R_{thc-sink}$	Thermal Resistance Case-sink Typ		0.5	$^{\circ}\text{C/W}$
T_j	Maximum Lead Temperature For Soldering Purpose		300	$^{\circ}\text{C}$

AVALANCHE CHARACTERISTICS

Symbol	Parameter	Max Value	Unit
I_{AR}	Avalanche Current, Repetitive or Not-Repetitive (pulse width limited by T_j max, $\delta < 1\%$)	4	A
E_{AS}	Single Pulse Avalanche Energy (starting $T_j = 25^{\circ}\text{C}$, $I_D = I_{AR}$, $V_{DD} = 50\text{ V}$)	110	mJ
E_{AR}	Repetitive Avalanche Energy (pulse width limited by T_j max, $\delta < 1\%$)	7	mJ
I_{AR}	Avalanche Current, Repetitive or Not-Repetitive ($T_c = 100^{\circ}\text{C}$, pulse width limited by T_j max, $\delta < 1\%$)	2.5	A

ELECTRICAL CHARACTERISTICS ($T_{case} = 25^{\circ}\text{C}$ unless otherwise specified)

OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source Breakdown Voltage	$I_D = 250\text{ }\mu\text{A}$ $V_{GS} = 0$	400			V
I_{DSS}	Zero Gate Voltage Drain Current ($V_{GS} = 0$)	$V_{DS} = \text{Max Rating}$ $V_{DS} = \text{Max Rating} \times 0.8$ $T_c = 125^{\circ}\text{C}$			250 1000	μA μA
I_{GSS}	Gate-body Leakage Current ($V_{DS} = 0$)	$V_{GS} = \pm 20\text{ V}$			± 100	nA

ON (*)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}$ $I_D = 250\text{ }\mu\text{A}$	2	3	4	V
$R_{DS(on)}$	Static Drain-source On Resistance	$V_{GS} = 10\text{ V}$ $I_D = 2\text{ A}$ $V_{GS} = 10\text{ V}$ $I_D = 2\text{ A}$ $T_c = 100^{\circ}\text{C}$		1.65	2.1 4.2	Ω Ω
$I_{D(on)}$	On State Drain Current	$V_{DS} > I_{D(on)} \times R_{DS(on)max}$ $V_{GS} = 10\text{ V}$	4			A

DYNAMIC

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$g_{fs} (*)$	Forward Transconductance	$V_{DS} > I_{D(on)} \times R_{DS(on)max}$ $I_D = 2\text{ A}$	1	2.1		S
C_{iss}	Input Capacitance	$V_{DS} = 25\text{ V}$ $f = 1\text{ MHz}$ $V_{GS} = 0$		350	450	pF
C_{oss}	Output Capacitance			68	90	pF
C_{rss}	Reverse Transfer Capacitance			32	45	pF

ELECTRICAL CHARACTERISTICS (continued)

SWITCHING ON

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on Time	$V_{DD} = 175\text{ V}$ $I_D = 2\text{ A}$		25	33	ns
t_r	Rise Time	$R_G = 50\ \Omega$ $V_{GS} = 10\text{ V}$ (see test circuit, figure 3)		70	90	ns
$(di/dt)_{on}$	Turn-on Current Slope	$V_{DD} = 320\text{ V}$ $I_D = 4\text{ A}$ $R_G = 50\ \Omega$ $V_{GS} = 10\text{ V}$ (see test circuit, figure 5)		110		A/ μ s
Q_g	Total Gate Charge	$V_{DD} = 320\text{ V}$ $I_D = 4\text{ A}$ $V_{GS} = 10\text{ V}$		25	35	nC
Q_{gs}	Gate-Source Charge			7		nC
Q_{gd}	Gate-Drain Charge			11		nC

SWITCHING OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{r(Voff)}$	Off-voltage Rise Time	$V_{DD} = 320\text{ V}$ $I_D = 4\text{ A}$		50	65	ns
t_f	Fall Time	$R_G = 50\ \Omega$ $V_{GS} = 10\text{ V}$		28	35	ns
t_c	Cross-over Time	(see test circuit, figure 5)		75	95	ns

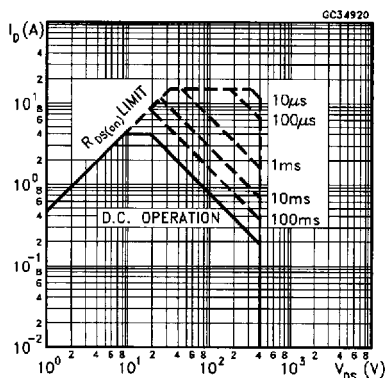
SOURCE DRAIN DIODE

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain Current				4	A
$I_{SDM}(\bullet)$	Source-drain Current (pulsed)				16	A
$V_{SD}(\ast)$	Forward On Voltage	$I_{SD} = 4\text{ A}$ $V_{GS} = 0$			2	V
t_{rr}	Reverse Recovery Time	$I_{SD} = 4\text{ A}$ $di/dt = 100\text{ A}/\mu\text{s}$ $V_{DD} = 100\text{ V}$ $T_j = 150\text{ }^\circ\text{C}$		400		ns
Q_{rr}	Reverse Recovery Charge	(see test circuit, figure 5)		5.9		μC
I_{RRM}	Reverse Recovery Current			29.5		A

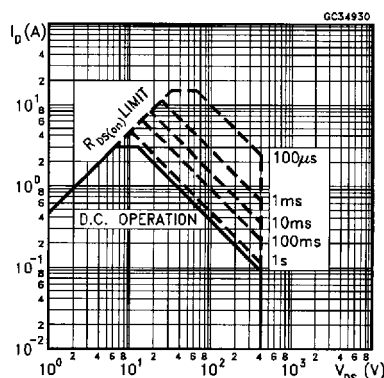
(*) Pulsed: Pulse duration = 300 μs , duty cycle 1.5 %

(\bullet) Pulse width limited by safe operating area

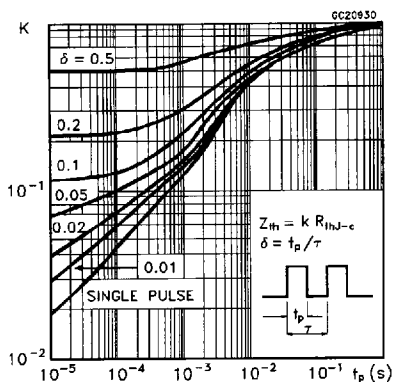
Safe Operating Areas For TO-220



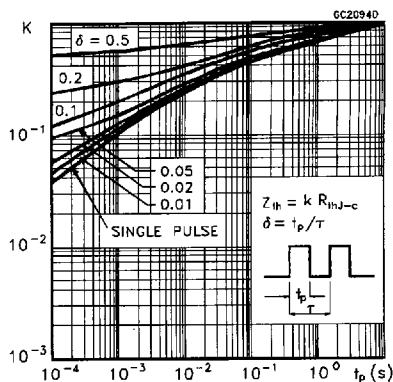
Safe Operating Areas For ISOWATT220



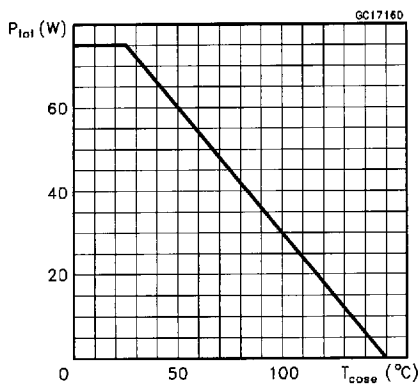
Thermal Impedance For TO-220



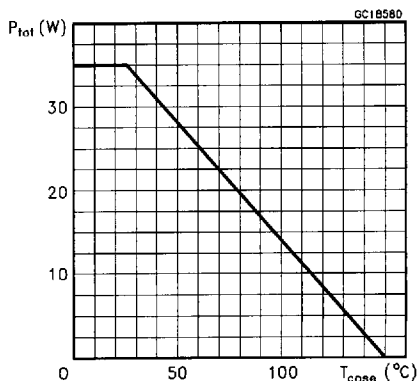
Thermal Impedance For ISOWATT220



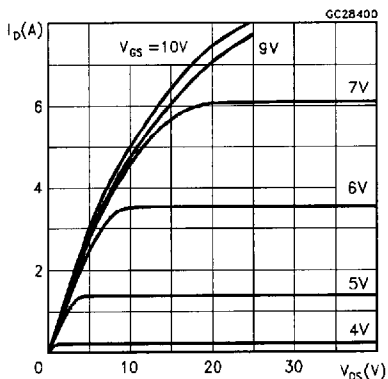
Derating Curve For TO-220



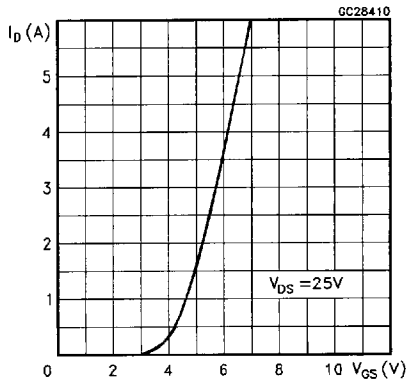
Derating Curve For ISOWATT220



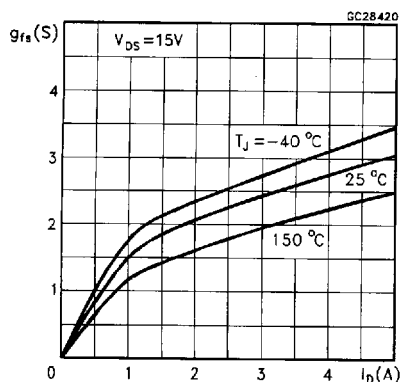
Output Characteristics



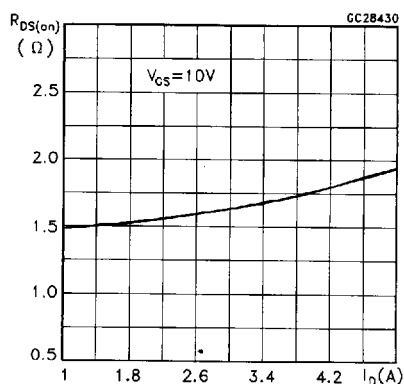
Transfer Characteristics



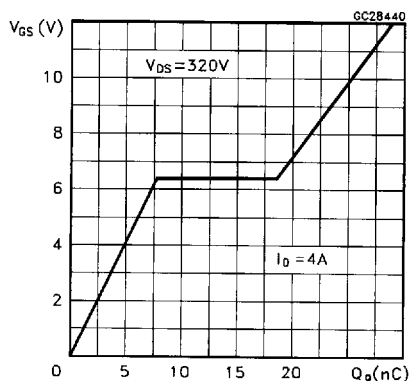
Transconductance



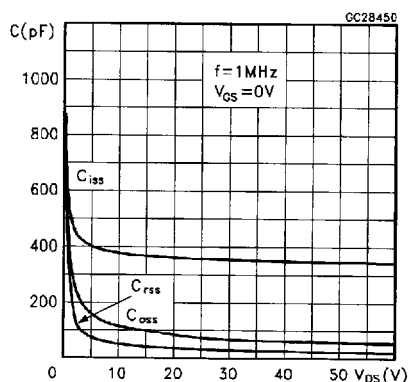
Static Drain-source On Resistance



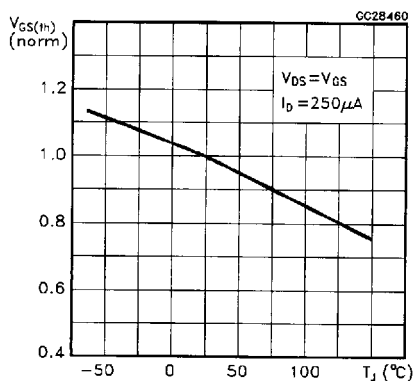
Gate Charge vs Gate-source Voltage



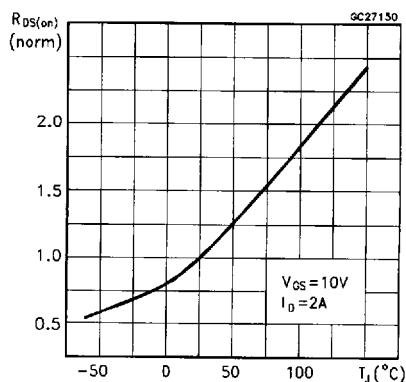
Capacitance Variations



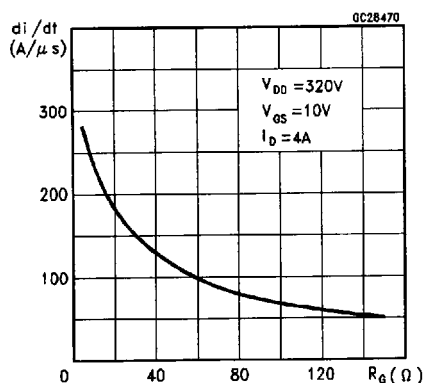
Normalized Gate Threshold Voltage vs Temperature



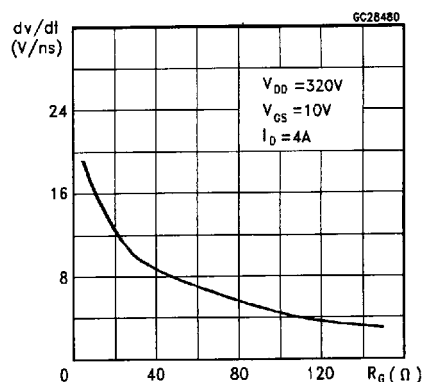
Normalized On Resistance vs Temperature



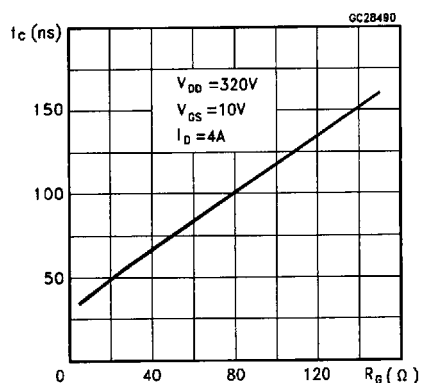
Turn-on Current Slope



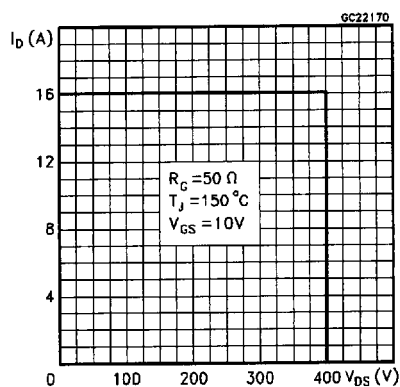
Turn-off Drain-source Voltage Slope



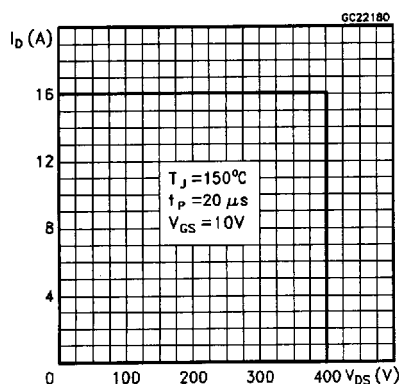
Cross-over Time



Switching Safe Operating Area



Accidental Overload Area



Source-drain Diode Forward Characteristics

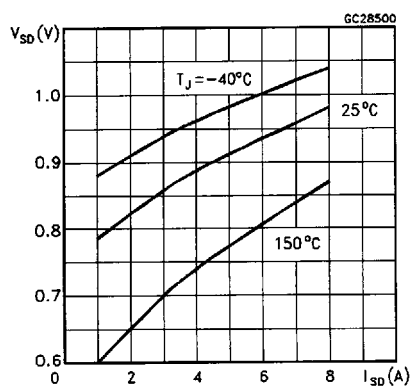


Fig. 1: Unclamped Inductive Load Test Circuits

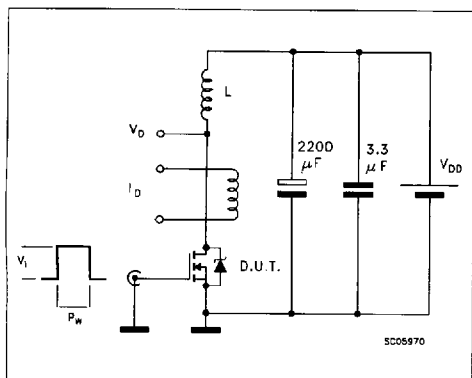


Fig. 2: Unclamped Inductive Waveforms

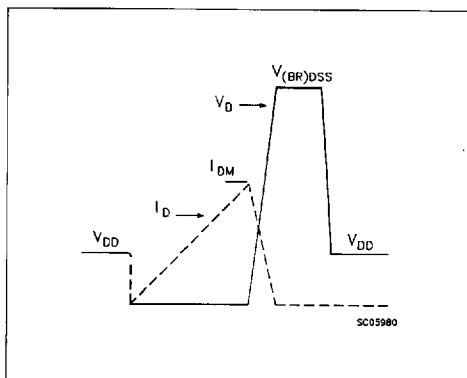


Fig. 3: Switching Times Test Circuits For Resistive Load

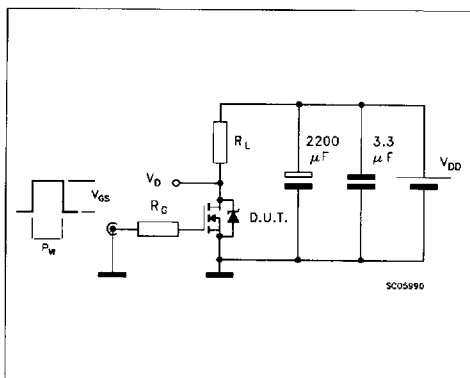


Fig. 4: Gate Charge Test Circuit

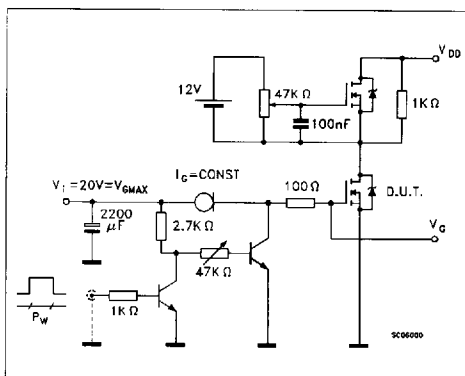


Fig. 5: Test Circuit For Inductive Load Switching And Diode Reverse Recovery Time

