



STP21NM60N-F21NM60N-STW21NM60N STB21NM60N-STB21NM60N-1

N-channel 600 V - 0.17 Ω - 17 A TO-220 - TO-220FP - D²PAK - I²PAK - TO-247 second generation MDmesh™ Power MOSFET

Features

Type	V _{DSS} (@T _{jmax})	R _{DS(on)} max	I _D
STB21NM60N	650 V	< 0.22 Ω	17 A
STB21NM60N-1	650 V	< 0.22 Ω	17 A
STF21NM60N	650 V	< 0.22 Ω	17 A ⁽¹⁾
STP21NM60N	650 V	< 0.22 Ω	17 A
STW21NM60N	650 V	< 0.22 Ω	17 A

1. Limited by maximum temperature allowed

- 100% avalanche tested
- Low input capacitance and gate charge
- Low gate input resistance

Application

- Switching applications

Description

This series of devices implements the second generation of MDmesh™ technology. This revolutionary Power MOSFET associates a new vertical structure to the company's strip layout to yield one of the world's lowest on-resistance and gate charge. It is therefore suitable for the most demanding high efficiency converters.

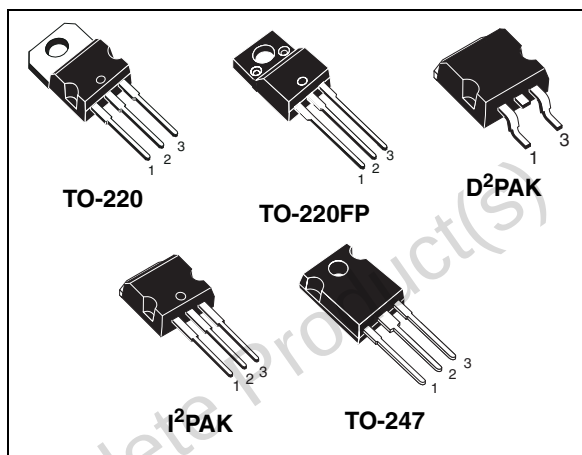


Figure 1. Internal schematic diagram

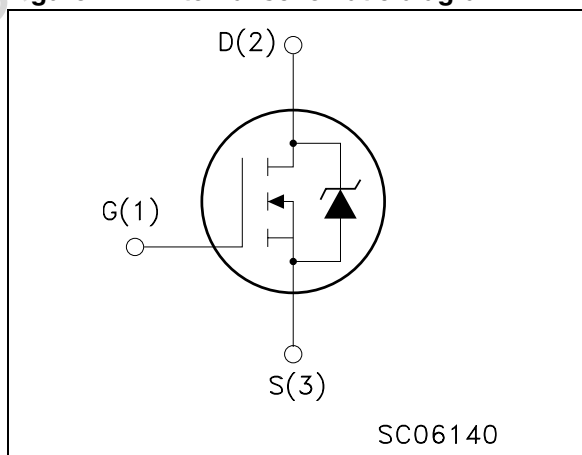


Table 1. Device summary

Order codes	Marking	Package	Packaging
STB21NM60N	B21NM60N	D ² PAK	Tape and reel
STB21NM60N-1	B21NM60N	I ² PAK	Tube
STF21NM60N	F21NM60N	TO-220FP	Tube
STP21NM60N	P21NM60N	TO-220	Tube
STW21NM60N	W21NM60N	TO-247	Tube

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1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value		Unit
		TO-220/D ² PAK I ² PAK / TO-247	TO-220FP	
V_{DS}	Drain-source voltage ($V_{GS} = 0$)	600		V
V_{GS}	Gate- source voltage	± 25		V
I_D	Drain current (continuous) at $T_C = 25\text{ }^{\circ}\text{C}$	17	17 ⁽¹⁾	A
I_D	Drain current (continuous) at $T_C = 100\text{ }^{\circ}\text{C}$	10	10 ⁽¹⁾	A
$I_{DM}^{(2)}$	Drain current (pulsed)	68	68 ⁽¹⁾	A
P_{TOT}	Total dissipation at $T_C = 25\text{ }^{\circ}\text{C}$	140	30	W
$dv/dt^{(3)}$	Peak diode recovery voltage slope	15		V/ns
V_{ISO}	Insulation withstand voltage (RMS) from all three leads to external heat sink ($t=1\text{ s}$; $T_C = 25\text{ }^{\circ}\text{C}$)	--	2500	V
T_{stg}	Storage temperature	-55 to 150		$^{\circ}\text{C}$
T_j	Max. operating junction temperature	150		$^{\circ}\text{C}$

1. Limited only by maximum temperature allowed
2. Pulse width limited by safe operating area
3. $I_{SD} \leq 17\text{ A}$, $di/dt \leq 480\text{ A}/\mu\text{s}$, $V_{DD} = 80\% V_{(BR)DSS}$

Table 3. Thermal data

Symbol	Parameter	TO-220	D ² PAK	I ² PAK	TO-220FP	TO-247	Unit
R _{thj-case}	Thermal resistance junction-case max	0.89			4.21	0.89	°C/W
R _{thj-pcb}	Thermal resistance junction-pcb max	--	30	--	--	--	°C/W
R _{thj-amb}	Thermal resistance junction-ambient max	62.5	--	62.5		50	°C/W
T _l	Maximum lead temperature for soldering purpose	300					°C

Table 4. Avalanche characteristics

Symbol	Parameter	Max value	Unit
I_{AS}	Avalanche current, repetitive or not-repetitive (pulse width limited by T_j max)	8.5	A
E_{AS}	Single pulse avalanche energy (starting $T_j = 25\text{ }^{\circ}\text{C}$, $I_D = I_{AS}$, $V_{DD} = 50\text{ V}$)	610	mJ

2 Electrical characteristics

($T_{CASE}=25^{\circ}\text{C}$ unless otherwise specified)

Table 5. On/off states

Symbol	Parameter	Test conditions	Value			Unit
			Min.	Typ.	Max.	
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = 1\text{ mA}$, $V_{GS} = 0$	600			V
$dv/dt^{(1)}$	Drain source voltage slope	$V_{DD} = 480\text{ V}$, $I_D = 17\text{ A}$, $V_{GS} = 10\text{ V}$	48			V/ns
I_{DSS}	Zero gate voltage drain current ($V_{GS} = 0$)	$V_{DS} = \text{Max rating}$ $V_{DS} = \text{Max rating @ } 125^{\circ}\text{C}$			1 100	μA μA
I_{GSS}	Gate-body leakage current ($V_{DS} = 0$)	$V_{GS} = \pm 20\text{ V}$			100	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$, $I_D = 250\text{ }\mu\text{A}$	2	3	4	V
$R_{DS(on)}$	Static drain-source on resistance	$V_{GS} = 10\text{ V}$, $I_D = 8.5\text{ A}$		0.170	0.220	Ω

1. Characteristic value at turn off on inductive load

Table 6. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$g_{fs}^{(1)}$	Forward transconductance	$V_{DS} = 15\text{ V}$, $I_D = 8.5\text{ A}$		12		S
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	$V_{DS} = 50\text{ V}$, $f = 1\text{ MHz}$, $V_{GS} = 0$		1900 110 15		pF pF pF
$C_{oss\text{ eq.}}^{(2)}$	Equivalent output capacitance	$V_{GS} = 0$, $V_{DS} = 0\text{ to }480\text{ V}$		282		pF
$t_{d(on)}$ t_r $t_{d(off)}$ t_f	Turn-on delay time Rise time Turn-off delay time Fall time	$V_{DD} = 300\text{ V}$, $I_D = 8.5\text{ A}$ $R_G = 4.7\text{ }\Omega$, $V_{GS} = 10\text{ V}$ (see Figure 23), (see Figure 18)		22 15 84 31		ns ns ns ns
Q_g Q_{gs} Q_{gd}	Total gate charge Gate-source charge Gate-drain charge	$V_{DD} = 480\text{ V}$, $I_D = 17\text{ A}$, $V_{GS} = 10\text{ V}$, (see Figure 19)		66 10 33		nC nC nC
R_g	Gate input resistance	$f = 1\text{ MHz}$ Gate DC Bias = 0 test signal level = 20 mV open drain		2		Ω

1. Pulsed: pulse duration = 300 μs , duty cycle 1.5%

2. $C_{oss\text{ eq.}}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current				17	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)				68	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 17\text{ A}$, $V_{GS} = 0$			1.5	V
t_{rr}	Reverse recovery time	$I_{SD} = 17\text{ A}$, $V_{DD} = 100\text{ V}$ $di/dt = 100\text{ A}/\mu\text{s}$ (see Figure 20)		372		ns
Q_{rr}	Reverse recovery charge			4.6		μC
I_{RRM}	Reverse recovery current			25		A
t_{rr}	Reverse recovery time	$I_{SD} = 17\text{ A}$, $V_{DD} = 100\text{ V}$ $di/dt = 100\text{ A}/\mu\text{s}$, $T_j = 150\text{ }^\circ\text{C}$ (see Figure 20)		486		ns
Q_{rr}	Reverse recovery charge			6.3		μC
I_{RRM}	Reverse recovery current			26		A

1. Pulse width limited by safe operating area

2. Pulsed: Pulse duration = 300 μs , duty cycle 1.5%.

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area for TO-220 / D²PAK / I²PAK

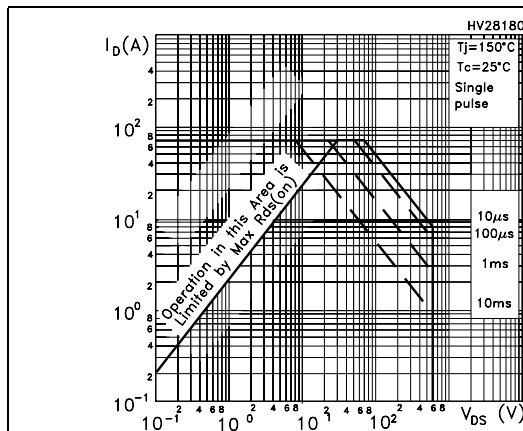


Figure 3. Thermal impedance for TO-220 / D²PAK / I²PAK

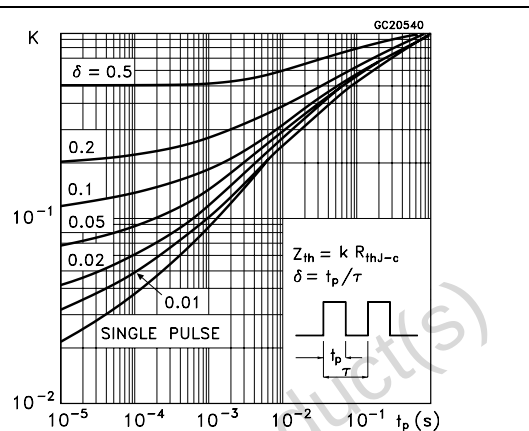


Figure 4. Safe operating area for TO-220FP

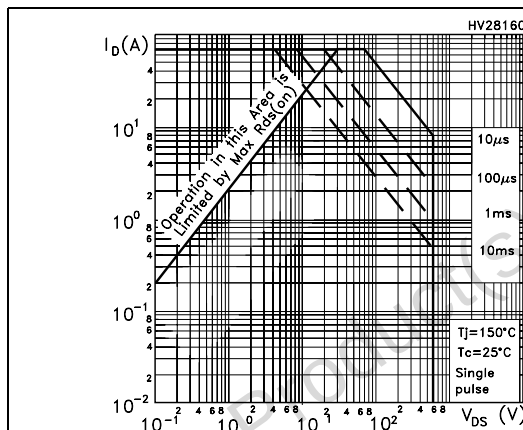


Figure 5. Thermal impedance for TO-220FP

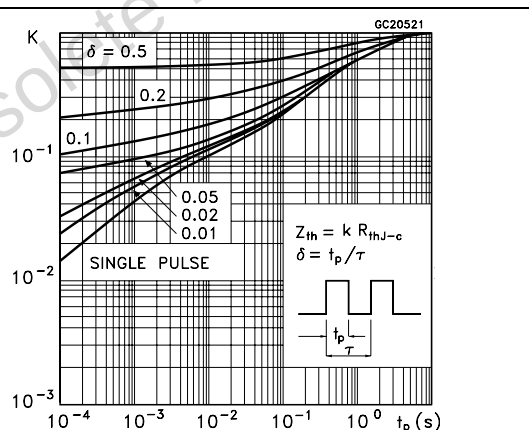


Figure 6. Safe operating area for TO-247

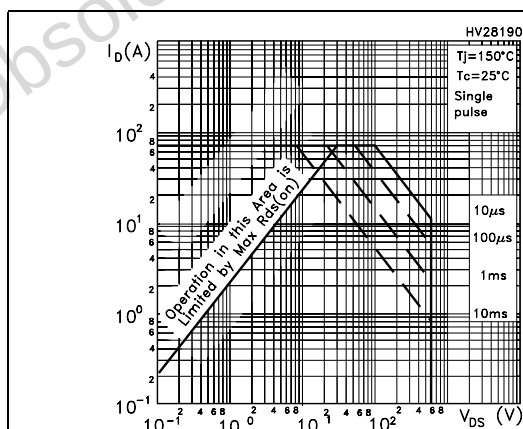


Figure 7. Thermal impedance for TO-247

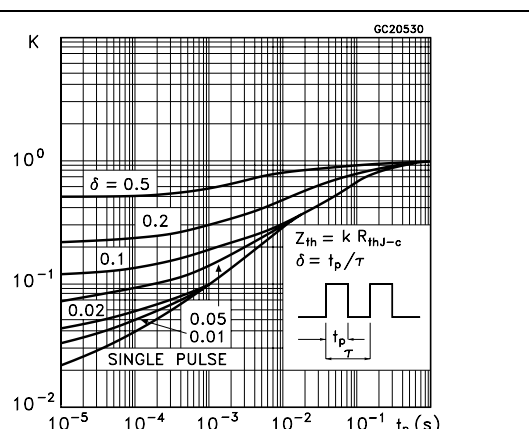


Figure 8. Output characteristics

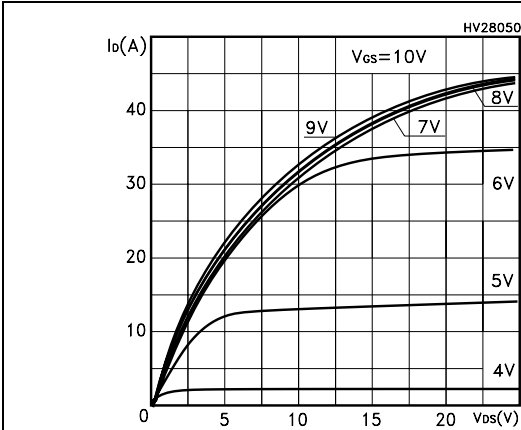


Figure 9. Transfer characteristics

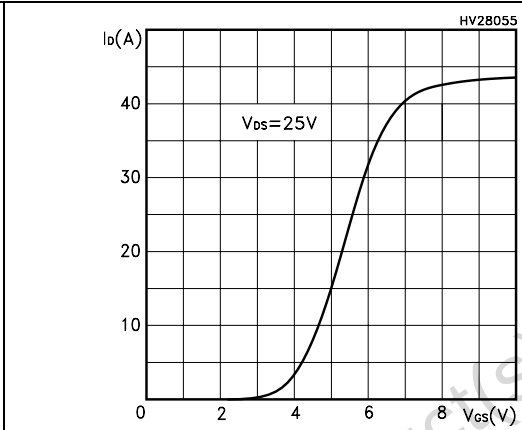


Figure 10. Transconductance

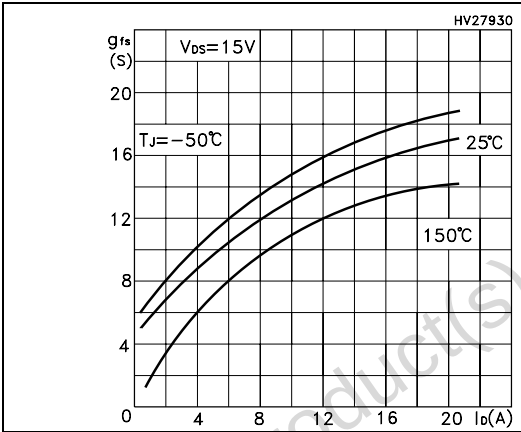


Figure 11. Static drain-source on resistance

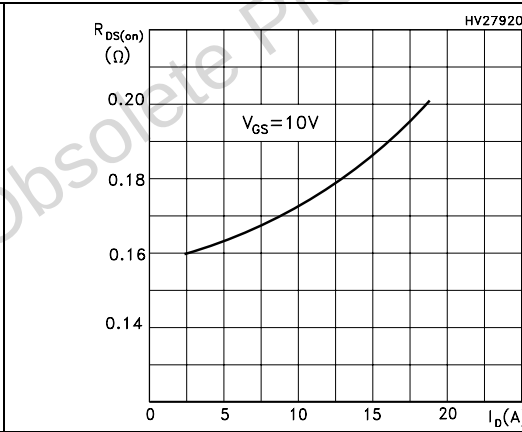


Figure 12. Gate charge vs gate-source voltage

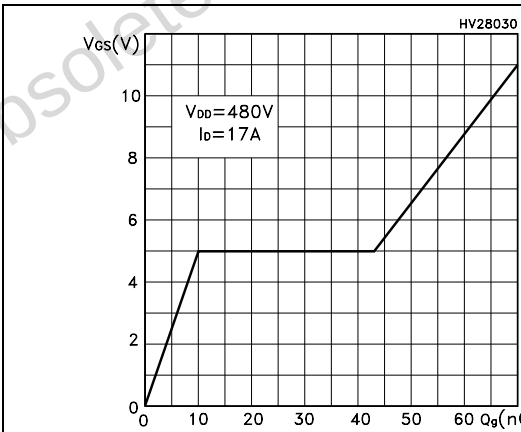


Figure 13. Capacitance variations

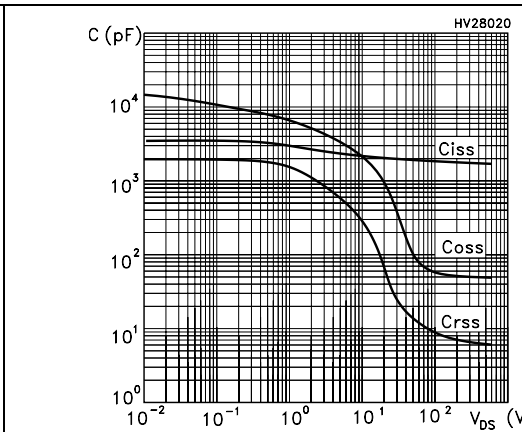


Figure 14. Normalized gate threshold voltage vs temperature

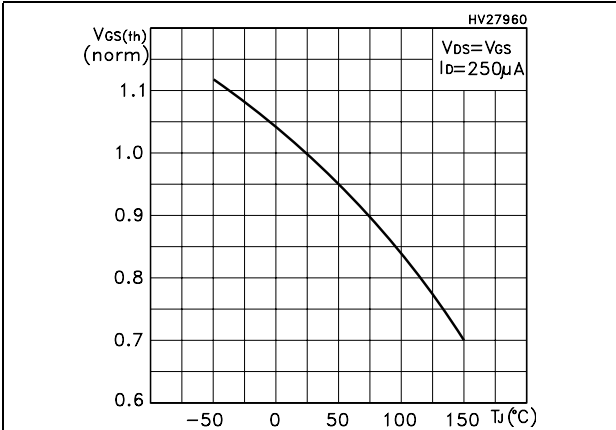


Figure 15. Normalized on resistance vs temperature

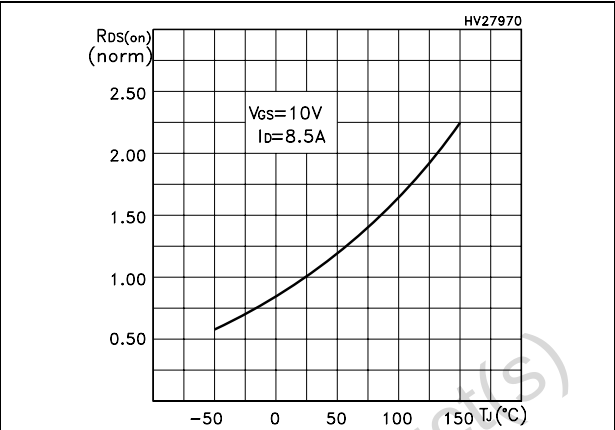


Figure 16. Source-drain diode forward characteristics

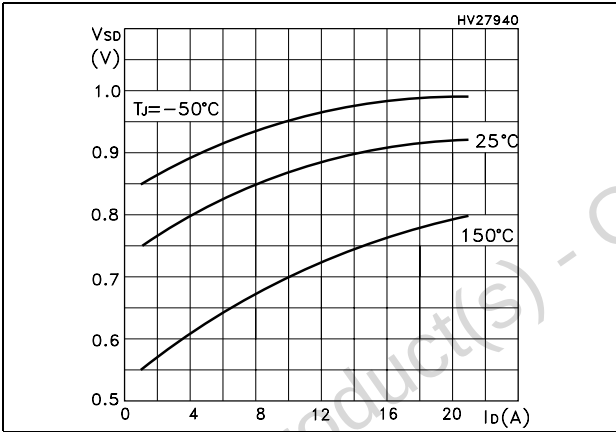
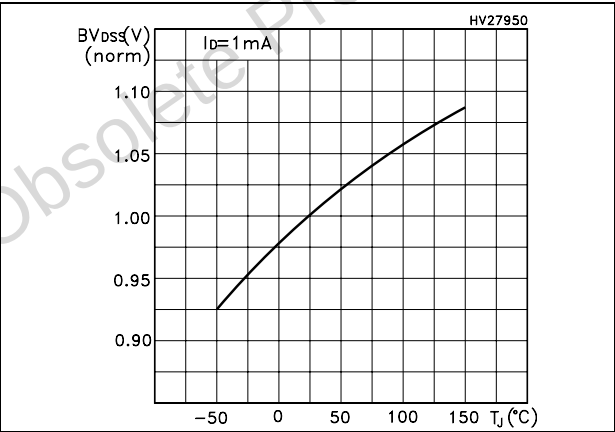


Figure 17. Normalized BV_{DSS} vs temperature



3 Test circuit

Figure 18. Switching times test circuit for resistive load

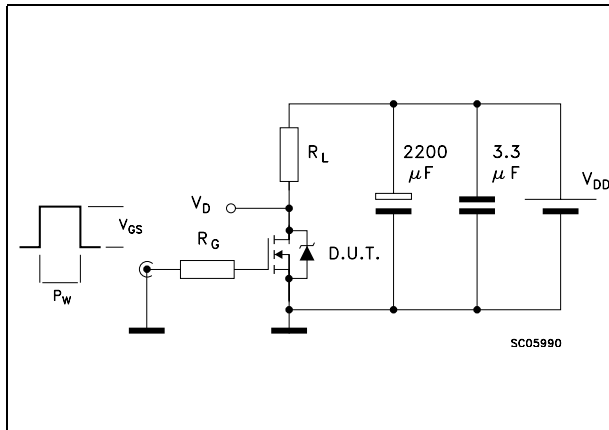


Figure 19. Gate charge test circuit

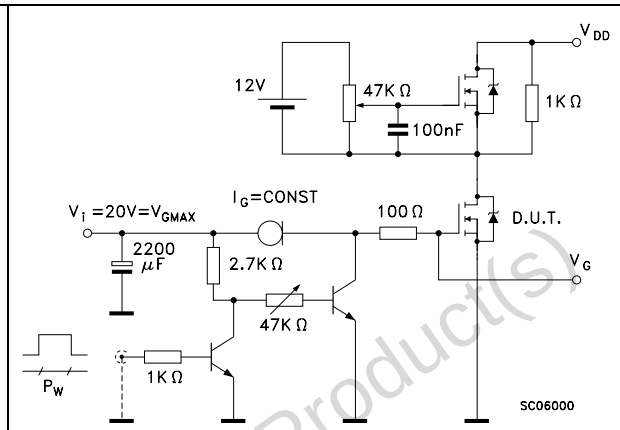


Figure 20. Test circuit for inductive load switching and diode recovery times

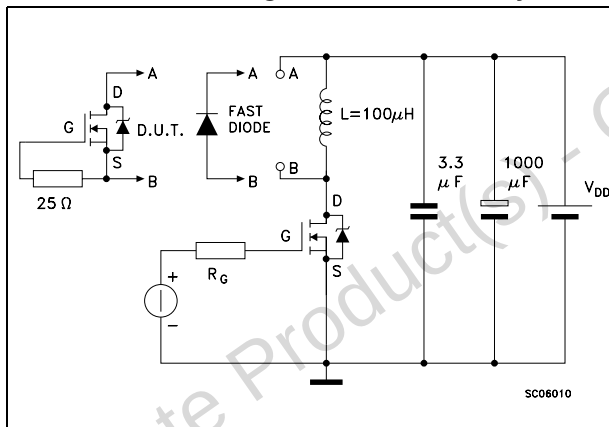


Figure 21. Unclamped Inductive load test circuit

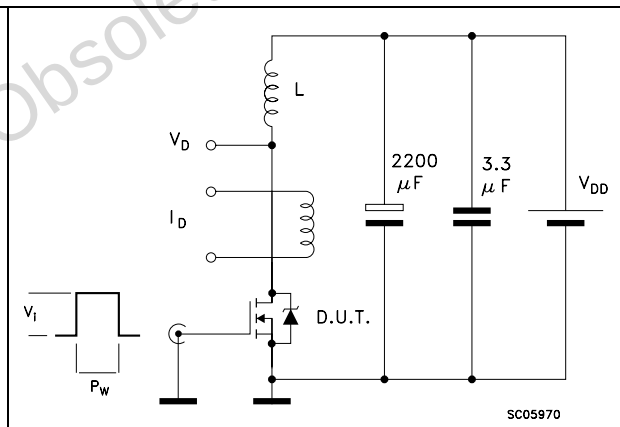


Figure 22. Unclamped inductive waveform

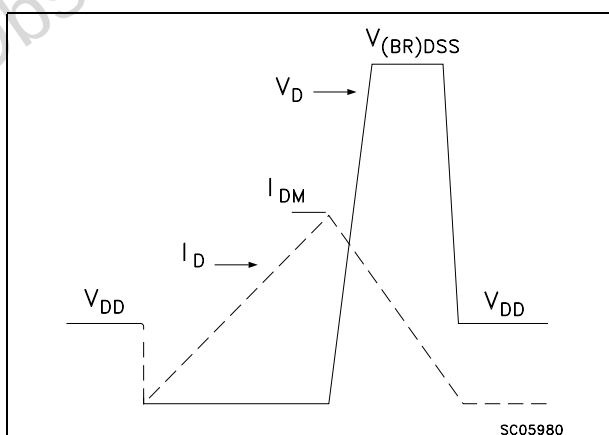
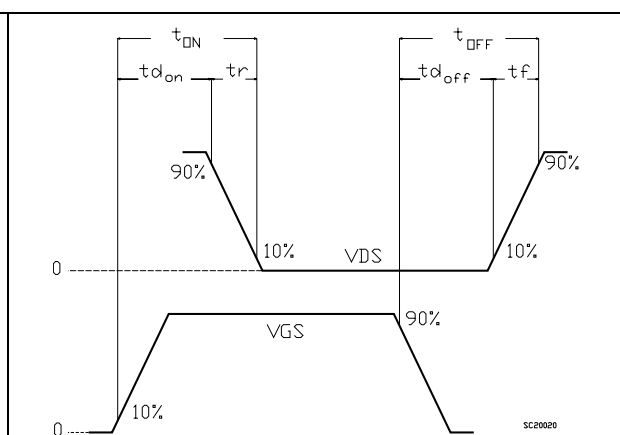


Figure 23. Switching time waveform



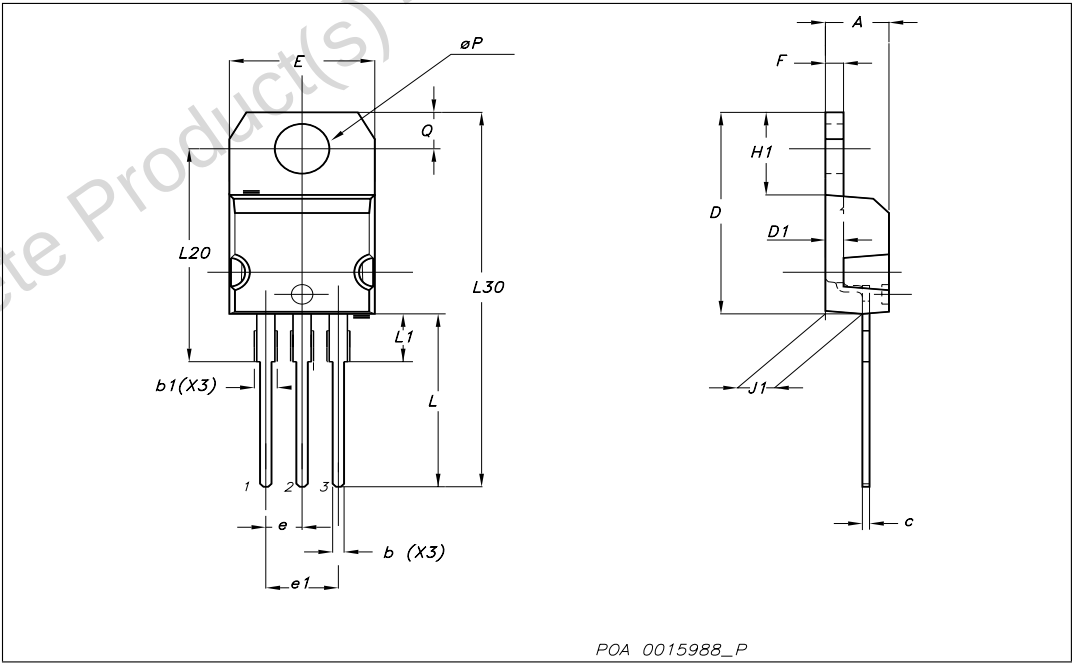
4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com

Obsolete Product(s) - Obsolete Product(s)

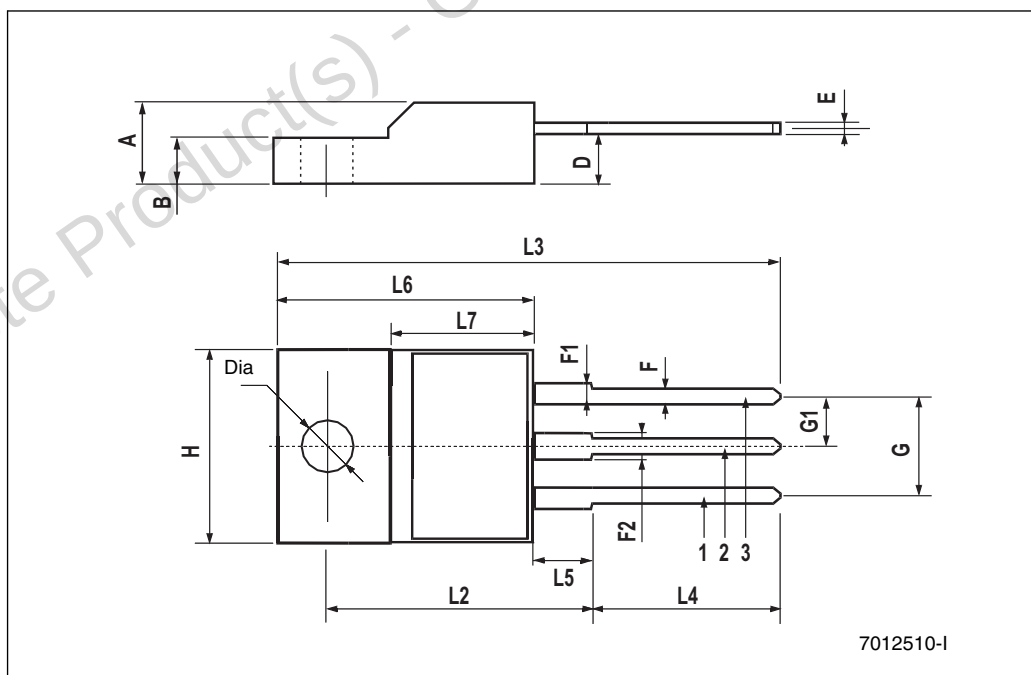
TO-220 mechanical data

Dim	mm			inch		
	Min	Typ	Max	Min	Typ	Max
A	4.40		4.60	0.173		0.181
b	0.61		0.88	0.024		0.034
b1	1.14		1.70	0.044		0.066
c	0.49		0.70	0.019		0.027
D	15.25		15.75	0.6		0.62
D1		1.27			0.050	
E	10		10.40	0.393		0.409
e	2.40		2.70	0.094		0.106
e1	4.95		5.15	0.194		0.202
F	1.23		1.32	0.048		0.051
H1	6.20		6.60	0.244		0.256
J1	2.40		2.72	0.094		0.107
L	13		14	0.511		0.551
L1	3.50		3.93	0.137		0.154
L20		16.40			0.645	
L30		28.90			1.137	
ØP	3.75		3.85	0.147		0.151
Q	2.65		2.95	0.104		0.116



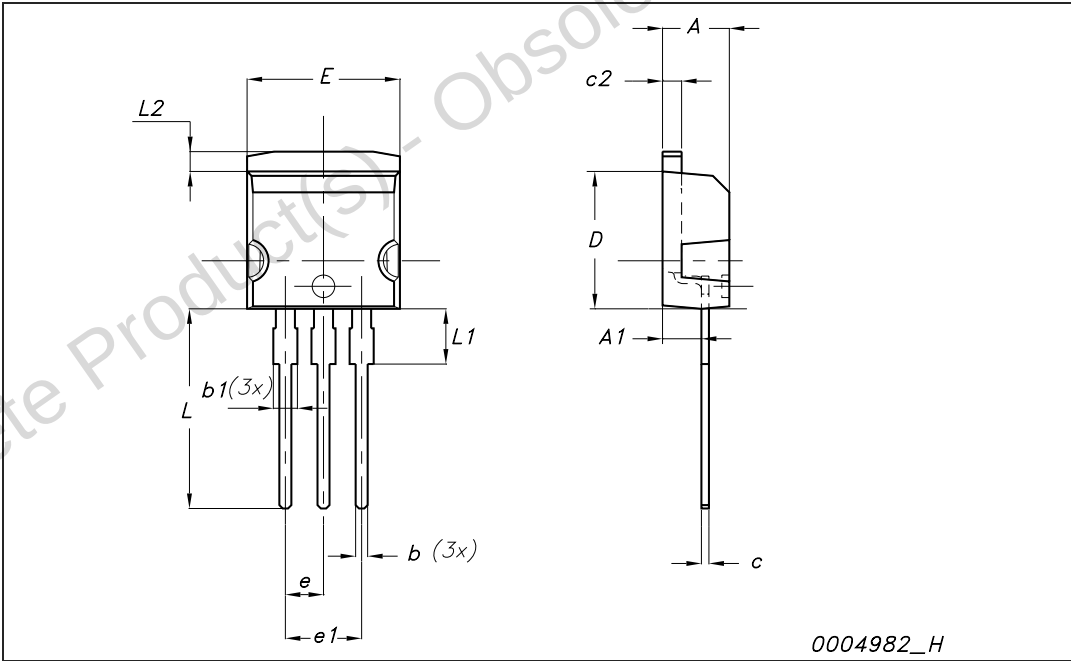
TO-220FP mechanical data

Dim.	mm.			inch		
	Min.	Typ	Max.	Min.	Typ.	Max.
A	4.40		4.60	0.173		0.181
B	2.5		2.7	0.098		0.106
D	2.5		2.75	0.098		0.108
E	0.45		0.70	0.017		0.027
F	0.75		1.00	0.030		0.039
F1	1.15		1.50	0.045		0.067
F2	1.15		1.50	0.045		0.067
G	4.95		5.20	0.195		0.204
G1	2.40		2.70	0.094		0.106
H	10		10.40	0.393		0.409
L2		16			0.630	
L3	28.6		30.6	1.126		1.204
L4	9.80		10.60	0.385		0.417
L5	2.9		3.6	0.114		0.141
L6	15.90		16.40	0.626		0.645
L7	9		9.30	0.354		0.366
Dia	3		3.2	0.118		0.126



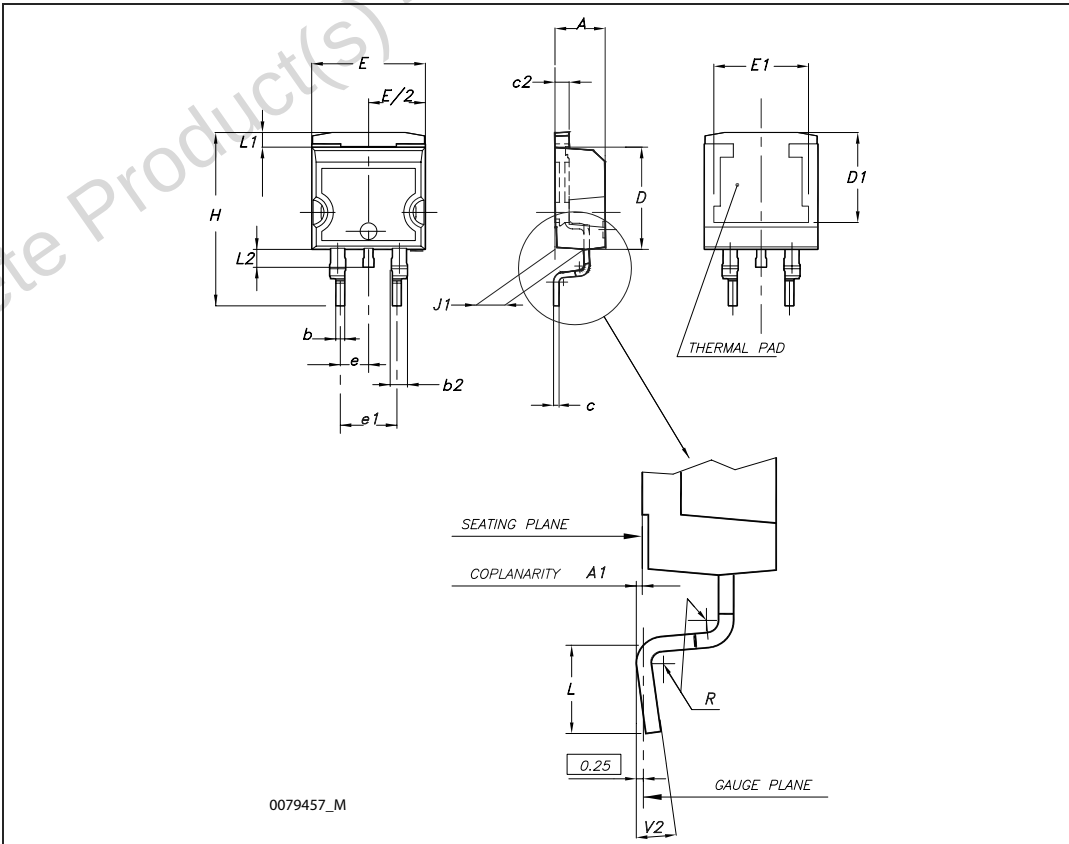
TO-262 mechanical data

Dim	mm			inch		
	Min	Typ	Max	Min	Typ	Max
A	4.40		4.60	0.173		0.181
A1	2.40		2.72	0.094		0.107
b	0.61		0.88	0.024		0.034
b1	1.14		1.70	0.044		0.066
c	0.49		0.70	0.019		0.027
c2	1.23		1.32	0.048		0.052
D	8.95		9.35	0.352		0.368
e	2.40		2.70	0.094		0.106
e1	4.95		5.15	0.194		0.202
E	10		10.40	0.393		0.410
L	13		14	0.511		0.551
L1	3.50		3.93	0.137		0.154
L2	1.27		1.40	0.050		0.055



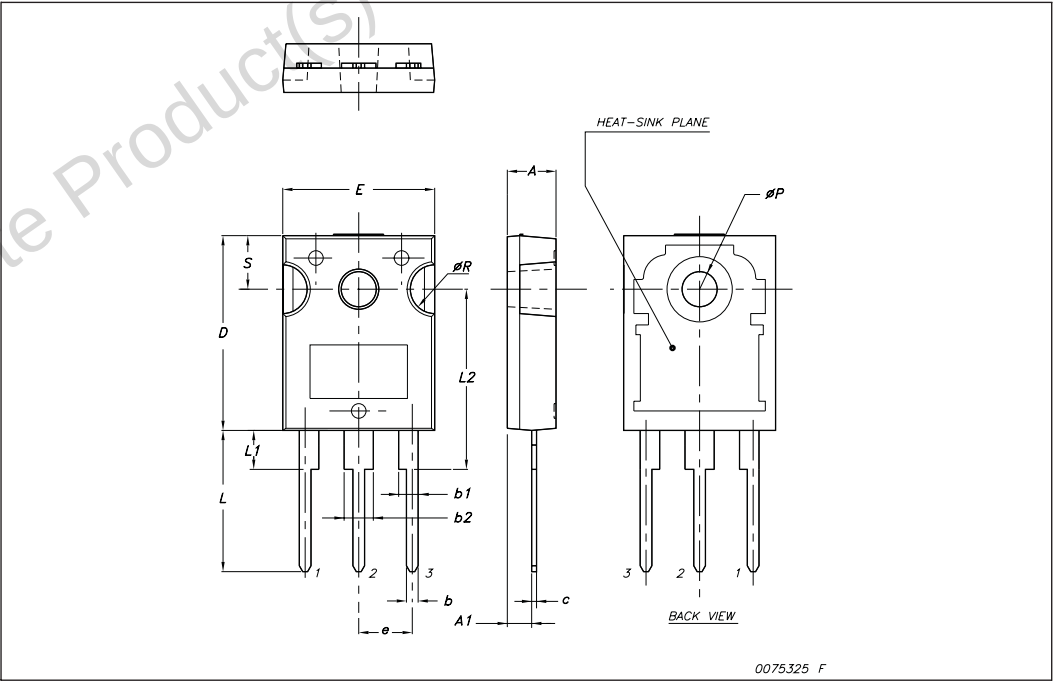
D²PAK (TO-263) mechanical data

Dim	mm			inch		
	Min	Typ	Max	Min	Typ	Max
A	4.40		4.60	0.173		0.181
A1	0.03		0.23	0.001		0.009
b	0.70		0.93	0.027		0.037
b2	1.14		1.70	0.045		0.067
c	0.45		0.60	0.017		0.024
c2	1.23		1.36	0.048		0.053
D	8.95		9.35	0.352		0.368
D1	7.50			0.295		
E	10		10.40	0.394		0.409
E1	8.50			0.334		
e		2.54			0.1	
e1	4.88		5.28	0.192		0.208
H	15		15.85	0.590		0.624
J1	2.49		2.69	0.099		0.106
L	2.29		2.79	0.090		0.110
L1	1.27		1.40	0.05		0.055
L2	1.30		1.75	0.051		0.069
R		0.4			0.016	
V2	0°		8°	0°		8°



TO-247 mechanical data

Dim.	mm.		
	Min.	Typ	Max .
A	4.85		5.15
A1	2.20		2.60
b	1.0		1.40
b1	2.0		2.40
b2	3.0		3.40
c	0.40		0.80
D	19.85		20.15
E	15.45		15.75
e		5.45	
L	14.20		14.80
L1	3.70		4.30
L2		18.50	
øP	3.55		3.65
øR	4.50		5.50
S		5.50	

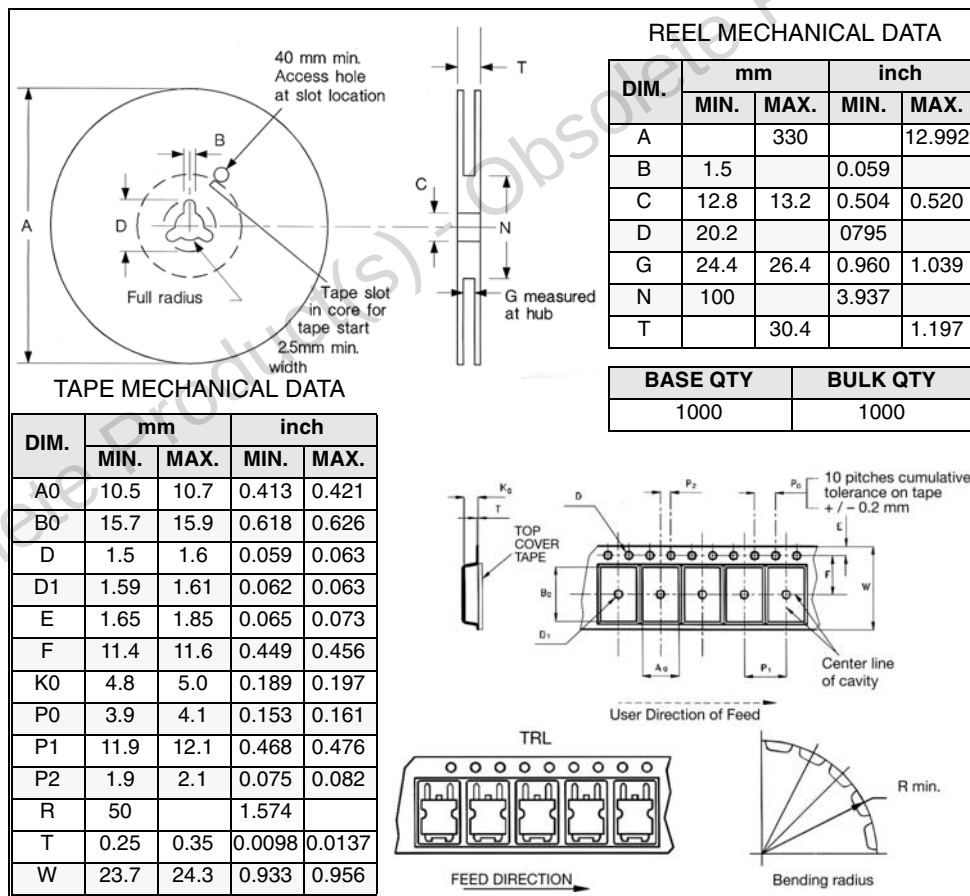


5 Packing mechanical data

D²PAK FOOTPRINT



TAPE AND REEL SHIPMENT



* on sales type

6 Revision history

Table 8. Document revision history

Date	Revision	Changes
19-Oct-2005	1	First release.
07-Nov-2005	2	Modified curves Figure 12
29-Nov-2005	3	Complete version
11-Jan-2007	4	The document has been reformatted
19-Jan-2007	5	Typo mistake on Table 6
27-Apr-2007	6	Modified curves Figure 11 and Figure 15
19-Feb-2008	7	Figure 13 has been modified

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