



STP10NK70ZFP STP10NK70Z

N-CHANNEL 700V - 0.75Ω - 8.6A - TO220-TO220FP
Zener-Protected SuperMESH™ MOSFET

General features

Type	V _{DSS}	R _{DS(on)}	I _D	P _w
STP10NK70Z	700 V	<0.85 Ω	8.6 A	110 W
STP10NK70ZFP	700 V	<0.85 Ω	8.6 A	35 W

- EXTREMELY HIGH dv/dt CAPABILITY
- IMPROVED ESD CAPABILITY
- 100% AVALANCHE TESTED
- GATE CHARGE MINIMIZED
- VERY LOW INTRINSIC CAPACITANCES
- VERY GOOD MANUFACTURING REPEATABILITY

Description

The SuperMESH™ series is obtained through an extreme optimization of ST's well established strip-based PowerMESH™ layout. In addition to pushing on-resistance significantly down, special care is taken to ensure a very good dv/dt capability for the most demanding applications.

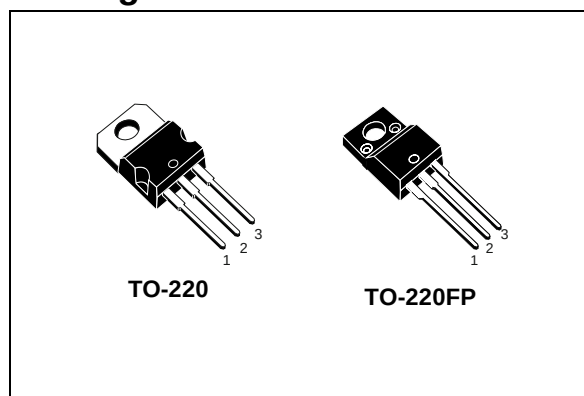
Applications

- HIGH CURRENT, HIGH SPEED SWITCHING
- IDEAL FOR OFF-LINE POWER SUPPLIES, ADAPTOR AND PFC

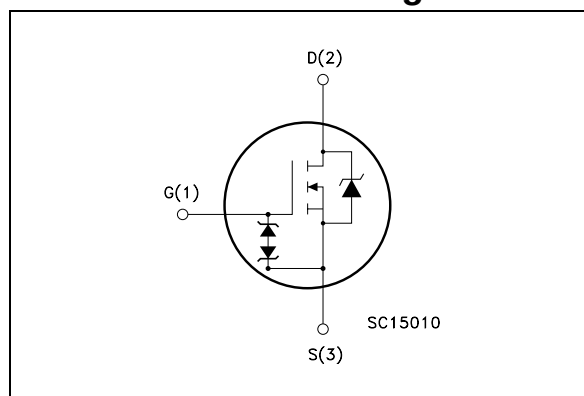
Order codes

Sales Type	Marking	Package	Packaging
STP10NK70Z	P10NK70Z	TO-220	TUBE
STP10NK70ZFP	P10NK70ZFP	TO-220FP	TUBE

Package



Internal schematic diagram



1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value		Unit
		TO-220	TO-220FP	
V_{DS}	Drain-Source Voltage ($V_{GS} = 0$)	700		V
V_{DGR}	Drain-gate Voltage ($R_{GS} = 20k\Omega$)	700		V
V_{GS}	Gate-Source Voltage	± 30		V
I_D	Drain Current (continuous) at $T_C = 25^\circ\text{C}$	8.6	8.6 (Note 3)	A
I_D	Drain Current (continuous) at $T_C = 100^\circ\text{C}$	5.4	5.4 (Note 3)	A
I_{DM} Note 2	Drain Current (pulsed)	34	34 (Note 3)	A
P_{TOT}	Total Dissipation at $T_C = 25^\circ\text{C}$	150	35	W
	Derating Factor	1.20	0.28	W/ $^\circ\text{C}$
Vesd(G-S)	G-S ESD (HBM C=100pF, R=1.5k Ω)	4000		V
$\frac{dv}{dt}$ Note 1	Peak Diode Recovery voltage slope	4.5		V/ns
V_{ISO}	Insulation Withstand Voltage (DC)	--	2500	V
T_j T_{stg}	Operating Junction Temperature Storage Temperature	-55 to 150		$^\circ\text{C}$

Table 2. Thermal data

		TO-220	TO-220FP	Unit
Rthj-case	Thermal Resistance Junction-case Max	0.83	3.6	$^\circ\text{C}/\text{W}$
Rthj-amb	Thermal Resistance Junction-amb Max	62.5		$^\circ\text{C}/\text{W}$
T_I	Maximum Lead Temperature For Soldering Purpose	300		$^\circ\text{C}$

Table 3. Avalanche characteristics

Symbol	Parameter	Max Value	Unit
I_{AR}	Avalanche Current, repetitive or Not-Repetitive (pulse width limited by T_j max)	8.6	A
E_{AS}	Single Pulse Avalanche Energy (starting $T_j=25^\circ\text{C}$, $I_D=I_{AR}$, $V_{DD}=50\text{V}$)	350	mJ

2 Electrical characteristics

(T_{CASE} = 25 °C unless otherwise specified)

Table 4. On/off states

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V _{(BR)DSS}	Drain-Source Breakdown Voltage	I _D = 1mA, V _{GS} = 0	700			V
I _{DSS}	Zero Gate Voltage Drain Current (V _{GS} = 0)	V _{DS} = Max Rating, V _{DS} = Max Rating, T _c = 125°C			1 50	μA μA
I _{GSS}	Gate Body Leakage Current (V _{DS} = 0)	V _{GS} = ±20V, V _{DS} = 0			±10	μA
V _{GS(th)}	Gate Threshold Voltage	V _{DS} = V _{GS} , I _D = 100 μA	3	3.75	4.5	V
R _{DS(on)}	Static Drain-Source On Resistance	V _{GS} = 10 V, I _D = 4.5 A		0.75	0.85	Ω

Table 5. Dynamic

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
g _{fs} <i>Note 4</i>	Forward Transconductance	V _{DS} = 15V, I _D = 4.5A		7.7		S
C _{iss}	Input Capacitance	V _{DS} = 25V, f = 1 MHz, V _{GS} = 0		2000		pF
C _{oss}	Output Capacitance			190		pF
C _{rss}	Reverse Transfer Capacitance			41		pF
C _{oss} eq. <i>Note 5</i>	Equivalent Output Capacitance	V _{GS} = 0, V _{DS} = 0V to 560V		98		pF
Q _g	Total Gate Charge	V _{DD} = 560V, I _D = 9 A		64	90	nC
Q _{gs}	Gate-Source Charge	V _{GS} = 10V		12		nC
Q _{gd}	Gate-Drain Charge	(see Figure 17)		33		nC

Table 6. Switching times

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
t _{d(on)} t _r	Turn-on Delay Time Rise Time	V _{DD} = 350 V, I _D = 4.5 A, R _G = 4.7Ω, V _{GS} = 10V (see Figure 18)		22 19		ns ns
t _{d(off)} t _f	Turn-off Delay Time Fall Time	V _{DD} = 350 V, I _D = 4.5A, R _G = 4.7Ω, V _{GS} = 10V (see Figure 18)		46 19		ns ns
t _{r(Voff)} t _f t _c	Off-voltage Rise Time Fall Time Cross-over Time	V _{DD} = 560 V, I _D = 9A, R _G = 4.7Ω, V _{GS} = 10V (see Figure 18)		11 10 22		ns ns ns

Table 7. Source drain diode

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain Current				8.6	A
I_{SDM} Note 2	Source-drain Current (pulsed)				34	A
V_{SD} Note 4	Forward on Voltage	$I_{SD}=8.6\text{ A}$, $V_{GS}=0$			1.6	V
t_{rr}	Reverse Recovery Time	$I_{SD}=9\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$, $V_{DD}=35\text{ V}$, $T_j=150^\circ\text{C}$		720		ns
Q_{rr}	Reverse Recovery Charge			5.4		μC
I_{RRM}	Reverse Recovery Current			15		A

Table 8. Gate-source zener diode

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
BV_{GSO} Note 6	Gate-Source Breakdown Voltage	$I_{GS}=\pm 1\text{ mA}$ (Open Drain)	30			V

(1) $I_{SD} \leq 8.6\text{ A}$, $di/dt \leq 200\text{ A}/\mu\text{s}$, $V_{DD} \leq V_{(BR)DSS}$, $T_j \leq T_{JMAX}$

(2) Pulse width limited by safe operating area

(3) Limited only by maximum temperature allowed

(4) Pulsed: pulse duration = 300 μs , duty cycle 1.5%

(5) $C_{OSS\text{eq}}$ is defined as a constant equivalent capacitance giving the same charging time as C_{OSS} when V_{DS} increases from 0 to 80% V_{DSS}

(6) The built-in back-to-back Zener diodes have specifically been designed to enhance not only the device's ESD capability, but also to make them safely absorb possible voltage transients that may occasionally be applied from gate to source. In this respect the Zener voltage is appropriate to achieve an efficient and cost-effective intervention to protect the device's integrity. These integrated Zener diodes thus avoid the usage of external components.

2.1 Electrical Characteristics (curves)

Figure 1. Safe Operating Area for TO-220

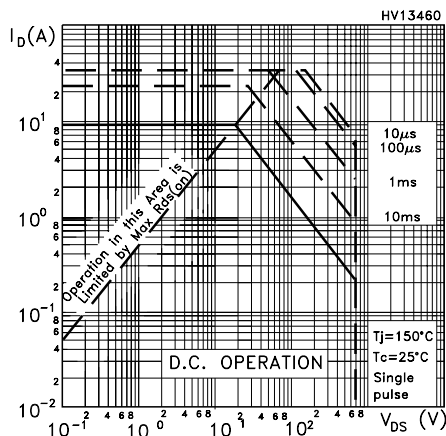


Figure 2. Thermal Impedance for TO-220

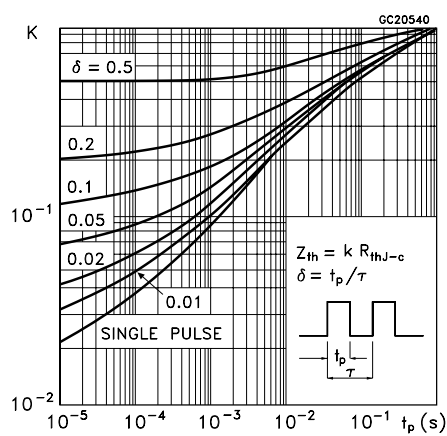


Figure 3. Safe Operating Area for TO-220FP

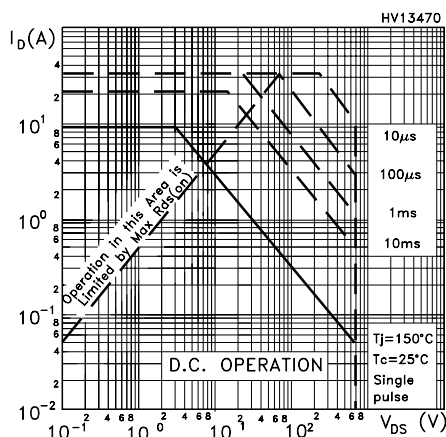


Figure 4. Thermal Impedance for TO-220FP

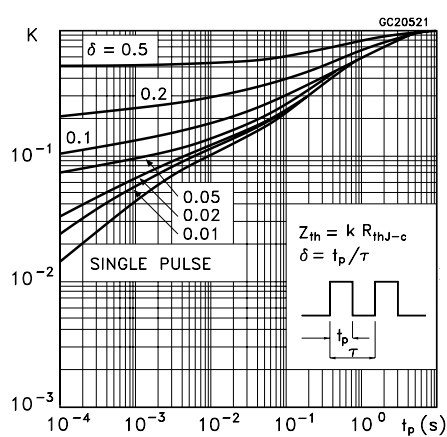


Figure 5. Output Characteristics

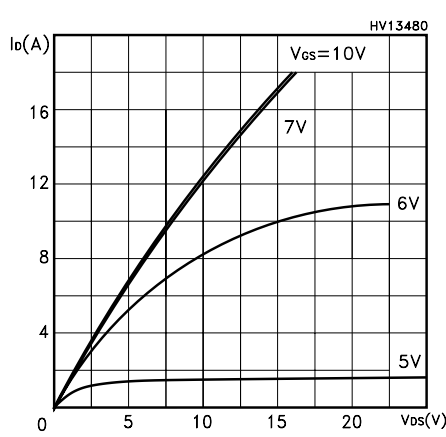


Figure 6. Transfer Characteristics

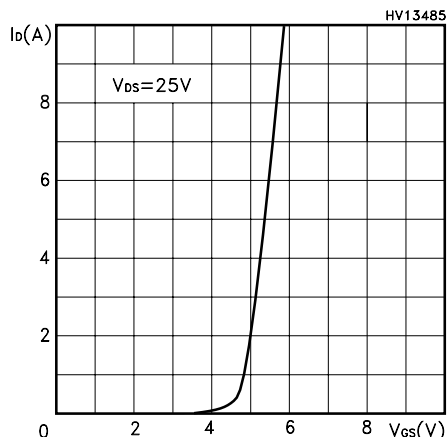


Figure 7. Transconductance

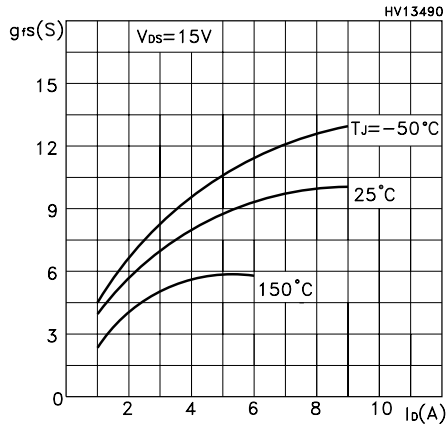


Figure 8. Static Drain-Source on Resistance

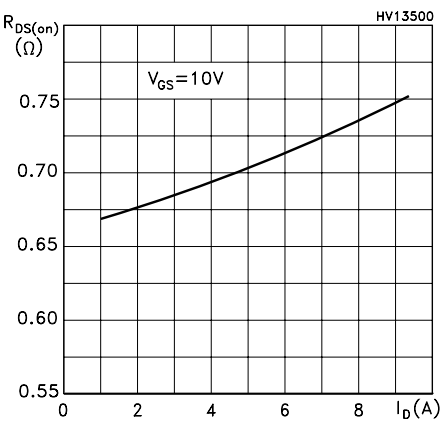


Figure 9. Gate Charge vs Gate -Source Voltage

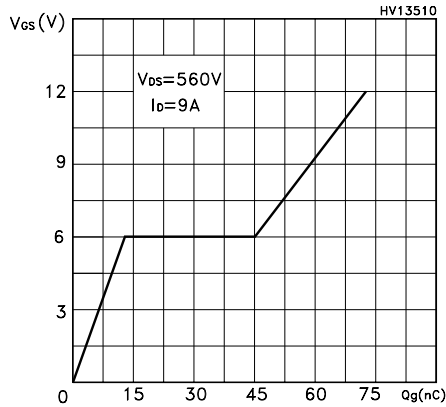


Figure 11. Capacitance Variations

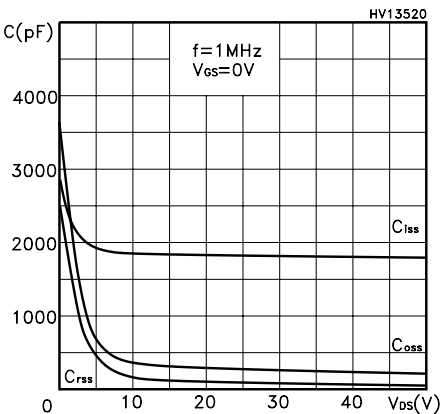


Figure 10. Normalized Gate Threshold Voltage vs Temperature

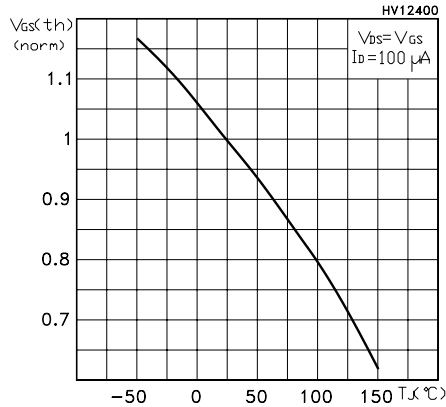


Figure 12. Normalized on Resistance vs Temperature

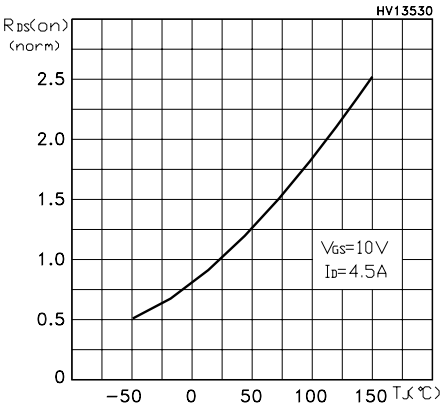


Figure 13. Source-drain Diode Forward Characteristics

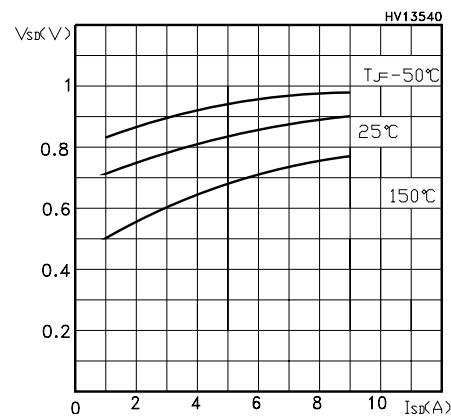


Figure 14. Normalized BVDSS vs Temperature

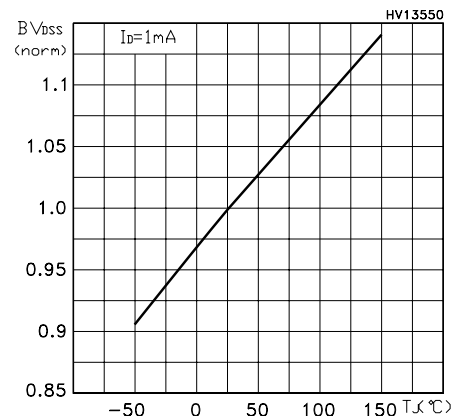
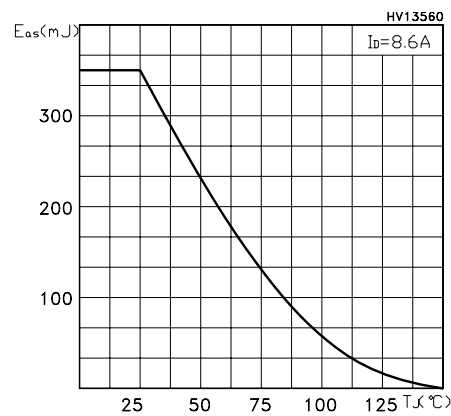


Figure 15. Maximum Avalanche Energy vs Temperature



3 Test circuits

Figure 16. Switching Times Test Circuit For Resistive Load

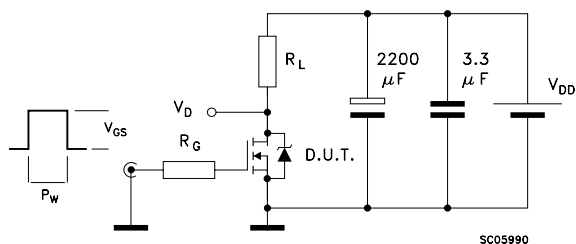


Figure 17. Gate Charge Test Circuit

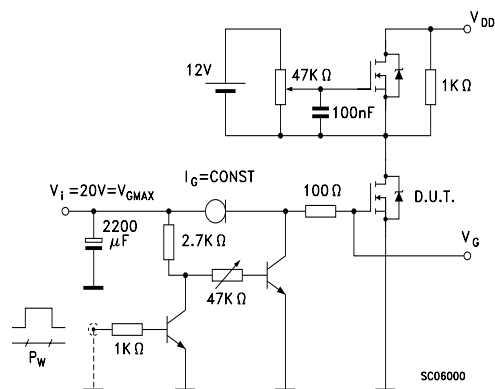


Figure 18. Test Circuit For Inductive Load Switching and Diode Recovery Times

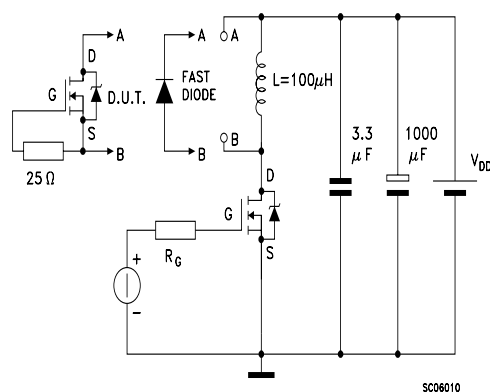


Figure 20. Unclamped Inductive Load Test Circuit

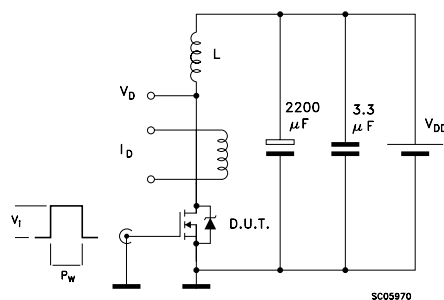
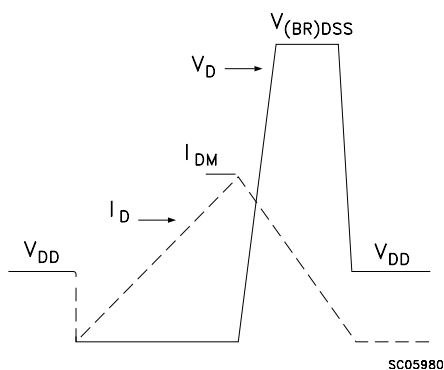


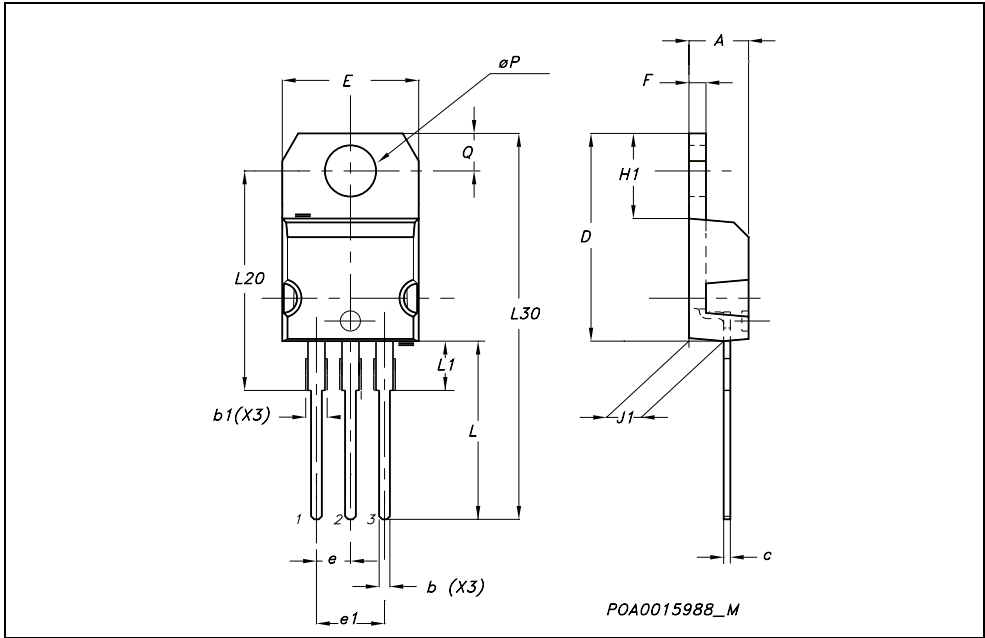
Figure 19. Unclamped Inductive Waveform



4 Package mechanical data

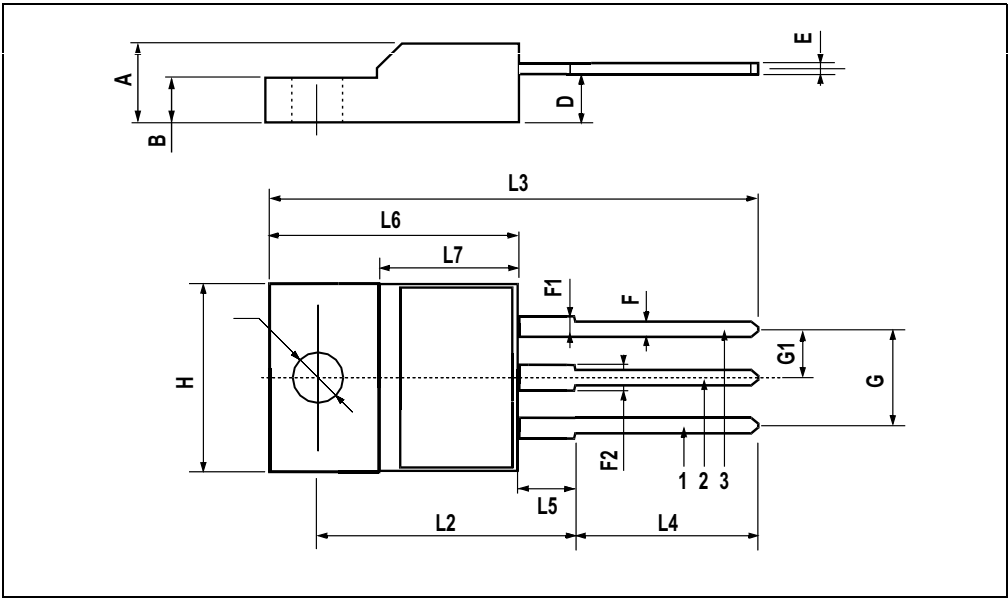
In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect . The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com

TO-220 MECHANICAL DATA						
DIM.	mm.			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	4.40		4.60	0.173		0.181
b	0.61		0.88	0.024		0.034
b1	1.15		1.70	0.045		0.066
c	0.49		0.70	0.019		0.027
D	15.25		15.75	0.60		0.620
E	10		10.40	0.393		0.409
e	2.40		2.70	0.094		0.106
e1	4.95		5.15	0.194		0.202
F	1.23		1.32	0.048		0.052
H1	6.20		6.60	0.244		0.256
J1	2.40		2.72	0.094		0.107
L	13		14	0.511		0.551
L1	3.50		3.93	0.137		0.154
L20		16.40			0.645	
L30		28.90			1.137	
øP	3.75		3.85	0.147		0.151
Q	2.65		2.95	0.104		0.116



TO-220FP MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A	4.4		4.6	0.173		0.181
B	2.5		2.7	0.098		0.106
D	2.5		2.75	0.098		0.108
E	0.45		0.7	0.017		0.027
F	0.75		1	0.030		0.039
F1	1.15		1.7	0.045		0.067
F2	1.15		1.7	0.045		0.067
G	4.95		5.2	0.195		0.204
G1	2.4		2.7	0.094		0.106
H	10		10.4	0.393		0.409
L2		16			0.630	
L3	28.6		30.6	1.126		1.204
L4	9.8		10.6	.0385		0.417
L5	2.9		3.6	0.114		0.141
L6	15.9		16.4	0.626		0.645
L7	9		9.3	0.354		0.366
Ø	3		3.2	0.118		0.126



5 Revision History

Date	Revision	Changes
22-Aug-2005	2	Inserted Ecopack indication

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