STM8AF622x/4x STM8AF6266/68
STM8AF612x/4x STM8AF6166/68

Automotive 8-bit MCU, with up to 32 Kbytes Flash, data EEPROM, 10-bit ADC, timers, LIN, SPI, I^2C, 3 to 5.5 V

Features

Core

- Max f_{CPU}: 16 MHz
- Advanced STM8A core with Harvard architecture and 3-stage pipeline
- Average 1.6 cycles/instruction resulting in 10 MIPS at 16 MHz f_{CPU} for industry standard benchmark

Memories

- Program memory: 16 to 32 Kbytes Flash; data retention 20 years at 55 °C after 1 kcycle
- Data memory: 0.5 to 1 Kbyte true data EEPROM; endurance 300 kcycles
- RAM: 1 to 2 Kbytes

Clock management

- Low power crystal resonator oscillator with external clock input
- Internal, user-trimmable 16 MHz RC and low power 128 kHz RC oscillators
- Clock security system with clock monitor

Reset and supply management

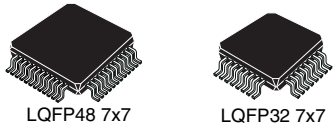
- Multiple low power modes (wait, slow, auto wakeup, halt) with user definable clock gating
- Low consumption power-on and power-down reset

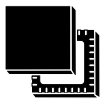
Interrupt management

- Nested interrupt controller with 32 interrupt vectors
- Up to 34 external interrupts on 5 vectors

Timers

- Up to 2 auto-reload 16-bit PWM timers with up to 3 CAPCOM channels each (IC, OC or PWM)
- Multipurpose timer: 16-bit, 4 CAPCOM channels, 3 complementary outputs, dead-time insertion and flexible synchronization
- 8-bit AR system timer with 8-bit prescaler
- Auto wakeup timer
- Two watchdog timers: Window and standard





Communication interfaces

- LINUART LIN 2.1 compliant, master/slave modes with automatic resynchronization
- SPI interface up to 8 Mbit/s or $f_{CPU}/2$
- I^2C interface up to 400 Kbit/s

Analog-to-digital converter (ADC)

- 10-bit accuracy, 2LSB TUE accuracy, 2 LSB TUE linearity ADC and up to 10 multiplexed channels with individual data buffer
- Analog watchdog, scan and continuous sampling mode

I/Os

- Up to 38 user pins including 10 high sink I/Os
- Highly robust I/O design, immune against current injection

Operating temperature

- Up to 150 °C

Table 1. Device summary[1]

Part numbers: STM8AF622x/4x STM8AF6266/68
STM8AF6268, STM8AF6248, STM8AF6266, STM8AF6246, STM8AF6226
Part numbers: STM8AF612x/4x STM8AF6166/68[2]
STM8AF6168, STM8AF6148, STM8AF6166, STM8AF6146, STM8AF6126

1. In the order code, the letter 'F' applies to devices featuring Flash and data EEPROM, while 'H' refers to devices with Flash memory only.
2. Not recommended for new design.

Contents

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1 Introduction

This datasheet refers to the STM8AF61xx (STM8AF612x, STM8AF614x, STM8AF6166, and STM8AF6168) and STM8AF62xx products with 16 to 32 Kbytes of program memory. The STM8AF61xx and STM8AF62xx are hereafter referred to as the STM8AF61xx and STM8AF62xx. ‘F’ refers to product versions with data EEPROM and ‘H’ refers to product versions without data EEPROM. The identifiers ‘F’ and ‘H’ do not coexist in a given order code.

The datasheet contains the description of family features, pinout, electrical characteristics, mechanical data and ordering information.

- For complete information on the STM8A microcontroller memory, registers and peripherals, please refer to STM8A microcontroller family reference manual (RM0009).
- For information on programming, erasing and protection of the internal Flash memory please refer to the STM8 Flash programming manual (PM0047).
- For information on the debug and SWIM (single wire interface module) refer to the STM8 SWIM communication protocol and debug module user manual (UM0470).
- For information on the STM8 core, please refer to the STM8 CPU programming manual (PM0044).

2 Description

The STM8AF61xx and STM8AF62xx automotive 8-bit microcontrollers offer from 16 to 32 Kbytes of program memory and integrated true data EEPROM.

All devices of the STM8A product line provide the following benefits: reduced system cost, performance and robustness, short development cycles, and product longevity.

- Reduced system cost
  - Integrated true data EEPROM for up to 300 kwrite/erase cycles
  - High system integration level with internal clock oscillators, watchdog and brown-out reset.
- Performance and robustness
  - Average performance 10 MIPS at 16 MHz CPU clock frequency
  - Robust I/O, independent watchdogs with separate clock source
  - Clock security system
- Short development cycles
  - Applications scalability across a common family product architecture with compatible pinout, memory map and modular peripherals.
  - Full documentation and a wide choice of development tools
- Product longevity
  - Advanced core and peripherals made in a state-of-the art technology
  - Native automotive product family operating both at 3.3 V and 5 V supply

All STM8A and ST7 microcontrollers are supported by the same tools including STVD/STVP development environment, the STice emulator and a low-cost, third party in-circuit debugging tool (for more details, see *Section 14: STM8 development tools on page 95*).

3 Product line-up

Table 2. STM8AF62xx product line-up

Order code	Package	Prog. (bytes)	RAM (bytes)	Data EE (bytes)	10-bit A/D ch.	Timers (IC/OC/PWM)	Serial interfaces	I/0 wakeup pins
STM8AF6268	LQFP48 (7x7)	32 K	2 K	1 K	10	1x8-bit: TIM4 3x16-bit: TIM1, TIM2, TIM3 (9/9/9)	LIN(UART), SPI, I²C	38/35
STM8AF6248		16 K	1 K	0.5 K				
STM8AF6266	LQFP32 (7x7)	32 K	2 K	1 K	7	1x8-bit: TIM4 3x16-bit: TIM1, TIM2, TIM3 (8/8/8)	LIN(UART), SPI, I²C	25/23
STM8AF6246		16 K	1 K	0.5 K				
STM8AF6226		8 K	512	384				
STM8AF6266	VFQFPN32	32 K	2 K	1 K	7	1x8-bit: TIM4 3x16-bit: TIM1, TIM2, TIM3 (8/8/8)	LIN(UART), SPI, I²C	25/23
STM8AF6246		16 K	1 K	0.5 K				

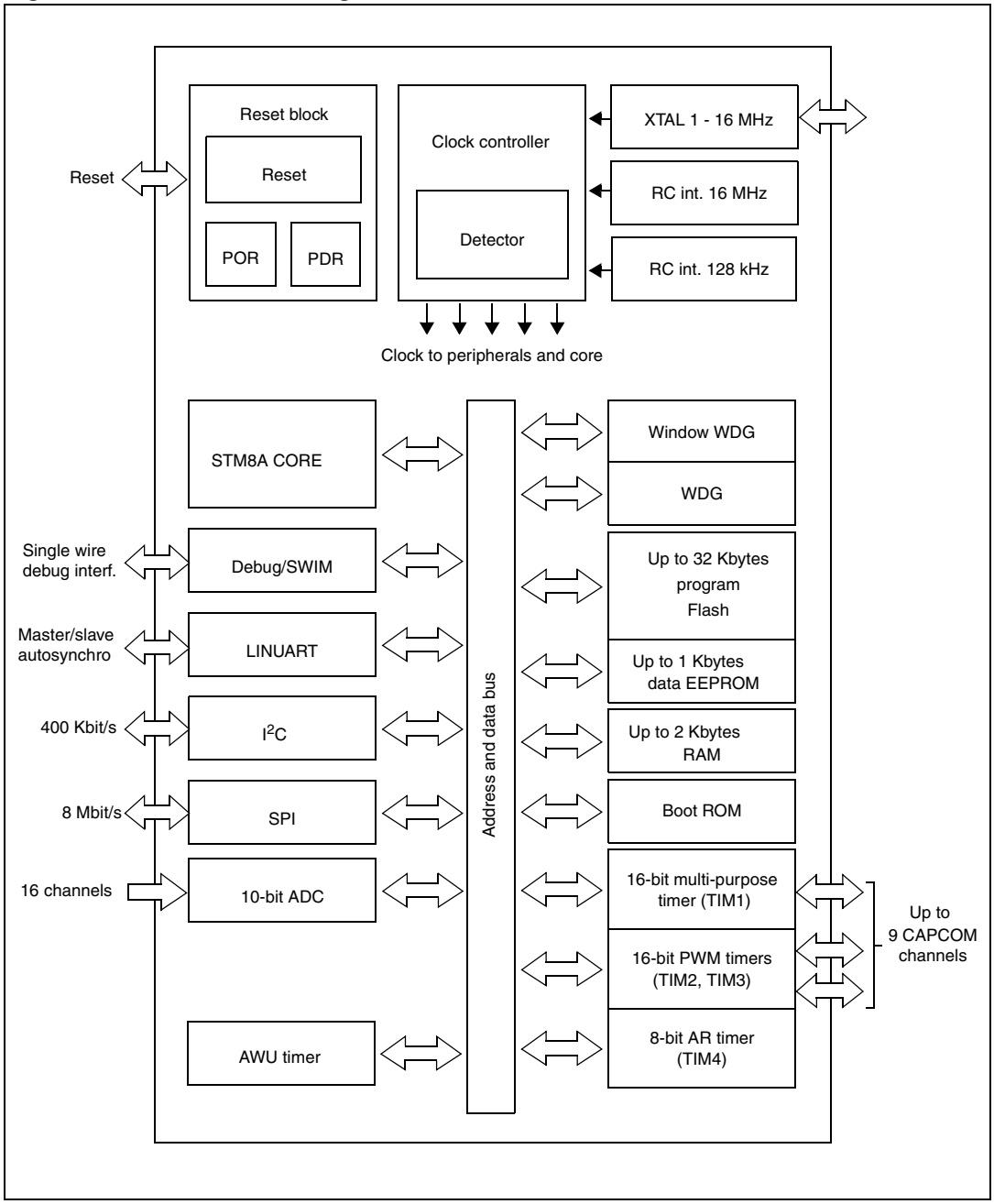
Table 3. STM8AF/H61xx product line-up(1)

Order code	Package	Prog. (bytes)	RAM (bytes)	Data EE (bytes)	10-bit A/D ch.	Timers (IC/OC/PWM)	Serial interfaces	I/0 wakeup pins
STM8AF/H6168	LQFP48 (7x7)	32 K	2 K	1 K	10	1x8-bit: TIM4 3x16-bit: TIM1, TIM2, TIM3 (9/9/9)	LIN(UART), SPI, I²C	38/35
STM8AF/H6148		16 K	1 K	0.5 K				
STM8AF/H6166	LQFP32 (7x7)	32 K	2 K	1 K	7	1x8-bit: TIM4 3x16-bit: TIM1, TIM2, TIM3 (8/8/8)	LIN(UART), SPI, I²C	25/23
STM8AF/H6146		16 K	1 K	0.5 K				
STM8AF/H6126		8 K	512	384				

1. These devices are not recommended for new design.

4 Block diagram

Figure 1. STM8A block diagram



5 Product overview

This section is intended to describe the family features that are actually implemented in the products covered by this datasheet.

For more detailed information on each feature please refer to the STM8A microcontroller family reference manual (RM0009).

5.1 STM8A central processing unit (CPU)

The 8-bit STM8A core is a modern CISC core and has been designed for code efficiency and performance. It contains 21 internal registers (six directly addressable in each execution context), 20 addressing modes including indexed indirect and relative addressing and 80 instructions.

5.1.1 Architecture and registers

- Harvard architecture
- 3-stage pipeline
- 32-bit wide program memory bus with single cycle fetching for most instructions
- X and Y 16-bit index registers, enabling indexed addressing modes with or without offset and read-modify-write type data manipulations
- 8-bit accumulator
- 24-bit program counter with 16-Mbyte linear memory space
- 16-bit stack pointer with access to a 64 Kbyte stack
- 8-bit condition code register with seven condition flags for the result of the last instruction.

5.1.2 Addressing

- 20 addressing modes
- Indexed indirect addressing mode for look-up tables located anywhere in the address space
- Stack pointer relative addressing mode for efficient implementation of local variables and parameter passing

5.1.3 Instruction set

- 80 instructions with 2-byte average instruction size
- Standard data movement and logic/arithmetic functions
- 8-bit by 8-bit multiplication
- 16-bit by 8-bit and 16-bit by 16-bit division
- Bit manipulation
- Data transfer between stack and accumulator (push/pop) with direct stack access
- Data transfer using the X and Y registers or direct memory-to-memory transfers

5.2 Single wire interface module (SWIM) and debug module

5.2.1 SWIM

The single wire interface module, SWIM, together with an integrated debug module, permits non-intrusive, real-time in-circuit debugging and fast memory programming. The interface can be activated in all device operation modes and can be connected to a running device (hot plugging).The maximum data transmission speed is 145 bytes/ms.

5.2.2 Debug module

The non-intrusive debugging module features a performance close to a full-flavored emulator. Besides memory and peripheral operation, CPU operation can also be monitored in real-time by means of shadow registers.

- R/W of RAM and peripheral registers in real-time
- R/W for all resources when the application is stopped
- Breakpoints on all program-memory instructions (software breakpoints), except the interrupt vector table
- Two advanced breakpoints and 23 predefined breakpoint configurations

5.3 Interrupt controller

- Nested interrupts with three software priority levels
- 21 interrupt vectors with hardware priority
- Five vectors for external interrupts (up to 34 depending on the package)
- Trap and reset interrupts

5.4 Flash program and data EEPROM

- 8 Kbytes to 32 Kbytes of single voltage program Flash memory
- Up to 1 Kbytes true (not emulated) data EEPROM
- Read while write: Writing in the data memory is possible while executing code in the program memory
- The device setup is stored in a user option area in the non-volatile memory

5.4.1 Architecture

- The memory is organized in blocks of 128 bytes each
- Read granularity: 1 word = 4 bytes
- Write/erase granularity: 1 word (4 bytes) or 1 block (128 bytes) in parallel
- Writing, erasing, word and block management is handled automatically by the memory interface.

5.4.2 Write protection (WP)

Write protection in application mode is intended to avoid unintentional overwriting of the memory. The write protection can be removed temporarily by executing a specific sequence in the user software.

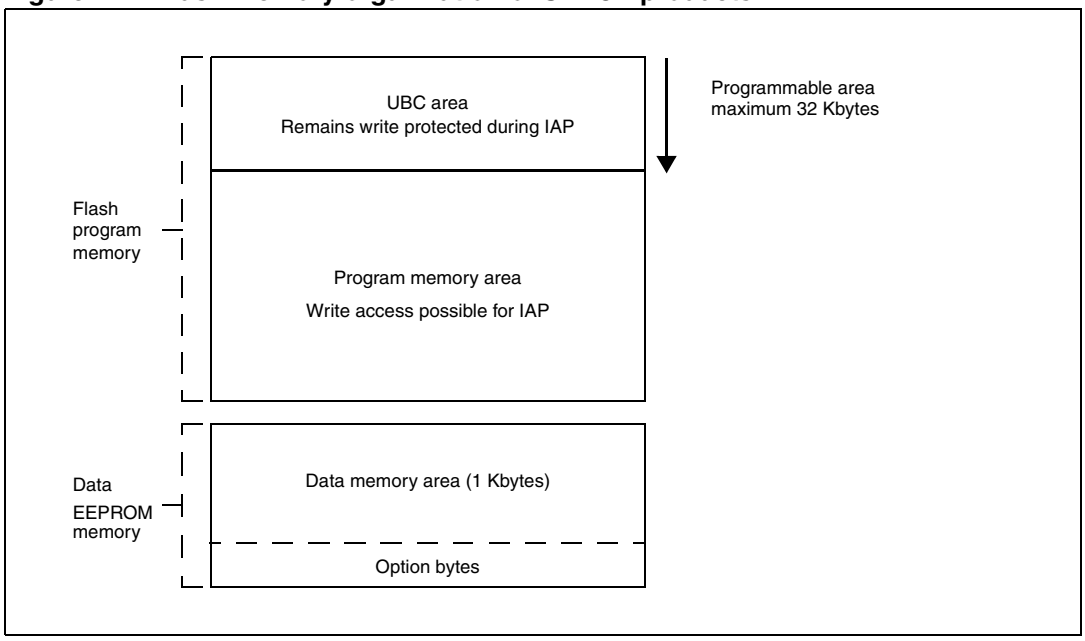
5.4.3 Protection of user boot code (UBC)

If the user chooses to update the program memory using a specific boot code to perform in application programming (IAP), this boot code needs to be protected against unwanted modification.

In the STM8A a memory area of up to 32 Kbytes can be protected from overwriting at user option level. Other than the standard write protection, the UBC protection can exclusively be modified via the debug interface, the user software cannot modify the UBC protection status.

The UBC memory area contains the reset and interrupt vectors and its size can be adjusted in increments of 512 bytes by programming the UBC and NUBC option bytes (see *Section 9: Option bytes on page 47*).

Figure 2. Flash memory organization of STM8A products



5.4.4 Read-out protection (ROP)

The STM8A provides a read-out protection of the code and data memory which can be activated by an option byte setting (see the ROP option byte in section 10).

The read-out protection prevents reading and writing program memory, data memory and option bytes via the debug module and SWIM interface. This protection is active in all device operation modes. Any attempt to remove the protection by overwriting the ROP option byte triggers a global erase of the program and data memory.

The ROP circuit may provide a temporary access for debugging or failure analysis. The temporary read access is protected by a user defined, 8-byte keyword stored in the option

byte area. This keyword must be entered via the SWIM interface to temporarily unlock the device.

If desired, the temporary unlock mechanism can be permanently disabled by the user.

5.5 Clock controller

The clock controller distributes the system clock coming from different oscillators to the core and the peripherals. It also manages clock gating for low-power modes and ensures clock robustness.

5.5.1 Features

- **Clock sources:**
  - Internal 16 MHz and 128 kHz RC oscillators
  - Crystal/resonator oscillator
  - External clock input
- **Reset**: After reset the microcontroller restarts by default with an internal 2-MHz clock (16 MHz/8). The clock source and speed can be changed by the application program as soon as the code execution starts.
- **Safe clock switching**: Clock sources can be changed safely on the fly in run mode through a configuration register. The clock signal is not switched until the new clock source is ready. The design guarantees glitch-free switching.
- **Clock management**: To reduce power consumption, the clock controller can stop the clock to the core or individual peripherals.
- **Wakeup**: In case the device wakes up from low-power modes, the internal RC oscillator (16 MHz/8) is used for quick startup. After a stabilization time, the device switches to the clock source that was selected before halt mode was entered.
- **Clock security system (CSS)**: The CSS permits monitoring of external clock sources and automatic switching to the internal RC (16 MHz/8) in case of a clock failure.
- **Configurable main clock output (CCO)**: This feature permits to outputs a clock signal for use by the application.

5.5.2 Internal 16 MHz RC oscillator

- Default clock after reset 2 MHz (16 MHz/8)
- Fast wakeup time

User trimming

The register CLK_HSITRIMR with three trimming bits plus one additional bit for the sign permits frequency tuning by the application program. The adjustment range covers all possible frequency variations versus supply voltage and temperature. This trimming does not change the initial production setting.

For reason of compatibility with other devices from the STM8A family, a special mode with only two trimming bits plus sign can be selected. This selection is controlled with the bit 16MHZTRIM0 in the option byte registers OPT3 and NOPT3.

5.5.3 Internal 128 kHz RC oscillator

The frequency of this clock is 128 kHz and it is independent from the main clock. It drives the independent watchdog or the AWU wakeup timer.

In systems which do not need independent clock sources for the watchdog counters, the 128 kHz signal can be used as the system clock. This configuration has to be enabled by setting an option byte (OPT3/OPT3N, bit LSI_EN).

5.5.4 Internal high-speed crystal oscillator

The internal high-speed crystal oscillator can be selected to deliver the main clock in normal run mode. It operates with quartz crystals and ceramic resonators.

- Frequency range: 1 MHz to 16 MHz
- Crystal oscillation mode: preferred fundamental
- I/Os: standard I/O pins multiplexed with OSCIN, OSCOUT

5.5.5 External clock input

An external clock signal can be applied to the OSCIN input pin of the crystal oscillator. The frequency range is 0 to 16 MHz.

5.5.6 Clock security system (CSS)

The clock security system protects against a system stall in case of an external crystal clock failure.

In case of a clock failure an interrupt is generated and the high-speed internal clock (HSI) is automatically selected with a frequency of 2 MHz (16 MHz/8).

5.6 Low-power operating modes

The product features various low-power modes:

- Slow mode: prescaled CPU clock, selected peripherals at full clock speed
- Active halt mode: CPU and peripheral clocks are stopped, the device cyclically goes back to run mode, controlled by the AWU timer. Wakeup through external events is possible.
- Halt mode: CPU and peripheral clocks are stopped, the device remains powered on. Wakeup is triggered by an external interrupt.

In all modes the CPU and peripherals remain permanently powered on, the system clock is applied only to selected modules. The RAM content is preserved and the brown-out reset circuit remains activated.

5.7 Timers

5.7.1 Watchdog timers

The watchdog system is based on two independent timers providing maximum security to the applications. The watchdog timer activity is controlled by the application program or option bytes. Once the watchdog is activated, it cannot be disabled by the user program without going through reset.

Window watchdog timer

The window watchdog is used to detect the occurrence of a software fault, usually generated by external interferences or by unexpected logical conditions, which cause the application program to abandon its normal sequence.

The window function can be used to trim the watchdog behavior to match the application timing perfectly. The application software must refresh the counter before time-out and during a limited time window. If the counter is refreshed outside this time window, a reset is issued.

Independent watchdog timer

The independent watchdog peripheral can be used to resolve malfunctions due to hardware or software failures.

It is clocked by the 128 kHz LSI internal RC clock source, and thus stays active even in case of a CPU clock failure. If the hardware watchdog feature is enabled through the device option bits, the watchdog is automatically enabled at power-on, and generates a reset unless the key register is written by software before the counter reaches the end of count.

5.7.2 Auto-wakeup counter

This counter is used to cyclically wakeup the device in active halt mode. It can be clocked by the internal 128 kHz internal low-frequency RC oscillator or external clock

5.7.3 Beeper

This function generates a rectangular signal in the range of 1, 2 or 4 kHz which can be output on a pin. This is useful when audible sounds without interference need to be generated for use in the application.

5.7.4 Multipurpose and PWM timers

STM8A devices described in this datasheet, contain up to three 16-bit multipurpose and PWM timers providing nine CAPCOM channels in total. A CAPCOM channel can be used either as input compare, output compare or PWM channel. These timers are named TIM1, TIM2 and TIM3.

Table 4. PWM timers

Timer	Counter width	Counter type	Prescaler factor	Channels	Inverted outputs	Repetition counter	trigger unit	External trigger	Break input
TIM1	16-bit	Up/down	1 to 65536	4	3	Yes	Yes	Yes	Yes
TIM2	16-bit	Up	2^n n = 0 to 15	3	None	No	No	No	No
TIM3	16-bit	Up	2^n n = 0 to 15	2	None	No	No	No	No

TIM1: Multipurpose PWM timer

This is a high-end timer designed for a wide range of control applications. With its complementary outputs, dead-time control and center-aligned PWM capability, the field of applications is extended to motor control, lighting and bridge driver.

- 16-bit up, down and up/down AR (auto-reload) counter with 16-bit fractional prescaler.
- Four independent CAPCOM channels configurable as input capture, output compare, PWM generation (edge and center aligned mode) and single pulse mode output
- Trigger module which allows the interaction of TIM1 with other on-chip peripherals. In the present implementation it is possible to trigger the ADC upon a timer event.
- External trigger to change the timer behavior depending on external signals
- Break input to force the timer outputs into a defined state
- Three complementary outputs with adjustable dead time
- Interrupt sources: 4 x input capture/output compare, 1 x overflow/update, 1 x break

TIM2 and TIM3: 16-bit PWM timers

- 16-bit auto-reload up-counter
- 15-bit prescaler adjustable to fixed power of two ratios 1…32768
- Timers with three or two individually configurable CAPCOM channels
- Interrupt sources: 2 or 3 x input capture/output compare, 1 x overflow/update

5.7.5 System timer

The typical usage of this timer (TIM4) is the generation of a clock tick.

Table 5. TIM4

Timer	Counter width	Counter type	Prescaler factor	Channels	Inverted outputs	Repetition counter	trigger unit	External trigger	Break input
TIM4	8-bit	Up	2^n n = 0 to 7	0	None	No	No	No	No

- 8-bit auto-reload, adjustable prescaler ratio to any power of two from 1 to 128
- Clock source: master clock
- Interrupt source: 1 x overflow/update

5.8 Analog-to-digital converter (ADC)

The STM8A products described in this datasheet contain a 10-bit successive approximation ADC with up to 16 multiplexed input channels, depending on the package.

ADC features:

- 10-bit resolution
- Single and continuous conversion modes
- Programmable prescaler: f_{MASTER} divided by 2 to 18
- Conversion trigger on timer events and external events
- Interrupt generation at end of conversion
- Selectable alignment of 10-bit data in 2 x 8 bit result register
- Shadow registers for data consistency
- ADC input range: $V_{SSA} = V_{IN} = V_{DDA}$
- Analog watchdog
- Schmitt-trigger on analog inputs can be disabled to reduce power consumption
- Scan mode (single and continuous)
- Dedicated result register for each conversion channel
- Buffer mode for continuous conversion

5.9 Communication interfaces

5.9.1 Serial peripheral interface (SPI)

The devices covered by this datasheet contain one SPI. The SPI is available on all the supported packages.

- Maximum speed: 8 Mbit/s or $f_{MASTER}/2$ both for master and slave
- Full duplex synchronous transfers
- Simplex synchronous transfers on two lines with a possible bidirectional data line
- Master or slave operation - selectable by hardware or software
- CRC calculation
- 1 byte Tx and Rx buffer
- Slave mode/master mode management by hardware or software for both master and slave
- Programmable clock polarity and phase
- Programmable data order with MSB-first or LSB-first shifting
- Dedicated transmission and reception flags with interrupt capability
- SPI bus busy status flag
- Hardware CRC feature for reliable communication:
  - CRC value can be transmitted as last byte in Tx mode
  - CRC error checking for last received byte

5.9.2 Inter integrated circuit (I^2C) interface

The devices covered by this datasheet contain one I^2C interface. The interface is available on all the supported packages.

- I^2C master features:
  - Clock generation
  - Start and stop generation
- I^2C slave features:
  - Programmable I^2C address detection
  - Stop bit detection
- Generation and detection of 7-bit/10-bit addressing and general call
- Supports different communication speeds:
  - Standard speed (up to 100 kHz),
  - Fast speed (up to 400 kHz)
- Status flags:
  - Transmitter/receiver mode flag
  - End-of-byte transmission flag
  - I^2C busy flag
- Error flags:
  - Arbitration lost condition for master mode
  - Acknowledgement failure after address/data transmission
  - Detection of misplaced start or stop condition
  - Overrun/underrun if clock stretching is disabled
- Interrupt:
  - Successful address/data communication
  - Error condition
  - Wakeup from halt
- Wakeup from halt on address detection in slave mode

5.9.3 Universal asynchronous receiver/transmitter with LIN support (LINUART)

The devices covered by this datasheet contain one LINUART interface. The interface is available on all the supported packages. The LINUART is an asynchronous serial communication interface which supports extensive LIN functions tailored for LIN slave applications. In LIN mode it is compliant to the LIN standards rev 1.2 to rev 2.1.

Detailed feature list:

LIN mode

Master mode:

- LIN break and delimiter generation
- LIN break and delimiter detection with separate flag and interrupt source for read back checking.

Slave mode:

- Autonomous header handling – one single interrupt per valid header
- Mute mode to filter responses
- Identifier parity error checking
- LIN automatic resynchronization, allowing operation with internal RC oscillator (HSI) clock source
- Break detection at any time, even during a byte reception
- Header errors detection:
  - Delimiter too short
  - Synch field error
  - Deviation error (if automatic resynchronization is enabled)
  - Framing error in synch field or identifier field
  - Header time-out

UART mode

- Full duplex, asynchronous communications - NRZ standard format (mark/space)
- High-precision baud rate generator
  - A common programmable transmit and receive baud rates up to $f_{MASTER}/16$
- Programmable data word length (8 or 9 bits) – 1 or 2 stop bits – parity control
- Separate enable bits for transmitter and receiver
- Error detection flags
- Reduced power consumption mode
- Multi-processor communication - enter mute mode if address match does not occur
- Wakeup from mute mode (by idle line detection or address mark detection)
- Two receiver wakeup modes:
  - Address bit (MSB)
  - Idle line

5.10 Input/output specifications

The product features four different I/O types:

- Standard I/O 2 MHz
- Fast I/O 10 MHz
- High sink 8 mA, 2 MHz
- True open drain (I^2C interface)

To decrease EMI (electromagnetic interference), high sink I/Os have a limited maximum slew rate. The rise and fall times are similar to those of standard I/Os.

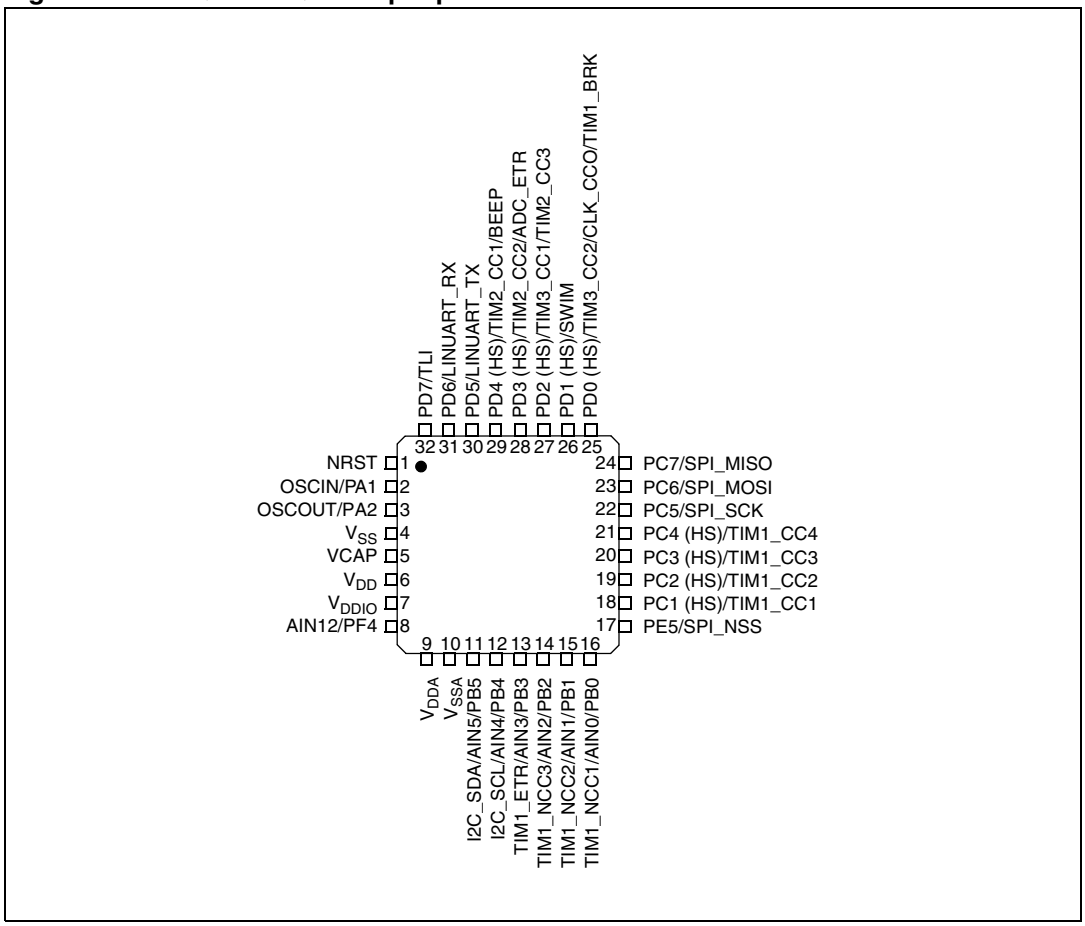
The analog inputs are equipped with a low leakage analog switch. Additionally, the schmitt-trigger input stage on the analog I/Os can be disabled in order to reduce the device standby consumption.

STM8A I/Os are designed to withstand current injection. For a negative injection current of 4 mA, the resulting leakage current in the adjacent input does not exceed 1 µA. Thanks to this feature, external protection diodes against current injection are no longer required.

6 Pinouts and pin description

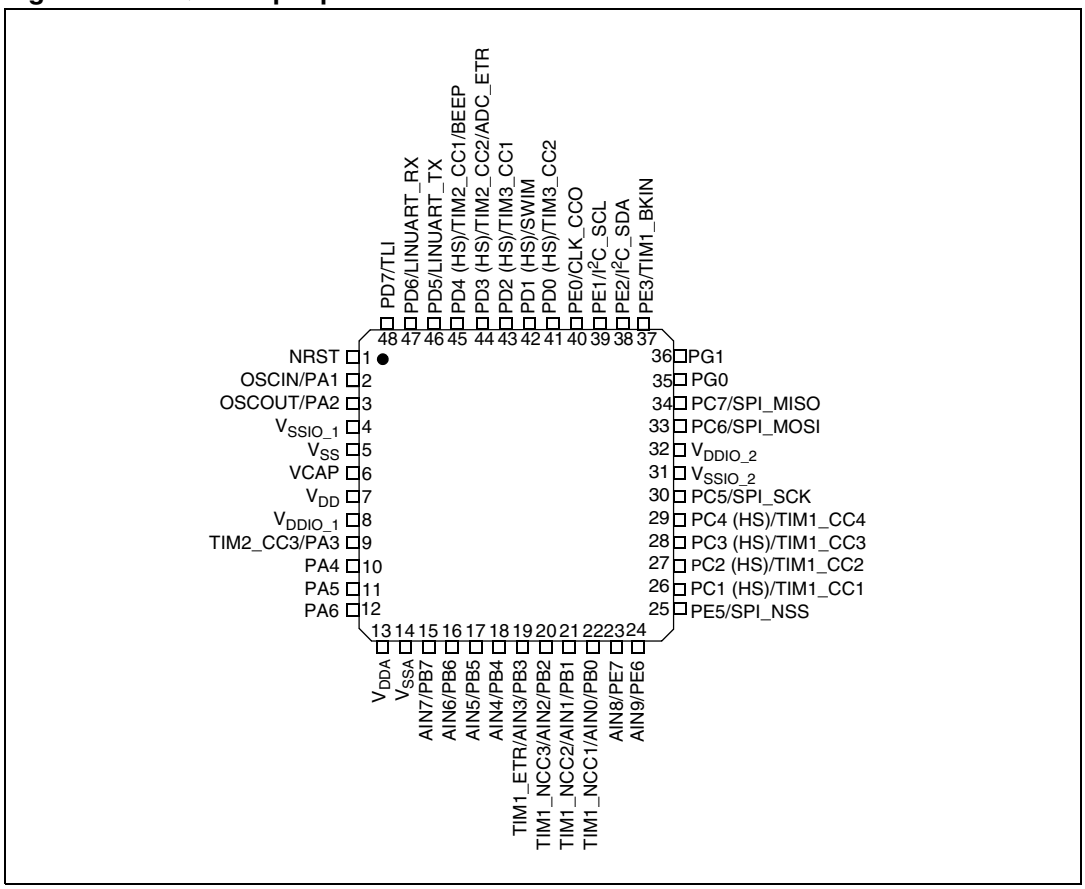
6.1 Package pinouts

Figure 3. VFQFPN/LQFP 32-pin pinout



1. (HS) high sink capability.

Figure 4. LQFP 48-pin pinout



2. (HS) high sink capability.

Table 6. Legend/abbreviation

Type	I= input, O = output, S = power supply	
Level	Input	CM = CMOS (standard for all I/Os)
	Output	HS = High sink (8 mA)
Output speed	O1 = Standard (up to 2 MHz) O2 = Fast (up to 10 MHz) O3 = Fast/slow programmability with slow as default state after reset O4 = Fast/slow programmability with fast as default state after reset	
Port and control configuration	Input	float = floating, wpu = weak pull-up
	Output	T = true open drain, OD = open drain, PP = push pull

Table 7. STM8AF61xx/62xx (32 Kbytes) microcontroller pin description(1)(2)

Pin number		Pin name	Type	Input			Output				Main function (after reset)	Default alternate function	Alternate function after remap [option bit]
LQFP48	VFQFPN/LQFP32			floating	wpu	Ext. interrupt	High sink	Speed	OD	PP			
1	1	NRST	I/O	-	**X**	-	-	-	-	-	Reset		—
2	2	PA1/OSCIN(3)	I/O	**X**	X	-	-	O1	X	X	**Port A1**	Resonator/crystal in	—
3	3	PA2/OSCOUT	I/O	**X**	X	X	-	O1	X	X	**Port A2**	Resonator/crystal out	—
4	-	V_{SSIO_1}	S	-	-	-	-	-	-	-	I/O ground		—
5	4	V_{SS}	S	-	-	-	-	-	-	-	Digital ground		—
6	5	VCAP	S	-	-	-	-	-	-	-	1.8 V regulator capacitor		—
7	6	V_{DD}	S	-	-	-	-	-	-	-	Digital power supply		—
8	7	V_{DDIO_1}	S	-	-	-	-	-	-	-	I/O power supply		—
-	8	PF4/AIN12(4)	I/O	**X**	X		-	O1	X	X	**Port F4**	Analog input 12	—
9	-	PA3/TIM2_CC3	I/O	**X**	X	X	-	O1	X	X	**Port A3**	Timer 2 - channel 3	TIM3_CC1 [AFR1]
10	-	PA4	I/O	**X**	X	X	-	O3	X	X	**Port A4**		—
11	-	PA5	I/O	**X**	X	X	-	O3	X	X	**Port A5**		—
12	-	PA6	I/O	**X**	X	X	-	O3	X	X	**Port A6**		—
13	9	V_{DDA}	S	-	-	-	-	-	-	-	Analog power supply		—
14	10	V_{SSA}	S	-	-	-	-	-	-	-	Analog ground		—
15	-	PB7/AIN7	I/O	**X**	X	X	-	O1	X	X	**Port B7**	Analog input 7	—
16	-	PB6/AIN6	I/O	**X**	X	X	-	O1	X	X	**Port B6**	Analog input 6	—
17	11	PB5/AIN5	I/O	**X**	X	X	-	O1	X	X	**Port B5**	Analog input 5	I^2C_SDA [AFR6]
18	12	PB4/AIN4	I/O	**X**	X	X	-	O1	X	X	**Port B4**	Analog input 4	I^2C_SCL [AFR6]
19	13	PB3/AIN3	I/O	**X**	X	X	-	O1	X	X	**Port B3**	Analog input 3	TIM1_ETR [AFR5]
20	14	PB2/AIN2	I/O	**X**	X	X	-	O1	X	X	**Port B2**	Analog input	TIM1_ NCC3 [AFR5]
21	15	PB1/AIN1	I/O	**X**	X	X	-	O1	X	X	**Port B1**	Analog input 1	TIM1_ NCC2 [AFR5]
22	16	PB0/AIN0	I/O	**X**	X	X	-	O1	X	X	**Port B0**	Analog input 0	TIM1_ NCC1 [AFR5]

Table 7. STM8AF61xx/62xx (32 Kbytes) microcontroller pin description(1)(2) (continued)

Pin number		Pin name	Type	Input			Output				Main function (after reset)	Default alternate function	Alternate function after remap [option bit]
LQFP48	VFQFPN/LQFP32			floating	wpu	Ext. interrupt	High sink	Speed	OD	PP			
23	-	PE7/AIN8	I/O	**X**	X		-	O1	X	X	**Port E7**	Analog input 8	—
24		PE6/AIN9	I/O	**X**	X	X	-	O1	X	X	**Port E7**	Analog input 9	—
25	17	PE5/SPI_NSS	I/O	**X**	X	X	-	O1	X	X	**Port E5**	SPI master/slave select	—
26	18	PC1/TIM1_CC1	I/O	**X**	X	X	HS	O3	X	X	**Port C1**	Timer 1 - channel 1	—
27	19	PC2/TIM1_CC2	I/O	**X**	X	X	HS	O3	X	X	**Port C2**	Timer 1- channel 2	—
28	20	PC3/TIM1_CC3	I/O	**X**	X	X	HS	O3	X	X	**Port C3**	Timer 1 - channel 3	—
29	21	PC4/TIM1_CC4	I/O	**X**	X	X	HS	O3	X	X	**Port C4**	Timer 1 - channel 4	—
30	22	PC5/SPI_SCK	I/O	**X**	X	X		O3	X	X	**Port C5**	SPI clock	—
31	-	V_{SSIO_2}	S	-	-	-	-	-	-	-	I/O ground		—
32	-	V_{DDIO_2}	S	-	-	-	-	-	-	-	I/O power supply		—
33	23	PC6/SPI_MOSI	I/O	**X**	X	X	-	O3	X	X	**Port C6**	SPI master out/ slave in	—
34	24	PC7/SPI_MISO	I/O	**X**	X	X	-	O3	X	X	**Port C7**	SPI master in/ slave out	—
35	-	PG0	I/O	**X**	X	-	-	O1	X	X	**Port G0**	-	—
36	-	PG1	I/O	**X**	X	-	-	O1	X	X	**Port G1**	-	—
37	-	PE3/TIM1_BKIN	I/O	**X**	X	X	-	O1	X	X	**Port E3**	Timer 1 - break input	—
38	-	PE2/I^2C_SDA	I/O	**X**	X	X	-	O1	T(5)	-	**Port E2**	I^2C data	—
39	-	PE1/I^2C_SCL	I/O	**X**	X	X	-	O1	T(5)	-	**Port E1**	I^2C clock	—
40	-	PE0/CLK_CCO	I/O	**X**	X	X	-	O3	X	X	**Port E0**	Configurable clock output	—
41	25	PD0/TIM3_CC2	I/O	**X**	X	X	HS	O3	X	X	**Port D0**	Timer 3 - channel 2	TIM1_BKIN [AFR3]/ CLK_CCO [AFR2]
42	26	PD1/SWIM	I/O	X	**X**	X	HS	O4	X	X	**Port D1**	SWIM data interface	—
43	27	PD2/TIM3_CC1	I/O	**X**	X	X	HS	O3	X	X	**Port D2**	Timer 3 - channel 1	TIM2_CC3 [AFR1]
44	28	PD3/TIM2_CC2	I/O	**X**	X	X	HS	O3	X	X	**Port D3**	Timer 2 - channel 2	ADC_ETR [AFR0]
45	29	PD4/TIM2_CC1/ BEEP	I/O	**X**	X	X	HS	O3	X	X	**Port D4**	Timer 2 - channel 1	BEEP output [AFR7]
46	30	PD5/ LINUART_TX	I/O	**X**	X	X	-	O1	X	X	**Port D5**	LINUART data transmit	—

Table 7. STM8AF61xx/62xx (32 Kbytes) microcontroller pin description(1)(2) (continued)

Pin number		Pin name	Type	Input			Output				Main function (after reset)	Default alternate function		Alternate function after remap [option bit]
LQFP48	VFQFPN/LQFP32			floating	wpu	Ext. interrupt	High sink	Speed	OD	PP				
47	31	PD6/ LINUART_RX	I/O	**X**	X	X	-	O1	X	X	**Port D6**	LINUART data receive		—
48	32	PD7/TLI(6)	I/O	**X**	X	X	-	O1	X	X	**Port D7**	Top level interrupt		—

1. Refer to *Table 6* for the definition of the abbreviations.
2. Reset state is shown in bold.
3. In halt/active halt mode this pad behaves in the following way:
   - the input/output path is disabled
   - if the HSE clock is used for wakeup, the internal weak pull up is disabled
   - if the HSE clock is off, internal weak pull up setting from corresponding OR bit is used
   By managing the OR bit correctly, it must be ensured that the pad is not left floating during halt/active halt.
4. On this pin, a pull-up resistor as specified in *Table 51*. I/O static characteristics is enabled during the reset phase of the product.
5. In the open-drain output column, 'T' defines a true open-drain I/O (P-buffer and protection diode to V_{DD} are not implemented)
6. If this pin is configured as interrupt pin, it will trigger the TLI.

6.2 Alternate function remapping

As shown in the rightmost column of *Table 7*, some alternate functions can be remapped at different I/O ports by programming one of eight AFR (alternate function remap) option bits. Refer to *Section 9: Option bytes on page 47*. When the remapping option is active, the default alternate function is no longer available.

To use an alternate function, the corresponding peripheral must be enabled in the peripheral registers.

Alternate function remapping does not effect GPIO capabilities of the I/O ports (see the GPIO section of the STM8A microcontroller family reference manual, RM0009).

7 Memory and register map

7.1 Memory map

Figure 5. Register and memory map of STM8A products

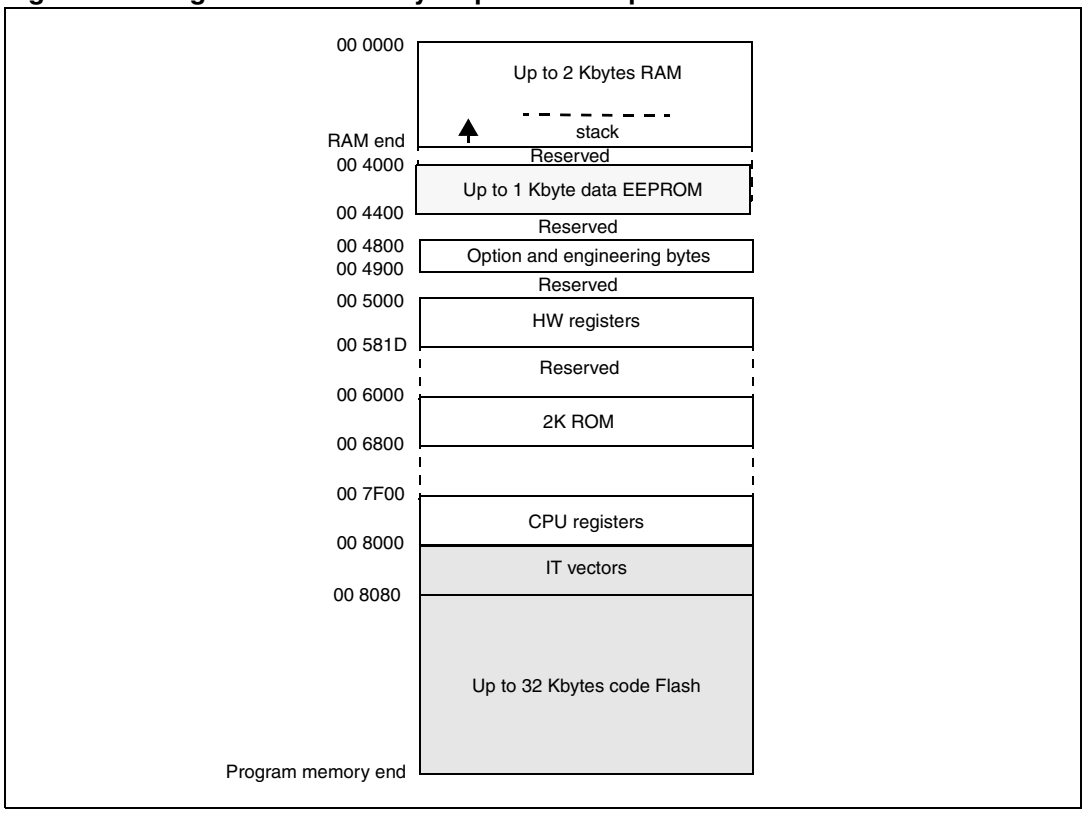


Table 8. Memory model for the devices covered in this datasheet

Program memory size	Program memory end address	RAM size	RAM end address	Stack roll-over address
32K	0FFFFh	2K	07FFh	0600h
16K	0BFFFh	1K	03FFh	n/a(1)
8K	09FFFh	512B	01FFh	n/a(1)

1. If the device is containing the super set silicon (salestype contains SSS), the roll-over address is the same as on the superset device. For more information on stack handling refer to section 2.1.2 in the reference manual RM0009. For more information on salestype composition, refer to section *Section 12* in the present document.

7.2 Register map

In this section the memory map of the devices covered by this datasheet is described. For a detailed description of the functionality of the registers, refer to the reference manual RM009.

7.2.1 I/O register map

Table 9. I/O port hardware register map

Address	Block	Register label	Register name	Reset status
00 5000h	Port A	PA_ODR	Port A data output latch register	00h
00 5001h		PA_IDR	Port A input pin value register	00h
00 5002h		PA_DDR	Port A data direction register	00h
00 5003h		PA_CR1	Port A control register 1	00h
00 5004h		PA_CR2	Port A control register 2	00h
00 5005h	Port B	PB_ODR	Port B data output latch register	00h
00 5006h		PB_IDR	Port B input pin value register	00h
00 5007h		PB_DDR	Port B data direction register	00h
00 5008h		PB_CR1	Port B control register 1	00h
00 5009h		PB_CR2	Port B control register 2	00h
00 500Ah	Port C	PC_ODR	Port C data output latch register	00h
00 500Bh		PB_IDR	Port C input pin value register	00h
00 500Ch		PC_DDR	Port C data direction register	00h
00 500Dh		PC_CR1	Port C control register 1	00h
00 500Eh		PC_CR2	Port C control register 2	00h
00 500Fh	Port D	PD_ODR	Port D data output latch register	00h
00 5010h		PD_IDR	Port D input pin value register	00h
00 5011h		PD_DDR	Port D data direction register	00h
00 5012h		PD_CR1	Port D control register 1	02h
00 5013h		PD_CR2	Port D control register 2	00h
00 5014h	Port E	PE_ODR	Port E data output latch register	00h
00 5015h		PE_IDR	Port E input pin value register	00h
00 5016h		PE_DDR	Port E data direction register	00h
00 5017h		PE_CR1	Port E control register 1	00h
00 5018h		PE_CR2	Port E control register 2	00h

Table 9. I/O port hardware register map (continued)

Address	Block	Register label	Register name	Reset status
00 5019h	Port F	PF_ODR	Port F data output latch register	00h
00 501Ah		PF_IDR	Port F input pin value register	00h
00 501Bh		PF_DDR	Port F data direction register	00h
00 501Ch		PF_CR1	Port F control register 1	00h
00 501Dh		PF_CR2	Port F control register 2	00h
00 501Eh	Port G	PG_ODR	Port G data output latch register	00h
00 501Fh		PG_IDR	Port G input pin value register	00h
00 5020h		PG_DDR	Port G data direction register	00h
00 5021h		PG_CR1	Port G control register 1	00h
00 5022h		PG_CR2	Port G control register 2	00h

7.2.2 Non-volatile memory

Table 10. Non-volatile memory

Address	Register name	7	6	5	4	3	2	1	0
00 505Ah	FLASH_CR1	-	-	-	-	HALT	AHALT	IE	FIX
	Reset value	0	0	0	0	0	0	0	0
00 505Bh	FLASH_CR2	OPT	WPRG	ERASE	FPRG	-	-	-	PRG
	Reset value	0	0	0	0	0	0	0	0
00 505Ch	FLASH_NCR2	NOPT	NWPRG	NERASE	NFPRG	-	-	-	NPRG
	Reset value	1	1	1	1	1	1	1	1
00 505Dh	FLASH_FPR	-	-	WPB5	WPB4	WPB3	WPB2	WPB1	WPB0
	Reset value			0	0	0	0	0	0
00 505Eh	FLASH_NFPR	-	-	NWPB5	NWPB4	NWPB3	NWPB2	NWPB1	NWPB0
	Reset value			1	1	1	1	1	1
00 505Fh	FLASH_IAPSR	-	HVOFF	-	-	DUL	EOP	PUL	WR_PG_DIS
	Reset value	0	1	0	0	0	0	0	0
00 5060h to 00 5061h	Reserved								
00 5062h	FLASH_PUKR	PUK7	PUK6	PUK5	PUK4	PUK3	PUK2	PUK1	PUK0
	Reset value	0	0	0	0	0	0	0	0
00 5063h	Reserved								
00 5064h	FLASH_DUKR	DUK7	DUK6	DUK5	DUK4	DUK3	DUK2	DUK1	DUK0
	Reset value	0	0	0	0	0	0	0	0

7.2.3 CPU registers

Table 11. CPU registers

Address	Block	Register label	Register name	Reset status
00 7F00h	CPU(1)	A	Accumulator	00h
00 7F01h		PCE	Program counter extended	00h
00 7F02h		PCH	Program counter high	80h
00 7F03h		PCL	Program counter low	00h
00 7F04h		XH	X index register high	00h
00 7F05h		XL	X index register low	00h
00 7F06h		YH	Y index register high	00h
00 7F07h		YL	Y index register low	00h
00 7F08h		SPH	Stack pointer high	17h(2)
00 7F09h		SPL	Stack pointer low	FFh
00 7F0Ah		CC	Condition code register	28h

1. Accessible by debug module only
2. Product dependent value, see *Figure 5: Register and memory map of STM8A products*.

7.2.4 Miscellaneous registers

Global configuration register

Table 12. CFG_GCR register map

Address	Register name	7	6	5	4	3	2	1	0
00 7F60h	CFG_GCR	-	-	-	-	-	-	AL	SWD
	Reset value	0	0	0	0	0	0	0	0

Reset status register

Table 13. RST_SR register map

Address	Register name	7	6	5	4	3	2	1	0
00 50B3h	RST_SR	-	-	-	EMCF	SWIMF	ILLOPF	IWDGF	WWDGF
	Reset value	x	x	x	x	x	x	x	x

Temporary memory unprotection key registers

Table 14. TMU register map and reset values

Address	Register name	7	6	5	4	3	2	1	0
00 5800h	TMU_K1	K7	K6	K5	K4	K3	K2	K1	K0
	Reset value	0	0	0	0	0	0	0	0
00 5801h	TMU_K2	K7	K6	K5	K4	K3	K2	K1	K0
	Reset value	0	0	0	0	0	0	0	0
00 5802h	TMU_K3	K7	K6	K5	K4	K3	K2	K1	K0
	Reset value	0	0	0	0	0	0	0	0
00 5803h	TMU_K4	K7	K6	K5	K4	K3	K2	K1	K0
	Reset value	0	0	0	0	0	0	0	0
00 5804h	TMU_K5	K7	K6	K5	K4	K3	K2	K1	K0
	Reset value	0	0	0	0	0	0	0	0
00 5805h	TMU_K6	K7	K6	K5	K4	K3	K2	K1	K0
	Reset value	0	0	0	0	0	0	0	0
00 5807h	TMU_K8	K7	K6	K5	K4	K3	K2	K1	K0
	Reset value	0	0	0	0	0	0	0	0
00 5808h	TMU_CSR	-	-	-	-	ROPS	TIMUE	TMUB	TMUS
	Reset value	0	0	0	0	0	0	0	0

7.2.5 Clock and clock controller

Table 15. CLK register map and reset values

Address	Register name	7	6	5	4	3	2	1	0
00 50C0h	CLK_ICKR	-	-	SWUAH	LSIRDY	LSIEN	FHWU	HSIRDY	HSIEN
	Reset value	0	0	0	0	0	0	0	1
00 50C1h	CLK_ ECKR	-	-	-	-	-	-	HSERDY	HSEEN
	Reset value	0	0	0	0	0	0	0	0
00 50C2h	Reserved								
00 50C3h	CLK_ CMSR	CKM7	CKM6	CKM5	CKM4	CKM3	CKM2	CKM1	CKM0
	Reset value	1	1	1	0	0	0	0	1
00 50C4h	CLK_SWR	SWI7	SWI6	SWI5	SWI4	SWI3	SWI2	SWI1	SWI0
	Reset value	1	1	1	0	0	0	0	1

Table 15. CLK register map and reset values (continued)

Address	Register name	7	6	5	4	3	2	1	0
00 50C5h	CLK_SWCR	-	-	-	-	SWIF	SWIEN	SWEN	SWBSY
	Reset value	x	x	x	x	0	0	0	0
00 50C6h	CLK_CKDIVR	-	-	-	HSIDIV1	HSIDIV0	CPUDIV2	CPUDIV1	CPUDIV
	Reset value	0	0	0	1	1	0	0	0
00 50C7h	CLK_PCKENR1	PCK EN17	PCK EN16	PCK EN15	PCK EN14	PCK EN13	Reserved	PCK EN11	PCK EN10
	Reset value	1	1	1	1	1	1	1	1
00 50C8h	CLK_CSSR	-	-	-	-	CSSD	CSSDIE	AUX	CSSEN
	Reset value	0	0	0	0	0	0	0	0
00 50C9h	CLK_CCOR	-	CCOBSY	CCORDY	CCO SEL3	CCO SEL2	CCO SEL1	CCO SEL0	CCOEN
	Reset value	0	0	0	0	0	0	0	0
00 50CAh	CLK_PCKENR2	Reserved	PCK EN26	Reserved	Reserved	PCK EN23	PCK EN22	Reserved	Reserved
	Reset value	1	1	1	1	1	1	1	1
00 50CCh	CLK_HSITRIMR	-	-	-	-	HSI TRIM3(1)	HSI TRIM2	HSI TRIM1	HSI TRIM0
	Reset value	x	x	x	x	0	0	0	0
00 50CDh	CLK_SWIMCCR	-	-	-	-	-	-	-	SWI MCLK
	Reset value	0	0	0	0	0	0	0	0

1. In compatibility mode, the HSITRIM3 is not available. This mode is selected through the option byte configuration.

7.2.6 Interrupt controller

Interrupt software priority registers

Table 16. Interrupt software priority registers map

Address	Register name	7	6	5	4	3	2	1	0
00 7F70h	ITC_SPR1 Reset value	VECT3SPR1 1	VECT3SPR0 1	VECT2SPR1 1	VECT2SPR0 1	VECT1SPR1 1	VECT1SPR0 1	Reserved 1	Reserved 1
00 7F71h	ITC_SPR2 Reset value	VECT7SPR1 1	VECT7SPR0 1	VECT6SPR1 1	VECT6SPR0 1	VECT5SPR1 1	VECT5SPR0 1	VECT4SPR1 1	VECT4SPR0 1
00 7F72h	ITC_SPR3 Reset value	VECT11SPR1 1	VECT11SPR0 1	VECT10SPR1 1	VECT10SPR0 1	Reserved 1	Reserved 1	Reserved 1	Reserved 1
00 7F73h	ITC_SPR4 Reset value	VECT15SPR1 1	VECT15SPR0 1	VECT14SPR1 1	VECT14SPR0 1	VECT13SPR1 1	VECT13SPR0 1	VECT12SPR1 1	VECT12SPR0 1
00 7F74h	ITC_SPR5 Reset value	VECT19SPR1 1	VECT19SPR0 1	Reserved 1	Reserved 1	Reserved 1	Reserved 1	VECT16SPR1 1	VECT16SPR0 1
00 7F75h	ITC_SPR6 Reset value	VECT23SPR1 1	VECT23SPR0 1	VECT22SPR1 1	VECT22SPR0 1	VECT21SPR1 1	VECT21SPR0 1	VECT20SPR1 1	VECT20SPR0 1

External interrupt control register

Table 17. External interrupt control register map

Address	Register name	7	6	5	4	3	2	1	0
00 50A0h	EXTI_CR1 Reset value	PDIS1 0	PDIS0 0	PCIS1 0	PCIS0 0	PBIS1 0	PBIS0 0	PAIS1 0	PAIS0 0
00 50A1h	EXTI_CR2 Reset value	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	TLIS 0	PEIS1 0	PEIS0 0

7.2.7 Timers

Window watchdog timer

Table 18. WWDG register map and reset values

Address	Register name	7	6	5	4	3	2	1	0
00 50D1h	WWDG_CR	WDGA	T6	T5	T4	T3	T2	T1	T0
	Reset value	0	1	1	1	1	1	1	1
00 50D2h	WWDG_WR	-	W6	W5	W4	W3	W2	W1	W0
	Reset value	0	1	1	1	1	1	1	1

Independent watchdog timer

Table 19. IWDG register map

Address	Register name	7	6	5	4	3	2	1	0
00 50E0h	IWDG_KR	KEY7	KEY6	KEY5	KEY4	KEY3	KEY2	KEY1	KEY0
	Reset value	x	x	x	x	x	x	x	x
00 50E1h	IWDG_PR	-	-	-	-	-	PR2	PR1	PR0
	Reset value	0	0	0	0	0	0	0	0
00 50E2h	IWDG_RLR	RL7	RL6	RL5	RL4	RL3	RL2	RL1	RL0
	Reset value	1	1	1	1	1	1	1	1

Auto- wakeup counter and beeper

Table 20. AWU register map

Address	Register name	7	6	5	4	3	2	1	0
00 50F0h	AWU_CSR	-	-	AWUF	AWUEN	-	-	-	MSR
	Reset value	0	0	0	0	0	0	0	0
00 50F1h	AWU_APR	-	-	APR5	APR4	APR3	APR2	APR1	APR0
	Reset value	0	0	1	1	1	1	1	1
00 50F2h	AWU_TBR	-	-	-	-	AWUTB3	AWUTB2	AWUTB1	AWUTB0
	Reset value	0	0	0	0	0	0	0	0

Table 21. BEEP register map

Address	Register name	7	6	5	4	3	2	1	0
00 50F3h	BEEP_CSR	BEEP SEL2	BEEP SEL1	BEEP EN	BEEP DIV4	BEEP DIV3	BEEP DIV2	BEEP DIV1	BEEP DIV0
	Reset value	0	0	0	0	0	0	0	0

TIM1

Table 22. TIM1 register map

Address	Register name	7	6	5	4	3	2	1	0
00 5250h	TIM1_CR1	ARPE	CMS1	CMS0	DIR	OPM	URS	UDIS	CEN
	Reset value	0	0	0	0	0	0	0	0
00 5251h	TIM1_CR2	TI1S	MMS2	MMS1	MMS0	-	COMS	-	CCPC
	Reset value	0	0	0	0	0	0	0	0
00 5252h	TIM1_SMCR	MSM	TS2	TS1	TS0	-	SMS2	SMS1	SMS0
	Reset value	0	0	0	0	0	0	0	0
00 5253h	TIM1_ETR	ETP	ECE	ETPS1	ETPS0	EFT3	EFT2	EFT1	EFT0
	Reset value	0	0	0	0	0	0	0	0
00 5254h	TIM1_IER	BIE	TIE	COMIE	CC4IE	CC3IE	CC2IE	CC1IE	UIE
	Reset value	0	0	0	0	0	0	0	0
00 5255h	TIM1_SR1	BIF	TIF	COMIF	CC4IF	CC3IF	CC2IF	CC1IF	UIF
	Reset value	0	0	0	0	0	0	0	0
00 5256h	TIM1_SR2	-	-	-	CC4OF	CC3OF	CC2OF	CC1OF	-
	Reset value	0	0	0	0	0	0	0	0
00 5257h	TIM1_EGR	BG	TG	COMG	CC4G	CC3G	CC2G	CC1G	UG
	Reset value	0	0	0	0	0	0	0	0
00 5258h	TIM1_CCMR1 (output mode)	OC1CE	OC1M2	OC1M1	OC1M0	OC1PE	OC1FE	CC1S1	CC1S0
	Reset value	0	0	0	0	0	0	0	0
	TIM1_CCMR1 (input mode)	IC1F3	IC1F2	IC1F1	IC1F0	IC1PSC1	IC1PSC0	CC1S1	CC1S0
	Reset value	0	0	0	0	0	0	0	0
00 5259h	TIM1_ CCMR2 (output mode)	OC2CE	OC2M2	OC2M1	OC2M0	OC2PE	OC2FE	CC2S1	CC2S0
	Reset value	0	0	0	0	0	0	0	0
	TIM1_CCMR2 (input mode)	IC2F3	IC2F2	IC2F1	IC2F0	IC2PSC1	IC2PSC0	CC2S1	CC2S0
	Reset value	0	0	0	0	0	0	0	0
00 525Ah	TIM1_CCMR3 (output mode)	OC3CE	OC3M2	OC3M1	OC3M0	OC3PE	OC3FE	CC3S1	CC3S0
	Reset value	0	0	0	0	0	0	0	0
	TIM1_CCMR3 (input mode)	IC3F3	IC3F2	IC3F1	IC3F0	IC3PSC1	IC3PSC0	CC3S1	CC3S0
	Reset value	0	0	0	0	0	0	0	0

Table 22. TIM1 register map (continued)

Address	Register name	7	6	5	4	3	2	1	0
00 525Bh	TIM1_CCMR4 (output mode)	OC4CE	OC4M2	OC4M1	OC4M0	OC4PE	OC4FE	CC4S1	CC4S0
	Reset value	0	0	0	0	0	0	0	0
	TIM1_CCMR4 (input mode)	IC4F3	IC4F2	IC4F1	IC4F0	IC4PSC1	IC4PSC0	CC4S1	CC4S0
	Reset value	0	0	0	0	0	0	0	0
00 525Ch	TIM1_CCER1	CC2NP	CC2NE	CC2P	CC2E	CC1NP	CC1NE	CC1P	CC1E
	Reset value	0	0	0	0	0	0	0	0
00 525Dh	TIM1_CCER2	-	-	CC4P	CC4E	CC3NP	CC3NE	CC3P	CC3E
	Reset value	0	0	0	0	0	0	0	0
00 525Eh	TIM1_CNTRH	CNT15	CNT14	CNT13	CNT12	CNT11	CNT10	CNT9	CNT8
	Reset value	0	0	0	0	0	0	0	0
00 525Fh	TIM1_CNTRL	CNT7	CNT6	CNT5	CNT4	CNT3	CNT2	CNT1	CNT0
	Reset value	0	0	0	0	0	0	0	0
00 5260h	TIM1_PSCRH	PSC15	PSC14	PSC13	PSC12	PSC11	PSC10	PSC9	PSC8
	Reset value	0	0	0	0	0	0	0	0
00 5261h	TIM1_PSCRL	PSC7	PSC6	PSC5	PSC4	PSC3	PSC2	PSC1	PSC0
	Reset value	0	0	0	0	0	0	0	0
00 5262h	TIM1_ARRH	ARR15	ARR14	ARR13	ARR12	ARR11	ARR10	ARR9	ARR8
	Reset value	1	1	1	1	1	1	1	1
00 5263h	TIM1_ARRL	ARR7	ARR6	ARR5	ARR4	ARR3	ARR2	ARR1	ARR0
	Reset value	1	1	1	1	1	1	1	1
00 5264h	TIM1_RCR	REP7	REP6	REP5	REP4	REP3	REP2	REP1	REP0
	Reset value	0	0	0	0	0	0	0	0
00 5265h	TIM1_CCR1H	CCR115	CCR114	CCR113	CCR112	CCR111	CCR110	CCR19	CCR18
	Reset value	0	0	0	0	0	0	0	0
00 5266h	TIM1_CCR1L	CCR17	CCR16	CCR15	CCR14	CCR13	CCR12	CCR11	CCR10
	Reset value	0	0	0	0	0	0	0	0
00 5267h	TIM1_CCR2H	CCR215	CCR214	CCR213	CCR212	CCR211	CCR210	CCR29	CCR28
	Reset value	0	0	0	0	0	0	0	0
00 5268h	TIM1_CCR2L	CCR27	CCR26	CCR25	CCR24	CCR23	CCR22	CCR21 0	CCR20
	Reset value	0	0	0	0	0	0		0
00 5269h	TIM1_CCR3H	CCR315	CCR314	CCR313	CCR312	CCR311	CCR310	CCR39	CCR38
	Reset value	0	0	0	0	0	0	0	0
00 526Ah	TIM1_CCR3L	CCR37	CCR36	CCR35	CCR34	CCR33	CCR32	CCR31	CCR3
	Reset value	0	0	0	0	0	0	0	0 0
00 526Bh	TIM1_CCR4H	CCR415	CCR414	CCR413	CCR412	CCR411	CCR410	CCR49 0	CCR48
	Reset value	0	0	0	0	0	0		0
00 526Ch	TIM1_CCR4L	CCR47	CCR46	CCR45	CCR44	CCR43	CCR42	CCR41	CCR40
	Reset value	0	0	0	0	0	0	0	0

Table 22. TIM1 register map (continued)

Address	Register name	7	6	5	4	3	2	1	0
00 526Dh	TIM1_BKR	MOE	AOE	BKP	BKE	OSSR	OSSI	LOCK	LOCK
	Reset value	0	0	0	0	0	0	0	0
00 526Eh	TIM1_DTR	DTG7	DTG6	DTG5	DTG4	DTG3	DTG2	DTG1	DTG0
	Reset value	0	0	0	0	0	0	0	0
00 526Fh	TIM1_OISR	-	OIS4	OIS3N	OIS3	OIS2N	OIS2	OIS1N	OIS1
	Reset value	0	0	0	0	0	0	0	0

TIM2

Table 23. TIM2 register map

Address	Register name	7	6	5	4	3	2	1	0
00 5300h	TIM2_CR1	ARPE	-	-	-	OPM	URS	UDIS	CEN
	Reset value	0	0	0	0	0	0	0	0
00 5301h	TIM2_IER	-	-	-	-	CC3IE	CC2IE	CC1IE	UIE
	Reset value	0	0	0	0	0	0	0	0
00 5302h	TIM2_SR1	-	-	-	-	CC3IF	CC2IF	CC1IF	UIF
	Reset value	0	0	0	0	0	0	0	0
00 5303h	TIM2_SR2	-	-	-	-	CC3OF	CC2OF	CC1OF	-
	Reset value	0	0	0	0	0	0	0	0
00 5304h	TIM2_EGR	-	-	-	-	CC3G	CC2G	CC1G	UG
	Reset value	0	0	0	0	0	0	0	0
00 5305h	TIM2_CCMR1 (output mode)	-	OC1M2	OC1M1	OC1M0	OC1PE	-	CC1S1	CC1S0
	Reset value	0	0	0	0	0	0	0	0
	TIM2_CCMR1 (input mode)	IC1F3	IC1F2	IC1F1	IC1F0	IC1PSC1	IC1PSC0	CC1S1	CC1S0
	Reset value	0	0	0	0	0	0	0	0
00 5306h	TIM2_ CCMR2 (output mode)	-	OC2M2	OC2M1	OC2M0	OC2PE	-	CC2S1	CC2S0
	Reset value	0	0	0	0	0	0	0	0
	TIM2_CCMR2 (input mode)	IC2F3	IC2F2	IC2F1	IC2F0	IC2PSC1	IC2PSC0	CC2S1	CC2S0
	Reset value	0	0	0	0	0	0	0	0
00 5307h	TIM2_CCMR3 (output mode)	-	OC3M2	OC3M1	OC3M0	OC3PE	-	CC3S1	CC3S0
	Reset value	0	0	0	0	0	0	0	0
	TIM2_CCMR3 (input mode)	IC3F3	IC3F2	IC3F1	IC3F0	IC3PSC1	IC3PSC0	CC3S1	CC3S0
	Reset value	0	0	0	0	0	0	0	0

Table 23. TIM2 register map (continued)

Address	Register name	7	6	5	4	3	2	1	0
00 5308h	TIM2_CCER1	-	-	CC2P	CC2E	-	-	CC1P	CC1E
	Reset value	0	0	0	0	0	0	0	0
00 5309h	TIM2_CCER2	-	-	-	-	-	-	CC3P	CC3E
	Reset value	0	0	0	0	0	0	0	0
00 530Ah	TIM2_CNTRH	CNT15	CNT14	CNT13	CNT12	CNT11	CNT10	CNT9	CNT8
	Reset value	0	0	0	0	0	0	0	0
00 530Bh	TIM2_CNTRL	CNT7	CNT6	CNT5	CNT4	CNT3	CNT2	CNT1	CNT0
	Reset value	0	0	0	0	0	0	0	0
00 530Ch	TIM2_PSCR	-	-	-	-	PSC3	PSC2	PSC1	PSC0
	Reset value	0	0	0	0	0	0	0	0
00 530Dh	TIM2_ARRH	ARR15	ARR14	ARR13	ARR12	ARR11	ARR10	ARR9	ARR8
	Reset value	1	1	1	1	1	1	1	1
00 530Eh	TIM2_ARRL	ARR7	ARR6	ARR5	ARR4	ARR3	ARR2	ARR1	ARR0
	Reset value	1	1	1	1	1	1	1	1
00 530Fh	TIM2_CCR1H	CCR115	CCR114	CCR113	CCR112	CCR111	CCR110	CCR19	CCR18
	Reset value	0	0	0	0	0	0	0	0
00 5310h	TIM2_CCR1L	CCR17	CCR16	CCR15	CCR14	CCR13	CCR12	CCR11	CCR10
	Reset value	0	0	0	0	0	0	0	0
00 5311h	TIM2_CCR2H	CCR215	CCR214	CCR213	CCR212	CCR211	CCR210	CCR29	CCR28
	Reset value	0	0	0	0	0	0	0	0
00 5312h	TIM2_CCR2L	CCR27	CCR26	CCR25	CCR24	CCR23	CCR22	CCR21	CCR20
	Reset value	0	0	0	0	0	0	0	0
00 5313h	TIM2_CCR3H	CCR315	CCR314	CCR313	CCR312	CCR311	CCR310	CCR39	CCR38
	Reset value	0	0	0	0	0	0	0	0
00 5314h	TIM2_CCR3L	CCR37	CCR36	CCR35	CCR34	CCR33	CCR32	CCR31	CCR30
	Reset value	0	0	0	0	0	0	0	0

TIM3

Table 24. TIM3 register map

Address	Register name	7	6	5	4	3	2	1	0
00 5320h	TIM3_CR1	ARPE	-	-	-	OPM	URS	UDIS	CEN
	Reset value	0	0	0	0	0	0	0	0
00 5321h	TIM3_IER	-	-	-	-	-	CC2IE	CC1IE	UIE
	Reset value	0	0	0	0	0	0	0	0
00 5322h	TIM3_SR1	-	-	-	-	-	CC2IF	CC1IF	UIF
	Reset value	0	0	0	0	0	0	0	0
00 5323h	TIM3_SR2	-	-	-	-	-	CC2OF	CC1OF	-
	Reset value	0	0	0	0	0	0	0	0

Table 24. TIM3 register map (continued)

Address	Register name	7	6	5	4	3	2	1	0
00 5324h	TIM3_EGR	-	-	-	-	-	CC2G	CC1G	UG
	Reset value	0	0	0	0	0	0	0	0
00 5325h	TIM3_CCMR1 (output mode)	-	OC1M2	OC1M1	OC1M0	OC1PE	-	CC1S1	CC1S0
	Reset value	0	0	0	0	0	0	0	0
	TIM3_CCMR1 (input mode)	IC1F3	IC1F2	IC1F1	IC1F0	IC1PSC1	IC1PSC0	CC1S1	CC1S0
	Reset value	0	0	0	0	0	0	0	0
00 5326h	TIM3_ CCMR2 (output mode)	-	OC2M2	OC2M1	OC2M0	OC2PE	-	CC2S1	CC2S0
	Reset value	0	0	0	0	0	0	0	0
	TIM3_CCMR2 (input mode)	IC2F3	IC2F2	IC2F1	IC2F0	IC2PSC1	IC2PSC0	CC2S1	CC2S0
	Reset value	0	0	0	0	0	0	0	0
00 5327h	TIM3_CCER1	-	-	CC2P	CC2E	-	-	CC1P	CC1E
	Reset value	0	0	0	0	0	0	0	0
00 5328h	TIM3_CNTRH	CNT15	CNT14	CNT13	CNT12	CNT11	CNT10	CNT9	CNT8
	Reset value	0	0	0	0	0	0	0	0
00 5329h	TIM3_CNTRL	CNT7	CNT6	CNT5	CNT4	CNT3	CNT2	CNT1	CNT0
	Reset value	0	0	0	0	0	0	0	0
00 532Ah	TIM3_PSCR	-	-	-	-	PSC3	PSC2	PSC1	PSC0
	Reset value	0	0	0	0	0	0	0	0
00 532Bh	TIM3_ARRH	ARR15	ARR14	ARR13	ARR12	ARR11	ARR10	ARR9	ARR8
	Reset value	1	1	1	1	1	1	1	1
00 532Ch	TIM3_ARRL	ARR7	ARR6	ARR5	ARR4	ARR3	ARR2	ARR1	ARR0
	Reset value	1	1	1	1	1	1	1	1
00 532Dh	TIM3_CCR1H	CCR115	CCR114	CCR113	CCR112	CCR111	CCR110	CCR19	CCR18
	Reset value	0	0	0	0	0	0	0	0
00 532Eh	TIM3_CCR1L	CCR17	CCR16	CCR15	CCR14	CCR13	CCR12	CCR11	CCR10
	Reset value	0	0	0	0	0	0	0	0
00 532Fh	TIM3_CCR2H	CCR215	CCR214	CCR213	CCR212	CCR211	CCR210	CCR29	CCR28
	Reset value	0	0	0	0	0	0	0	0
00 5330h	TIM3_CCR2L	CCR27	CCR26	CCR25	CCR24	CCR23	CCR22	CCR21	CCR20
	Reset value	0	0	0	0	0	0	0	0

TIM4

Table 25. TIM4 register map

Address	Register name	7	6	5	4	3	2	1	0
00 5340h	TIM4_CR1	ARPE	-	-	-	OPM	URS	UDIS	CEN
	Reset value	0	0	0	0	0	0	0	0
00 5341h	TIM4_IER	-	-	-	-	-	-	-	UIE
	Reset value	0	0	0	0	0	0	0	0
00 5342h	TIM4_SR1	-	-	-	-	-	-	-	UIF
	Reset value	0	0	0	0	0	0	0	0
00 5343h	TIM4_EGR	-	-	-	-	-	-	-	UG
	Reset value	0	0	0	0	0	0	0	0
00 5344h	TIM4_CNTR	CNT7	CNT6	CNT5	CNT4	CNT3	CNT2	CNT1	CNT0
	Reset value	0	0	0	0	0	0	0	0
00 5345h	TIM4_PSCR	-	-	-	-	-	PSC2	PSC1	PSC0
	Reset value	0	0	0	0	0	0	0	0
00 5346h	TIM4_ARR	ARR7	ARR6	ARR5	ARR4	ARR3	ARR2	ARR1	ARR0
	Reset value	1	1	1	1	1	1	1	1

7.2.8 Communication interfaces

Serial peripheral interface (SPI)

Table 26. SPI register map and reset value

Address	Register name	7	6	5	4	3	2	1	0
005200h	SPI_CR1	LSBFIRST	SPE	BR2	BR1	BR1	MSTR	CPOL	CPHA
	Reset value	0	0	0	0	0	0	0	0
005201h	SPI_CR2	BDM	BDOE	CRCEN	CRCNEXT	Reserved	RXONLY	SSM	SSI
	Reset value	0	0	0	0	0	0	0	0
005202h	SPI_ICR	TXIE	RXIE	ERRIE	WKIE	Reserved	Reserved	Reserved	Reserved
	Reset value	0	0	0	0	0	0	0	0
005203h	SPI_SR	BSY	OVR	MODF	CRCERR	WKUP	Reserved	TXE	RXNE
	Reset value	0	0	0	0	0	0	1	0
005204h	SPI_DR	MSB	-	-	-	-	-	-	LSB
	Reset value	0	0	0	0	0	0	0	0
005205h	SPI_CRCPR	MSB	-	-	-	-	-	-	LSB
	Reset value	0	0	0	0	0	1	1	1

Table 26. SPI register map and reset value (continued)

Address	Register name	7	6	5	4	3	2	1	0
005206h	SPI_ RXCRCR	MSB	-	-	-	-	-	-	LSB
	Reset value	0	0	0	0	0	0	0	0
005207h	SPI_ TXCRCR	MSB	-	-	-	-	-	-	LSB
	Reset value	0	0	0	0	0	0	0	0

Inter integrated circuit (I^2C) interface

Table 27. I^2C register map

Address	Register name	7	6	5	4	3	2	1	0
00 5210h	I2C_CR1	NO STRETCH	ENGC	-	-	-	-	-	PE
	Reset value	0	0	0	0	0	0	0	0
00 5211h	I2C_CR2	SWRST	-	-	-	POS	ACK	STOP	START
	Reset value	0	0	0	0	0	0	0	0
00 5212h	I2C_ FREQR	-	-	FREQ5	FREQ4	FREQ3	FREQ2	FREQ1	FREQ0
	Reset value	0	0	0	0	0	0	0	0
00 5213h	I2C_OARL	ADD7	ADD6	ADD5	ADD4	ADD3	ADD2	ADD1	ADD0
	Reset value	0	0	0	0	0	0	0	0
00 5214h	I2C_OARH	ADD MODE	ADD CONF	-	-	-	ADD9	ADD8	-
	Reset value	0	0	0	0	0	0	0	0
00 5215h	Reserved								
00 5216h	I2C_DR	DR7	DR6	DR5	DR4	DR3	DR2	DR1	DR0
	Reset value	0	0	0	0	0	0	0	0
00 5217h	I2C_SR1	TxE	RxNE	-	STOPF	ADD10	BTF	ADDR	SB
	Reset value	0	0	0	0	0	0	0	0
00 5218h	I2C_SR2	-	-	WUFH	-	OVR	AF	ARLO	BERR
	Reset value	0	0	0	0	0	0	0	0

Table 27. I²C register map (continued)

Address	Register name	7	6	5	4	3	2	1	0
00 5219h	I2C_SR3 Reset value	- 0	- 0	- 0	GEN CALL 0	- 0	TRA 0	BUSY 0	MSL 0
00 521Ah	I2C_ITR Reset value	- 0	- 0	- 0	- 0	- 0	ITBUFEN 0	ITEVTEN 0	ITERREN 0
00 521Bh	I2C_CCRL Reset value	CCR7 0	CCR6 0	CCR5 0	CCR4 0	CCR3 0	CCR2 0	CCR1 0	CCR0 0
00 521Ch	I2C_CCRH Reset value	FS 0	DUTY 0	- 0	- 0	CCR11 0	CCR10 0	CCR9 0	CCR8 0
00 521Dh	I2C_ TRISER Reset value	- 0	- 0	TRISE5 0	TRISE4 0	TRISE3 0	TRISE2 0	TRISE1 1	TRISE0 0

Universal asynchronous receiver/transmitter with LIN support (LINUART)

Table 28. LINUART register map and reset value

Address	Register name	7	6	5	4	3	2	1	0
00 5240h	LINUART_SR Reset value	TXE 1	TC 1	RXNE 0	IDLE 0	OR/LHE 0	NF 0	FE 0	PE 0
005241h	LINUART_DR Reset value	DR7 0	DR6 0	DR5 0	DR4 0	DR3 0	DR2 0	DR1 0	DR0 0
00 5242h	LINUART_BRR1 Reset value	LDIV[11:8] 00000000							
00 5243h	LINUART_BRR2 Reset value	LDIV[15:12] 0000				LDIV[3:0] 0000			
00 5244h	LINUART_CR1 Reset value	R8 0	T8 0	UARTD 0	M 0	WAKE 0	PCEN 0	PS 0	PIEN 0
00 5245h	LINUART_CR2 Reset value	TIEN 0	TCIEN 0	RIEN 0	ILIEN 0	TEN 0	REN 0	RWU 0	SBK 0
00 5246h	LINUART_CR3 Reset value	- 0	LINEN 0	STOP 00		- 0	- 0	- 0	- 0
00 5247h	LINUART_CR4 Reset value	- 0	LBDIEN 0	LBDL 0	LBDF 0	ADD[3:0] 0000			

Table 28. LINUART register map and reset value (continued)

Address	Register name	7	6	5	4	3	2	1	0
00 5248h	Reserved								
00 5249h	LINUART_CR6 Reset value	LDUM 0	- 0	LSLV 0	LASE 0	- 0	LHDIEN 0	LHDF 0	LSF 0

7.2.9 Analog-to-digital converter (ADC)

Table 29. ADC register map and reset values

Address	Register name	7	6	5	4	3	2	1	0
00 53E0h	ADC _DB0RH(1) Reset value	DATA9 0	DATA8 0	DATA7 0	DATA6 0	DATA5 0	DATA4 0	DATA3 0	DATA2 0
00 53E1h	ADC_DB0RL(1) Reset value	DATA1 0	DATA0 0	- 0	- 0	- 0	- 0	- 0	- 0
. . .									
00 53F2h	ADC _DB9RH(1) Reset value	DATA9 0	DATA8 0	DATA7 0	DATA6 0	DATA5 0	DATA4 0	DATA3 0	DATA2 0
00 53F3h	ADC_DB9RL(1) Reset value	DATA1 0	DATA0 0	- 0	- 0	- 0	- 0	- 0	- 0
00 5400h	ADC _CSR Reset value	EOC 0	AWD 0	EOCIE 0	AWDIE 0	CH3 0	CH2 0	CH1 0	CH0 0
00 5401h	ADC_CR1 Reset value	- 0	SPSEL2 0	SPSEL1 0	SPSEL0 0	- 0	- 0	CONT 0	ADON 0
00 5402h	ADC_CR2 Reset value	- 0	EXTTRIG 0	EXTSEL1 0	EXTSEL0 0	ALIGN 0	- 0	SCAN 0	- 0
00 5403h	ADC_CR3 Reset value	DBUF 0	OVR 0	- 0	- 0	- 0	- 0	- 0	- 0
00 5404h	ADC_DRH1 Reset value	DATA9 0	DATA8 0	DATA7 0	DATA6 0	DATA5 0	DATA4 0	DATA3 0	DATA2 0
00 5405h	ADC_DRL1 Reset value	DATA1 0	DATA0 0	- 0	- 0	- 0	- 0	- 0	- 0
00 5406h	ADC_TDRH Reset value	- 0	- 0	- 0	- 0	- 0	- 0	TD9 0	TD8 0
00 5407h	ADC_TDRL Reset value	TD7 0	TD6 0	TD5 0	TD4 0	TD3 0	TD2 0	TD1 0	TD0 0
00 5408h	ADC _HTRH Reset value	HT9 1	HT8 1	HT7 1	HT6 1	HT5 1	HT4 1	HT3 1	HT2 1
00 5409h	ADC_HTRL Reset value	HT1 1	HT0 1	- 0	- 0	- 0	- 0	- 0	- 0
00 540Ah	ADC _LTRH Reset value	LT9 0	LT8 0	LT7 0	LT6 0	LT5 0	LT4 0	LT3 0	LT2 0

Table 29. ADC register map and reset values (continued)

Address	Register name	7	6	5	4	3	2	1	0
00 540Bh	ADC_LTRL Reset value	LT1 0	LT0 0	- 0	- 0	- 0	- 0	- 0	- 0
00 540Ch	ADC _AWSRH Reset value	- 0	- 0	- 0	- 0	- 0	- 0	AWS9 0	AWS8 0
00 540Dh	ADC_AWSRL Reset value	AWS7 0	AWS6 0	AWS5 0	AWS4 0	AWS3 0	AWS2 0	AWS1 0	AWS0 0
00 540Eh	ADC _AWCRH Reset value	- 0	- 0	- 0	- 0	- 0	- 0	AWEN9 0	AWEN8 0
00 540Fh	ADC_AWCRL Reset value	AWEN7 0	AWEN6 0	AWEN5 0	AWEN4 0	AWEN3 0	AWEN2 0	AWEN1 0	AWEN0 0

1. In this table, the default alignment of the register is shown. The register alignment can be chosen by software.

8 Interrupt table

Table 30. STM8A interrupt table

Priority	Source block	Description	Interrupt vector address	Wakeup from halt	Comments
—	Reset	Reset	6000h	Yes	Reset vector in ROM
—	TRAP	SW interrupt	8004h	—	—
0	TLI	External top level interrupt	8008h	—	—
1	AWU	Auto-wakeup from halt	800Ch	Yes	—
2	Clock controller	Main clock controller	8010h	—	—
3	MISC	Ext interrupt E0	8014h	Yes	Port A interrupts
4	MISC	Ext interrupt E1	8018h	Yes	Port B interrupts
5	MISC	Ext interrupt E2	801Ch	Yes	Port C interrupts
6	MISC	Ext interrupt E3	8020h	Yes	Port D interrupts
7	MISC	Ext interrupt E4	8024h	Yes	Port E interrupts
8	Reserved(1)	—	—	—	—
9	Reserved(1)	—	—	—	—
10	SPI	End of transfer	8030h	Yes	—
11	Timer 1	Update/overflow/ trigger/break	8034h	—	—
12	Timer 1	Capture/compare	8038h	—	—
13	Timer 2	Update/overflow	803Ch	—	—
14	Timer 2	Capture/compare	8040h	—	—
15	Timer 3	Update/overflow	8044h	—	—
16	Timer 3	Capture/compare	8048h	—	—
17	Reserved(1)	—	—	—	—
18	Reserved(1)	—	—	—	—
19	I^2C	I^2C interrupts	8054h	Yes	—
20	LINUART (SCI2)	Tx complete/error	8058h	—	—
21	LINUART (SCI2)	Receive data full reg.	805Ch	—	—
22	ADC	End of conversion	8060h	—	—
23	Timer 4	Update/overflow	8064h	—	—
24	EEPROM	End of Programming/ Write in not allowed area	8068h	—	—

1. All reserved and unused interrupts must be initialized with ‘IRET’ for robust programming.

9 Option bytes

Option bytes contain configurations for device hardware features as well as the memory protection of the device. They are stored in a dedicated block of the memory. Each option byte has to be stored twice, for redundancy, in a regular form (OPTx) and a complemented one (NOPTx), except for the ROP (read-out protection) option byte and option bytes 8 to 16.

Option bytes can be modified in ICP mode (via SWIM) by accessing the EEPROM address shown in *Table 31: Option bytes* below.

Option bytes can also be modified 'on the fly' by the application in IAP mode, except the ROP and UBC options that can only be toggled in ICP mode (via SWIM).

Refer to the STM8 Flash programming manual (PM0047) and STM8 SWIM communication protocol and debug module user manual (UM0470) for information on SWIM programming procedures.

Table 31. Option bytes

Addr.	Option name	Option byte no.	Option bits								Factory default setting
			7	6	5	4	3	2	1	0	
4800h	Read-out protection (ROP)	OPT0	ROP[7:0]								00h
4801h	User boot code (UBC)	OPT1	Reserved		UBC[5:0]						00h
4802h		NOPT1	Reserved		NUBC[5:0]						FFh
4803h	Alternate function remapping (AFR)	OPT2	AFR7	AFR6	AFR5	AFR4	AFR3	AFR2	AFR1	AFR0	00h
4804h		NOPT2	NAFR 7	NAFR 6	NAFR 5	NAFR 4	NAFR 3	NAFR 2	NAFR 1	NAFR 0	FFh
4805h	Watchdog option	OPT3	Reserved			16MHZ TRIM0	LSI _EN	IWDG _HW	WWDG _HW	WWDG _HALT	00h
4806h		NOPT3	Reserved			N16MHZ TRIM0	NLSI _EN	NIWDG _HW	NWWD G_HW	NWWG _HALT	FFh
4807h	Clock option	OPT4	Reserved				EXT CLK	CKAWU SEL	PRS C1	PRS C0	00h
4808h		NOPT4	Reserved				NEXT CLK	NCKAW USEL	NPR SC1	NPR SC0	FFh
4809h	HSE clock startup	OPT5	HSECNT[7:0]								00h
480Ah		NOPT5	NHSECNT[7:0]								FFh
480Bh	TMU	OPT6	TMU[3:0]								00h
480Ch		NOPT6	NTMU[3:0]								FFh
480Dh	Flash wait states	OPT7	Reserved							WAIT STATE	00h
480Eh		NOPT7	Reserved							NWAIT STATE	FFh

Table 31. Option bytes (continued)

Addr.	Option name	Option byte no.	Option bits								Factory default setting
			7	6	5	4	3	2	1	0	
480Fh	Reserved										
4810h	TMU	OPT8	TMU_KEY 1 [7:0]								00h
4811h		OPT9	TMU_KEY 2 [7:0]								00h
4812h		OPT10	TMU_KEY 3 [7:0]								00h
4813h		OPT11	TMU_KEY 4 [7:0]								00h
4814h		OPT12	TMU_KEY 5 [7:0]								00h
4815h		OPT13	TMU_KEY 6 [7:0]								00h
4816h		OPT14	TMU_KEY 7 [7:0]								00h
4817h		OPT15	TMU_KEY 8 [7:0]								00h
4818h		OPT16	TMU MAX_ATT [7:0]								00h
4819h to 487Dh	Reserved										
487Eh	Boot-loader	OPT17	BL [7:0]								00h
487Fh		NOPT17	NBL[7:0]								00h

Table 32. Option byte description

Option byte no.	Description
OPT0	**ROP[7:0]: Memory readout protection (ROP)** AAh: Enable readout protection (write access via SWIM protocol) *Note: Refer to the STM8A microcontroller family reference manual (RM0009) section on Flash/EEPROM memory readout protection for details.*
OPT1	**UBC[5:0]: User boot code area** 00h: No UBC, no write-protection 01h: Page 0 to 1 defined as UBC, memory write-protected 02h: Page 0 to 3 defined as UBC, memory write-protected 03h to 3Fh: Pages 4 to 63 defined as UBC, memory write-protected *Note: Refer to the STM8A microcontroller family reference manual (RM0009) section on Flash/EEPROM write protection for more details.*
OPT2	**AFR7: Alternate function remapping option 7** 0: Port D4 alternate function = TIM2_CC1 1: Port D4 alternate function = BEEP **AFR6: Alternate function remapping option 6** 0: Port B5 alternate function = AIN5, port B4 alternate function = AIN4 1: Port B5 alternate function = I^2C_SDA, port B4 alternate function = I^2C_SCL. **AFR5: Alternate function remapping option 5** 0: Port B3 alternate function = AIN3, port B2 alternate function = AIN2, port B1 alternate function = AIN1, port B0 alternate function = AIN0. 1: Port B3 alternate function = TIM1_ETR, port B2 alternate function = TIM1_NCC3, port B1 alternate function = TIM1_NCC2, port B0 alternate function = TIM1_NCC1. **AFR4: Alternate function remapping option 4** Reserved, bit must be kept at "0" **AFR3: Alternate function remapping option 3** 0: Port D0 alternate function = TIM3_CC2 1: Port D0 alternate function = TIM1_BKIN **AFR2: Alternate function remapping option 2** 0: Port D0 alternate function = TIM3_CC2 1: Port D0 alternate function = CLK_CCO *Note: AFR2 option has priority over AFR3 if both are activated* **AFR1: Alternate function remapping option 1** 0: Port A3 alternate function = TIM2_CC3, port D2 alternate function TIM3_CC1. 1: Port A3 alternate function = TIM3_CC1, port D2 alternate function TIM2_CC3. **AFR0: Alternate function remapping option 0** 0: Port D3 alternate function = TIM2_CC2 1: Port D3 alternate function = ADC_ETR

Table 32. Option byte description (continued)

Option byte no.	Description
OPT3	**HSITRIM: Trimming option for 16 MHz internal RC oscillator** 0: 3-bit on-the-fly trimming (compatible with devices based on the 128K silicon) 1: 4-bit on-the-fly trimming
	LSI_EN: Low speed internal clock enable 0: LSI clock is not available as CPU clock source 1: LSI clock is available as CPU clock source
	IWDG_HW: Independent watchdog 0: IWDG independent watchdog activated by software 1: IWDG independent watchdog activated by hardware
	WWDG_HW: Window watchdog activation 0: WWDG window watchdog activated by software 1: WWDG window watchdog activated by hardware
	WWDG_HALT: Window watchdog reset on halt 0: No reset generated on halt if WWDG active 1: Reset generated on halt if WWDG active
OPT4	**EXTCLK: External clock selection** 0: External crystal connected to OSCIN/OSCOUT 1: External clock signal on OSCIN
	CKAWUSEL: Auto-wakeup unit/clock 0: LSI clock source selected for AWU 1: HSE clock with prescaler selected as clock source for AWU
	PRSC[1:0]: AWU clock prescaler 00: Reserved 01: 16 MHz to 128 kHz prescaler 10: 8 MHz to 128 kHz prescaler 11: 4 MHz to 128 kHz prescaler
OPT5	**HSECNT[7:0]: HSE crystal oscillator stabilization time** This configures the stabilization time to 0.5, 8, 128, and 2048 HSE cycles with corresponding option byte values of E1h, D2h, B4h, and 00h.
OPT6	**TMU[3:0]: Enable temporary memory unprotection** 0101: TMU disabled (permanent ROP). Any other value: TMU enabled.
OPT7	**Reserved**
OPT8	**TMU_KEY 1 [7:0]: Temporary unprotection key 0** Temporary unprotection key: Must be different from 00h or FFh
OPT9	**TMU_KEY 2 [7:0]: Temporary unprotection key 1** Temporary unprotection key: Must be different from 00h or FFh
OPT10	**TMU_KEY 3 [7:0]: Temporary unprotection key 2** Temporary unprotection key: Must be different from 00h or FFh
OPT11	**TMU_KEY 4 [7:0]: Temporary unprotection key 3** Temporary unprotection key: Must be different from 00h or FFh

Table 32. Option byte description (continued)

Option byte no.	Description
OPT12	**TMU_KEY 5 [7:0]: Temporary unprotection key 4** Temporary unprotection key: Must be different from 00h or FFh
OPT13	**TMU_KEY 6 [7:0]: Temporary unprotection key 5** Temporary unprotection key: Must be different from 00h or FFh
OPT14	**TMU_KEY 7 [7:0]: Temporary unprotection key 6** Temporary unprotection key: Must be different from 00h or FFh
OPT15	**TMU_KEY 8 [7:0]: Temporary unprotection key 7** Temporary unprotection key: Must be different from 00h or FFh
OPT16	**TMU_MAXATT [7:0]: TMU access failure counter** Every unsuccessful trial to enter the temporary unprotection procedure increments the counter. More than 64 unsuccessful trials trigger the global erase of the code and data memory.
OPT17	**BL [7:0]: Bootloader enable** If this option byte is set to 55h (complementary value AAh) the bootloader program is activated also in case of a programmed code memory (for more details, see the bootloader user manual, UM0500).

10 Electrical characteristics

10.1 Parameter conditions

Unless otherwise specified, all voltages are referred to V_{SS}.

10.1.1 Minimum and maximum values

Unless otherwise specified the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage and frequencies by tests in production on 100 % of the devices with an ambient temperature at T_A = -40 °C, T_A = 25 °C, and T_A = T_{Amax} (given by the selected temperature range).

Data based on characterization results, design simulation and/or technology characteristics are indicated in the table footnotes and are not tested in production.

10.1.2 Typical values

Unless otherwise specified, typical data are based on T_A = 25 °C, V_{DD} = 5.0 V. They are given only as design guidelines and are not tested.

Typical ADC accuracy values are determined by characterization of a batch of samples from a standard diffusion lot over the full temperature range.

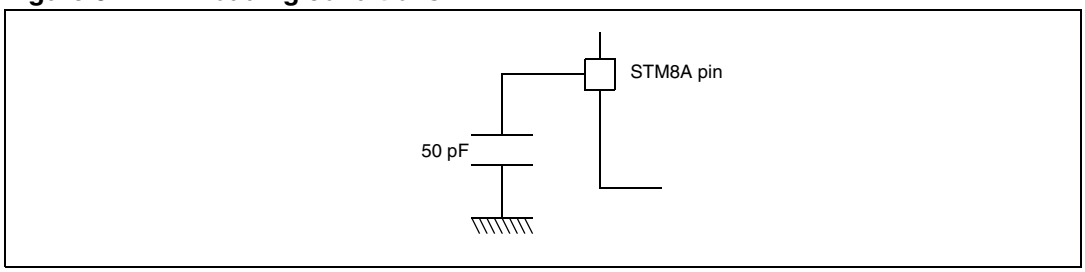
10.1.3 Typical curves

Unless otherwise specified, all typical curves are given only as design guidelines and are not tested.

10.1.4 Loading capacitor

The loading conditions used for pin parameter measurement are shown in *Figure 6*.

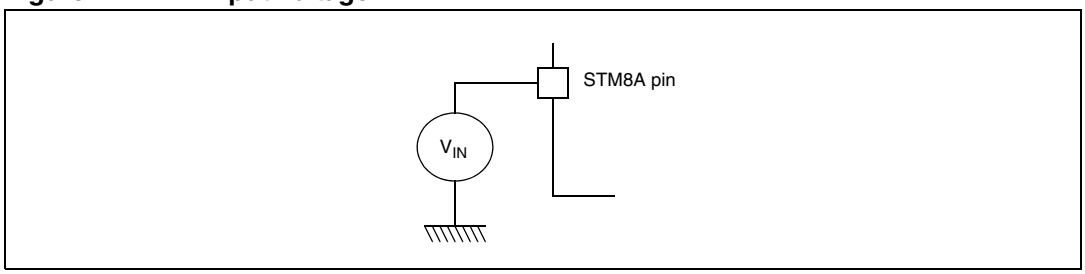
Figure 6. Pin loading conditions



10.1.5 Pin input voltage

The input voltage measurement on a pin of the device is described in *Figure 7*.

Figure 7. Pin input voltage



10.2 Absolute maximum ratings

Stresses above those listed as 'absolute maximum ratings' may cause permanent damage to the device. This is a stress rating only and functional operation of the device under these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 33. Voltage characteristics

Symbol	Ratings	Min	Max	Unit
V_{DDx} - V_{SS}	Supply voltage (including V_{DDA} and V_{DDIO})(1)	-0.3	6.5	V
V_{IN}	Input voltage on true open drain pins (PE1, PE2)(2)	V_{SS} - 0.3	6.5	V
	Input voltage on any other pin(2)	V_{SS} - 0.3	V_{DD} + 0.3	
$\lvert V_{DDx} - V_{DD} \rvert$	Variations between different power pins	-	50	mV
$\lvert V_{SSx} - V_{SS} \rvert$	Variations between all the different ground pins	-	50	
V_{ESD}	Electrostatic discharge voltage	see *Absolute maximum ratings (electrical sensitivity) on page 79*		

1. All power (V_{DD}, V_{DDIO}, V_{DDA}) and ground (V_{SS}, V_{SSIO}, V_{SSA}) pins must always be connected to the external power supply
2. $I_{INJ(PIN)}$ must never be exceeded. This is implicitly insured if V_{IN} maximum is respected. If V_{IN} maximum cannot be respected, the injection current must be limited externally to the $I_{INJ(PIN)}$ value. A positive injection is induced by $V_{IN} > V_{DD}$ while a negative injection is induced by $V_{IN} < V_{SS}$. For true open-drain pads, there is no positive injection current, and the corresponding V_{IN} maximum must always be respected

Table 34. Current characteristics

Symbol	Ratings	Max.	Unit
I_{VDDIO}	Total current into V_{DDIO} power lines (source)(1)(2)(3)	100	mA
I_{VSSIO}	Total current out of $V_{SS\ IO}$ ground lines (sink)(1)(2)(3)	100	
I_{IO}	Output current sunk by any I/O and control pin	20	
	Output current source by any I/Os and control pin	-20	
$I_{INJ(PIN)}$(4)	Injected current on any pin	±10	
$I_{INJ(TOT)}$	Sum of injected currents	50	

1. All power (V_{DD}, V_{DDIO}, V_{DDA}) and ground (V_{SS}, V_{SSIO}, V_{SSA}) pins must always be connected to the external supply.
2. The total limit applies to the sum of operation and injected currents.
3. V_{DDIO} includes the sum of the positive injection currents. V_{SSIO} includes the sum of the negative injection currents.
4. This condition is implicitly insured if V_{IN} maximum is respected. If V_{IN} maximum cannot be respected, the injection current must be limited externally to the $I_{INJ(PIN)}$ value. A positive injection is induced by $V_{IN} > V_{DD}$ while a negative injection is induced by $V_{IN} < V_{SS}$. For true open-drain pads, there is no positive injection current allowed and the corresponding V_{IN} maximum must always be respected.

Table 35. Thermal characteristics

Symbol	Ratings	Value	Unit
T_{STG}	Storage temperature range	–65 to 150	°C
T_J	Maximum junction temperature	160	

Table 36. Operating lifetime(1)

Symbol	Ratings	Value	Unit
OLF	Conforming to AEC-Q100 rev G	–40 to 125 °C	Grade 1
		–40 to 150 °C	Grade 0

1. For detailed mission profile analysis, please contact your local ST Sales Office.

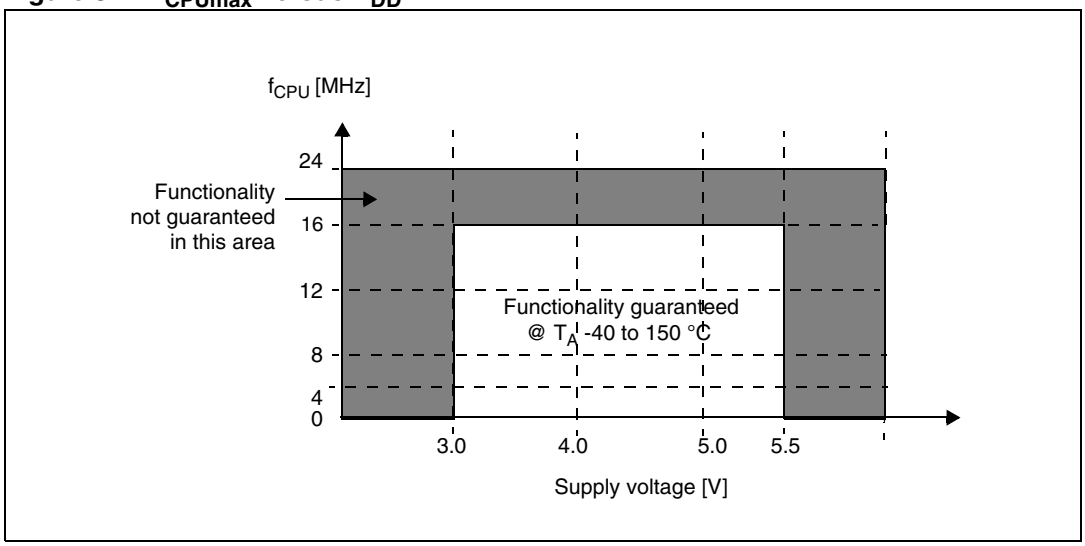
10.3 Operating conditions

Table 37. General operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
f_{CPU}	Internal CPU clock frequency	T_A = -40 °C to 150 °C	0	16	MHz
V_{DD}/V_{DDIO}	Standard operating voltage	-	3.0	5.5	V
V_{CAP}	C_{EXT}: capacitance of external capacitor(1)	-	470	3300	nF
	ESR of external capacitor(1)	at 1 MHz	-	0.3	Ω
	ESL of external capacitor(1)	-	-	15	nH
P_D	Power dissipation (all temperature ranges)	LQFP32	-	85	mW
		VFQFPN32	-	200	
		LQFP48	-	88	
T_A	Ambient temperature	Suffix A	-40	85	°C
		Suffix B		105	
		Suffix C		125	
		Suffix D(2)		150	
T_J	Junction temperature range	Suffix A		90	
		Suffix B		110	
		Suffix C		130	
		Suffix D(2)		155	

1. This parameter range must be respected for the full application range, and taking into account the physical capacitor characteristics and tolerance.
2. Available on STM8AF62xx devices only.

Figure 8. f_{CPUmax} versus V_{DD}



1. This figure is valid only for STM8AF62xx devices.

Table 38. Operating conditions at power-up/power-down

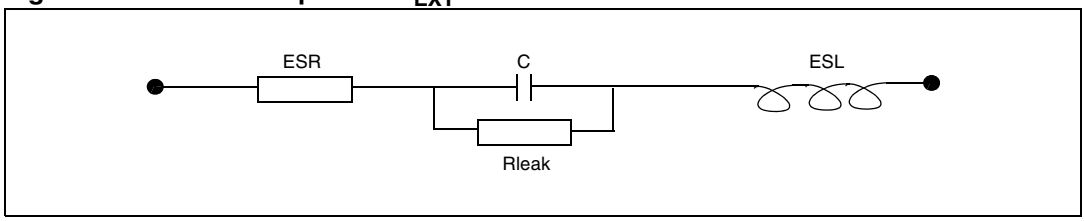
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{VDD}	V_{DD} rise time rate	-	2(1)	-	∞	µs/V
	V_{DD} fall time rate	-	2(1)	-	∞	
t_{TEMP}	Reset release delay	V_{DD} rising	-	3	-	ms
	Reset generation delay	V_{DD} falling	-	3	-	µs
V_{IT+}	Power-on reset threshold(2)	-	2.65	2.8	2.95	V
V_{IT-}	Brown-out reset threshold	-	2.58	2.73	2.88	
$V_{HYS(BOR)}$	Brown-out reset hysteresis	-	-	70(1)	-	mV

1. Guaranteed by design, not tested in production
2. If V_{DD} is below 3 V, the code execution is guaranteed above the V_{IT-} and V_{IT+} thresholds. RAM content is kept. The EEPROM programming sequence must not be initiated.

10.3.1 VCAP external capacitor

Stabilization for the main regulator is achieved connecting an external capacitor C_{EXT} to the V_{CAP} pin. C_{EXT} is specified in *Table 37*. Care should be taken to limit the series inductance to less than 15 nH.

Figure 9. External capacitor C_{EXT}



1. Legend: ESR is the equivalent series resistance and ESL is the equivalent inductance.

10.3.2 Supply current characteristics

The current consumption is measured as described in *Figure 6 on page 52* and *Figure 7 on page 53*.

If not explicitly stated, general conditions of temperature and voltage apply.

General conditions for VDD apply. TA = -40 °C to 150 °C unless otherwise stated.

Table 39. Total current consumption in run, wait and slow mode.

Symbol	Parameter	Conditions		Typ	Max	Unit
$I_{DD(RUN)}$(1)	Supply current in run mode	All peripherals clocked, code executed from EEPROM, HSE external clock	f_{CPU} = 16 MHz	7.4	14	mA
			f_{CPU} = 8 MHz	4.0	7.4(2)	
			f_{CPU} = 4 MHz	2.4	4.1(2)	
			f_{CPU} = 2 MHz	1.5	2.5	
$I_{DD(RUN)}$(1)	Supply current in run mode	All peripherals clocked, code executed from RAM and EEPROM, HSE external clock	f_{CPU} = 16 MHz	3.7	5.0	
			f_{CPU} = 8 MHz	2.2	3.0(2)	
			f_{CPU} = 4 MHz	1.4	2.0(2)	
			f_{CPU} = 2 MHz	1.0	1.5	
$I_{DD(WFI)}$(1)	Supply current in wait mode	CPU stopped, all peripherals off, HSE external clock	f_{CPU} = 16 MHz	1.65	2.5	
			f_{CPU} = 8 MHz	1.15	1.9(2)	
			f_{CPU} = 4 MHz	0.90	1.6(2)	
			f_{CPU} = 2 MHz	0.80	1.5	
$I_{DD(SLOW)}$(1)	Supply current in slow mode	f_{CPU} scaled down, all peripherals off, code executed from RAM	Extclock 16 MHz f_{CPU} = 125 kHz	1.50	1.95	
			LSI internal RC f_{CPU} = 128 kHz	1.50	1.80(2)	

1. The current due to I/O utilization is not taken into account in these values.
2. Values not tested in production. Design guidelines only.

Table 40. Total current consumption in halt and active halt modes.

Symbol	Parameter	Conditions	Typ	Max	Unit
$I_{DD(H)}$	Supply current in halt mode	Clocks stopped, Flash in power-down mode	5	35(1)	µA
		Clocks stopped, Flash in power-down mode, T_A = 25 °C	5	25	
$I_{DD(FAH)}$	Supply current in fast active halt mode	Extclock 16 MHz f_{MASTER} = 125 kHz	770	900(1)	
		LSI clock 128 kHz	150	230(1)	
$I_{DD(SAH)}$	Supply current in slow active halt mode	LSI clock 128 kHz	25	42(1)	
		LSI clock 128 kHz, T_A = 25 °C	25	30	
$t_{WU(FAH)}$	Wakeup time from fast active halt mode	T_A = -40 °C to 150 °C	10	30(1)	µs
$t_{WU(SAH)}$	Wakeup time from slow active halt mode		50	80(1)	

1. Data based on characterization results. Not tested in production.

Current consumption for on-chip peripherals

Table 41. Oscillator current consumption

Symbol	Parameter	Conditions		Typ	Max(1)	Unit
$I_{DD(OSC)}$	HSE oscillator current consumption(2)	Quartz or ceramic resonator, CL = 33 pF V_{DD} = 5 V	f_{OSC} = 24 MHz	1	2.0(3)	mA
			f_{OSC} = 16 MHz	0.6	-	
			f_{OSC} = 8 MHz	0.57	-	
$I_{DD(OSC)}$	HSE oscillator current consumption(2)	Quartz or ceramic resonator, CL = 33 pF V_{DD} = 3.3 V	f_{OSC} = 24 MHz	0.5	1.0(3)	
			f_{OSC} = 16 MHz	0.25	-	
			f_{OSC} = 8 MHz	0.18	-	

1. During startup, the oscillator current consumption may reach 6 mA.
2. The supply current of the oscillator can be further optimized by selecting a high quality resonator with small R_m value. Refer to crystal manufacturer for more details
3. Informative data.

Table 42. Programming current consumption

Symbol	Parameter	Conditions	Typ	Max	Unit
$I_{DD(PROG)}$	Programming current	V_{DD} = 5 V, -40 °C to 150 °C, erasing and programming data or program memory	1.0	1.7	mA

Table 43. Typical peripheral current consumption V_{DD} = 5.0 V(1)

Symbol	Parameter	Typ. f_{master} = 2 MHz	Typ. f_{master} = 16 MHz	Unit
$I_{DD(TIM1)}$	TIM1 supply current(2)	0.03	0.23	mA
$I_{DD(TIM2)}$	TIM2 supply current (2)	0.02	0.12	
$I_{DD(TIM3)}$	TIM3 supply current(2)	0.01	0.1	
$I_{DD(TIM4)}$	TIM4 supply current(2)	0.004	0.03	
$I_{DD(USART)}$	USART supply current(2)	0.03	0.09	
$I_{DD(LINUART)}$	LINUART supply current(2)	0.03	0.11	
$I_{DD(SPI)}$	SPI supply current(2)	0.01	0.04	
$I_{DD(I^2C)}$	I^2C supply current(2)	0.02	0.06	
$I_{DD(AWU)}$	AWU supply current(2)	0.003	0.02	
$I_{DD(TOT\_DIG)}$	All digital peripherals on	0.22	1	
$I_{DD(ADC)}$	ADC supply current when converting(3)	0.93	0.95	

1. Typical values not tested in production. Since the peripherals are powered by an internally regulated, constant digital supply voltage, the values are similar in the full supply voltage range.
2. Data based on a differential I_{DD} measurement between no peripheral clocked and a single active peripheral. This measurement does not include the pad toggling consumption.
3. Data based on a differential I_{DD} measurement between reset configuration and continuous A/D conversions.

Current consumption curves

Figure 10 to *Figure 15* show typical current consumption measured with code executing in RAM.

Figure 10. Typ. $I_{DD(RUN)HSE}$ vs. V_{DD} @f_{CPU} = 16 MHz, peripheral = on

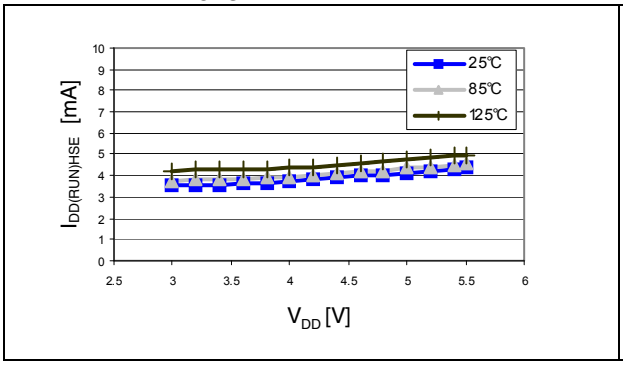


Figure 11. Typ. $I_{DD(RUN)HSE}$ vs. f_{CPU} @ V_{DD} = 5.0 V, peripheral = on

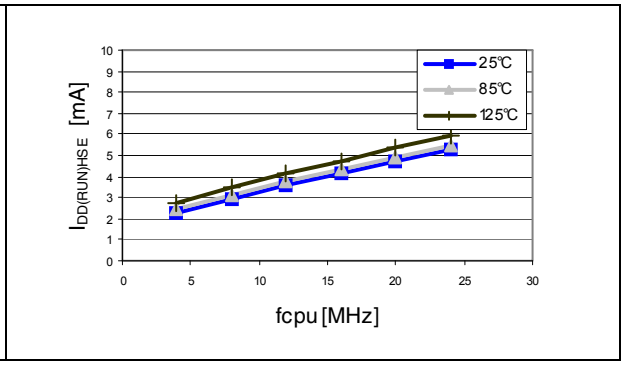


Figure 12. Typ. $I_{DD(RUN)HSI}$ vs. V_{DD} @ f_{CPU} = 16 MHz, peripheral = off

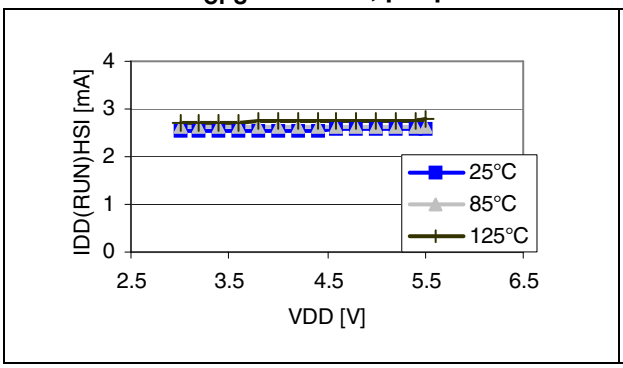


Figure 13. Typ. $I_{DD(WFI)HSE}$ vs. V_{DD} @ f_{CPU} = 16 MHz, peripheral = on

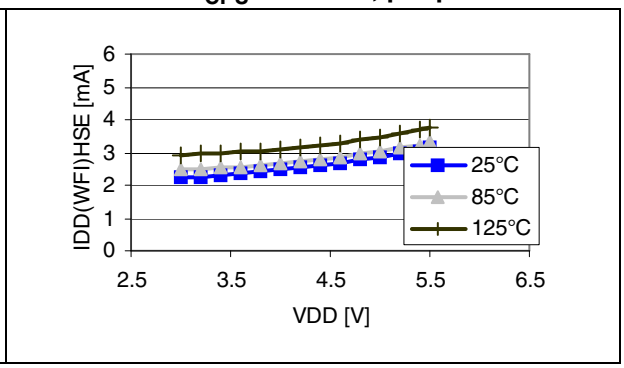


Figure 14. Typ. $I_{DD(WFI)HSE}$ vs. f_{CPU} @ V_{DD} = 5.0 V, peripheral = on

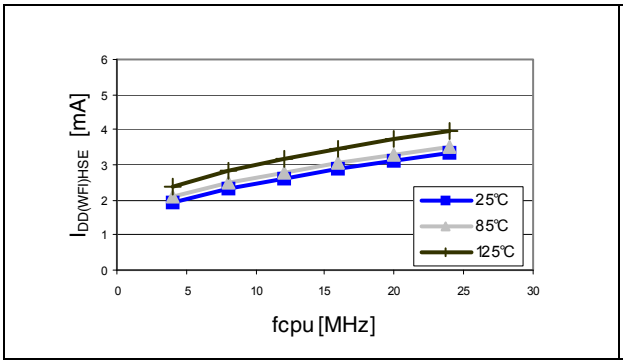
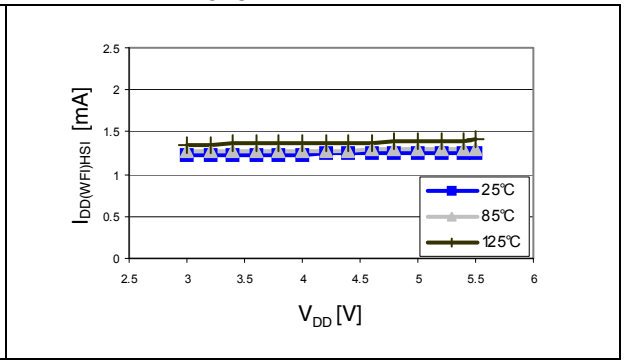


Figure 15. Typ. $I_{DD(WFI)HSI}$ vs. V_{DD} @ f_{CPU} = 16 MHz, peripheral = off



10.3.3 External clock sources and timing characteristics

HSE user external clock

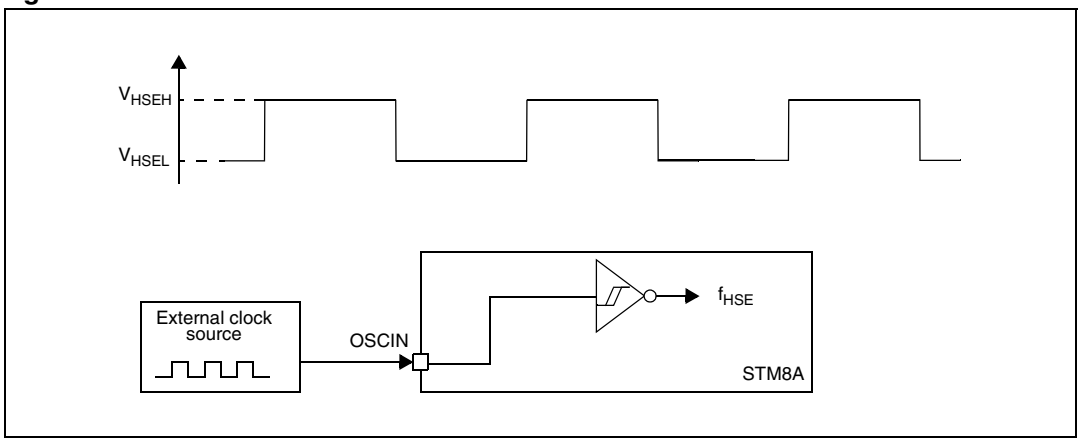
Subject to general operating conditions for V_{DD} and T_A.

Table 44. HSE user external clock characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSE_ext}	User external clock source frequency	T_A is -40 to 150 °C	0(1)	-	16	MHz
V_{HSEdHL}	Comparator hysteresis	-	0.1 x V_{DD}	-	-	V
V_{HSEH}	OSCIN input pin high level voltage	-	0.7 x V_{DD}	-	V_{DD}	
V_{HSEL}	OSCIN input pin low level voltage	-	V_{SS}	-	0.3 x V_{DD}	
I_{LEAK_HSE}	OSCIN input leakage current	$V_{SS} < V_{IN} < V_{DD}$	-1	-	+1	µA

1. In CSS is used, the external clock must have a frequency above 500 kHz.

Figure 16. HSE external clock source



HSE crystal/ceramic resonator oscillator

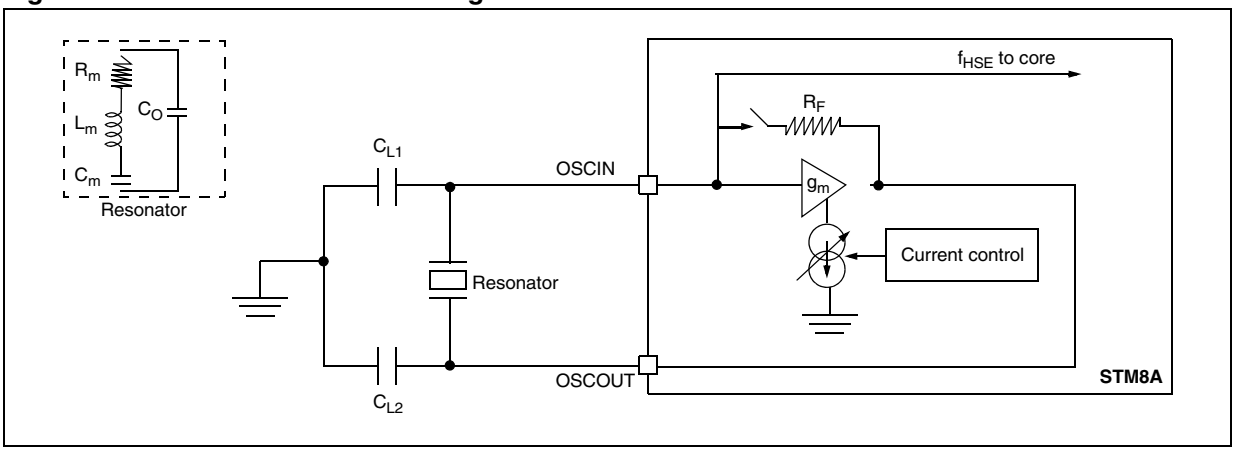
The HSE clock can be supplied using a crystal/ceramic resonator oscillator of up to 16 MHz. All the information given in this paragraph is based on characterization results with specified typical external components. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details (frequency, package, accuracy...).

Table 45. HSE oscillator characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
R_F	Feedback resistor	-	-	220	-	kΩ
C_{L1}/C_{L2} (1)	Recommended load capacitance	-	-	-	20	pF
g_m	Oscillator transconductance	-	5	-	-	mA/V
$t_{SU(HSE)}$ (2)	Startup time	V_{DD} is stabilized	-	2.8	-	ms

1. The oscillator needs two load capacitors, C_{L1} and C_{L2}, to act as load for the crystal. The total load capacitance (C_{load}) is $(C_{L1} * C_{L2})/(C_{L1} + C_{L2})$. If $C_{L1} = C_{L2}$, $C_{load} = C_{L1} / 2$. Some oscillators have built-in load capacitors, C_{L1} and C_{L2}.
2. This value is the startup time, measured from the moment it is enabled (by software) until a stabilized 16 MHz oscillation is reached. It can vary with the crystal type that is used.

Figure 17. HSE oscillator circuit diagram



HSE oscillator critical g_m formula

The crystal characteristics have to be checked with the following formula:

$$g_m \gg g_{mcrit}$$

where g_{mcrit} can be calculated with the crystal parameters as follows:

$$g_{mcrit} = (2 \times \Pi \times {}^{f}HSE)^2 \times R_m(2Co + C)^2$$

R_m: Notional resistance (see crystal specification)
L_m: Notional inductance (see crystal specification)
C_m: Notional capacitance (see crystal specification)
Co: Shunt capacitance (see crystal specification)
$C_{L1} = C_{L2} = C$: Grounded external capacitance

10.3.4 Internal clock sources and timing characteristics

Subject to general operating conditions for V_{DD} and T_A.

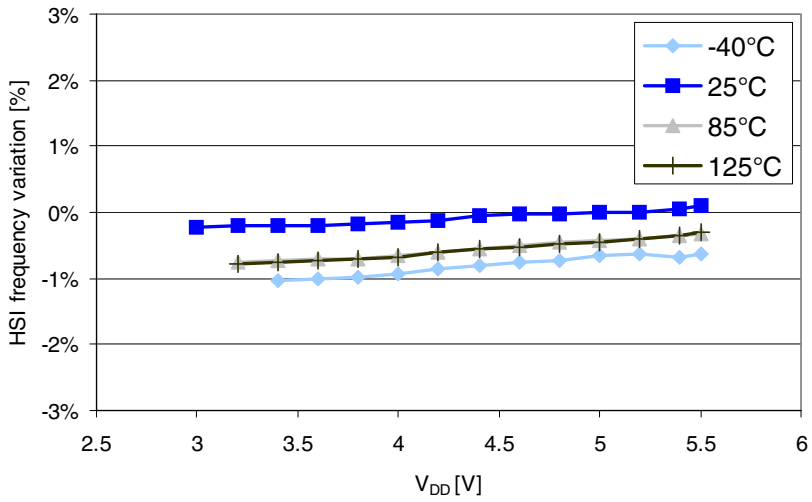
High speed internal RC oscillator (HSI)

Table 46. HSI oscillator characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSI}	Frequency		-	16	-	MHz
ACC_{HS}	HSI oscillator user trimming accuracy	Trimmed by the application for any V_{DD} and T_A conditions	-1(1)	-	1(1)	%
			-0.5(1)	-	0.5(1)	
	HSI oscillator accuracy (factory calibrated)	V_{DD} = 3.0 V ≤ V_{DD} ≤ 5.5 V, -40 °C ≤ T_A ≤ 150 °C	-5	-	5	
$t_{su(HSI)}$	HSI oscillator wakeup time		-	-	2(2)	µs

1. Depending on option byte setting (OPT3 and NOPT3)
2. Guaranteed by characterization, not tested in production

Figure 18. Typical HSI frequency vs V_{DD}



Low speed internal RC oscillator (LSI)

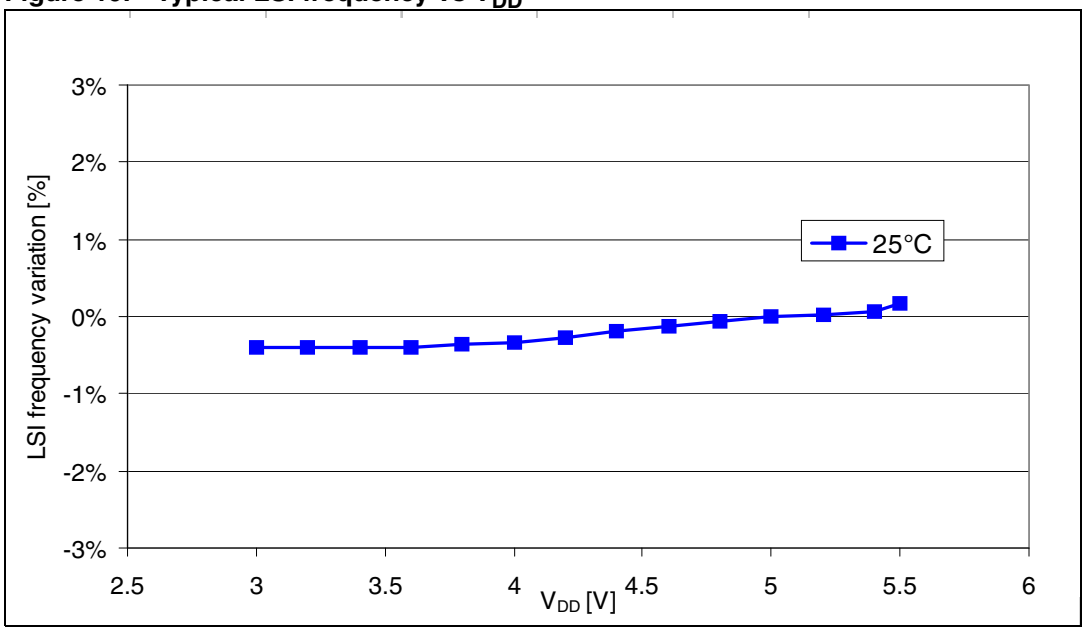
Subject to general operating conditions for V_{DD} and T_A.

Table 47. LSI oscillator characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LSI}	Frequency	-	112	128	144	kHz
$t_{su(LSI)}$	LSI oscillator wakeup time	-	-	-	7(1)	µs

1. Data based on characterization results, not tested in production.

Figure 19. Typical LSI frequency vs V_{DD}



10.3.5 Memory characteristics

Flash program memory/data EEPROM memory

General conditions: T_A = -40 to 125 °C.

Table 48. Flash program memory/data EEPROM memory

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DD}	Operating voltage (all modes, execution/write/erase)	f_{CPU} is 0 to 16 MHz with 0 ws	3.0	-	5.5	V
V_{DD}	Operating voltage (code execution)	f_{CPU} is 0 to 16 MHz with 0 ws	2.6	-	5.5	
t_{prog}	Standard programming time (including erase) for byte/word/block (1 byte/4 bytes/128 bytes)	-	-	6	6.6	ms
	Fast programming time for 1 block (128 bytes)	-	-	3	3.3	
t_{erase}	Erase time for 1 block (128 bytes)	-	-	3	3.3	ms

Table 49. Program memory

Symbol	Parameter	Condition	Min	Max	Unit
T_{WE}	Temperature for writing and erasing	-	-40	125	°C
N_{WE}	Program memory endurance (erase/write cycles)(1)	T_A = 25 °C	1000	-	cycles
t_{RET}	Data retention time	T_A = 25 °C	40	-	years
		T_A = 55 °C	20	-	

1. The physical granularity of the memory is four bytes, so cycling is performed on four bytes even when a write/erase operation addresses a single byte.

Table 50. Data memory

Symbol	Parameter	Condition	Min	Max	Unit
T_{WE}	Temperature for writing and erasing		-40	125	°C
				150	
N_{WE}	Data memory endurance(1) (erase/write cycles)	T_A = 25 °C	300 k	-	cycles
		T_A = -40°C to 125 °C	100 k(2)	-	
t_{RET}	Data retention time	T_A = 25 °C	40(2)(3)	-	years
		T_A = 55 °C	20(2)(3)	-	

1. The physical granularity of the memory is four bytes, so cycling is performed on four bytes even when a write/erase operation addresses a single byte.
2. More information on the relationship between data retention time and number of write/erase cycles is available in a separate technical document.
3. Retention time for 256B of data memory after up to 1000 cycles at 125 °C.

10.3.6 I/O port pin characteristics

General characteristics

Subject to general operating conditions for V_{DD} and T_A unless otherwise specified. All unused pins must be kept at a fixed voltage, using the output mode of the I/O for example or an external pull-up or pull-down resistor.

Table 51. I/O static characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IL}	Input low level voltage		-0.3 V		0.3 x V_{DD}	—
V_{IH}	Input high level voltage		0.7 x V_{DD}		V_{DD} + 0.3 V	
V_{hys}	Hysteresis(1)		-	0.1 x V_{DD}	-	
V_{OH}	Output high level voltage	Standard I/0, V_{DD} = 5 V, I = 3 mA	V_{DD} - 0.5 V	-	-	
		Standard I/0, V_{DD} = 3 V, I = 1.5 mA	V_{DD} - 0.4 V	-	-	
V_{OL}	Output low level voltage	High sink and true open drain I/0, V_{DD} = 5 V I = 8 mA	-	-	0.5	V
		Standard I/0, V_{DD} = 5 V I = 3 mA	-	-	0.6	
		Standard I/0, V_{DD} = 3 V I = 1.5 mA	-	-	0.4	
R_{pu}	Pull-up resistor	V_{DD} = 5 V, V_{IN} = V_{SS}	35	50	65	kΩ
t_R, t_F	Rise and fall time (10% - 90%)	Fast I/Os Load = 50 pF	-	-	20(2)	ns
		Standard and high sink I/Os Load = 50 pF	-	-	125(2)	
I_{lkg}	Digital input pad leakage current	$V_{SS} \leq V_{IN} \leq V_{DD}$	-	-	±1	µA
$I_{lkg\ ana}$	Analog input pad leakage current	$V_{SS} \leq V_{IN} \leq V_{DD}$ -40 °C < T_A < 125 °C	-	-	±250	nA
$I_{lkg\ ana}$	Analog input pad leakage current	$V_{SS} \leq V_{IN} \leq V_{DD}$ -40 °C < T_A < 150 °C	-	-	TBD	
$I_{lkg(inj)}$	Leakage current in adjacent I/O(2)	Injection current ±4 mA	-	-	±1(2)	µA
I_{DDIO}	Total current on either V_{DDIO} or V_{SSIO}	Including injection currents	-	-	60	mA

1. Hysteresis voltage between Schmitt trigger switching levels. Based on characterization results, not tested in production.
2. Data based on characterization results, not tested in production.

Figure 20. Typical V_{IL} and V_{IH} vs V_{DD} @ four temperatures

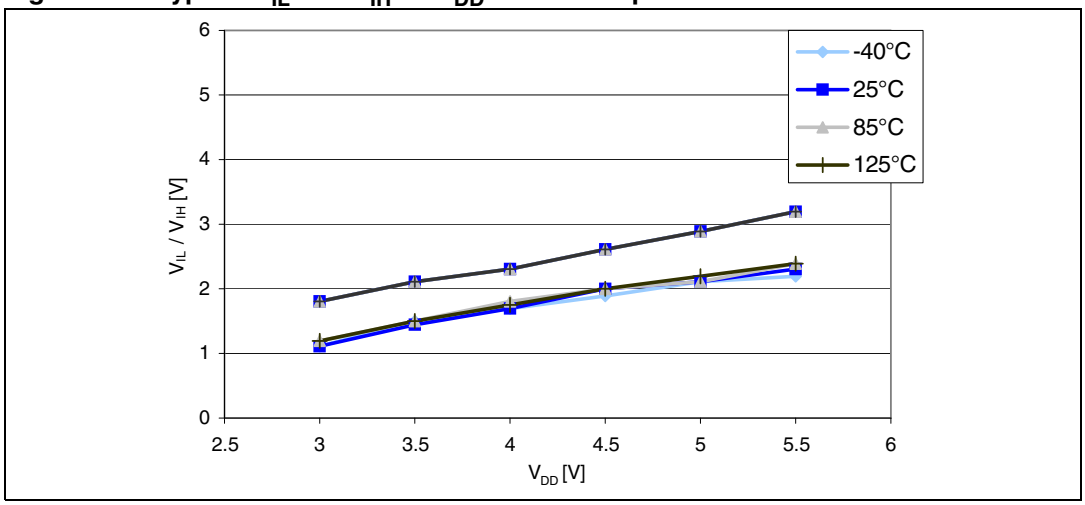


Figure 21. Typical pull-up resistance R_{PU} vs V_{DD} @ four temperatures

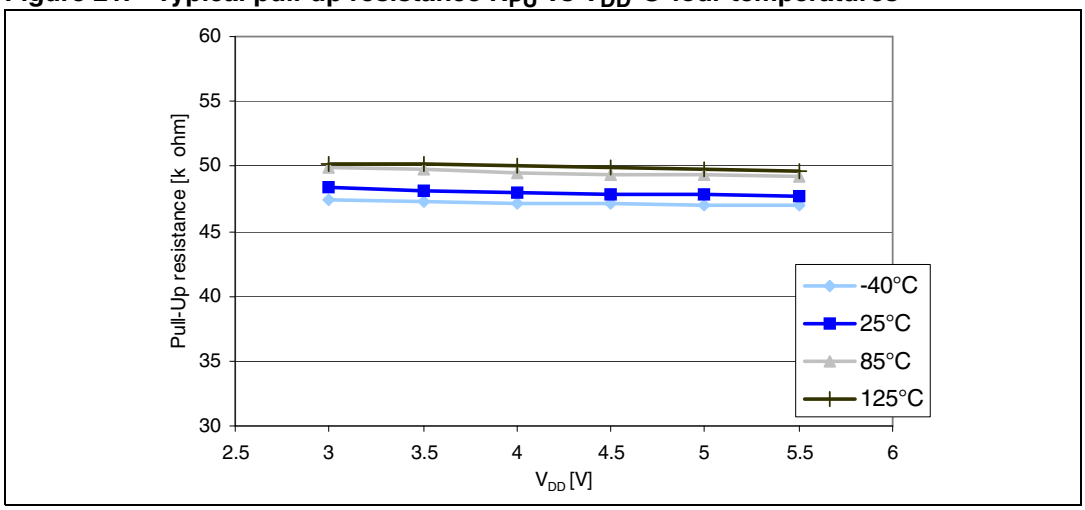
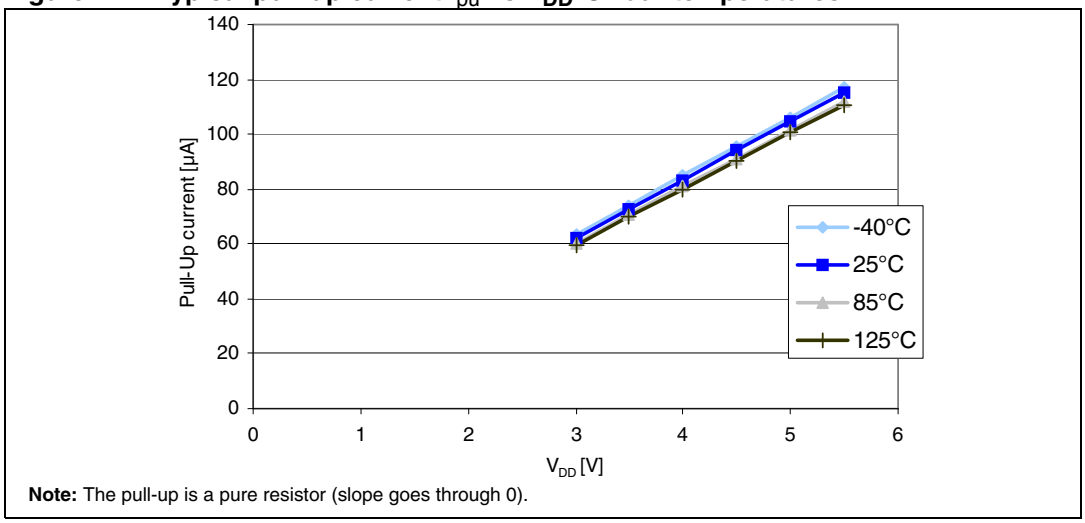


Figure 22. Typical pull-up current I_{pu} vs V_{DD} @ four temperatures



Note: The pull-up is a pure resistor (slope goes through 0).

Typical output level curves

Figure 23 to *Figure 32* show typical output level curves measured with output on a single pin.

Figure 23. Typ. V_{OL} @ V_{DD} = 3.3 V (standard ports)

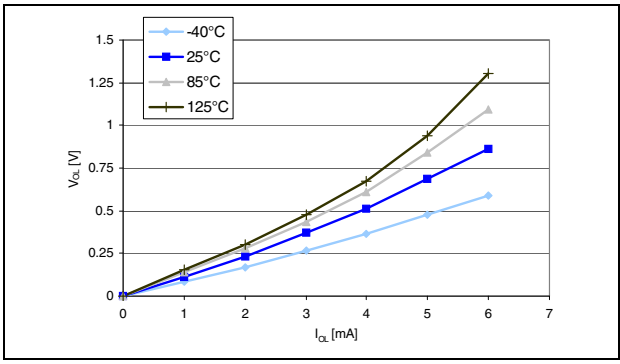


Figure 24. Typ. V_{OL} @ V_{DD} = 5.0 V (standard ports)

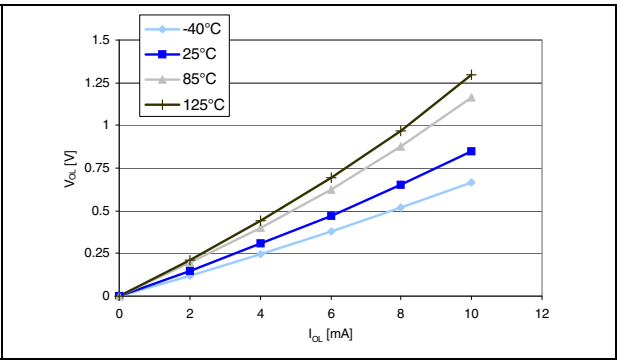


Figure 25. Typ. V_{OL} @ V_{DD} = 3.3 V (true open drain ports)

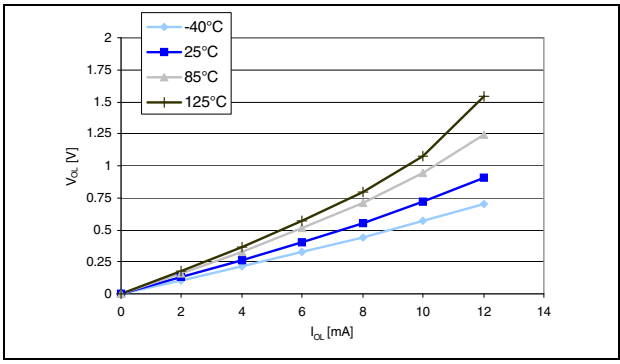


Figure 26. Typ. V_{OL} @ V_{DD} = 5.0 V (true open drain ports)

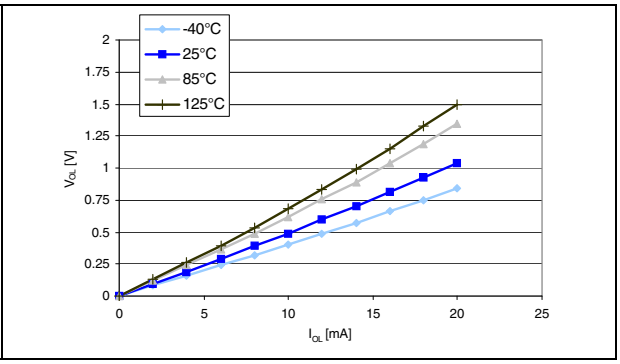


Figure 27. Typ. V_{OL} @ V_{DD} = 3.3 V (high sink ports)

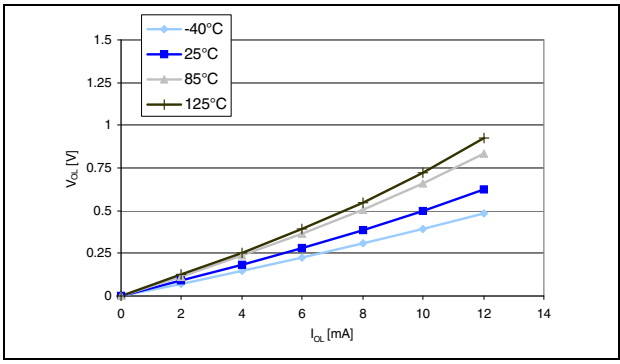


Figure 28. Typ. V_{OL} @ V_{DD} = 5.0 V (high sink ports)

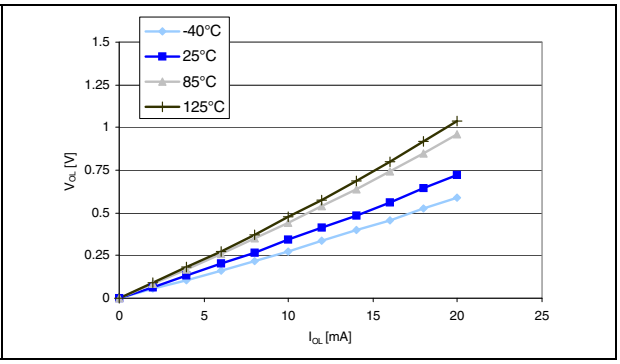


Figure 29. Typ. V_{DD} - V_{OH} @ V_{DD} = 3.3 V (standard ports)

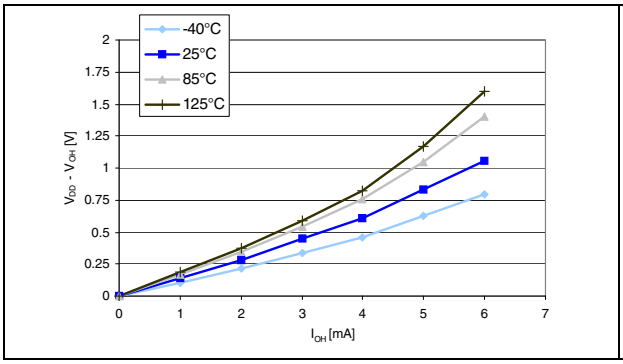


Figure 30. Typ. V_{DD} - V_{OH} @ V_{DD} = 5.0 V (standard ports)

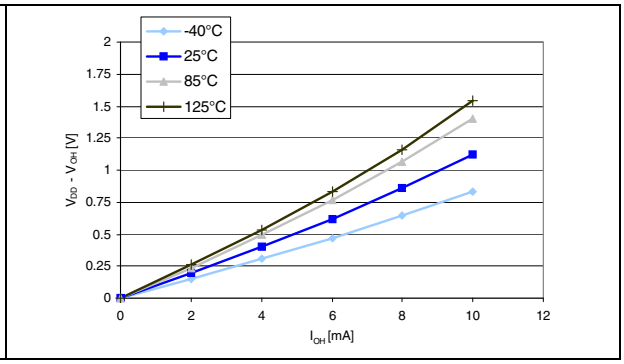


Figure 31. Typ. V_{DD} - V_{OH} @ V_{DD} = 3.3 V (high sink ports)

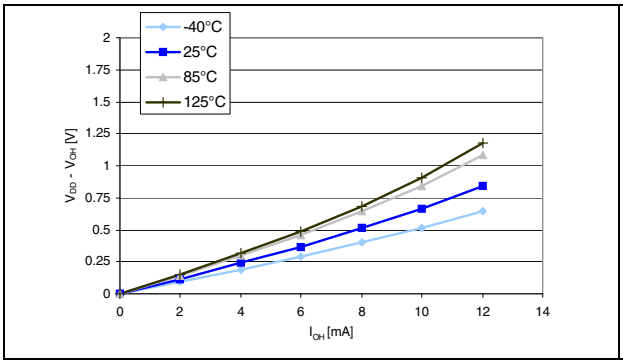
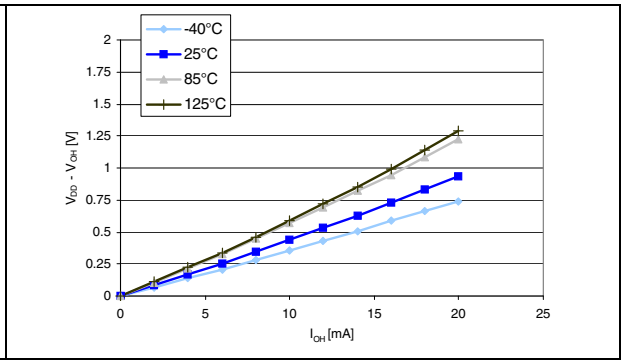


Figure 32. Typ. V_{DD} - V_{OH} @ V_{DD} = 5.0 V (high sink ports)



10.3.7 Reset pin characteristics

Subject to general operating conditions for V_{DD} and T_A unless otherwise specified.

Table 52. NRST pin characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{IL(NRST)}$	NRST input low level voltage(1)	-	V_{SS}	-	0.3 x V_{DD}	
$V_{IH(NRST)}$	NRST input high level voltage(1)	-	0.7 x V_{DD}	-	V_{DD}	
$V_{OL(NRST)}$	NRST output low level voltage(1)	I_{OL}= 3 mA	-	-	0.6	V
$R_{PU(NRST)}$	NRST pull-up resistor	-	30	40	60	kΩ
$V_{F(NRST)}$	NRST input filtered pulse(1)	-	85	-	315	ns

1. Data based on characterization results, not tested in production.

Figure 33. Typical NRST V_{IL} and V_{IH} vs V_{DD} @ four temperatures

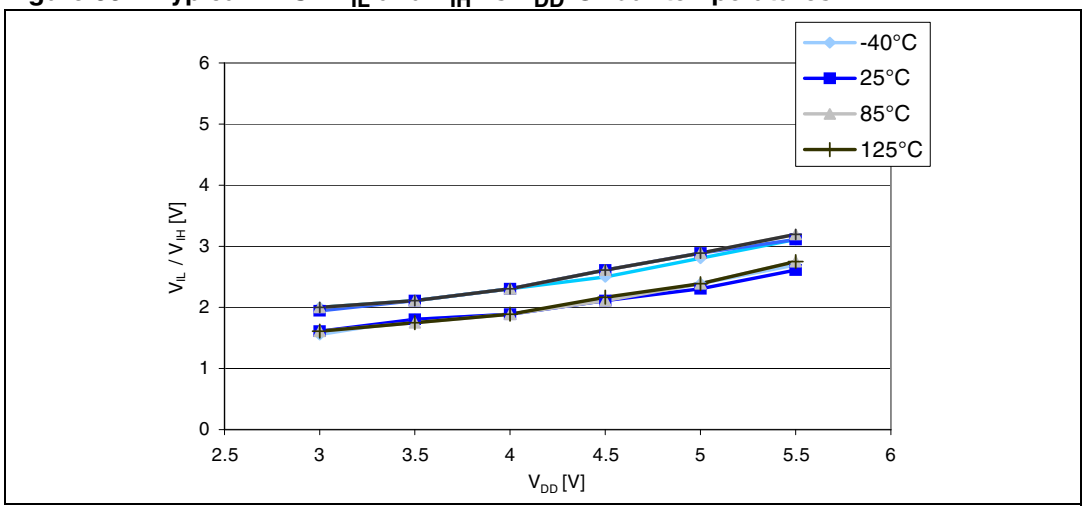


Figure 34. Typical NRST pull-up resistance R_{PU} vs V_{DD}

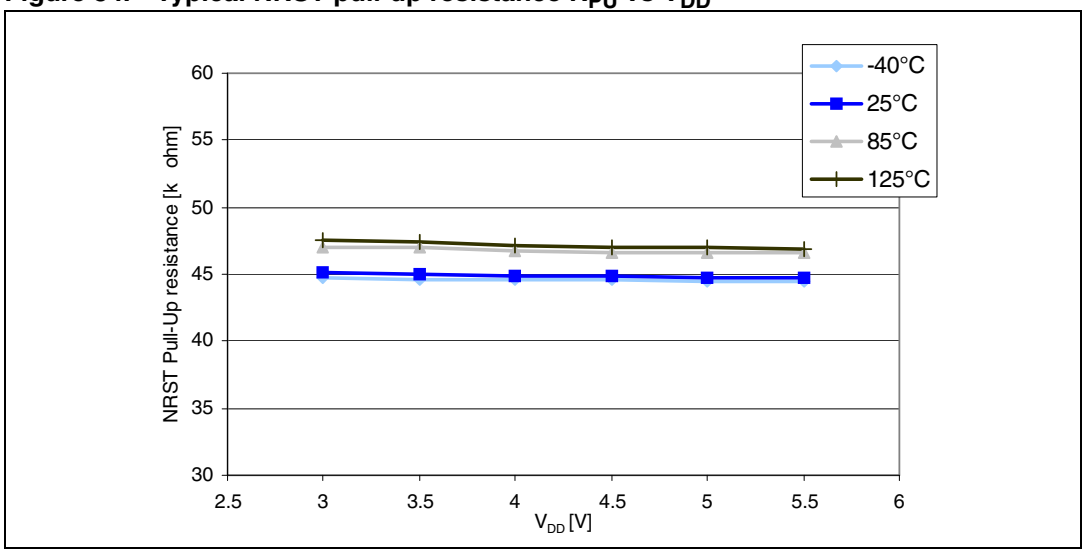
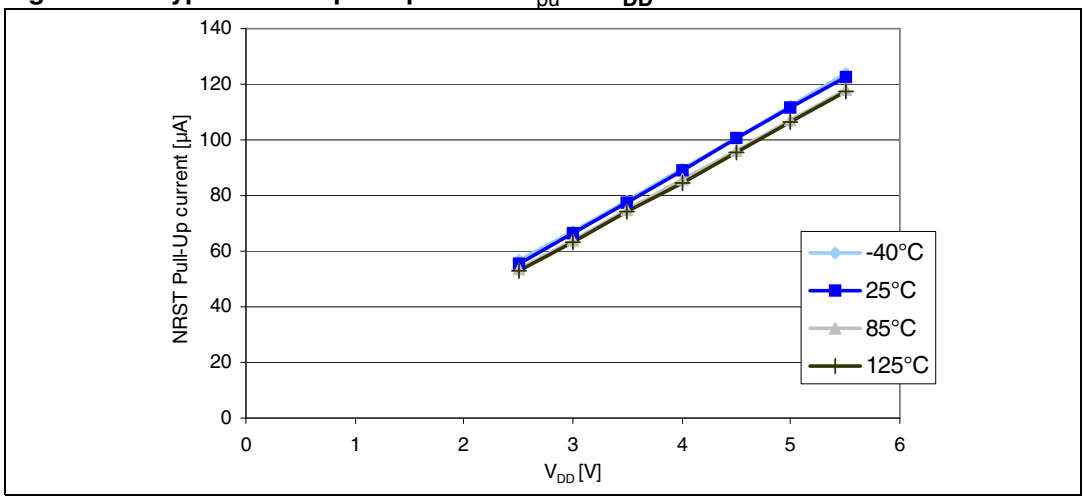
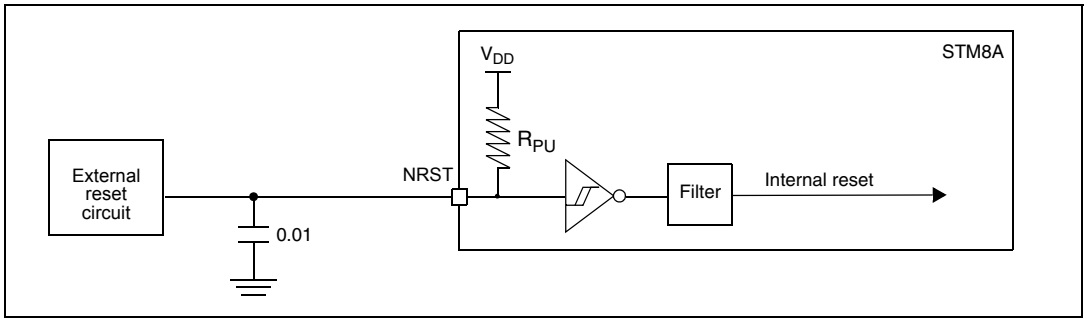


Figure 35. Typical NRST pull-up current I_{pu} vs V_{DD}



The reset network shown in *Figure 36* protects the device against parasitic resets.

Figure 36. Recommended reset pin protection



10.3.8 TIM 1, 2, 3, and 4 timer specifications

Subject to general operating conditions for V_{DD}, f_{MASTER}, and T_A unless otherwise specified.

Table 53. TIM 1, 2, 3, and 4 electrical specifications

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{EXT}	Timer external clock frequency(1)	-	-	-	16	MHz

1. Not tested in production. On 64 Kbyte devices, the frequency is limited to 16 MHz.

10.3.9 SPI serial peripheral interface

Unless otherwise specified, the parameters given in *Table 54* are derived from tests performed under ambient temperature, f_{MASTER} frequency and V_{DD} supply voltage conditions. $t_{MASTER} = 1/f_{MASTER}$.

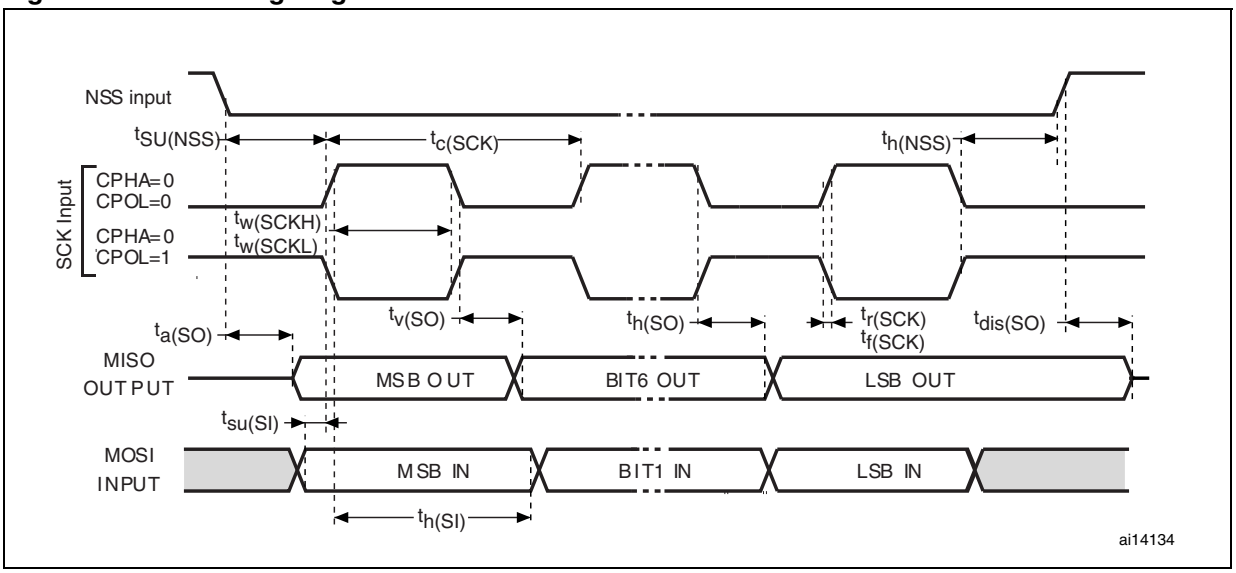
Refer to I/O port characteristics for more details on the input/output alternate function characteristics (NSS, SCK, MOSI, MISO).

Table 54. SPI characteristics

Symbol	Parameter	Conditions		Min	Max	Unit
f_{SCK} $1/t_{c(SCK)}$	SPI clock frequency	Master mode		0	10	MHz
		Slave mode	V_{DD} < 4.5 V	0	6(1)	
			V_{DD} = 4.5 V to 5.5 V	0	8(1)	
$t_{r(SCK)}$ $t_{f(SCK)}$	SPI clock rise and fall time	Capacitive load: C = 30 pF		-	25(2)	ns
$t_{su(NSS)}$(3)	NSS setup time	Slave mode		4 * t_{MASTER}	-	
$t_{h(NSS)}$(3)	NSS hold time	Slave mode		70	-	
$t_{w(SCKH)}$(3) $t_{w(SCKL)}$(3)	SCK high and low time	Master mode, f_{MASTER} = 8 MHz, f_{SCK}= 4 MHz		110	140	
$t_{su(MI)}$(3) $t_{su(SI)}$(3)	Data input setup time	Master mode		5	-	
		Slave mode		5	-	
$t_{h(MI)}$(3) $t_{h(SI)}$(3)	Data input hold time	Master mode		7	-	
		Slave mode		10	-	
$t_{a(SO)}$(3)(4)	Data output access time	Slave mode		-	3* t_{MASTER}	
$t_{dis(SO)}$(3)(5)	Data output disable time	Slave mode		25		
$t_{v(SO)}$(3)	Data output valid time	Slave mode (after enable edge)	V_{DD} < 4.5 V	-	75	
			V_{DD} = 4.5 V to 5.5 V	-	53	
$t_{v(MO)}$(3)	Data output valid time	Master mode (after enable edge)		-	30	
$t_{h(SO)}$(3)	Data output hold time	Slave mode (after enable edge)		31	-	
$t_{h(MO)}$(3)		Master mode (after enable edge)		12	-	

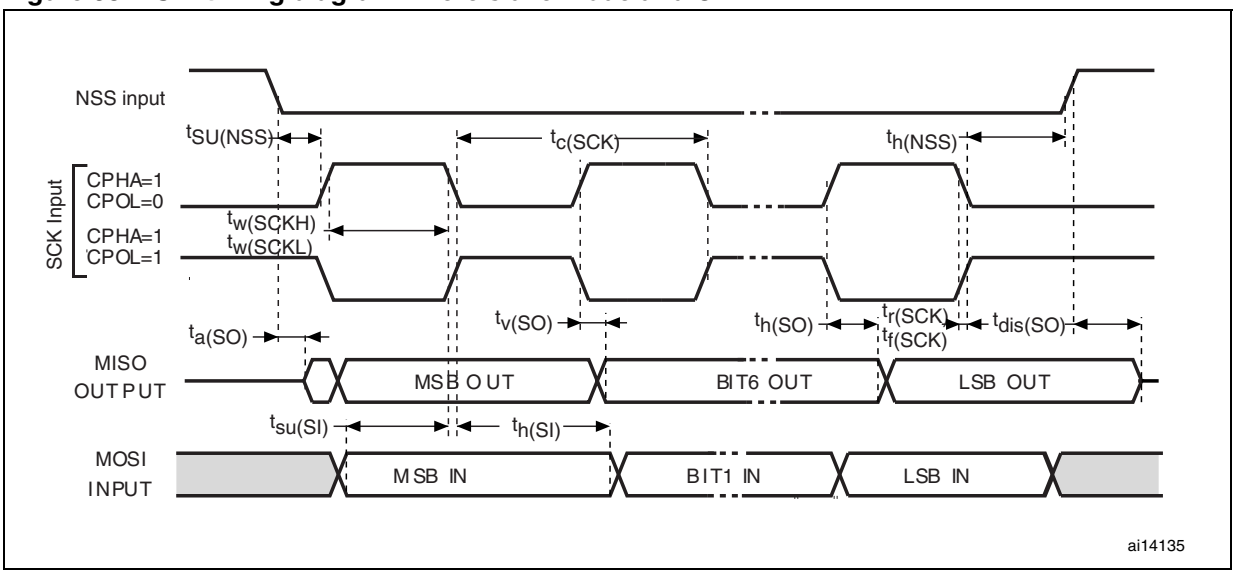
1. f_{MAX} is $f_{MASTER}/2$.
2. The pad has to be configured accordingly (fast mode).
3. Values based on design simulation and/or characterization results, and not tested in production.
4. Min time is for the minimum time to drive the output and the max time is for the maximum time to validate the data.
5. Min time is for the minimum time to invalidate the output and the max time is for the maximum time to put the data in Hi-Z.

Figure 37. SPI timing diagram where slave mode and CPHA = 0



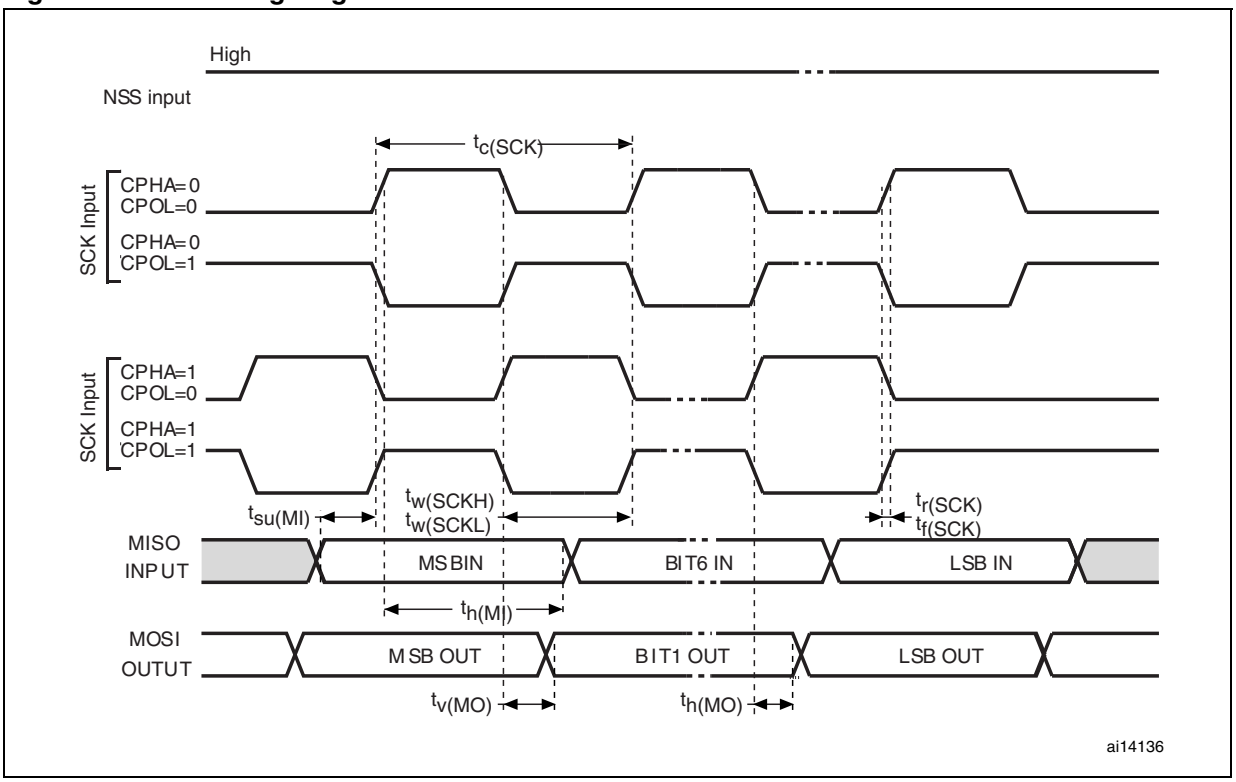
1. Measurement points are at CMOS levels: 0.3 V_{DD} and 0.7 V_{DD}.

Figure 38. SPI timing diagram where slave mode and CPHA = 1



1. Measurement points are at CMOS levels: 0.3 V_{DD} and 0.7 V_{DD}.

Figure 39. SPI timing diagram - master mode



1. Measurement points are at CMOS levels: 0.3 V_{DD} and 0.7 V_{DD}.

10.3.10 I²C interface characteristics

Table 55. I²C characteristics

Symbol	Parameter	Standard mode I²C		Fast mode I²C(1)		Unit
		Min(2)	Max(2)	Min(2)	Max(2)	
$t_{w(SCLL)}$	SCL clock low time	4.7	-	1.3	-	µs
$t_{w(SCLH)}$	SCL clock high time	4.0	-	0.6	-	
$t_{su(SDA)}$	SDA setup time	250	-	100	-	ns
$t_{h(SDA)}$	SDA data hold time	0(3)	-	0(4)	900(3)	
$t_{r(SDA)}$ $t_{r(SCL)}$	SDA and SCL rise time (V_{DD} = 3 to 5.5 V)	-	1000	-	300	
$t_{f(SDA)}$ $t_{f(SCL)}$	SDA and SCL fall time (V_{DD} = 3 to 5.5 V)	-	300	-	300	
$t_{h(STA)}$	START condition hold time	4.0	-	0.6	-	µs
$t_{su(STA)}$	Repeated START condition setup time	4.7	-	0.6	-	
$t_{su(STO)}$	STOP condition setup time	4.0	-	0.6	-	µs
$t_{w(STO:STA)}$	STOP to START condition time (bus free)	4.7	-	1.3	-	µs
C_b	Capacitive load for each bus line	-	400	-	400	pF

1. f_{MASTER}, must be at least 8 MHz to achieve max fast I²C speed (400 kHz)
2. Data based on standard I²C protocol requirement, not tested in production
3. The maximum hold time of the start condition has only to be met if the interface does not stretch the low time
4. The device must internally provide a hold time of at least 300 ns for the SDA signal in order to bridge the undefined region of the falling edge of SCL

10.3.11 10-bit ADC characteristics

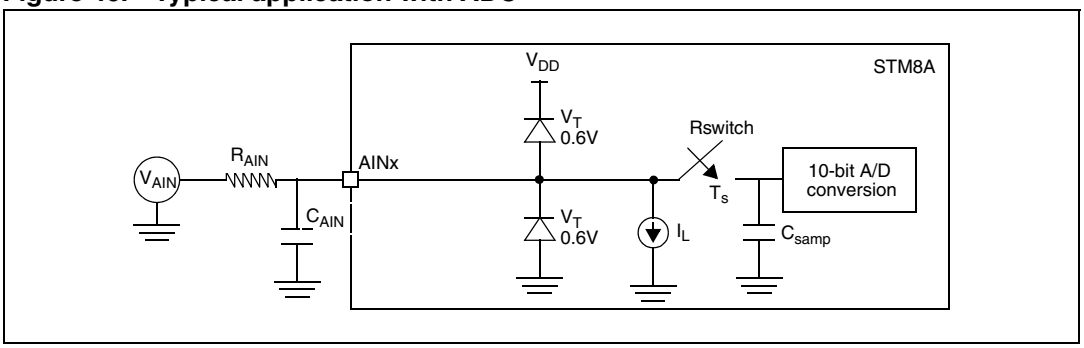
Subject to general operating conditions for V_{DDA}, f_{MASTER}, and T_A unless otherwise specified.

Table 56. ADC characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{ADC}	ADC clock frequency	-	111 kHz	-	4 MHz	kHz/MHz
V_{DDA}	Analog supply	-	3	-	5.5	V
V_{REF+}	Positive reference voltage	-	2.75	-	V_{DDA}	
V_{REF-}	Negative reference voltage	-	V_{SSA}	-	0.5	
V_{AIN}	Conversion voltage range(1)	-	V_{SSA}	-	V_{DDA}	
		Devices with external V_{REF+}/ V_{REF-} pins	V_{REF-}	-	V_{REF+}	
C_{samp}	Internal sample and hold capacitor	-	-	-	3	pF
t_S(1)	Sampling time (3 x 1/f_{ADC})	f_{ADC} = 2 MHz	-	1.5	-	µs
		f_{ADC} = 4 MHz	-	0.75	-	
t_{STAB}	Wakeup time from standby	f_{ADC} = 2 MHz	-	7	-	
		f_{ADC} = 4 MHz	-	3.5	-	
t_{CONV}	Total conversion time including sampling time (14 x 1/f_{ADC})	f_{ADC} = 2 MHz	-	7	-	
		f_{ADC} = 4 MHz	-	3.5	-	
R_{switch}	Equivalent switch resistance	-	-	-	30	kΩ

1. During the sample time, the sampling capacitance, C_{samp} (3 pF typ), can be charged/discharged by the external source. The internal resistance of the analog source must allow the capacitance to reach its final voltage level within t_S. After the end of the sample time t_S, changes of the analog input voltage have no effect on the conversion result.

Figure 40. Typical application with ADC



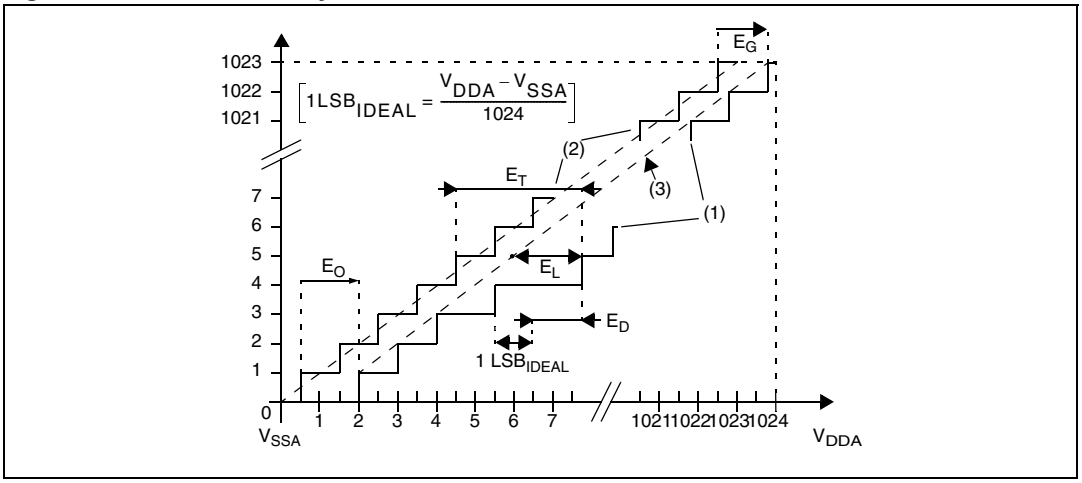
1. Legend: R_{AIN} = external resistance, C_{AIN} = capacitors, C_{samp} = internal sample and hold capacitor.

Table 57. ADC accuracy for V_{DDA} = 5 V

Symbol	Parameter	Conditions	Typ	Max(1)	Unit
$\|E_T\|$	Total unadjusted error(2)	f_{ADC} = 2 MHz	1.4	3(3)	LSB
$\|E_O\|$	Offset error(2)		0.8	3	
$\|E_G\|$	Gain error(2)		0.1	2	
$\|E_D\|$	Differential linearity error(2)		0.9	1	
$\|E_L\|$	Integral linearity error(2)		0.7	1.5	
$\|E_T\|$	Total unadjusted error(2)	f_{ADC} = 4 MHz	1.9(4)	4(4)	
$\|E_O\|$	Offset error(2)		1.3(4)	4(4)	
$\|E_G\|$	Gain error(2)		0.6(4)	3(4)	
$\|E_D\|$	Differential linearity error(2)		1.5(4)	2(4)	
$\|E_L\|$	Integral linearity error(2)		1.2(4)	1.5(4)	

1. Max value is based on characterization, not tested in production.
2. ADC accuracy vs. injection current: Any positive or negative injection current within the limits specified for $I_{INJ(PIN)}$ and $\Sigma I_{INJ(PIN)}$ in *Section 10.3.6* does not affect the ADC accuracy.
3. TUE 2LSB can be reached on specific salestypes in the whole temperature range.
4. Target values.

Figure 41. ADC accuracy characteristics



1. Example of an actual transfer curve
2. The ideal transfer curve
3. End point correlation line
   E_T = Total unadjusted error: Maximum deviation between the actual and the ideal transfer curves.
   E_O = Offset error: Deviation between the first actual transition and the first ideal one.
   E_G = Gain error: Deviation between the last ideal transition and the last actual one.
   E_D = Differential linearity error: Maximum deviation between actual steps and the ideal one.
   E_L = Integral linearity error: Maximum deviation between any actual transition and the end point correlation line.

10.3.12 EMC characteristics

Susceptibility tests are performed on a sample basis during product characterization.

Functional EMS (electromagnetic susceptibility)

While executing a simple application (toggling 2 LEDs through I/O ports), the product is stressed by two electromagnetic events until a failure occurs (indicated by the LEDs).

- **ESD**: Electrostatic discharge (positive and negative) is applied on all pins of the device until a functional disturbance occurs. This test conforms with the IEC 1000-4-2 standard.
- **FTB**: A burst of fast transient voltage (positive and negative) is applied to V_{DD} and V_{SS} through a 100 pF capacitor, until a functional disturbance occurs. This test conforms with the IEC 1000-4-4 standard.

A device reset allows normal operations to be resumed. The test results are given in the table below based on the EMS levels and classes defined in application note AN1709.

Designing hardened software to avoid noise problems

EMC characterization and optimization are performed at component level with a typical application environment and simplified MCU software. It should be noted that good EMC performance is highly dependent on the user application and the software in particular.

Therefore it is recommended that the user applies EMC software optimization and prequalification tests in relation with the EMC level requested for his application.

Software recommendations

The software flowchart must include the management of runaway conditions such as:

- Corrupted program counter
- Unexpected reset
- Critical data corruption (control registers...)

Prequalification trials

Most of the common failures (unexpected reset and program counter corruption) can be recovered by applying a low state on the NRST pin or the oscillator pins for 1 second.

To complete these trials, ESD stress can be applied directly on the device, over the range of specification values. When unexpected behavior is detected, the software can be hardened to prevent unrecoverable errors occurring (see application note AN1015).

Table 58. EMS data

Symbol	Parameter	Conditions	Level/class
V_{FESD}	Voltage limits to be applied on any I/O pin to induce a functional disturbance	V_{DD} = 3.3 V, T_A= 25 °C, f_{MASTER} = 16 MHz (HSI clock), Conforms to IEC 1000-4-2	3B
V_{EFTB}	Fast transient voltage burst limits to be applied through 100 pF on V_{DD} and V_{SS} pins to induce a functional disturbance	V_{DD}= 3.3 V, T_A= 25 °C, f_{MASTER} = 16 MHz (HSI clock), Conforms to IEC 1000-4-4	4A

Electromagnetic interference (EMI)

Emission tests conform to the SAE J 1752/3 standard for test software, board layout and pin loading.

Table 59. EMI data

Symbol	Parameter	Conditions				Unit
		General conditions	Monitored frequency band	Max f_{CPU}(1)		
				8 MHz	16 MHz	
S_{EMI}	Peak level	V_{DD} = 5 V, T_A = 25 °C, LQFP80 package conforming to SAE J 1752/3	0.1 MHz to 30 MHz	15	17	dBµV
			30 MHz to 130 MHz	18	22	
			130 MHz to 1 GHz	-1	3	
	SAE EMI level		—	2	2.5	

1. Data based on characterization results, not tested in production.

Absolute maximum ratings (electrical sensitivity)

Based on two different tests (ESD and LU) using specific measurement methods, the product is stressed to determine its performance in terms of electrical sensitivity. For more details, refer to the application note AN1181.

Electrostatic discharge (ESD)

Electrostatic discharges (3 positive then 3 negative pulses separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts*(n+1) supply pin). This test conforms to the JESD22-A114A/A115A standard. For more details, refer to the application note AN1181.

Table 60. ESD absolute maximum ratings

Symbol	Ratings	Conditions	Class	Maximum value(1)	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (Human body model)	T_A = 25°C, conforming to JESD22-A114	3A	4000	V
$V_{ESD(CDM)}$	Electrostatic discharge voltage (Charge device model)	T_A= 25°C, conforming to JESD22-C101	3	500	
$V_{ESD(MM)}$	Electrostatic discharge voltage (Machine model)	T_A= 25°C, conforming to JESD22-A115	B	200	

1. Data based on characterization results, not tested in production

Static latch-up

Two complementary static tests are required on 10 parts to assess the latch-up performance.

- A supply overvoltage (applied to each power supply pin) and
- A current injection (applied to each input, output and configurable I/O pin) are performed on each sample.

This test conforms to the EIA/JESD 78 IC latch-up standard. For more details, refer to the application note AN1181.

Table 61. Electrical sensitivities

Symbol	Parameter	Conditions	Class(1)
LU	Static latch-up class	$T_A = 25$ °C	A
		$T_A = 85$ °C	
		$T_A = 125$ °C	
		$T_A = 150$ °C(2)	

1. Class description: A Class is an STMicroelectronics internal specification. All its limits are higher than the JEDEC specifications, that means when a device belongs to class A it exceeds the JEDEC standard. B class strictly covers all the JEDEC criteria (international standard).
2. Available on STM8AF62xx devices only.

10.4 Thermal characteristics

In case the maximum chip junction temperature (T_{Jmax}) specified in *Table 37: General operating conditions on page 55* is exceeded, the functionality of the device cannot be guaranteed.

T_{Jmax}, in degrees Celsius, may be calculated using the following equation:

$$T_{Jmax} = T_{Amax} + (P_{Dmax} \times \Theta_{JA})$$

Where:

- T_{Amax} is the maximum ambient temperature in °C
- Θ_{JA} is the package junction-to-ambient thermal resistance in ° C/W
- P_{Dmax} is the sum of P_{INTmax} and $P_{I/Omax}$ ($P_{Dmax} = P_{INTmax} + P_{I/Omax}$)
- P_{INTmax} is the product of I_{DD} and V_{DD}, expressed in Watts. This is the maximum chip internal power.
- $P_{I/Omax}$ represents the maximum power dissipation on output pins
  Where:
  $P_{I/Omax} = \Sigma (V_{OL}*I_{OL}) + \Sigma((V_{DD}-V_{OH})*I_{OH})$,
  taking into account the actual V_{OL}/I_{OL} and V_{OH}/I_{OH} of the I/Os at low and high level in the application.

Table 62. Thermal characteristics(1)

Symbol	Parameter	Value	Unit
Θ_{JA}	Thermal resistance junction-ambient LQFP 48 - 7 x 7 mm	57	°C/W
Θ_{JA}	Thermal resistance junction-ambient LQFP 32 - 7 x 7 mm	59	°C/W
Θ_{JA}	Thermal resistance junction-ambient VFQFPN32	25	°C/W

1. Thermal resistances are based on JEDEC JESD51-2 with 4-layer PCB in a natural convection environment.

10.4.1 Reference document

JESD51-2 integrated circuits thermal test method environment conditions - natural convection (still air). Available from www.jedec.org.

10.4.2 Selecting the product temperature range

When ordering the microcontroller, the temperature range is specified in the order code (see *Section 12: Ordering information*).

The following example shows how to calculate the temperature range needed for a given application.

Assuming the following application conditions:

Maximum ambient temperature T_{Amax}= 82 °C (measured according to JESD51-2), I_{DDmax} = 14 mA, V_{DD} = 5 V, maximum 20 I/Os used at the same time in output at low level with I_{OL} = 8 mA, V_{OL}= 0.4 V

P_{INTmax} = 14 mA x 5 V= 70 mW

P_{IOmax} = 20 x 8 mA x 0.4 V = 64 mW

This gives: P_{INTmax} = 70 mW and P_{IOmax} 64 mW:

P_{Dmax} = 70 mW + 64 mW

Thus: P_{Dmax} = 134 mW.

Using the values obtained in *Table 62: Thermal characteristics on page 81* T_{Jmax} is calculated as follows:

For LQFP64 46 °C/W

T_{Jmax} = 82 °C + (46 °C/W x 134 mW) = 82 °C + 6 °C = 88 °C

This is within the range of the suffix B version parts (-40 < T_J < 105 °C).

Parts must be ordered at least with the temperature range suffix B.

11 Package characteristics

To meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions, and product status are available at *www.st.com*.

11.1 Package mechanical data

Figure 42. 32-lead very thin fine pitch quad flat no-lead package (5 x 5)

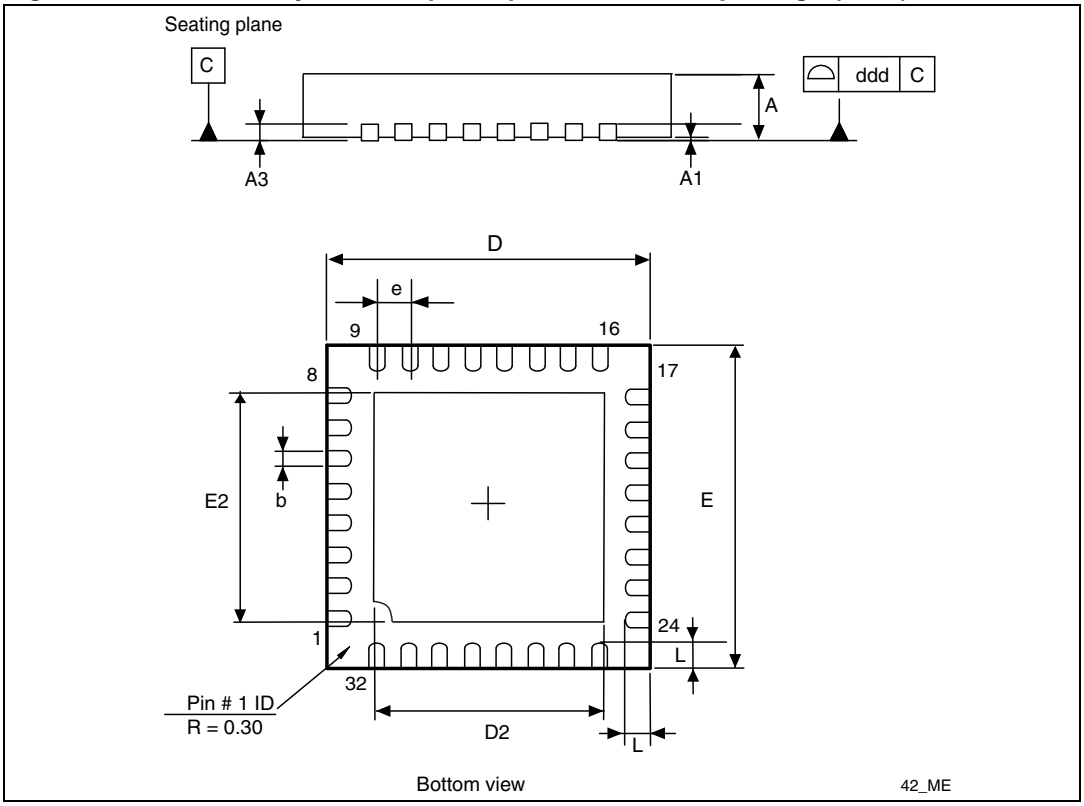


Table 63. 32-lead very thin fine pitch quad flat no-lead package mechanical data

Dim.	mm			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	0.80	0.90	1.00	0.0315	0.0354	0.0394
A1	0	0.02	0.05		0.0008	0.0020
A3		0.20			0.0079	
b	0.18	0.25	0.30	0.0071	0.0098	0.0118
D	4.85	5.00	5.15	0.1909	0.1969	0.2028
D2	3.20	3.45	3.70	0.1260		0.1457
E	4.85	5.00	5.15	0.1909	0.1969	0.2028
E2	3.20	3.45	3.70	0.1260	0.1358	0.1457
e		0.50			0.0197	
L	0.30	0.40	0.50	0.0118	0.0157	0.0197
ddd			0.08			0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits

Figure 43. 48-pin low profile quad flat package (7 x 7)

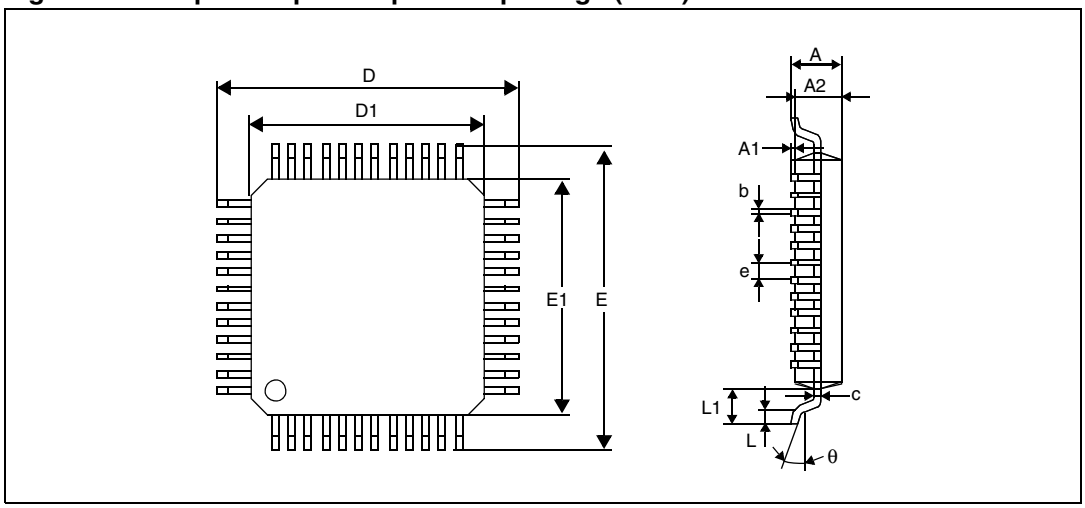


Table 64. 48-pin low profile quad flat package mechanical data

Dim.	mm			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	—	—	1.60	—	—	0.0630
A1	0.05	—	0.15	0.0020	—	0.0059
A2	1.35	1.40	1.45	0.0531	0.0551	0.0571
b	0.17	0.22	0.27	0.0067	0.0087	0.0106
c	0.09	—	0.20	0.0035	—	0.0079
D	—	9.00	—	—	0.3543	—
D1	—	7.00	—	—	0.2756	—
E	—	9.00	—	—	0.3543	—
E1	—	7.00	—	—	0.2756	—
e	—	0.50	—	—	0.0197	—
θ	0°	3.5°	7°	0°	3.5°	7°
L	0.45	0.60	0.75	0.0177	0.0236	0.0295
L1	—	1.00	—	—	0.0394	—

1. Values in inches are converted from mm and rounded to 4 decimal digits

Figure 44. 32-pin low profile quad flat package (7 x 7)

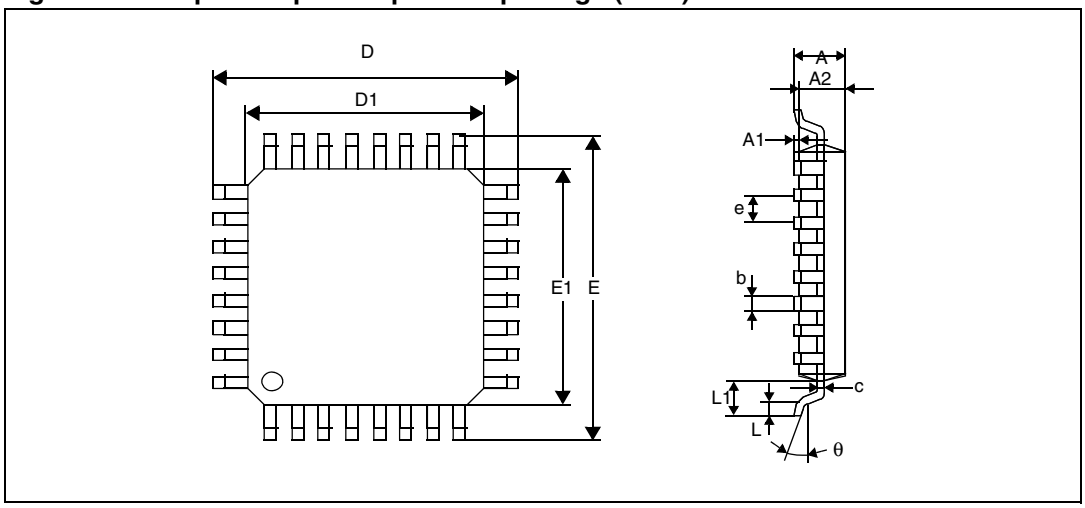


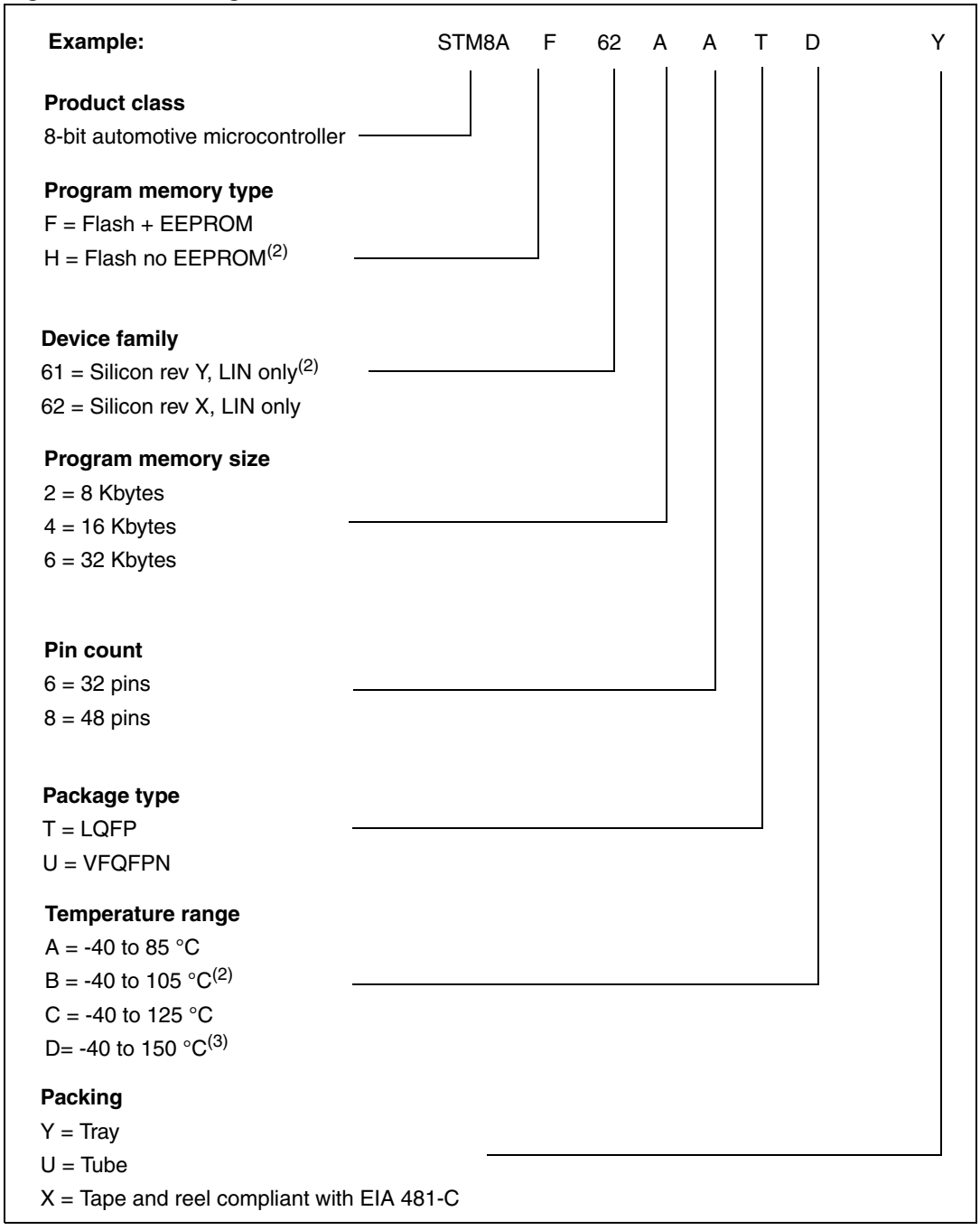
Table 65. 32-pin low profile quad flat package mechanical data

Dim.	mm			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	—	—	1.60	—	—	0.0630
A1	0.05	—	0.15	0.0020	—	0.0059
A2	1.35	1.40	1.45	0.0531	0.0551	0.0571
b	0.30	0.37	0.45	0.0118	0.0146	0.0177
c	0.09	—	0.20	0.0035	—	0.0079
D	—	9.00	—	—	0.3543	—
D1	—	7.00	—	—	0.2756	—
E	—	9.00	—	—	0.3543	—
E1	—	7.00	—	—	0.2756	—
e	—	0.80	—	—	0.0315	—
θ	0°	3.5°	7°	0°	3.5°	7°
L	0.45	0.60	0.75	0.0177	0.0236	0.0295
L1	—	1.00	—	—	0.0394	—

1. Values in inches are converted from mm and rounded to 4 decimal digits

12 Ordering information

Figure 45. Ordering information scheme



1. For a list of available options (e.g. memory size, package) and orderable part numbers or for further information on any aspect of this device, please go to *www.st.com* or contact the ST Sales Office nearest to you.
2. Not recommended for new design.
3. Available on STM8AF62xx devices.

13 Known limitations

Table 66 gives a summary of the fix status.

Table 66. Product evolution summary

Section	Limitation	Rev Y	Rev X
STM8A core			
Section 13.1.1	*Wait for event (WFE) instruction not supported*	Not fixed	Not fixed
Section 13.1.2	*JRIL and JRIH instructions not supported*		
Section 13.1.3	*CPU not returning to HALT if the AL bit is set*		
Section 13.1.4	*Main program not resuming after ISR has resets the AL bit*		
I²C interface			
Section 13.2.1	*Misplaced NACK when receiving 2 bytes in master mode*	Not fixed	Not fixed
Section 13.2.2	*Data register corrupted*		
Section 13.2.3	*Delay in STOP bit programming leading to reception of supplementary byte*		
Section 13.2.4	*START condition badly generated after misplaced STOP*		
USART interface			
Section 13.3.1	*Parity error flag (PE) is not correctly set in overrun condition*	Not fixed	Not fixed
LINUART interface			
Section 13.4.1	*Framing error issue with data byte 0x00*	Not fixed	Not fixed
Section 13.4.2	*Framing error when receiving an identifier (ID)*		
Section 13.4.3	*Parity error issue when receiving an identifier (ID)*		
Section 13.4.4	*OR flag not correctly set in LIN master mode*		
Section 13.4.5	*LIN header error when automatic resynchronization is enabled*		Fixed
Clock controller			
Section 13.5.1	*HSI cannot be switched off in run mode*	Not fixed	Not fixed
SPI interface			
Section 13.6.1	*Last bit too short if SPI is disabled during communication*	Not fixed	Not fixed
ADC			
Section 13.7.1	*EOC interrupt triggered when AWDIE and EOCIE set to '1'*	Not fixed	Not fixed

13.1 STM8A core

13.1.1 Wait for event (WFE) instruction not supported

Description

The WFE instruction is not implemented in devices covered by this datasheet. The WFE instruction is used to synchronize computing resources and not relevant for the present implementation. For further details on this instruction, refer to the STM8 CPU programming manual (PM0044) on *www.st.com*.

Workaround

None.

13.1.2 JRIL and JRIH instructions not supported

Description

JRIL (jump if port INT pin = 0) and JRIH (jump if port INT pin = 1) are not supported in devices covered by this datasheet. If implemented, they are conditional jumps: JRIL jumps if one of the external interrupt lines is low and JRIH jumps if one of the external interrupt lines is high.

In the devices covers by this datasheet, JRIL is equivalent to an unconditional jump and JRIH is equivalent to NOP. For further details on these instructions, refer to the STM8 CPU programming manual (PM0044) on *www.st.com*.

Workaround

None.

13.1.3 CPU not returning to HALT if the AL bit is set

Description

When the AL bit of the CFG_GCR register is set, the CPU does not return to HALT mode after exiting an interrupt service routine (ISR). It returns to the main program and executes the next instruction after the HALT instruction.

Workaround

None.

13.1.4 Main program not resuming after ISR has resets the AL bit

Description

If the CPU is in wait for interrupt state and the AL bit is set, the CPU returns to the wait for interrupt state after executing an ISR. To continue executing the main program, the AL bit must be reset inside the ISR. When AL is reset just before exiting the ISR, the CPU may remain stalled.

Workaround

The AL bit has to be reset at least two instructions before the IRET instruction.

13.2 I²C interface

13.2.1 Misplaced NACK when receiving 2 bytes in master mode

Description

When receiving two bytes in Master mode the usual sequence is the following:

1. Set POS and ACK bits of the I2C_CR2 register to ’1’.
2. Wait for ADDR event (address sent bit in the I2C_CR1 register). When ADDR is set to ‘1’, program ACK to ’0’ and clear ADDR.
3. Wait for BTF event (byte transfer finished bit in the I2C_CR1 register). When BTF is set to ‘1’, program the STOP bit to ’1’ in the I2C_CR2 register and read the 2 received bytes.

The NACK bit may be sent erroneously after the first byte.

Workaround

Use a different software sequence for ADDR and ACK clearing:

1. Wait for ADDR flag to be set
2. Mask interrupts
3. Clear ADDR
4. Clear ACK bit
5. Re-enable interrupts

As the TLI is not maskable, this sw workaround can not be applied in an application that makes use of the TLI.

13.2.2 Data register corrupted

Description

The content of the shift register may be shifted to the left by 1 bit and the second read operation will return an incorrect value when the following conditions are met:

- BTF bit (last data received) set to 1
- Software sequence (SET STOP, READ N-1, READ N) delayed (for instance by an interrupt)
- N-1 byte not read before the next SCL rising edge.

Workaround

Mask all active interrupts between the SET STOP and the READ N-1 instruction. As the TLI is not maskable, this software workaround can not be applied in an application that makes use of the TLI interrupt.

13.2.3 Delay in STOP bit programming leading to reception of supplementary byte

Description

When receiving one byte in master mode, the STOP bit in the I2C_CR2 register is programmed just after ADDR bit is cleared in order to generate a STOP condition after the reception of the byte. If the programming of the STOP bit is delayed after the end of the first

byte reception, the master may receive another byte before the STOP condition is generated and a wrong data will be received.

Workaround

Mask interrupts while clearing the ADDR bit and programming the STOP bit. As the TLI is not maskable, this software workaround can not be applied in an application that makes use of the TLI interrupt.

13.2.4 START condition badly generated after misplaced STOP

Description

When the START bit is set in the I2C_CR2 register and a misplaced STOP occurs on the bus thus leading to a bus error, a START condition on the bus may be badly generated by the I^2C peripheral (glitch on SDA resulting in SDA and SCL tied low simultaneously).

Workaround

When a bus error is detected (though a flag and/or an interrupt), check if a START condition was requested through the I2C_CR2 register. If so, a STOP condition should be generated followed by a new START condition. This does not avoid the badly generated START condition, but allows to resynchronize the network on the new START condition.

13.3 USART interface

13.3.1 Parity error flag (PE) is not correctly set in overrun condition

Description

If an overrun condition occurs, the parity error flag (PE) of the UART_SR register is not set for the frame which caused to the overrun condition. The PE flag represents the status of the last correctly received frame.

Workaround

None.

13.4 LINUART interface

13.4.1 Framing error issue with data byte 0x00

Description

If the LINUART interface is configured in LIN slave mode, and the active mode with break detection threshold set to 11 (LBDL bit of UART_CR4 register set to 1), FE and RXNE flags are not set to 0x00 when receiving a data byte with a framing error, followed by a recessive state. This occurs only if the dominant state length is in between 9.56 and 10.56 bit times the baud rate.

Workaround

The LIN driver software can handle this exceptional case by implementing frame timeouts to comply with the LIN standard. This method has been implemented in ST LIN 2.1 driver package which passed the LIN compliance tests.

13.4.2 Framing error when receiving an identifier (ID)

Description

If an ID framing error occurs when the LINUART is in active mode, both LHE and LHDF flags are set at the end of the LIN header with ID framing error.

Workaround

The LIN software driver can handle this case by checking both LHE and LHDF flags upon header reception.

13.4.3 Parity error issue when receiving an identifier (ID)

Description

If an ID parity occurs, the LINUART wakes up from mute mode and both LHE and LHDF flags are set at the end of the LIN header with parity error. The PE flag is also set.

Workaround

The LIN software driver can handle this case by checking all the flags upon header reception.

13.4.4 OR flag not correctly set in LIN master mode

Description

When the LINUART operates in master mode, the OR flag is not set if an overrun condition occurs.

Workaround

The LIN software driver can detect this case through a LIN protocol error.

13.4.5 LIN header error when automatic resynchronization is enabled

Description

If the LINUART is configured in LIN slave mode (LSLV bit set in LINUART_CR6 register) and the automatic resynchronization is enabled (LASE bit set in LINUART_CR6), the LHE flag may be set instead of LHDF flag when receiving a valid header.

This limitation is fixed in silicon revision X.

Workaround

None.

13.5 Clock controller

13.5.1 HSI cannot be switched off in run mode

Description

The internal 16 MHz RC oscillator cannot be switched off in run mode, even if the HSIEN bit is programmed to ‘0’.

Workaround

None.

13.6 SPI interface

13.6.1 Last bit too short if SPI is disabled during communication

Description

When the SPI interface operates in master mode and the baud rate generator prescaler is equal to 2, the SPI is disabled during ongoing communications, and the data and clock output signals are switched off at the last strobing edge of the SPI clock.

As a consequence the length of the last bit is out of range and its reception on the bus is not ensured.

Workaround

Check if a communication is ongoing before disabling the SPI interface. This can be done by monitoring the BSY bit in the SPI_SR register.

13.7 ADC

13.7.1 EOC interrupt triggered when AWDIE and EOCIE set to ‘1’

Description

When the analog watchdog is enabled and AWDIE and EOCIE are both set to ‘1’, the ADC interrupt should only be triggered when the conversion result exceeds one of the analog watchdog thresholds (see table 79 in the STM8A reference manual RM0009).

However, for the devices covered by this datasheet, the interrupt is triggered after each conversion, thus leading to a high interrupt load.

Workaround

Set AWDIE to ‘1’ and EOCIE to ‘0’ instead and stop the conversions inside the ISR by resetting the CONT bit. However the latest conversion result having triggered the watchdog may be overwritten.

14 STM8 development tools

Development tools for the STM8A microcontrollers include the

- STice emulation system offering tracing and code profiling
- STVD high-level language debugger including assembler and visual development environment - seamless integration of third party C compilers.
- STVP Flash programming software

In addition, the STM8A comes with starter kits, evaluation boards and low-cost in-circuit debugging/programming tools.

14.1 Emulation and in-circuit debugging tools

The STM8 tool line includes the STice emulation system offering a complete range of emulation and in-circuit debugging features on a platform that is designed for versatility and cost-effectiveness. In addition, STM8A application development is supported by a low-cost in-circuit debugger/programmer.

The STice is the fourth generation of full-featured emulators from STMicroelectronics. It offers new advanced debugging capabilities including tracing, profiling and code coverage analysis to help detect execution bottlenecks and dead code.

In addition, STice offers in-circuit debugging and programming of STM8A microcontrollers via the STM8 single wire interface module (SWIM), which allows non-intrusive debugging of an application while it runs on the target microcontroller.

For improved cost effectiveness, STice is based on a modular design that allows you to order exactly what you need to meet your development requirements and to adapt your emulation system to support existing and future ST microcontrollers.

14.1.1 STice key features

- Program and data trace recording up to 128 K records
- Advanced breakpoints with up to 4 levels of conditions
- Data breakpoints
- Real-time read/write of all device resources during emulation
- Occurrence and time profiling and code coverage analysis (new features)
- In-circuit debugging/programming via SWIM protocol
- 8-bit probe analyzer
- 1 input and 2 output triggers
- USB 2.0 high speed interface to host PC
- Power supply follower managing application voltages between 1.62 to 5.5 V
- Modularity that allows you to specify the components you need to meet your development requirements and adapt to future requirements.
- Supported by free software tools that include integrated development environment (IDE), programming software interface and assembler for STM8.

14.2 Software tools

STM8 development tools are supported by a complete, free software package from STMicroelectronics that includes ST visual develop (STVD) IDE and the ST visual programmer (STVP) software interface. STVD provides seamless integration of the Cosmic C compiler for STM8, which is available in a free version that outputs up to 16 Kbytes of code.

14.2.1 STM8 toolset

The STM8 toolset with STVD integrated development environment and STVP programming software is available for free download at www.st.com/mcu. This package includes:

ST visual develop

Full-featured integrated development environment from STMicroelectronics, featuring:

- Seamless integration of C and ASM toolsets
- Full-featured debugger
- Project management
- Syntax highlighting editor
- Integrated programming interface
- Support of advanced emulation features for STice such as code profiling and coverage

ST visual programmer (STVP)

Easy-to-use, unlimited graphical interface allowing read, write and verification of the STM8A microcontroller's Flash memory. STVP also offers project mode for saving programming configurations and automating programming sequences.

14.2.2 C and assembly toolchains

Control of C and assembly toolchains is seamlessly integrated into the STVD integrated development environment, making it possible to configure and control the building of your application directly from an easy-to-use graphical interface.

Available toolchains include:

C compiler for STM8

Available in a free version that outputs up to 16 Kbytes of code. For more information, see www.cosmic-software.com, www.raisonance.com

STM8 assembler linker

Free assembly toolchain included in the STM8 toolset, which allows you to assemble and link your application source code.

14.3 Programming tools

During the development cycle, STice provides in-circuit programming of the STM8A Flash microcontroller on your application board via the SWIM protocol. Additional tools are to include a low-cost in-circuit programmer as well as ST socket boards, which provide dedicated programming platforms with sockets for programming your STM8A.

For production environments, programmers will include a complete range of gang and automated programming solutions from third-party tool developers already supplying programmers for the STM8 family.

15 Revision history

Table 67. Document revision history

Date	Revision	Changes
22-Aug-2008	1	Initial release
10-Aug-2009	2	Document revised as the following: Updated *Features on page 1*; Updated *Table 1: Device summary*; Updated *Section 3: Product line-up*; Changed *Section 5: Product overview*; Updated *Section 6: Pinouts and pin description*; Changed *Section 7.2: Register map*; Updated *Section 8: Interrupt table*; Updated *Section 9: Option bytes*; Updated *Section 10: Electrical characteristics*; Updated *Section 11: Package characteristics*; Updated *Section 12: Ordering information*; Added *Section 13: Known limitations*.
22-Oct-2009	3	Adapted *Table 7: STM8AF61xx/62xx (32 Kbytes) microcontroller pin description*. Added *Section 13.4.5: LIN header error when automatic resynchronization is enabled*.
08-Jul-2010	4	Updated title on cover page. Added VFQFPN32 5x 5 mm package. Added STM8AF62xx devices, and modified cover page header to clarify the part numbers covered by the datasheets. Updated *Note 1* below *Table 1: Device summary*. Updated D temperature range to -40 to 150°C. Content of *Section 5: Product overview* reorganized. Renamed *Section 7 Memory and register map*, and content merged with Register map section. Renamed BL_EN and NBL_EN, BL and NBL, respectively, in *Table 31: Option bytes*. Added *Table 36: Operating lifetime*. Added CEXT and P_D (power dissipation) in *Table 37: General operating conditions*, and *Section 10.3.1: VCAP external capacitor*. Suffix D maximum junction temperature (T_J) updated in *Table 37: General operating conditions*. Update t_{VDD} in *Table 38: Operating conditions at power-up/power-down*. Moved *Table 43: Typical peripheral current consumption VDD = 5.0 V* to *Section : Current consumption for on-chip peripherals* and removed $I_{DD(CAN)}$. Updated *Section 12: Ordering information* for the devices supported by the datasheet. Updated *Section 13: Known limitations*.

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