



STL15N3LLH5

N-channel 30 V, 0.0045 Ω , 15 A, PowerFLAT™ (3.3 x 3.3)
STripFET™ V Power MOSFET

Preliminary Data

Features

Type	V _{DSS}	R _{DS(on)}	I _D
STL15N3LLH5	30V	<0.0054 Ω	15A ⁽¹⁾

1. The value is rated according R_{thj-pcb}

- R_{DS(on)} * Q_g industry benchmark
- Extremely low on-resistance R_{DS(on)}
- Very low switching gate charge
- High avalanche ruggedness
- Low gate drive power losses

Applications

- Switching applications

Description

This product utilizes the 5th generation of design rules of ST's proprietary STripFET™ technology. The lowest available R_{DS(on)} * Q_g, in this chip scale package, makes this device suitable for the most demanding DC-DC converter applications, where high power density is to be achieved.

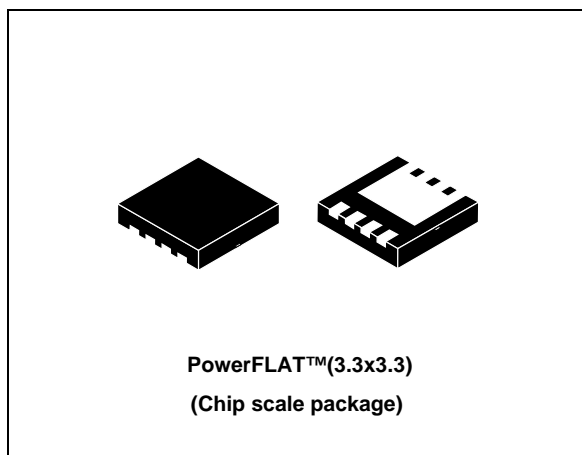


Figure 1. Internal schematic diagram

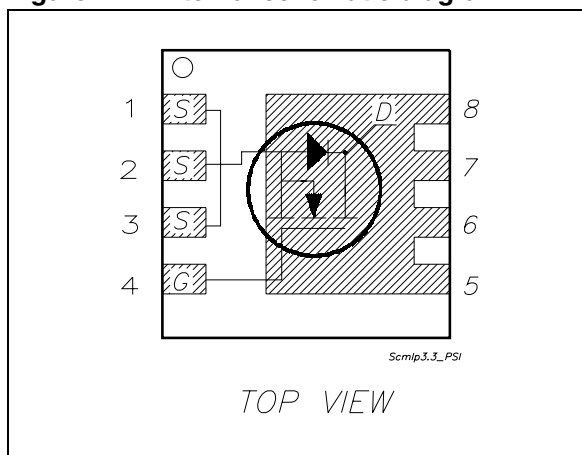


Table 1. Device summary

Order code	Marking	Package	Packaging
STL15N3LLH5	15N3LLH5	PowerFLAT™ (3.3 x 3.3)	Tape and reel

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1 Electrical ratings

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Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage ($V_{GS} = 0$)	30	V
V_{GS}	Gate-source voltage	± 22	V
$I_D^{(1)}$	Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$	15	A
$I_D^{(1)}$	Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$	9.3	A
$I_{DM}^{(2)}$	Drain current (pulsed)	60	A
$P_{TOT}^{(3)}$	Total dissipation at $T_C = 25\text{ }^\circ\text{C}$	50	W
$P_{TOT}^{(1)}$	Total dissipation at $T_C = 25\text{ }^\circ\text{C}$	2	W
	Derating factor	0.4	W/ $^\circ\text{C}$
T_J T_{stg}	Operating junction temperature storage temperature	-55 to 150	$^\circ\text{C}$

1. The value is rated according $R_{thj-pcb}$
2. Pulse width limited by safe operating area.
3. The value is rated according R_{thj-c}

Table 3. Thermal resistance

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case (drain)	2.5	$^\circ\text{C}/\text{W}$
$R_{thj-pcb}^{(1)}$	Thermal resistance junction-pcb	42.8	$^\circ\text{C}/\text{W}$
$R_{thj-pcb}^{(2)}$	Thermal resistance junction-pcb	63.5	$^\circ\text{C}/\text{W}$

1. When mounted on FR-4 board of 1inch², 2oz Cu, $t < 10\text{sec}$
2. Steady state

2 Electrical characteristics

($T_{CASE}=25^{\circ}\text{C}$ unless otherwise specified)

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Table 4. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = 250\ \mu\text{A}$, $V_{GS} = 0$	30			V
I_{DSS}	Zero gate voltage drain current ($V_{GS} = 0$)	$V_{DS} = \text{Max rating}$, $V_{DS} = \text{Max rating @ } 125^{\circ}\text{C}$			1 10	μA μA
I_{GSS}	Gate body leakage current ($V_{DS} = 0$)	$V_{GS} = \pm 22\ \text{V}$			± 100	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$, $I_D = 250\ \mu\text{A}$	1		2.5	V
$R_{DS(on)}$	Static drain-source on resistance	$V_{GS} = 10\ \text{V}$, $I_D = 7.5\ \text{A}$ $V_{GS} = 4.5\ \text{V}$, $I_D = 7.5\ \text{A}$		0.0045 0.006	0.0054 0.0075	Ω Ω

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	$V_{DS} = 25\ \text{V}$, $f = 1\ \text{MHz}$, $V_{GS} = 0$		1500		pF
C_{oss}	Output capacitance			295		pF
C_{rss}	Reverse transfer capacitance			39		pF
Q_g	Total gate charge	$V_{DD} = 15\ \text{V}$, $I_D = 15\ \text{A}$		12		nC
Q_{gs}	Gate-source charge	$V_{GS} = 4.5\ \text{V}$		4		nC
Q_{gd}	Gate-drain charge	(see Figure 3)		4.7		nC
R_G	Gate input resistance	$f = 1\ \text{MHz}$ Gate DC Bias = 0 Test signal level = 20 mV Open drain	0.5	1.5	2.5	Ω

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD}=15\text{ V}$, $I_D=7.5\text{ A}$, $R_G=4.7\ \Omega$, $V_{GS}=4.5\text{ V}$ (see Figure 2)		9.3		ns
t_r	Rise time			14.5		ns
$t_{d(off)}$	Turn-off delay time			22.7		ns
t_f	Fall time			4.5		ns

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current				15	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)				60	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD}=15\text{ A}$, $V_{GS}=0$			1.1	V
t_{rr}	Reverse recovery time	$I_{SD}=15\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$, $V_{DD}=20\text{ V}$, $T_j=150\text{ }^\circ\text{C}$ (see Figure 7)		25		ns
Q_{rr}	Reverse recovery charge			17.5		nC
I_{RRM}	Reverse recovery current			1.4		A

1. Pulse width limited by safe operating area
2. Pulsed: pulse duration=300 μs , duty cycle 1.5%

3 Test circuit

Figure 2. Switching times test circuit for resistive load

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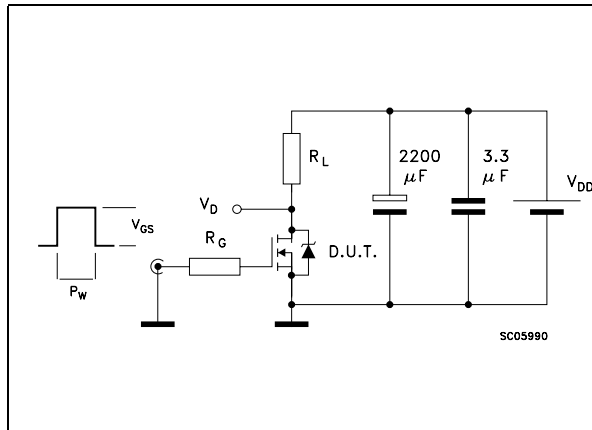


Figure 3. Gate charge test circuit

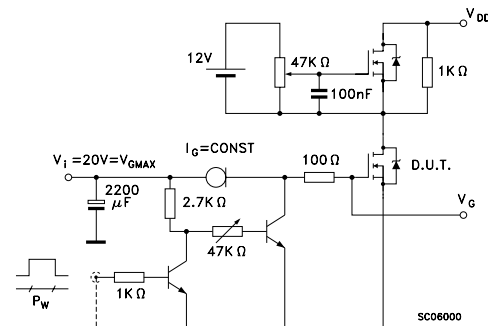


Figure 4. Test circuit for inductive load switching and diode recovery times

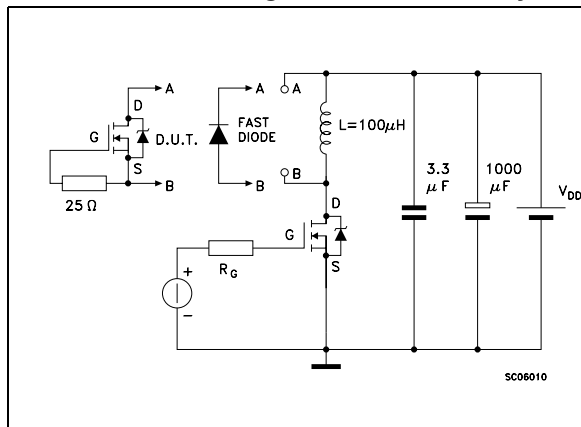


Figure 5. Unclamped inductive load test circuit

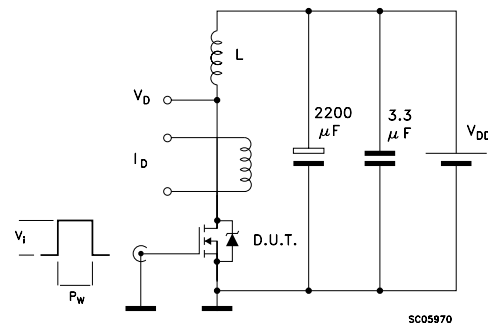


Figure 6. Unclamped inductive waveform

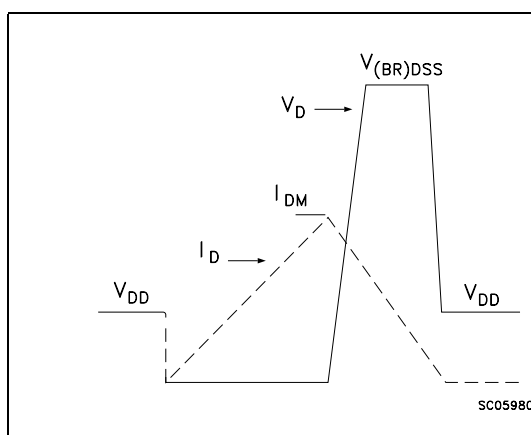
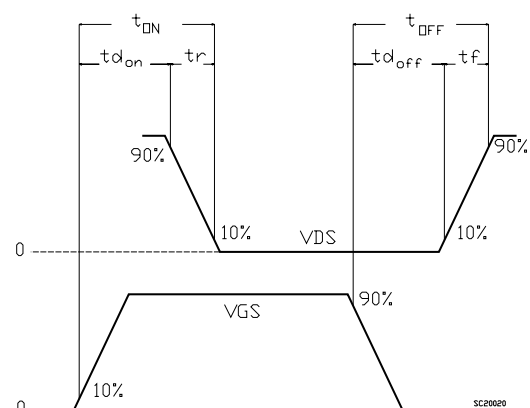


Figure 7. Switching time waveform



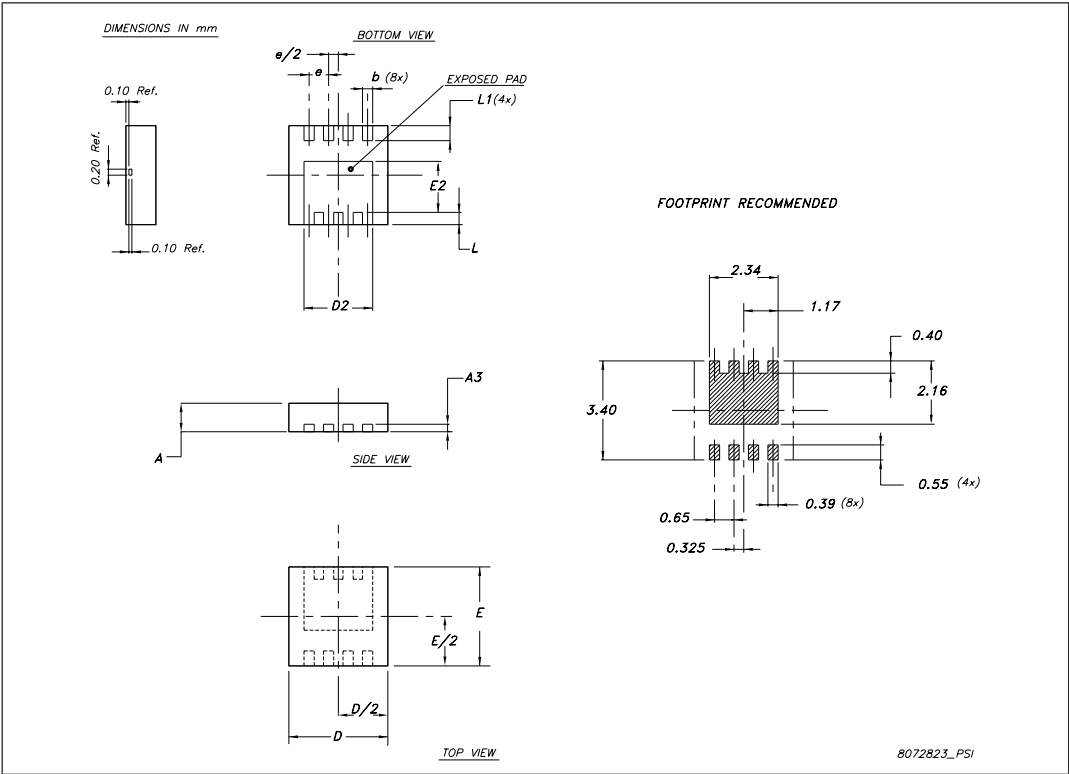
4 Package mechanical data

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In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a lead-free second level interconnect . The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com

PowerFLAT™ (3.3 x 3.3) mechanical data

Dim	mm			inch		
	Min	Typ	Max	Min	Typ	Max
A	0.950		1.000	0.037		0.039
A3		0.200			0.008	
b	0.29	0.34	0.39	0.011	0.013	0.015
D	3.200	3.300	3.400	0.126	0.123	0.134
D2	2.24	2.29	2.34	0.088	0.090	0.092
E	2.20	3.30	3.40	0.086	0.123	0.1338
E2	1.660	1.710	1.760	0.065	0.067	0.069
e		0.650			0.025	
L		0.40			0.0157	
L1	0.45	0.50	0.55	0.017	0.0196	0.021



5 Revision history

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Table 8. Document revision history

Date	Revision	Changes
25-Aug-2008	1	First release

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