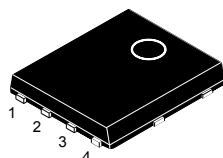
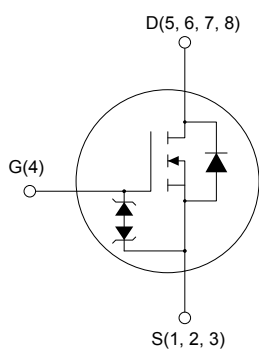


N-channel 600 V, 550 mΩ typ., 5.5 A, MDmesh™ M6 Power MOSFET in a PowerFLAT™ 5x6 HV package



PowerFLAT™ 5x6 HV



AM15540v7



Features

Order code	V _{DS}	R _{DS(on)} max.	I _D	P _{TOT}
STL10N60M6	600 V	660 mΩ	5.5 A	48 W

- Reduced switching losses
- Lower R_{DS(on)} per area vs previous generation
- Low gate input resistance
- 100% avalanche tested
- Zener-protected

Applications

- Switching applications
- LLC converters
- Boost PFC converters

Description

The new MDmesh™ M6 technology incorporates the most recent advancements to the well-known and consolidated MDmesh family of SJ MOSFETs. STMicroelectronics builds on the previous generation of MDmesh devices through its new M6 technology, which combines excellent R_{DS(on)} per area improvement with one of the most effective switching behaviors available, as well as a user-friendly experience for maximum end-application efficiency.

Product status link

[STL10N60M6](#)

Product summary

Order code	STL10N60M6
Marking	10N60M6
Package	PowerFLAT™ 5x6 HV
Packing	Tape and reel

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{GS}	Gate-source voltage	± 25	V
I_D	Drain current (continuous) at $T_{case} = 25\text{ }^{\circ}\text{C}$	5.5	A
	Drain current (continuous) at $T_{case} = 100\text{ }^{\circ}\text{C}$	3.5	
$I_{DM}^{(1)}$	Drain current (pulsed)	16	A
P_{TOT}	Total power dissipation at $T_{case} = 25\text{ }^{\circ}\text{C}$	48	W
$I_{AR}^{(2)}$	Avalanche current, repetitive or not repetitive	1.4	A
$E_{AS}^{(3)}$	Single pulse avalanche energy	120	mJ
$dv/dt^{(4)}$	Peak diode recovery voltage slope	15	V/ns
$dv/dt^{(5)}$	MOSFET dv/dt ruggedness	100	
T_{stg}	Storage temperature range	-55 to 150	$^{\circ}\text{C}$
T_j	Operating junction temperature range		

1. Pulse width is limited by safe operating area.
2. Pulse width limited by T_{jmax} .
3. Starting $T_j = 25\text{ }^{\circ}\text{C}$, $I_D = I_{AR}$, $V_{DD} = 50\text{ V}$.
4. $I_{SD} \leq 5.5\text{ A}$, $di/dt = 400\text{ A}/\mu\text{s}$, V_{DS} peak $< V_{(BR)DSS}$, $V_{DD} = 400\text{ V}$
5. $V_{DS} \leq 480\text{ V}$

Table 2. Thermal data

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case	2.6	$^{\circ}\text{C}/\text{W}$
$R_{thj-pcb}^{(1)}$	Thermal resistance junction-pcb	50	

1. When mounted on an 1-inch² FR-4, 2 Oz copper board.

2 Electrical characteristics

($T_{\text{case}} = 25\text{ }^{\circ}\text{C}$ unless otherwise specified)

Table 3. Static

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(\text{BR})\text{DSS}}$	Drain-source breakdown voltage	$V_{\text{GS}} = 0\text{ V}$, $I_{\text{D}} = 1\text{ mA}$	600			V
I_{DSS}	Zero gate voltage drain current	$V_{\text{GS}} = 0\text{ V}$, $V_{\text{DS}} = 600\text{ V}$			1	μA
		$V_{\text{GS}} = 0\text{ V}$, $V_{\text{DS}} = 600\text{ V}$, $T_{\text{case}} = 125\text{ }^{\circ}\text{C}$ ⁽¹⁾			100	
I_{GSS}	Gate-body leakage current	$V_{\text{DS}} = 0\text{ V}$, $V_{\text{GS}} = \pm 25\text{ V}$			± 10	μA
$V_{\text{GS(th)}}$	Gate threshold voltage	$V_{\text{DS}} = V_{\text{GS}}$, $I_{\text{D}} = 250\text{ }\mu\text{A}$	3.25	4	4.75	V
$R_{\text{DS(on)}}$	Static drain-source on-resistance	$V_{\text{GS}} = 10\text{ V}$, $I_{\text{D}} = 2.75\text{ A}$		550	660	m Ω

1. Defined by design, not subject to production test.

Table 4. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	$V_{\text{DS}} = 100\text{ V}$, $f = 1\text{ MHz}$, $V_{\text{GS}} = 0\text{ V}$	-	338	-	pF
C_{oss}	Output capacitance		-	26.2	-	
C_{rss}	Reverse transfer capacitance		-	3.8	-	
$C_{\text{oss eq.}}^{(1)}$	Equivalent output capacitance	$V_{\text{DS}} = 0\text{ to }480\text{ V}$, $V_{\text{GS}} = 0\text{ V}$	-	59	-	pF
R_{G}	Intrinsic gate resistance	$f = 1\text{ MHz}$, $I_{\text{D}} = 0\text{ A}$	-	7	-	Ω
Q_{g}	Total gate charge	$V_{\text{DD}} = 480\text{ V}$, $I_{\text{D}} = 6.4\text{ A}$, $V_{\text{GS}} = 0\text{ to }10\text{ V}$ (see Figure 14. Test circuit for gate charge behavior)	-	8.8	-	nC
Q_{gs}	Gate-source charge		-	4.8	-	
Q_{gd}	Gate-drain charge		-	2.7	-	

1. $C_{\text{oss eq.}}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS} .

Table 5. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{\text{d(on)}}$	Turn-on delay time	$V_{\text{DD}} = 300\text{ V}$, $I_{\text{D}} = 3.2\text{ A}$, $R_{\text{G}} = 4.7\text{ }\Omega$, $V_{\text{GS}} = 10\text{ V}$ (see Figure 13. Test circuit for resistive load switching times and Figure 18. Switching time waveform)	-	11	-	ns
t_{r}	Rise time		-	8.2	-	
$t_{\text{d(off)}}$	Turn-off delay time		-	23	-	
t_{f}	Fall time		-	10	-	

Table 6. Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		5.5	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		16	A
$V_{SD}^{(2)}$	Forward on voltage	$V_{GS} = 0\text{ V}$, $I_{SD} = 5.5\text{ A}$	-		1.6	V
t_{rr}	Reverse recovery time	$I_{SD} = 6.4\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$, $V_{DD} = 60\text{ V}$ (see Figure 15. Test circuit for inductive load switching and diode recovery times)	-	155		ns
Q_{rr}	Reverse recovery charge		-	0.813		μC
I_{RRM}	Reverse recovery current	$I_{SD} = 6.4\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$, $V_{DD} = 60\text{ V}$, $T_j = 150\text{ }^\circ\text{C}$ (see Figure 15. Test circuit for inductive load switching and diode recovery times)	-	10.5		A
t_{rr}	Reverse recovery time		-	250		ns
Q_{rr}	Reverse recovery charge		-	1.35		μC
I_{RRM}	Reverse recovery current		-	10.8		A

1. Pulse width is limited by safe operating area.
2. Pulse test: pulse duration = 300 μs , duty cycle 1.5%.

2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

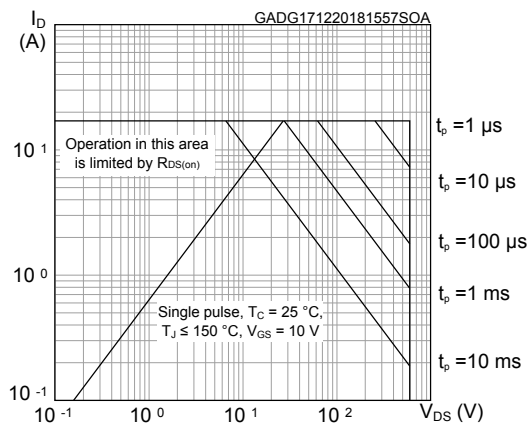


Figure 2. Thermal impedance

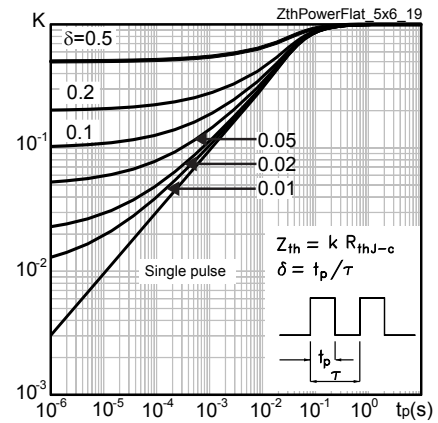


Figure 3. Output characteristics

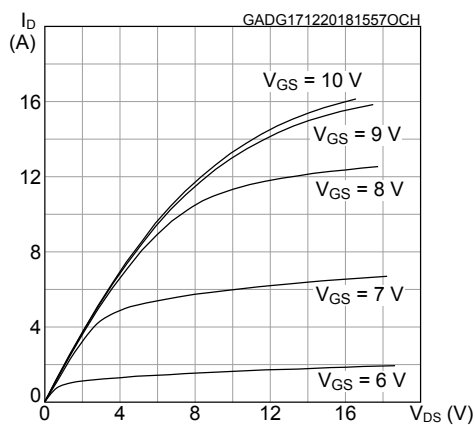


Figure 4. Transfer characteristics

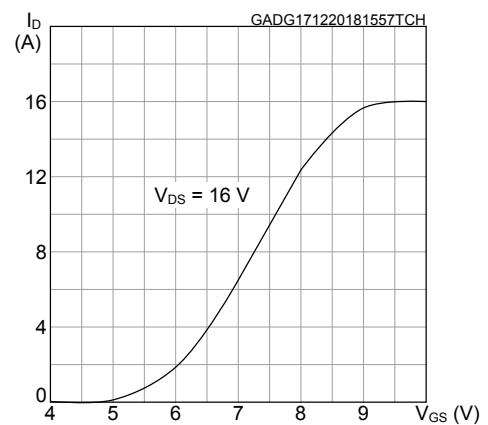


Figure 5. Gate charge vs gate-source voltage

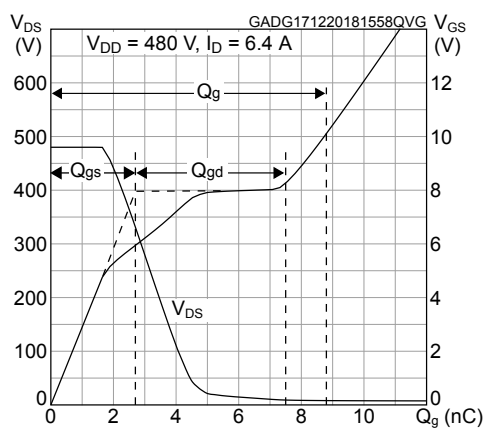


Figure 6. Static drain-source on-resistance

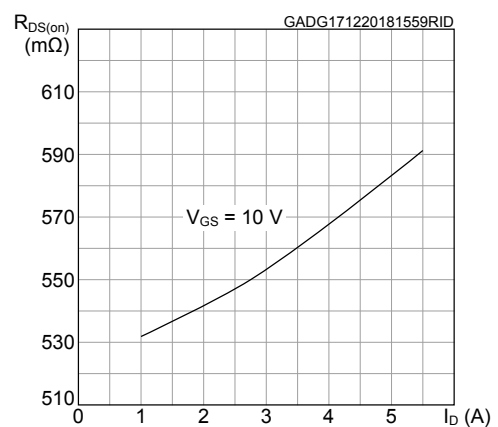


Figure 7. Capacitance variations

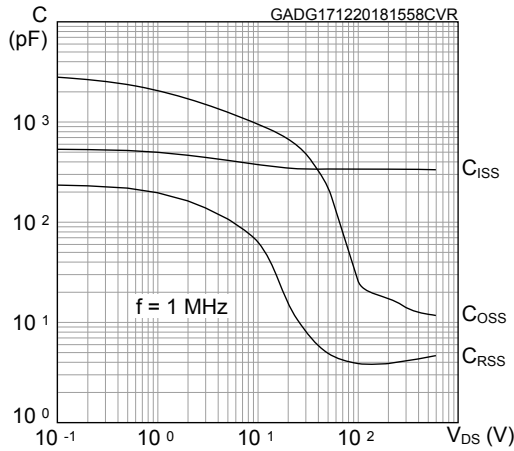


Figure 8. Output capacitance stored energy

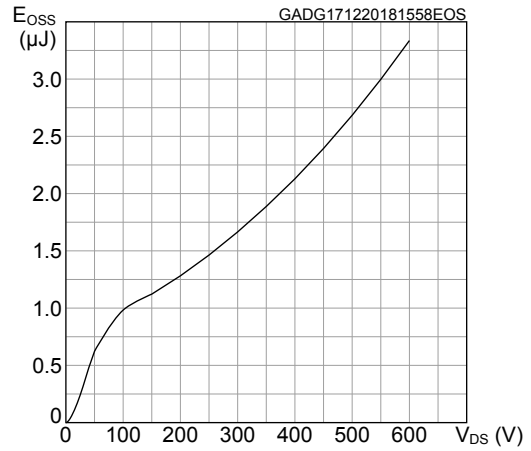


Figure 9. Normalized gate threshold voltage vs temperature

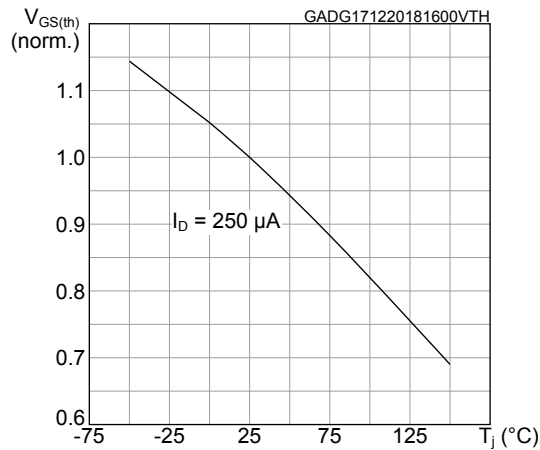


Figure 10. Normalized on-resistance vs temperature

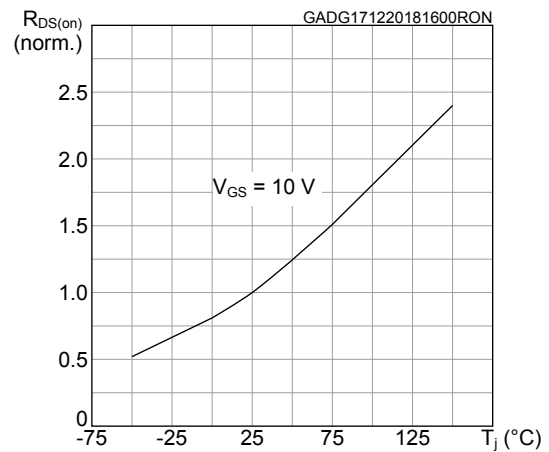


Figure 11. Normalized $V_{(BR)DSS}$ vs temperature

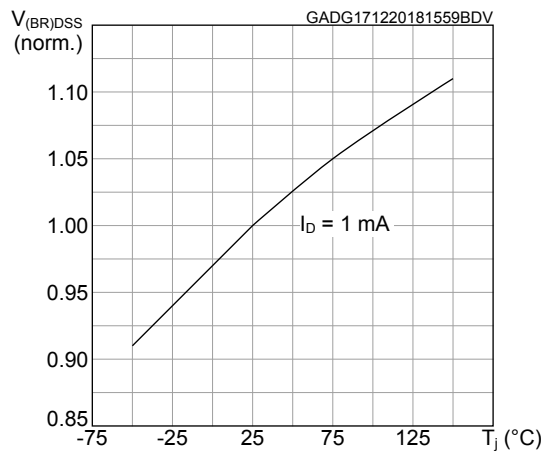
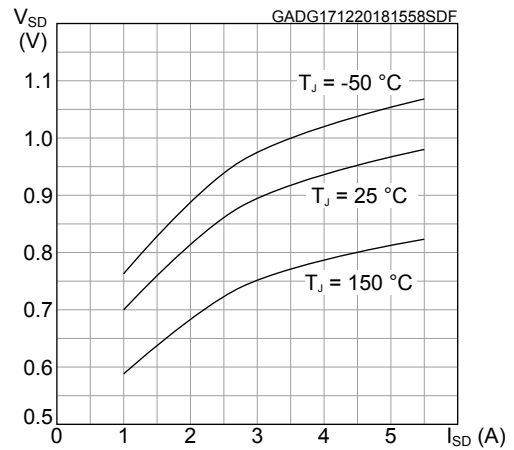
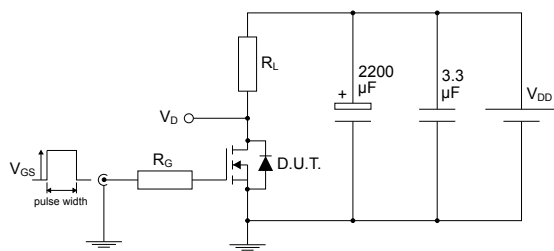


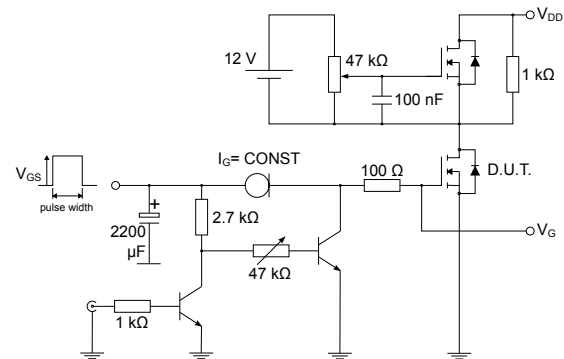
Figure 12. Source-drain diode forward characteristics



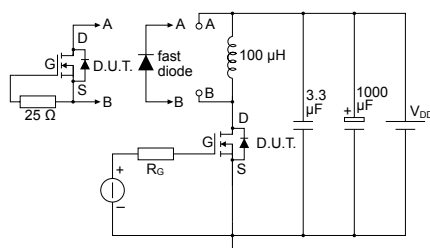
3 Test circuits

Figure 13. Test circuit for resistive load switching times


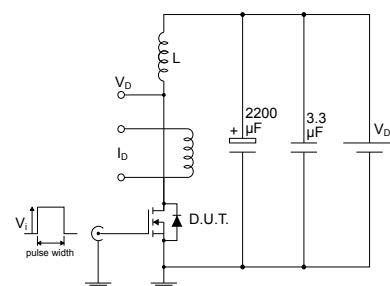
AM01468v1

Figure 14. Test circuit for gate charge behavior


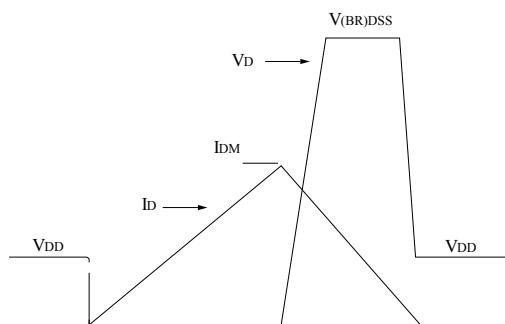
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Figure 15. Test circuit for inductive load switching and diode recovery times


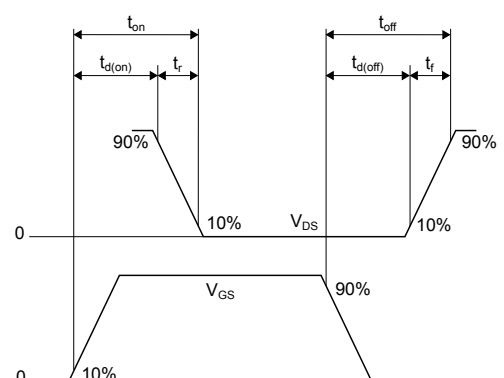
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Figure 16. Unclamped inductive load test circuit


AM01471v1

Figure 17. Unclamped inductive waveform


AM01472v1

Figure 18. Switching time waveform


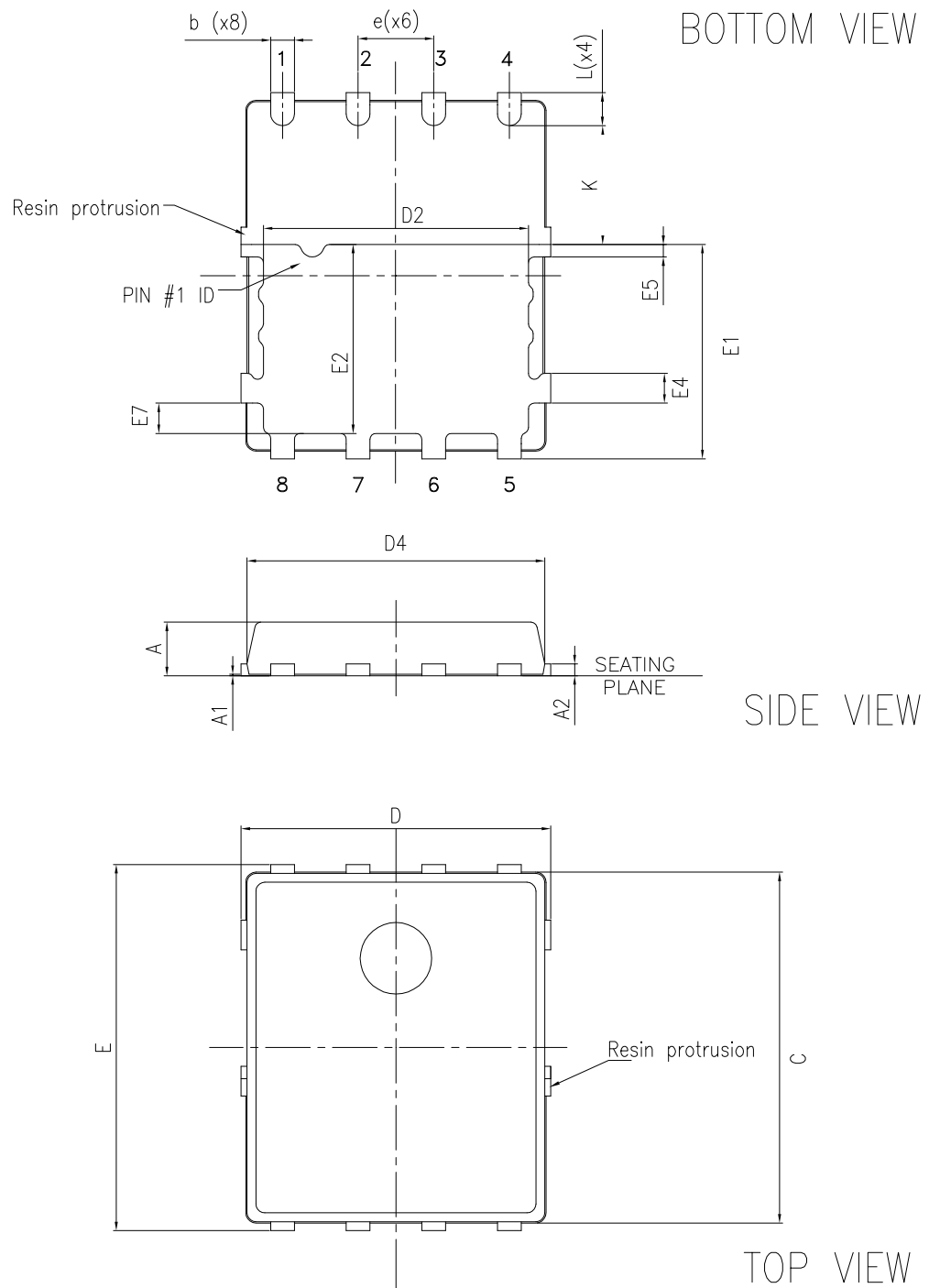
AM01473v1

4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of **ECOPACK®** packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

4.1 PowerFLAT™ 5x6 HV package information

Figure 19. PowerFLAT™ 5x6 HV package outline

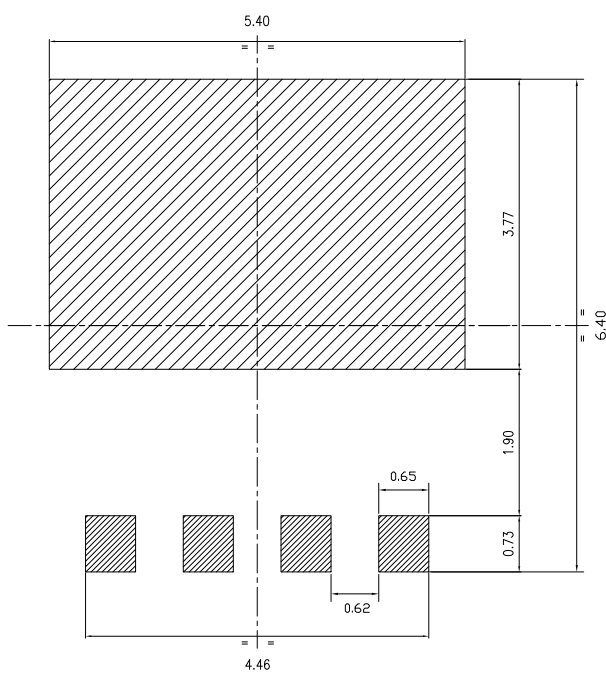


8368143_Rev_4

Table 7. PowerFLAT™ 5x6 HV mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	0.80		1.00
A1	0.02		0.05
A2		0.25	
b	0.30		0.50
C	5.60	5.80	6.00
D	5.10	5.20	5.30
D2	4.30	4.40	4.50
D4	4.60	4.80	5.00
E	6.05	6.15	6.25
E1	3.50	3.60	3.70
E2	3.10	3.20	3.30
E4	0.40	0.50	0.60
E5	0.10	0.20	0.30
E7	0.40	0.50	0.60
e		1.27	
L	0.50	0.55	0.60
K	1.90	2.00	2.10

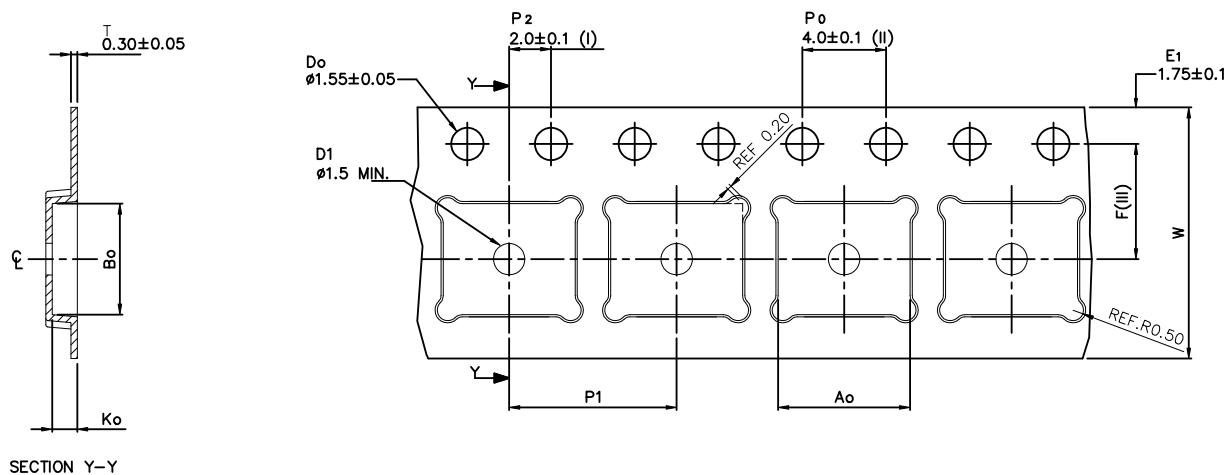
Figure 20. PowerFLAT™ 5x6 HV recommended footprint (dimensions are in mm)



8368143_Rev_4_footprint

4.2 PowerFLAT™ 5x6 packing information

Figure 21. PowerFLAT™ 5x6 tape (dimensions are in mm)



Ao	6.30 +/– 0.1
Bo	5.30 +/– 0.1
Ko	1.20 +/– 0.1
F	5.50 +/– 0.1
P1	8.00 +/– 0.1
W	12.00 +/– 0.3

(I) Measured from centreline of sprocket hole to centreline of pocket.

(II) Cumulative tolerance of 10 sprocket holes is ± 0.20 .

(III) Measured from centreline of sprocket hole to centreline of pocket

Base and bulk quantity 3000 pcs
All dimensions are in millimeters

8234350_Tape_rev_C

Figure 22. PowerFLAT™ 5x6 package orientation in carrier tape

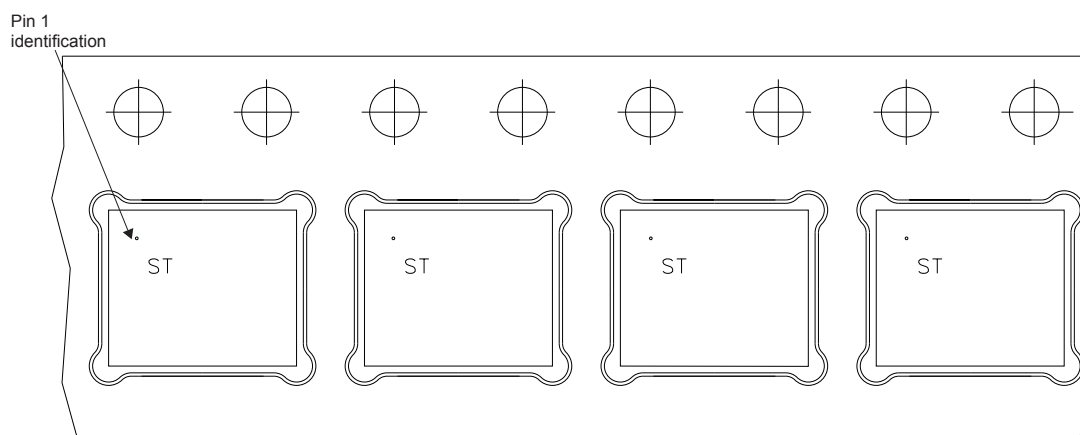
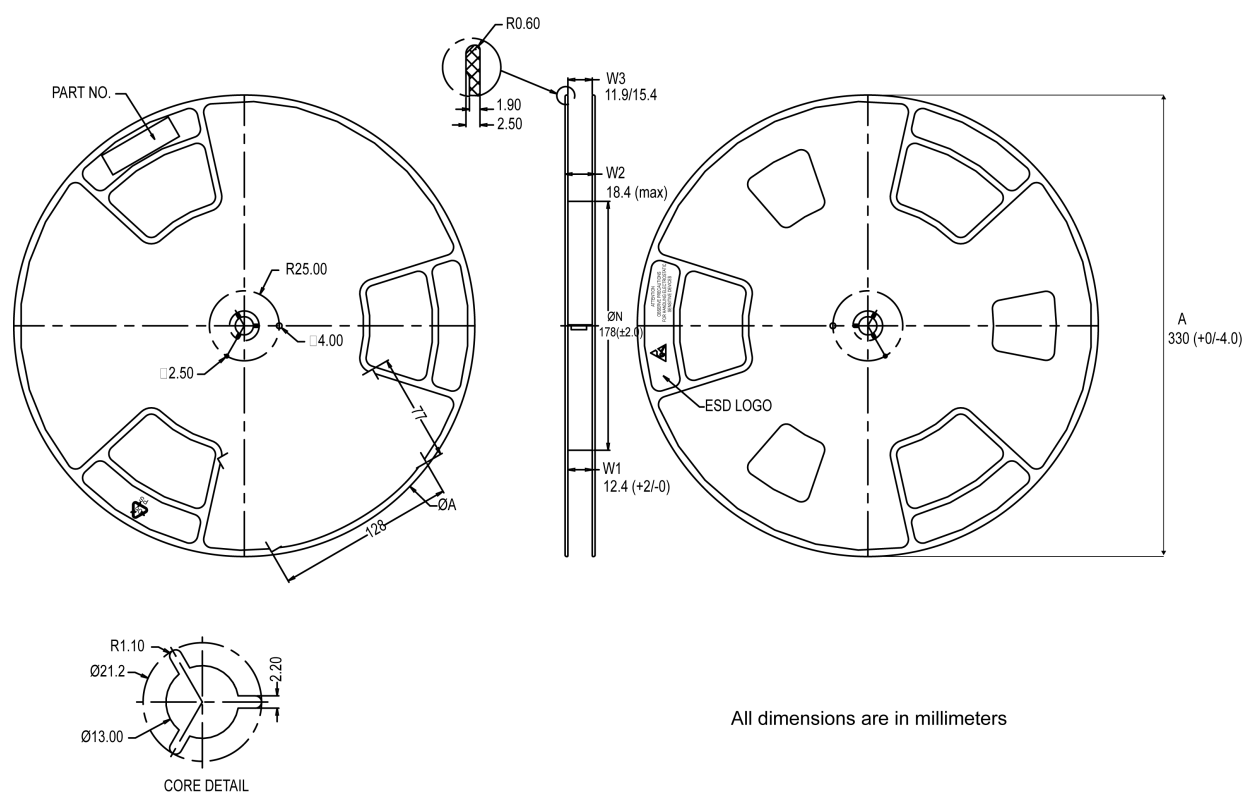


Figure 23. PowerFLAT™ 5x6 reel



8234350_Reel_rev_C

Revision history

Table 8. Document revision history

Date	Version	Changes
18-Dec-2018	1	First release.

Contents

1	Electrical ratings	2
2	Electrical characteristics.....	3
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