STL100NHS3LL

N-channel 30V - 0.0032Ω - 22A - PowerFLAT™ (6x5) STripFET™ Power MOSFET plus monolithic Schottky

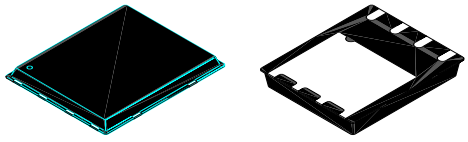
Preliminary Data

Features

Type	V_{DSS}	$R_{DS(on)}$	I_D
STL100NHS3LL	30V	< 0.0042Ω	22A(1)

1. This value is rated according to Rthj-pcb

- Optimal $R_{DS(on)}$ x Qg trade-off @ 4.5V
- Reduced switching losses
- Reduced conduction losses
- Improved junction-case thermal resistance



PowerFLAT™(6x5)

Application

- Switching applications

Description

This product utilizes the latest advanced design rules of ST's proprietary STripFET™ technology and a proprietary process for integrating a monolithic Schottky diode. The new Power MOSFET is optimized for the most important demanding synchronous switch function in DC-DC converter for Computer and Telecom.

Figure 1. Internal schematic diagram

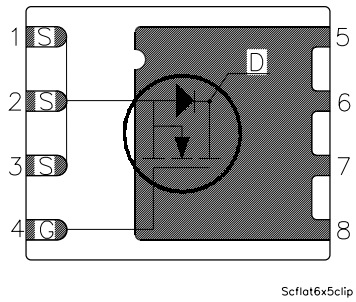


Table 1. Device summary

Order code	Marking	Package	Packaging
STL100NHS3LL	L100NHS3LL	PowerFLAT™ (6 x 5)	Tape & reel

1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage (V_{GS} = 0)	30	V
V_{GS}	Gate-source voltage	± 16	V
I_D (1)	Drain current (continuous) at T_C = 25°C	22	A
I_D (1)	Drain current (continuous) at T_C = 100°C	13.7	A
I_D(2)	Drain current (continuous) at T_C = 25°C	100	A
I_{DM} (3)	Drain current (pulsed)	88	A
P_{TOT}(1)	Total dissipation at T_C = 25°C	80	W
P_{TOT}(2)	Total dissipation at T_C = 25°C	4	W
T_j T_{stg}	Operating junction temperature Storage temperature	-55 to 150	°C

1. The value is rated accordingly to $R_{thj\text{-}pcb}$
2. This value is according $R_{thj\text{-}c}$
3. Pulse width limited by safe operating area

Table 3. Thermal resistance

Symbol	Parameter	Value	Unit
Rthj-case	Thermal resistance junction-case (drain) Max	1.56	°C/W
Rthj-pcb (1)	Thermal resistance junction-pcb Max	31.3	°C/W

1. When mounted on FR-4 board of 1inch^2, 2 oz. Cu., t<10sec

Table 4. Thermal resistance

Symbol	Parameter	Value	Unit
I_{AV}	Avalanche current, not repetitive (pulse width limited by Tjmax)	10	A
E_{AS}	Single pulse avalanche energy (starting Tj = 25°C, I_D=I_{AV}, V_{DD}=24V)	1.8	J

2 Electrical characteristics

(T_{CASE}=25°C unless otherwise specified)

Table 5. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	I_D = 1mA, V_{GS}= 0	30			V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = 24V			500	µA
I_{GSS}	Gate body leakage current (V_{DS} = 0)	V_{DS} = ± 16V			±100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS}= V_{GS}, I_D = 1mA	1		2.5	V
$R_{DS(on)}$	Static drain-source on resistance	V_{GS}= 10V, I_D= 11A V_{GS}= 4.5V, I_D= 11A		0.0032 0.004	0.0042 0.0057	Ω Ω
		V_{GS}=10V, I_D=11A@125°C V_{GS}=4.5V, I_D=11A@125°C		0.005 0.006		Ω Ω

Table 6. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS}=25V, f = 1MHz, V_{GS}=0		4200 700 46.2		pF pF pF
Q_g Q_{gs} Q_{gd}	Total gate charge Gate-source charge Gate-drain charge	V_{DD} = 15V, I_D = 22A, V_{GS} = 4.5V (see Figure 3)		27 8.5 7.2	35	nC nC nC

Table 7. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$ t_r	Turn-on delay time Rise time	V_{DD} = 15V, I_D = 11A R_G= 4.7Ω, V_{GS}= 10V, (see Figure 2), (see Figure 7)		16 45		ns ns
$t_{d(off)}$ t_f	Turn-off delay time Fall time	V_{DD} = 15V, I_D = 11A R_G= 4.7Ω, V_{GS}= 10V, (see Figure 2) (see Figure 7)		68 8		ns ns

Table 8. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max	Unit
I_{SD} I_{SDM}	Source-drain current Source-drain current (pulsed)				22 88	A A
V_{SD} (1)	Forward on voltage	I_{SD} = 5A, V_{GS} = 0			0.75	V
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	I_{SD} = 22V, di/dt = 100A/µs V_{DD} = 20V, T_j = 25°C (see Figure 4)		30 30 2		ns nC A

1. Pulsed: Pulse duration = 300µs, duty cycle 1.5%

3 Test circuit

Figure 2. Switching times test circuit for resistive load

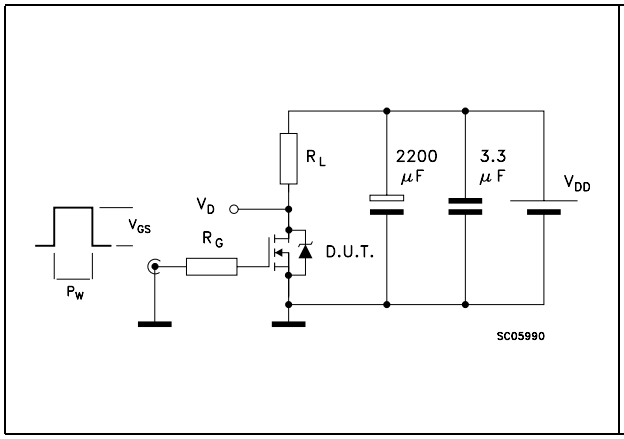


Figure 3. Gate charge test circuit

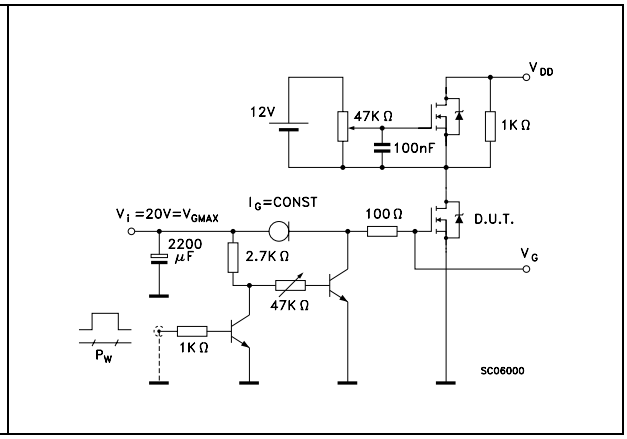


Figure 4. Test circuit for inductive load switching and diode recovery times

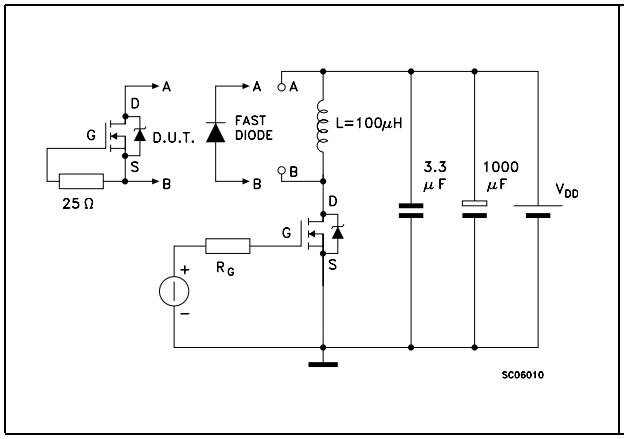


Figure 5. Unclamped inductive load test circuit

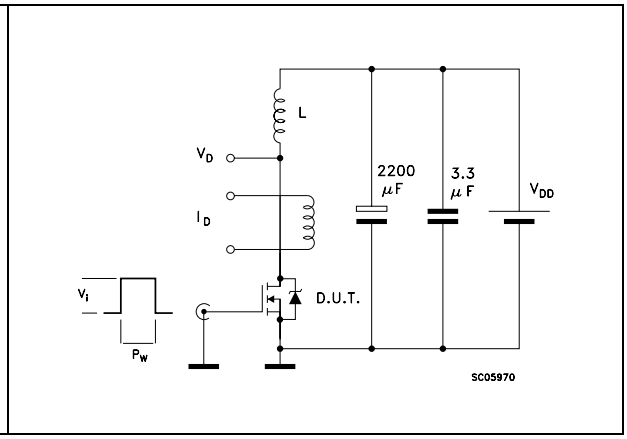


Figure 6. Unclamped inductive waveform

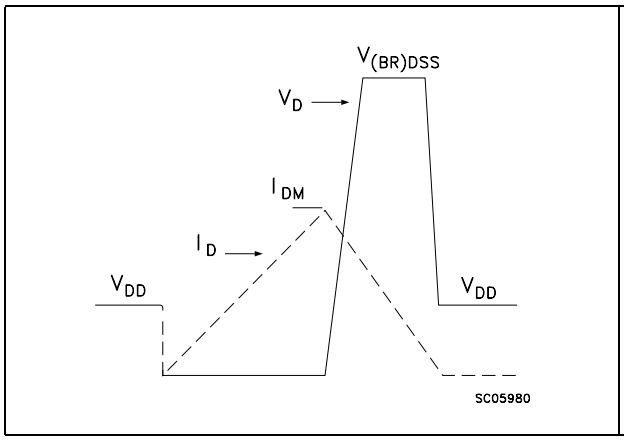
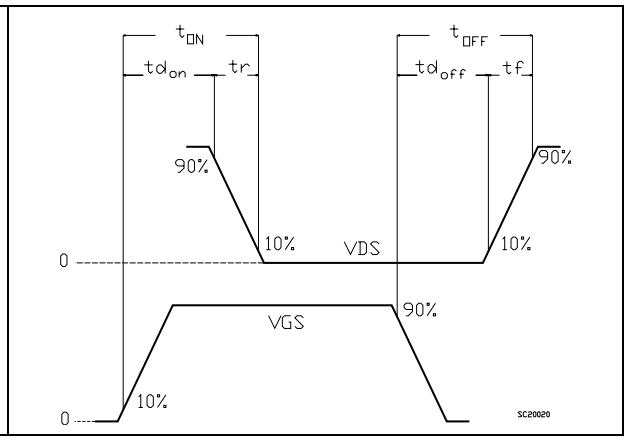


Figure 7. Switching time waveform

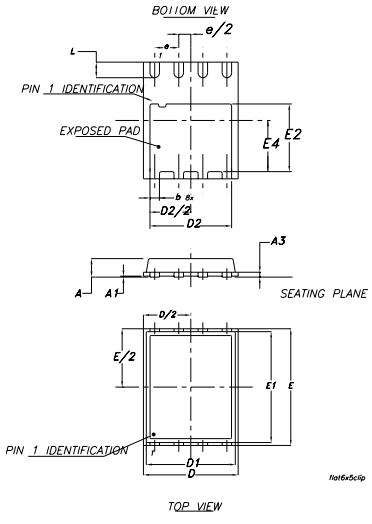


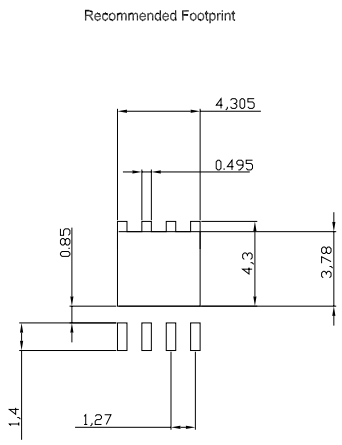
4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: *www.st.com*

PowerFLAT™ (6x5) MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A	0.80	0.83	0.93	0.031	0.032	0.036
A1		0.02	0.05		0.0007	0.0019
A3		0.20			0.007	
b	0.35	0.40	0.47	0.013	0.015	0.018
D		5.00			0.196	
D1		4.75			0.187	
D2	4.15	4.20	4.25	0.163	0.165	0.167
E		6.00			0.236	
E1		5.75			0.226	
E2	3.43	3.48	3.53	0.135	0.137	0.139
E4	2.58	2.63	2.68		0.103	0.105
e		1.27			0.050	
L	0.70	0.80	0.90	0.027	0.031	0.035





Note: all dimentions are in mm.

5 Revision history

Table 9. Document revision history

Date	Revision	Changes
03-Sep-2007	1	First release

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