



# STK391-020

## 2-Channel Convergence Correction Circuit (I<sub>C</sub> max = 6A)

### Overview

The STK391-020 is a convergence correction circuit IC for video projectors. It incorporates two output amplifiers in a single package, making possible the construction of CRT horizontal and vertical convergence correction output circuits for each of the RGB colors using just three hybrid ICs.

### Applications

- Video projectors

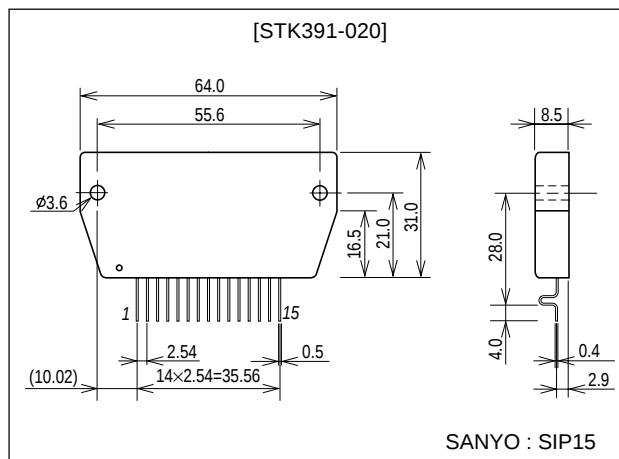
### Features

- 2 output amplifier circuits in a single package
- High maximum supply voltage ( $V_{CC}$  max =  $\pm 44V$ )
- Low thermal resistance ( $\theta_{j-c}=2.7^{\circ}C/W$ )
- High temperature stability (good idling current temperature compensation)
- Low correction coil inductance for improved oscillator stability (up to  $f_H = 64kHz$ )
- Pin compatible with the STK4274 for easy replacement

### Package Dimensions

unit:mm

4062



### Specifications

Maximum Ratings at  $T_a = 25^{\circ}C$ 

| Parameter                 | Symbol         | Conditions                       | Ratings     | Unit          |
|---------------------------|----------------|----------------------------------|-------------|---------------|
| Maximum supply voltage    | $V_{CC}$ max   |                                  | $\pm 44$    | V             |
| Maximum collector current | $I_C$          | Tr9, 11, 20, 22                  | 6.0         | A             |
| Thermal resistance        | $\theta_{j-c}$ | Tr9, 11, 20, 22 (per transistor) | 2.7         | $^{\circ}C/W$ |
| Junction temperature      | $T_j$          |                                  | 150         | $^{\circ}C$   |
| Operating temperature     | $T_c$          |                                  | 105         | $^{\circ}C$   |
| Storage temperature       | $T_{stg}$      |                                  | -30 to +105 | $^{\circ}C$   |

Operating Characteristics at  $T_a = 25^{\circ}C$ ,  $R_g=50\Omega$ ,  $V_{CC}=\pm 24V$ 

| Parameter            | Symbol    | Conditions                                              | Ratings |     |     | Unit    |
|----------------------|-----------|---------------------------------------------------------|---------|-----|-----|---------|
|                      |           |                                                         | min     | typ | max |         |
| Output noise voltage | $V_{NO}$  |                                                         |         |     | 0.2 | mVrms   |
| Quiescent current    | $I_{CCO}$ |                                                         |         | 20  | 40  | mA      |
| Neutral voltage      | $V_N$     |                                                         | -50     | 0   | +50 | mV      |
| Output delay time    | $t_D$     | $f=15.75kHz$ , triangular wave input, $V_{OUT}=1.5Vp-p$ |         |     | 1   | $\mu s$ |

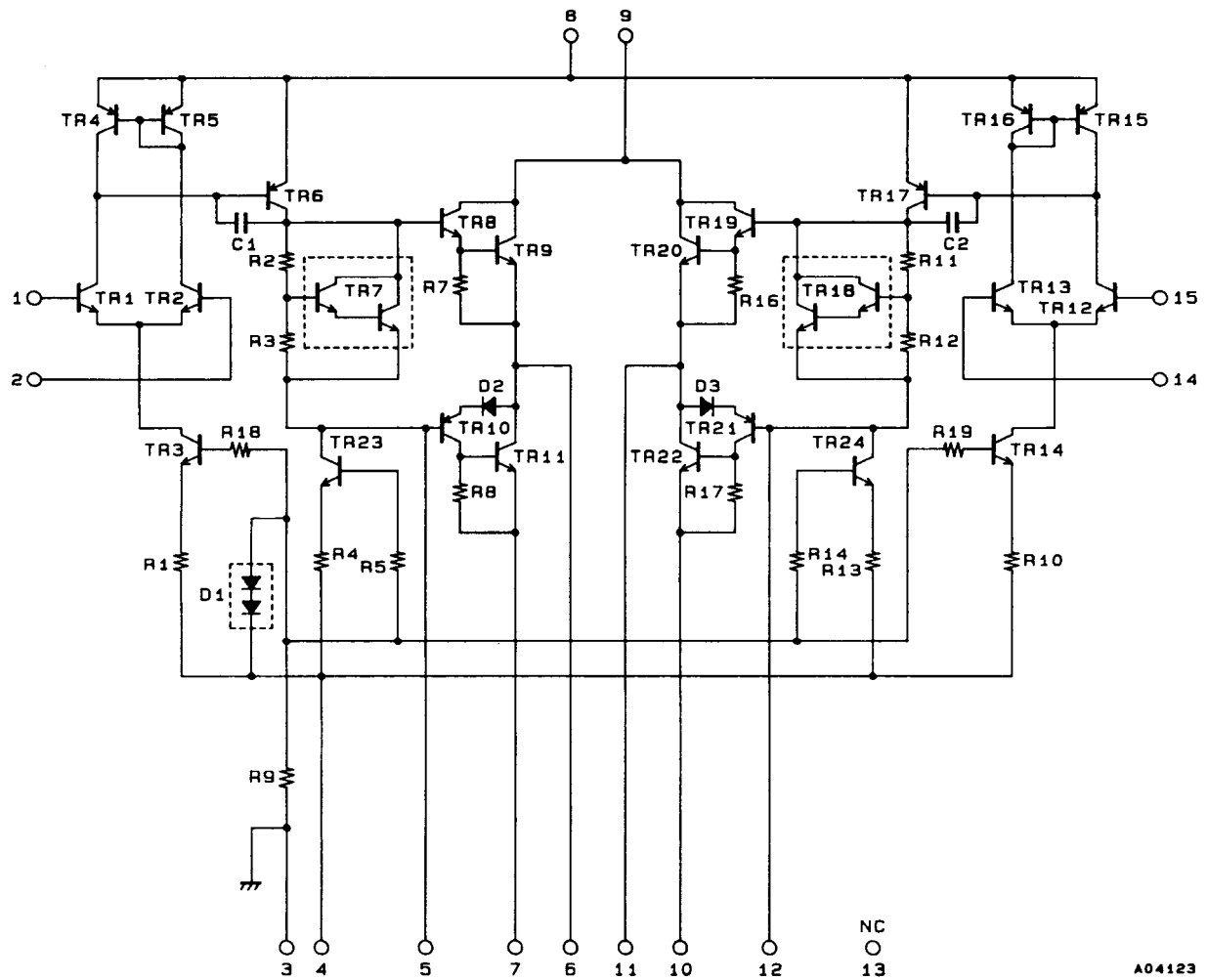
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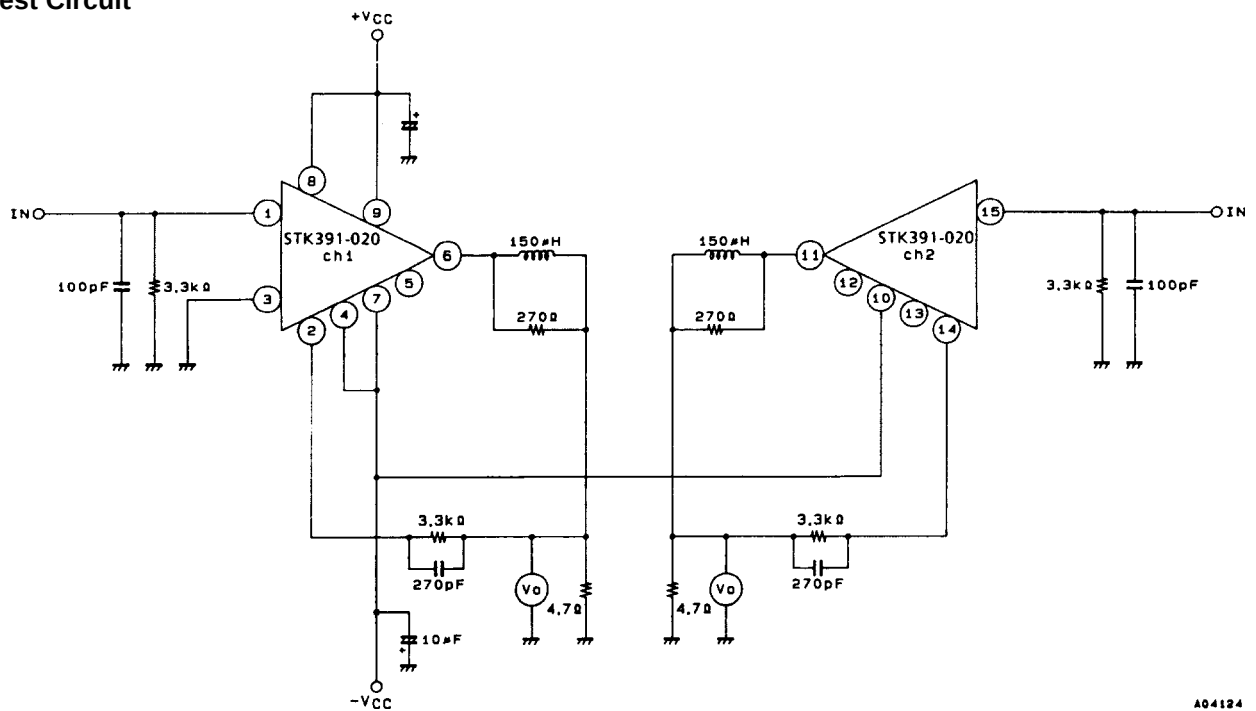
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# Equivalent Circuit



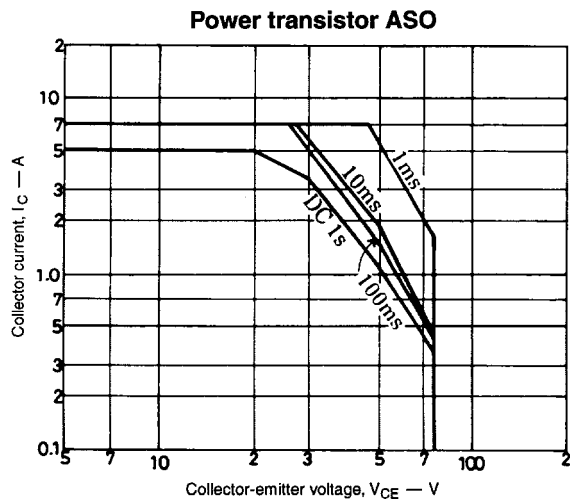
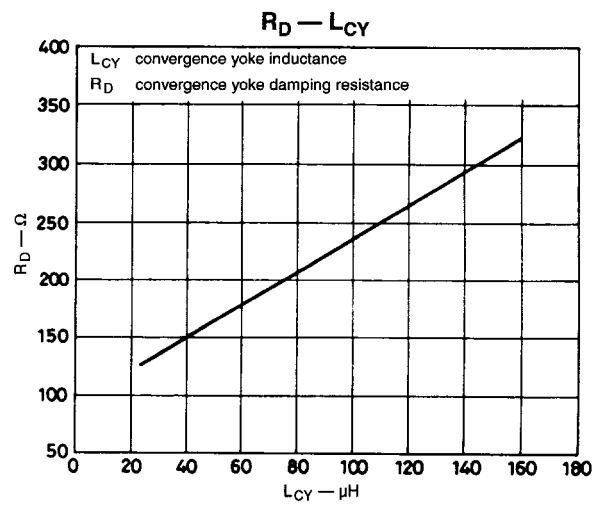
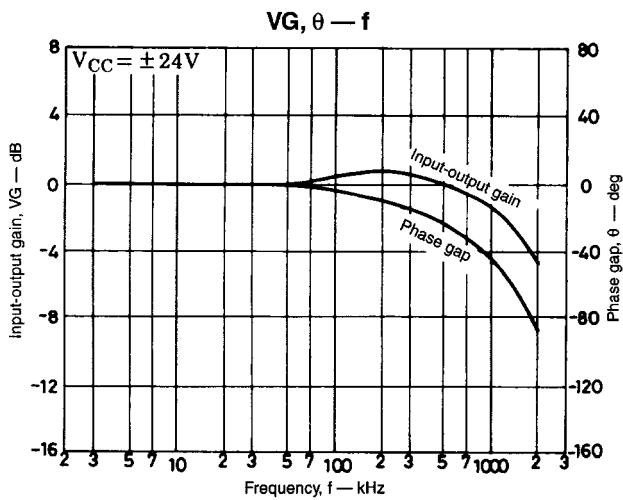
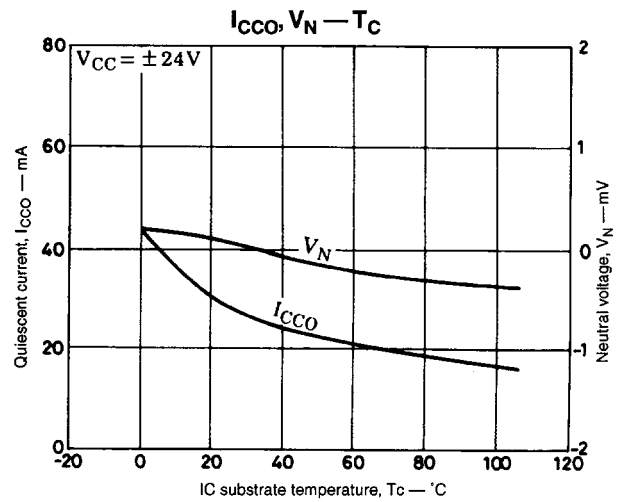
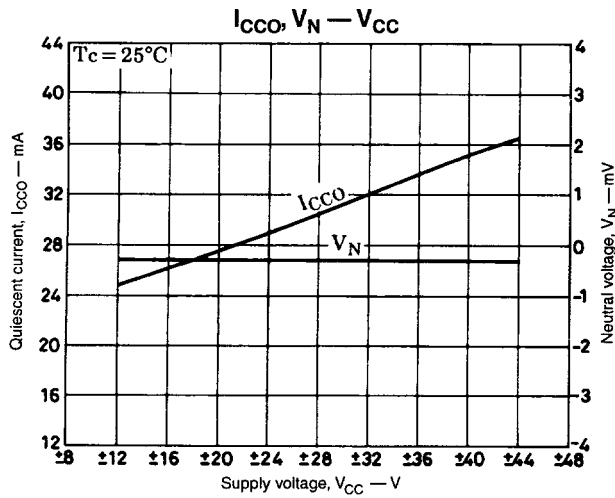
A04123

# Test Circuit



A04124

Vo :  $V_{NO}$  is measured by connecting a VTVM.  
 $V_N$  is measured by connecting a DC voltmeter.  
 $t_D$  is measured by connecting an oscilloscope.



## Maximum Ratings

### T<sub>j</sub> max, T<sub>c</sub> max, θ<sub>j-c</sub>

The heatsink design is determined by the maximum ratings of several key parameters—T<sub>j</sub> max, T<sub>c</sub> max and θ<sub>j-c</sub>.

- T<sub>j</sub> max (junction temperature)  
T<sub>j</sub> max is dependent on the physical structure of each functional element. A junction temperature exceeding this rating can lead to device deterioration and breakdown, so the design must not exceed this rating.
- T<sub>c</sub> max (operating substrate temperature)  
T<sub>c</sub> max is dependent on the materials used within an element and on the circuit design, and should be selected on the basis of reliability. Operation exceeding this value is not guaranteed.
- θ<sub>j-c</sub> (thermal resistance)  
θ<sub>j-c</sub> is dependent on the heatsink design, which can vary greatly. the heatsink necessary is determined by calculation using the maximum rating for T<sub>j</sub>.

As T<sub>j</sub> and T<sub>c</sub> operating conditions are independent, the heatsink must be designed to satisfy the maximum ratings for both parameters.

## Heatsink Design Considerations

In the expressions below P<sub>d</sub> represents the operating IC substrate internal power dissipation and P<sub>c</sub> represents the power dissipation per transistor. The heatsink thermal resistance, θ<sub>c-a</sub>, required to dissipate the total power dissipation, P<sub>d</sub>, is determined as follows :

Condition 1: IC substrate temperature not to exceed 105°C  

$$P_d \times \theta_{c-a} + T_a < 105^\circ\text{C} \quad (\text{T}_c \text{ max}) \quad \dots\dots\dots (1)$$

Where T<sub>a</sub> is the guaranteed maximum ambient temperature.

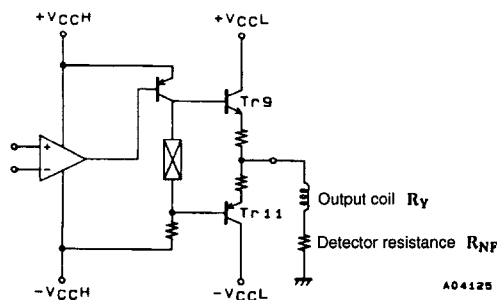
Condition 2: Power transistor junction temperature, T<sub>j</sub>, not to exceed 150°C  

$$P_d \times \theta_{c-a} + P_c \times \theta_{j-c} + T_a < 150^\circ\text{C} \quad (\text{T}_j \text{ max}) \quad \dots\dots\dots (2)$$

Where θ<sub>j-c</sub> is the power transistor thermal resistance per transistor. Therefore, the heatsink design must satisfy both these expression.

## Design Process

A model circuit for a single channel in the STK319-020 is shown below.



The power dissipation, P<sub>d</sub>, is the sum of channel 1, P<sub>d1</sub>, and channel 2, P<sub>d2</sub>, power dissipations.

$$P_d \text{ max} = P_{d1} \text{ max} + P_{d2} \text{ max}$$

Therefore, from equation (1),

$$\theta_{c-a} < \frac{T_c \text{ max} - T_a \text{ max}}{P_d \text{ max}} \quad \dots\dots\dots (3)$$

the necessary heatsink resistance is determined (note that T<sub>c</sub> max=105°C)

The power dissipation per power transistor per channel, P<sub>c</sub>, is related to the transistor junction temperature by the following equation.

$$T_j = P_d \text{ max} \times \theta_{c-a} + T_a + P_c \times \theta_{j-c} \quad \dots\dots\dots (4)$$

where T<sub>j</sub> cannot exceed T<sub>j</sub> max=105°C. Therefore, in order to maintain T<sub>j</sub> below 150°C, a lower heatsink thermal resistance, θ<sub>c-a</sub>, is necessary to lower T<sub>c</sub>.

## Heatsink Design Example

This example assumes the following worst-case conditions—V<sub>CC</sub>H=±35V, V<sub>CC</sub>L=±25V, output coil L<sub>Y</sub>=80μH and R<sub>Y</sub>=0Ω, current detector resistance R<sub>NF</sub>=4.7Ω, I<sub>p-o</sub> max=0.6A<sub>p-o</sub> (I<sub>p-o</sub> (I<sub>p-p</sub>=1.2A) sawtooth wave input, I<sub>o</sub> (DC) max=0.6A DC input, both channels operating, T<sub>a</sub> max=60°C (guaranteed maximum).

The channel1 power dissipation, P<sub>d1</sub>, is given from Figures 1 and 2.

- P<sub>d1</sub> max=7.0W (AC) with sawtooth wave input
- P<sub>d1</sub> max=13.2W (DC) with DC input

As P<sub>d1</sub> max (AC) < P<sub>d1</sub> max (DC), the power dissipation is greater with DC input. Also, looking at the output transistor dissipation, P<sub>c</sub>,

- P<sub>c</sub>=0.5P<sub>d1</sub> with sawtooth wave input
- P<sub>c</sub>=P<sub>d1</sub> with DC input (one side transistor continuously ON)

the power dissipation is also higher with DC input. Accordingly, the heatsink design example below assumes DC input. The power dissipation in the predriver stage is ignored.

As P<sub>d1</sub> max=P<sub>d2</sub> max+13.2W, P<sub>d</sub> max (both channels) is given by.

$$P_d \text{ max} = P_{d1} \text{ max} + P_{d2} \text{ max} = 26.4\text{W}$$

From equation (3) with T<sub>a</sub>=60°C,

$$\theta_{c-a} = \frac{T_c \text{ max} - T_a}{P_d \text{ max}} = \frac{105 - 60}{26.4} = \dots\dots\dots 1.70^\circ\text{C/W}$$

For a 2mm aluminum heatsink with no surface coating, the necessary surface area, S, is given from Figure 3.

$$S = 780\text{cm}^2 \quad (28\text{cm} \times 28\text{cm})$$

Also from equation (4), the output stage power transistor junction temperature is given by

$$\begin{aligned} T_j &= P_{d \max} \times \theta_{c-a} + T_a + P_{c \max} \times \theta_{j-c} \\ &= 26.4 \times 1.7 + 60 + 13.2 \times 2.7 \\ &= 140.5^\circ\text{C} \end{aligned}$$

which provides a  $9.5^\circ\text{C}$  derating below  $T_{j \max} = 150^\circ\text{C}$ . However, an allowance for the predriver stage power dissipation (transistors, resistors, etc.) should also be included in the substrate internal power dissipation,  $P_d$ .

Figure 1.  $P_d$  —  $I_{p-o}$

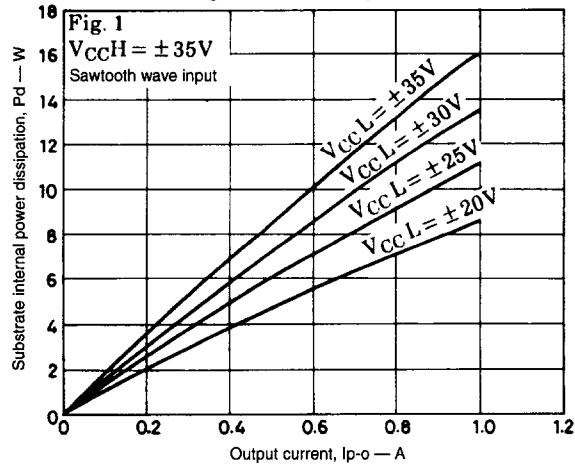


Figure 2.  $P_d$  —  $I_o$

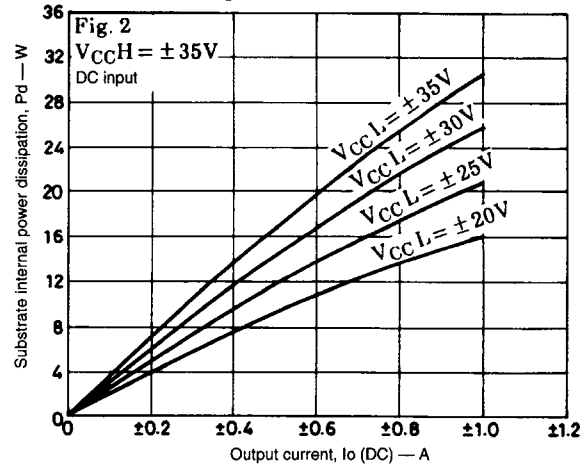
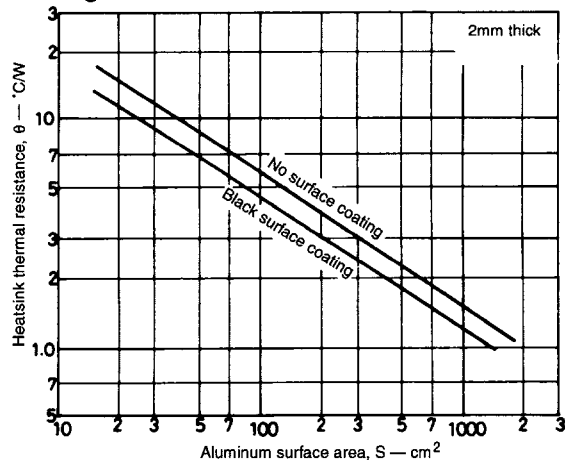


Figure 3. Al heatsink thermal resistance



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