STK3321

Ambient Light Sensor and Proximity Sensor with Built-in IR LED

Preliminary Datasheet

Version - 0.9

Sensortek Technology Corporation

1. OVERVIEW

Description

The STK3321 is an integrated ambient and infrared light to digital converter with a built-in IR LED and I^2C interface. This device provides not only ambient light sensing to allow robust backlight/display brightness control but also infrared sensing to allow proximity estimation featured with interrupt function.

For ambient light sensing, the STK3321 incorporates a photodiode, timing controller and ADC in a single chip. The excellent spectral response is designed to be close-to human eye. The STK3321 is suitable for detecting a wide range of light intensity environment.

For proximity sensing, the STK3321 also incorporates a photodiode, timing controller and ADC in the same chip. The spectral response of STK3321 is optimized for wavelength 940nm infrared light. The STK3321 provides programmable duty setting to drive IR LED and employs a noise cancellation scheme to highly reject unwanted ambient IR noise.

The STK3321 has excellent temperature compensation, robust on-chip refresh rate setting without external components. Software shutdown mode control is provided for power saving application. The STK3321 operating voltage range is 1.7V to 3.6V.

Feature

- Integrated ambient light sensor, proximity sensor and infrared LED in one package.

Proximity Sensor

- 16 bits resolution for proximity detection
- Built-in LED driver with flexible setting
  - LED turn-on time : 16 steps IT x 64 duty cycle options
  - LED current : 12.5 / 25 / 50 / 100 mA
- Flexible interrupt setting
  - Several interrupt modes meet application requirements.
  - Flag modes are included.
  - Interrupt persistence : 1 / 4 times
- Low noise design
- Ambient IR noise cancellation
  - Immunity to 50Hz/60Hz fluorescent light flicker
- 940nm LED for STK3321.

Ambient Light Sensor

- Convert ambient light intensity to 16-bit digital data format
- 3rd generation ambient light sensor which closes to human-eye response and suppress IR portion.
- Flexible digital settings
  - Integration time : 0.2ms~6400ms
- Flexible interrupt setting
  - Interrupt while out-of- window
  - Persistence : 1 / 4 times
- IR sensing mode

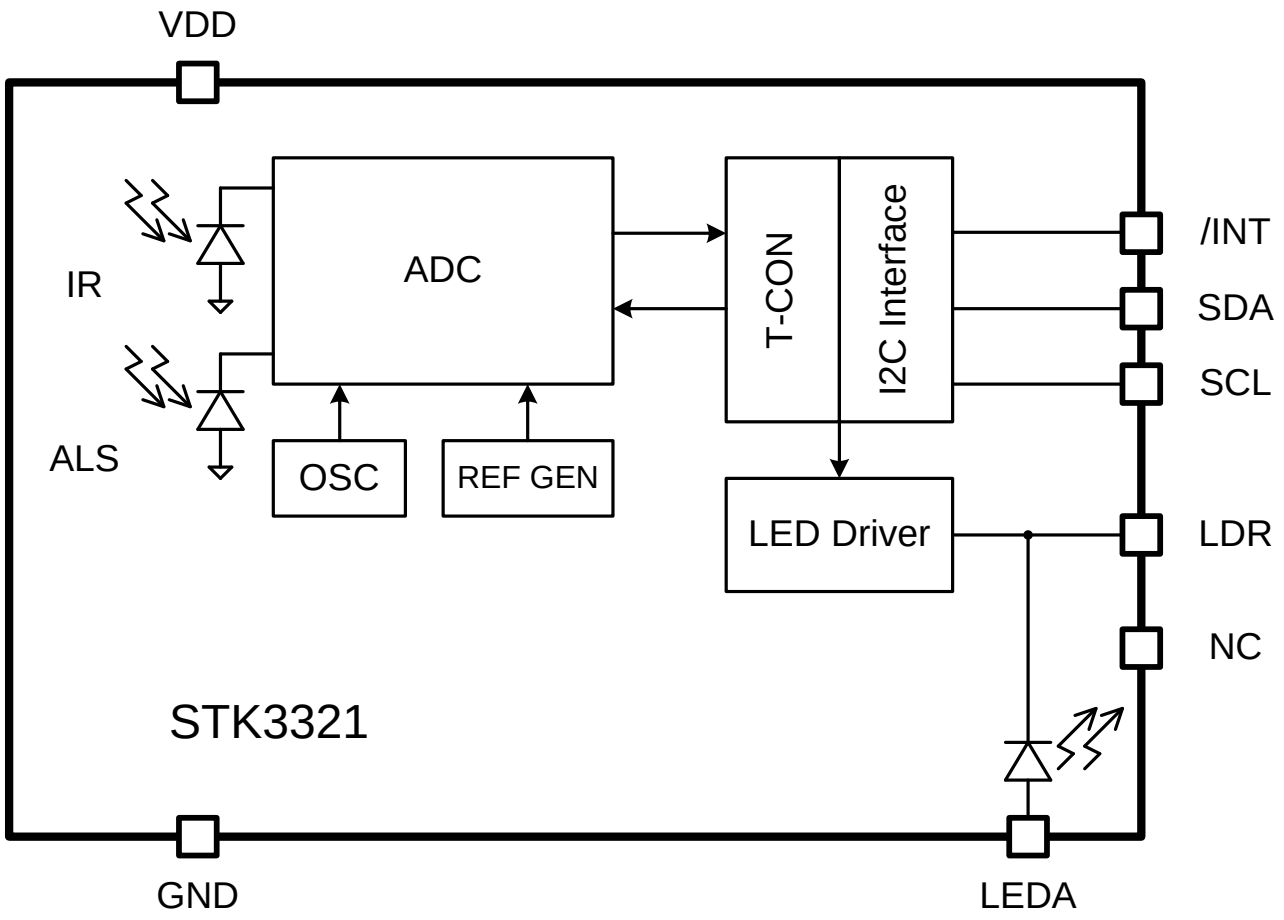
General

- Fully digital control with I^2C interface
  - 1.7 ~ 3.6V I^2C interface
- Low power design
  - Standby mode
  - Wait mode
- Time-multiplexing for sensing
- V_{DD} wide operation voltage : 1.7~3.6V
- Excellent temperature compensation: -40 to 85°C
- Available package options: OLGA
  - STK3321 : 3.94x2.36x1.35 (mm)
- Lead-free package (RoHS compliant)
- Moisture Sensitivity Level 3

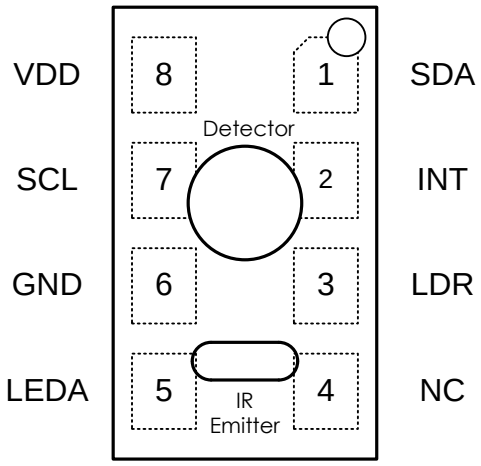
Applications

- Mobile Phone, Smart-phone, PDA

2. FUNCTION BLOCK



3. PINOUT DIAGRAM



STK3321

Top View

4. PIN DESCRIPTION

Pin No.	Pin Name	Dir.	Pin Function
1	SDA	B	I^2C serial data line. (Open Drain)
2	/INT	O	Interrupt pin, LO for interrupt alarming. (Open Drain)
3	LDR	I	IR LED driver pin connecting to the cathode of the external IR LED. The sink current of the IR LED driver can be programmed through I^2C or the external resistor.
4	NC		No Connect.
5	LEDA	I	Anode of the embedded IR LED, connect to power.
6	GND	GND	Ground. The thermal pad is also connected to the GND pin.
7	SCL	I	I^2C serial clock line.
8	VDD	PWR	Power supply: 1.7V to 3.6V.

Direction denotation:

O	Output	GND	Ground
I	Input	B	Bi-direction
PWR	Power	NC	Not Connect

5. ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{DD}	Supply voltage	-0.3	—	3.8	V
V_{LEDA}	Voltage of LED's anode	-0.3	—	4.7	V
V_{LDR}	Voltage of LDR			3.8	V
Ta	Operation temperature	-40	—	85	°C
Ts	Storage temperature	-40	—	85	°C

NOTE: All voltages are measured with respect to GND

Recommended Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{DD}	Supply voltage	1.7	—	3.6	V
V_{LEDA}	Voltage of LED's anode	2.4	—	4.6	V
f_{I2C}	Clock frequency of I^2C	—	—	400	KHz
Ta	Operation temperature	-40	—	85	°C

NOTE: All voltages are measured with respect to GND

Symbol	Parameter	Max.	Unit
ESD	Electrostatic discharge protection	2 (HBM)	kV
		200 (MM)	V
		100 (Latch Up)	mA

NOTE: All voltages are measured with respect to GND

5.1 Electrical and Optical Characteristics

V_{DD} = V_{LED} = 2.8V, under room temperature 25°C (unless otherwise noted)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
Operation Characteristics						
I_{ALS}	ALS only supply current	Note1,2		90		μA
I_{PS}	PS only supply current	Note1,2		100		μA
I_{WAIT}	Supply current at wait state	Note1,2		29		μA
I_{SD}	Shutdown current	Note1,2		0.2	1	μA
V_{IH}	Logic high, I^2C	Note6	1.3		V_{DD}	V
V_{IL}	Logic low, I^2C	Note7	—		0.4	V
ALS Characteristics						
λp_1	Peak sensitivity wavelength for ALS			550		nm
ALS_{FSCNT}	Full scale ALS counts				65535	counts
ALS_{DARK}	ALS dark offset	Note2,3,4		0	3	counts
ALS_{SENSE}	ALS sensing tolerance	Note2,3			±10	%

Proximity Characteristics						
λp_2	High sensitivity wavelength range for PS		800		1000	nm
PS_{FSCNT}	Full scale PS counts				65535	counts
$ILED_{SINK}$	LED sink current	IRDR_LED[1:0] Note5				
		00		12.5		mA
		01		25		mA
		10		50		mA
		11		100		mA
LED_{DUTY}	LED duty adjust steps				64	steps

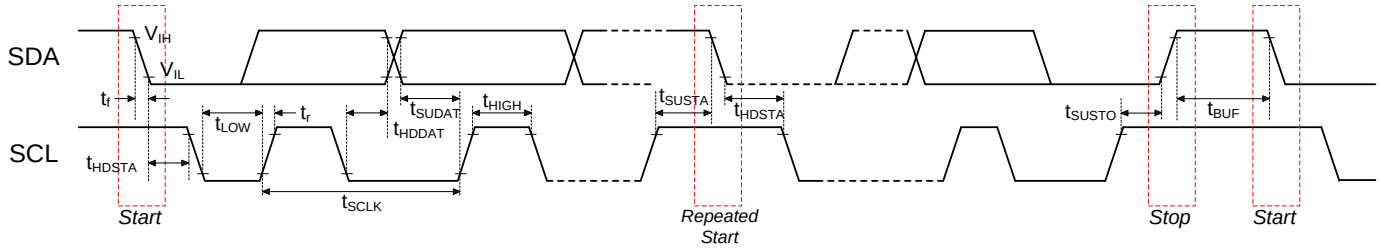
Note 1 : No LED operation.
Note 2 : GAIN_ALS[1:0] = 2'b11, .IT_ALS[3:0] = 4'b1001, GAIN_PS[1:0] = 2'b11, .IT_PS[3:0] = 4'b0001.
Note 3 : White LED parallel light source.
Note 4 : $E_{ambient}$ = 0 Lux.
Note 5 : The voltage of LDR pin is fixed at 1V.
Note 6 : I^2C logical high voltage level is specified as worst-case condition when all of the recommended operation supply voltages (V_{DD}) are taken into consideration. The logical high level is different when different supply voltage is applied.
Note 7 : I^2C logical low voltage level is specified as worst-case condition when all of the recommended operation supply voltages (V_{DD}) are taken into consideration. The logical low level is different when different supply voltage is applied.

5.2 Timing Chart

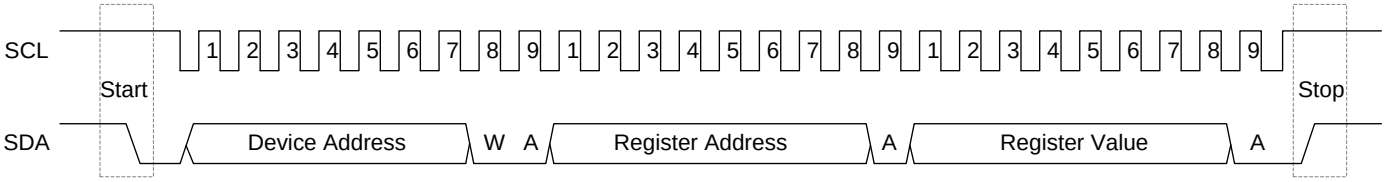
Characteristics of the SDA and SCL I/O

Symbol	Parameter	Standard Mode		Fast Mode		Unit
		Min.	Max.	Min.	Max.	
f_{SCLK}	SCL clock frequency	10	100	10	400	KHz
t_{HDSTA}	Hold time after (repeated) start condition. After this period, the first clock is generated	4.0	—	0.6	—	μs
t_{LOW}	LOW period of the SCL clock	4.7	—	1.3	—	μs
t_{HIGH}	HIGH period of the SCL clock	4.0	—	0.6	—	μs
t_{SUSTA}	Set-up time for a repeated START condition	4.7	—	0.6	—	μs
t_{HDDAT}	Data hold time	0	—	0	—	ns
t_{SUDAT}	Data set-up time	250	—	100	—	ns
t_r	Rise time of both SDA and SCL signals	—	1000	—	300	ns
t_f	Fall time of both SDA and SCL signals	—	300	—	300	ns
t_{SUSTO}	Set-up time for STOP condition	4.0	—	0.6	—	μs
t_{BUF}	Bus free time between a STOP and START condition	4.7	—	1.3	—	μs

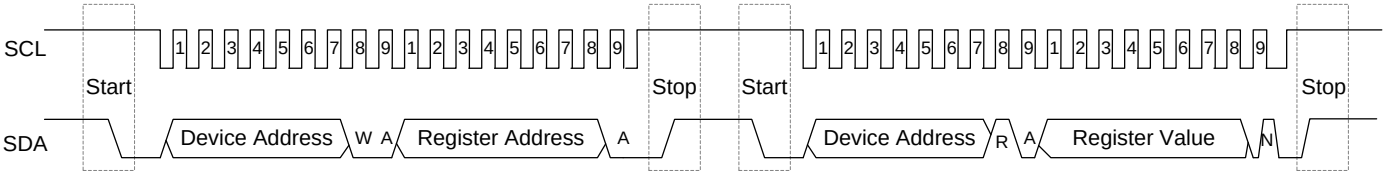
Note 1: f_{SCLK} is the $(t_{SCLK})^{-1}$.



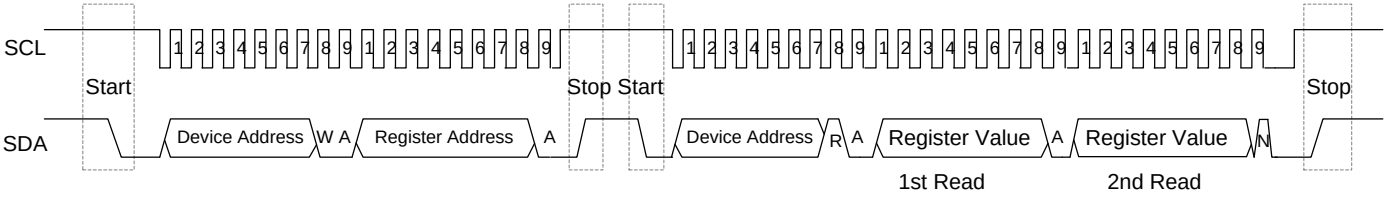
Timing Chart of the SDA and SCL



Write Command



Read Data



Sequential Read Data

6. PRINPICLE OF OPERATION

Digital Interface

STK3321 contains eight-bit registers accessed via the I^2C bus. All operations can be controlled by the command register. The simple command structure makes user easy to program the operation setting and latch the output data from STK3321. Section 5.2 Timing chart displays the STK3321 I^2C command format for reading and writing operation between host and STK3321.

6.1 General Operations

Slave Address

STK3321 provides fixed I^2C slave address of 0x48 using 7 bit addressing protocol.

Slave Address	R/W Command Bit	OPERATION
0x48 (followed by the R/W bit)	0	Write Command to STK3321
	1	Read Data form STK3321

Function Description

ADDR	REG NAME	BIT								Default
		7	6	5	4	3	2	1	0	
00h	STATE	EN_IRS		EN_ASO	EN_IRO		EN_WAIT	EN_ALS	EN_PS	00h
01h	PSCTRL	PRS_PS[1:0]		GAIN_PS[1:0]		IT_PS[3:0]				31h
02h	ALSCTRL	PRS_ALS[1:0]		GAIN_ALS[1:0]		IT_ALS[3:0]				39h
03h	LEDCTRL	IRDR_LED[1:0]		DT_LED[5:0]						FFh
04h	INT	INT_CTRL			INT_OUI	INT_ALS	INT_PS[2:0]			00h
05h	WAIT	WAIT[7:0]								00h
06h	THDH1_PS	THDH_PS[15:8]								FFh
07h	THDH2_PS	THDH_PS[7:0]								FFh
08h	THDL1_PS	THDL_PS[15:8]								00h
09h	THDL2_PS	THDL_PS[7:0]								00h
0Ah	THDH1_ALS	THDH_ALS[15:8]								FFh
0Bh	THDH2_ALS	THDH_ALS[7:0]								FFh
0Ch	THDL1_ALS	THDL_ ALS[15:8]								00h
0Dh	THDL2_ALS	THDL_ ALS[7:0]								00h
10h	FLAG	FLG_ALSDR	FLG_PSDR	FLG_ALSINT	FLG_PSINT		FLG_OUI	FLG_IR_RDY	FLG_NF	01h
11h	DATA1_PS	DATA_PS[15:8]								00h
12h	DATA2_PS	DATA_PS[7:0]								00h
13h	DATA1_ALS	DATA_ALS[15:8]								00h
14h	DATA2_ALS	DATA_ALS[7:0]								00h
15h	DATA1_OFFSET	DATA_OFFSET[15:8]								00h
16h	DATA2_OFFSET	DATA_OFFSET[7:0]								00h
17h	DATA1_IR	DATA_IR[15:8]								00h
18h	DATA2_IR	DATA_ IR[7:0]								00h
3Eh	PDT_ID	0	0	0	1	0	1	0	1	15h
3Fh	Reserved	Reserved								
80h	SOFT_RESET	Write to soft reset								

STATE Register (00h)

1. EN_PS (Bit[0]), EN_ALS (Bit[1]), EN_WAIT (Bit[2]) :
   These bits are used to define what state for the device to be. The operation state flow will be stated later.

BIT [2:0]	Description
000	Standby
001	No Wait Time, Disable ALS, Enable PS
010	No Wait Time, Enable ALS, Disable PS
011	No Wait Time, Enable ALS, Enable PS
100	Not Applied
101	Set Wait Time, Disable ALS, Enable PS
110	Set Wait Time, Enable ALS, Disable PS
111	Set Wait Time, Enable ALS, Enable PS

2. EN_IRO (Bit[4]) :
   To enable (1) / disable (0) Interrupt Run Once function while Interrupt Run Once will be stated in the later section.

3. EN_ASO (Bit[5]) :
   To enable (1) / disable (0) PS DATA stored in register 11h/12h is the result that ADC output subtract offset data stored in register 15h/16h. This is used to cancel the system cross talk (offset).
   ex: DATA_PS[15:0] = DATA_PS_ADC – DATA_OFFSET[15:0] where DATA_PS_ADC is the ADC output while PS conversion is completed.

4. EN_IRS (Bit[7]) :
   To enable (1) / disable (0) IR sensing function. It will update DATA_IR[15:0] (register 17h/18h) once and set FLG_IR_RDY to 1. The IR sensing function is a one-time measurement. If another measure is needed, EN_IRS shall be disabled first and enable. IR sensing and FLG_IR_RDY will be stated in the later section.

PSCTRL Register (01h)

1. IT_PS[3:0] (Bit[3:0]) :
   The refresh time of PS can be tuned by IT_PS[3:0]. Through setting IT_PS[3:0], user could achieve very wide range flexibly in choosing refresh time for different application demand. It is suggested to choose IT_PS time less than 1.56ms to minimize the influence coming from flicker noise. STK3321 takes 2 times of IT_PS to perform proximity sensing. The default value of IT_PS is 0.37ms.

BIT [3:0]	REFRESH TIME	Multiple of Base Refresh Time
0000	0.185 ms (Base Refresh Time)	x 1
0001	0.37 ms	x 2
0010	0.741 ms	x 4
…..	…….	…..
1111	6070 ms	x 32768

2. GAIN_PS[1:0] (Bit[5:4]) :
   The Gain setting for PS sensitivity range is summarized in following table. It is suggested to choose x64 gain setting to get the optimum performance. The default value of GAIN_PS is x64.

BIT [5:4]	Gain
00	x1
01	x4
10	x16
11	x64

3. PRS_PS[1:0] (Bit[7:6]) :

The PS has an interrupt persistence filter. The persistence filter allows user to specify the number of consecutive out-of-threshold PS occurrences before an interrupt is triggered.

BIT [7:6]	Consecutive Out-of-threshold PS Occurrences
00	1 time
01	4 times

ALSCTRL Register (02h)

1. IT_ALS[3:0] (Bit[3:0]) :
The refresh time of ALS can be tuned by IT_ALS. Through setting IT_ALS, user could achieve very wide range flexibly in choosing refresh time for different application demand. The default value of IT_ALS is 94.85ms. (IT_ALS[3:0]=4'b1001)

BIT [3:0]	REFRESH TIME	Multiple of Base Refresh Time	LUX/LSB under GAIN_ALS = 2'b11
0000	0.185 ms	x 1	…..
0001	0.37 ms	x 2	…..
0010	0.741 ms	x 4	$0.027 / 2^{(IT\_ALS[3:0]-9)}$
…..	…….	…..	…..
1000	47.36 ms	x 256	0.054
1001	94.85 ms	x 512	0.027
1010	189.44 ms	x 1024	0.0135
…..	…….	…..	…..
1111	6062 ms	x 32768	…..

2. GAIN_ALS[1:0] (Bit[5:4]) :
The Gain setting for ALS sensitivity range is summarized in following table. It is suggested to choose x64 gain setting to get the optimum performance. The default value of GAIN_ALS is x64.

BIT [5:4]	Gain	LUX/LSB under IT_ALS = 4'b1001
00	x1	1.728
01	x4	0.432
10	x16	0.108
11	x64	0.027

3. PRS_ALS[1:0] (Bit[7:6]) :
The ALS has an interrupt persistence filter. The persistence filter allows user to specify the number of consecutive out-of-threshold ALS occurrences before an interrupt is triggered.

BIT [7:6]	Consecutive Out-of-threshold ALS Occurrences
00	1 time
01	4 times

LEDCTRL Register (03h)

1. DT_LED[5:0] (Bit[5:0]) :
IRLED driving ON-duty (with respect to refresh time) could be adjusted through DT_LED. Through setting DT_LED, IRLED ON-duty period can vary from 1/64 to 64/64 of the set IT_PS time.

For the following example table, when the IT_PS[3:0] = 4'b0000 (PS refresh time is 0.185ms), user may set the IRLED ON-duty period 1/64 of 0.185ms (= 2.89us) by defining DT_LED[5:0] = 6'b000000. By following this, user can choose the desired LED ON-duty period for STK3321.

BIT [5:0]	IRLED ON-Duty Period	IRLED ON-Duty Period under IT_PS = 0000
000000	IT_PS X 1/64	2.89 us
000001	IT_PS X 2/64	5.78 us
……..	….	…….
111111	IT_PS X 64/64	0.185 ms

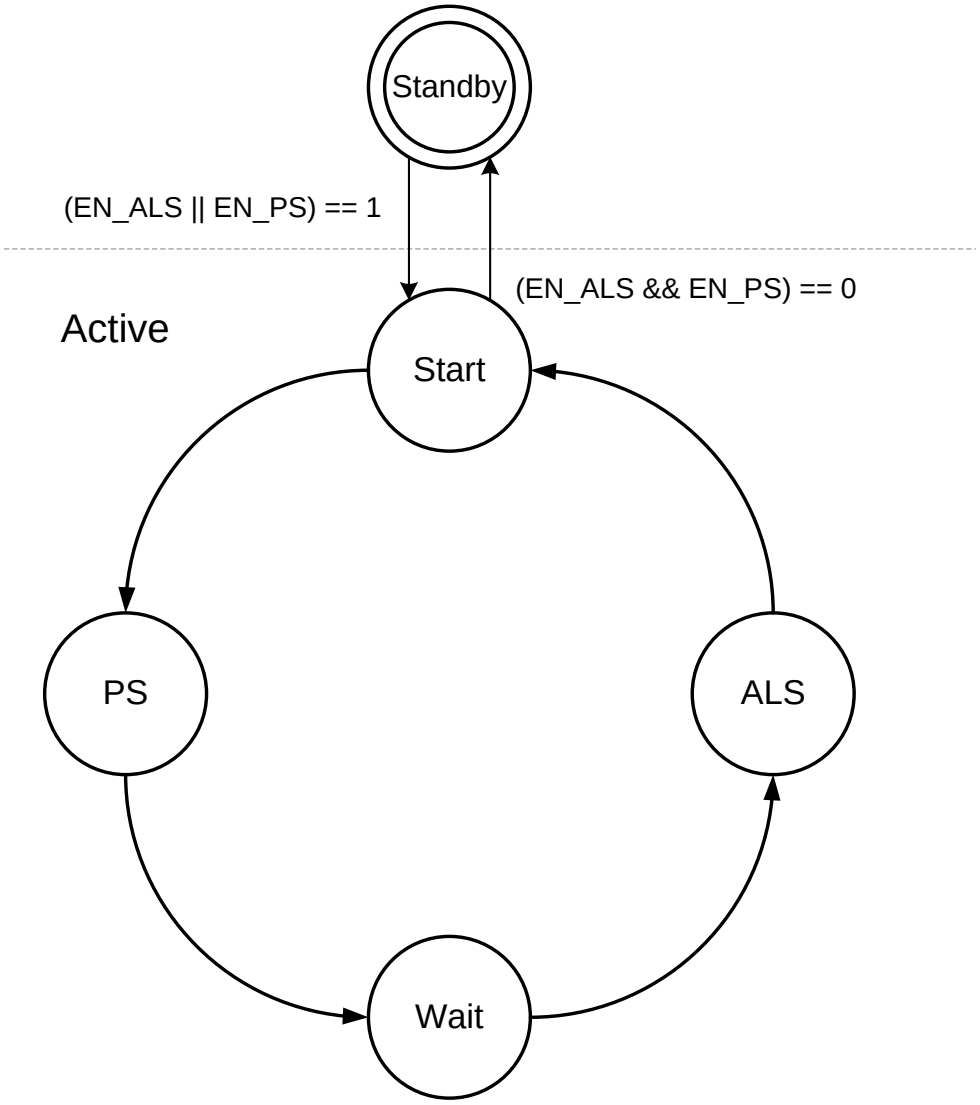
2. IRDR[1:0] (Bit[7:6]) :
The STK3321 provides different driving ability for IRLED through setting IRDR.

BIT [7:6]	IRLED Driving Current
00	12.5mA current sink
01	25mA current sink
10	50mA current sink
11	100mA current sink

System Operation State

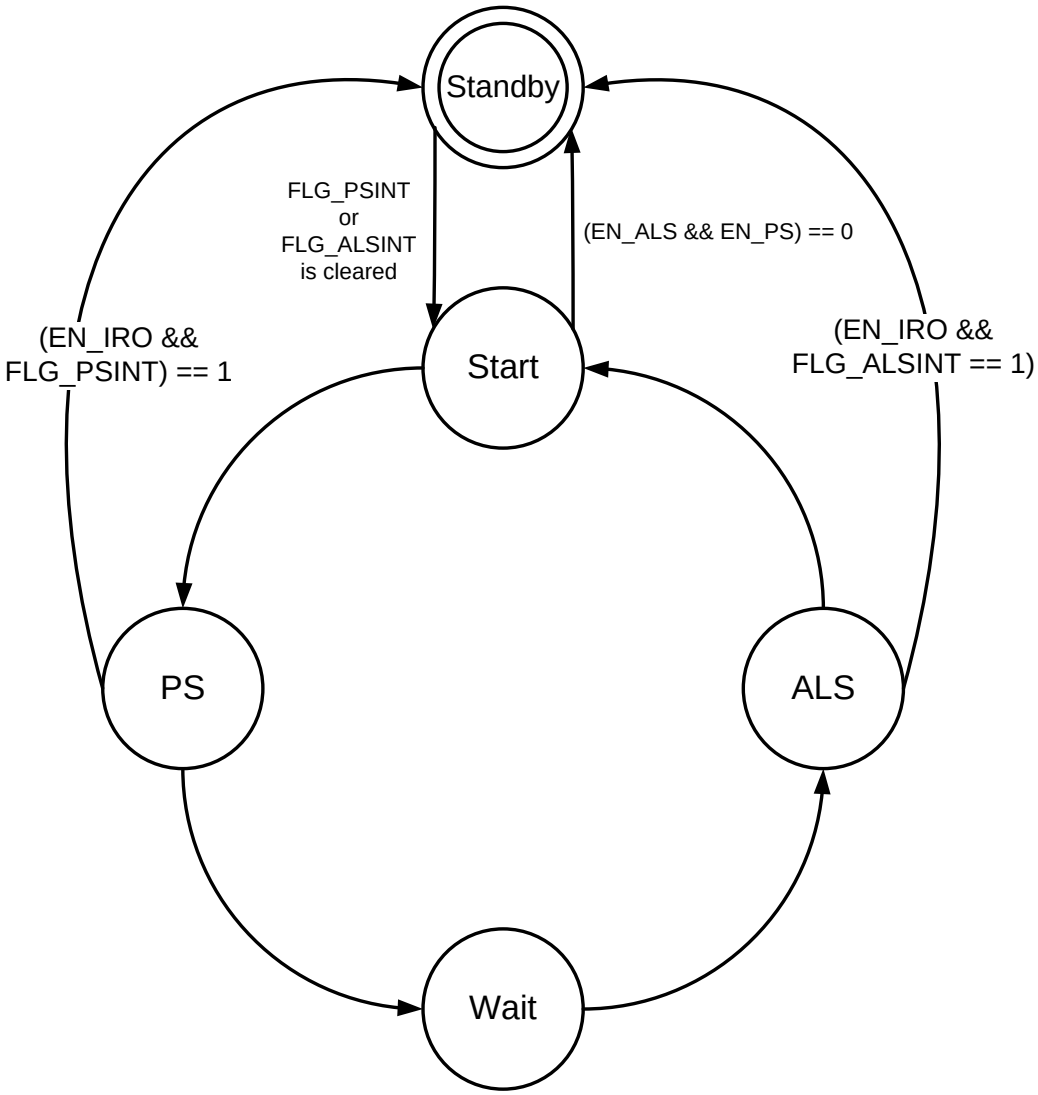
Normal Mode

The STK3321 provides control of ALS, proximity detection, and power management functionality through an internal state machine. After a power-on-reset, the device is in the standby mode. As soon as EN_WAIT or EN_ALS or EN_PS is set to 1, the device will move to the start state. It will then continue go through the PS, Wait, and ALS states cyclic. If these states are enabled, the device will execute each function. If EN_WAIT, EN_ALS or EN_PS is changed during active mode it will jump to start state immediately and remains the data of registers DATA_PS and DATA_ALS without updating. It will go into a low power standby mode again only when EN_WAIT, EN_ALS and EN_PS are all set to 0.



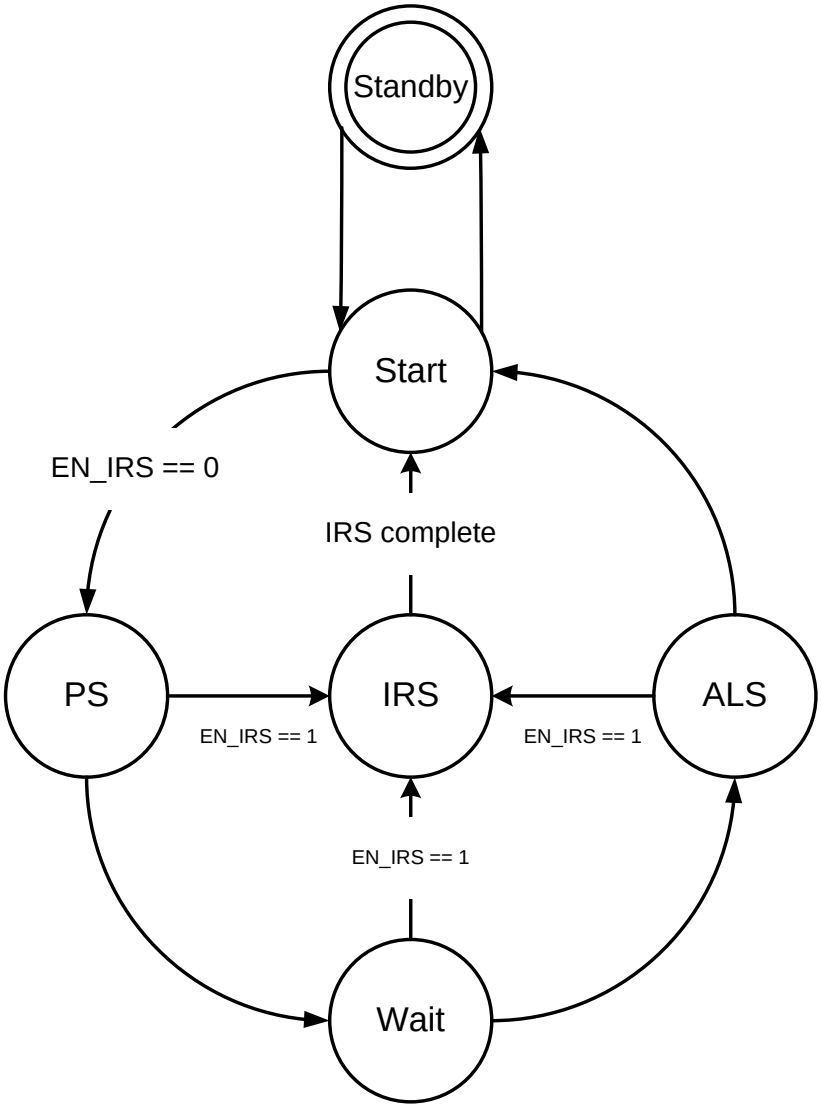
Interrupt Run Once mode

STK3321 is provided IRO mode to save power and simplify system control. While EN_IRO is enabled, the state machine will go to standby mode after PS/ALS interrupt event triggered and IC will stop sensing for saving power. The state machine will leave standby mode once the FLG_PSINT or FLG_ALSINT is cleared. Please see the following state diagram.



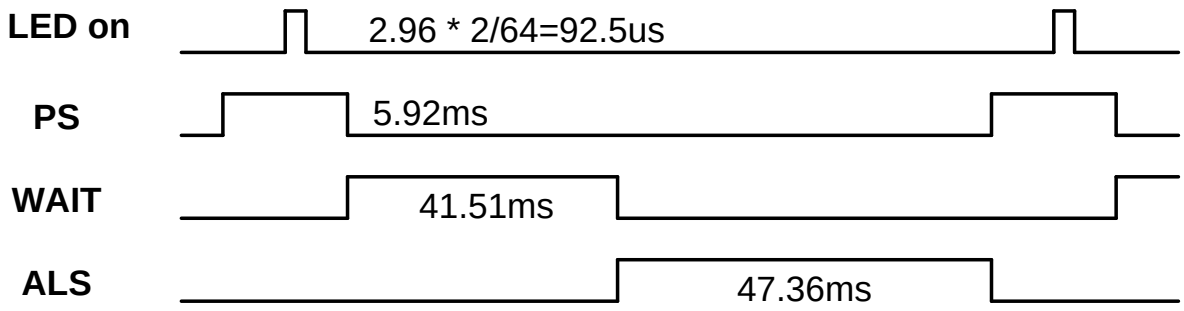
IR Sensing mode

While EN_IRS is set, STK3321 will immediately switch to IR sensing state. The IR sensing function will use the circuit setting of ALS defined in ALSCTRL register to operate the IR sensor to sense incoming light energy in IR range. Once the IR sensing is completed, the DATA_IR[15:0] is updated, EN_IRS bit will be cleared automatically and FLG_IR_RDY bit will be set to 1. The DATA_IR[15:] is not valid until FLG_IR_RDY is set to 1.



Power management

Example: Around 100 ms Cycle Time



State	Duration (ms)	Current (mA)
LED on	2.96 * 2/64	100.0
PS	5.92	0.100
WAIT	41.51	0.029
ALS	47.36	0.09

Avg = ((2.96*2/64*100)+(5.92*0.1)+(41.51*0.029)+(47.36*0.09))/95= 161.10uA

INT Register (04h)

1. INT_PS[2:0] (Bit[2:0]) :
   INT_PS programs interrupt occurrence criteria for PS.

BIT [2:0]	OPERATION
000	PS INT Disable
001	PS INT Enable, interrupt is issued while FLG_NF is toggled. FLG_NF is defined at bit0 of FLAG Register (10h) to indicate the PS state is near or far.
010	/INT is treated as a flag and not an interrupt. /INT = 1 if DATA_PS[15:0] > THDH_PS[15:0] and /INT = 0 if DATA_PS[15:0] < THDL_PS[15:0].
011	/INT is treated as a flag and not an interrupt. /INT = 0 if DATA_PS[15:0] > THDH_PS[15:0] and /INT = 1 if DATA_PS[15:0] < THDL_PS[15:0].
100	PS INT Enable, interrupt according to system pre-defined sequence. Refer to the following description.
101	PS INT Enable, interrupt only if the PS Data value is higher than THDH_PS[15:0].
110	PS INT Enable, interrupt only if the PS Data value is lower than THDL_PS[15:0].
111	PS INT Enable, interrupt if the PS Data value is higher than THDH_PS[15:0] or the PS Data value is lower than THDL_PS[15:0]. Threshold hystersis is not applied.

FLAG mode

While INT_PS[2:0] is set to 3'b010 or 3'b011. The /INT pin is intended to be used as flag to indicate if any object is proximity to the sensor or not. The MCU or application processor just reads the value of the /INT pin to recognize the state without access the I^2C interface. /INT can not be cleared by host's access.

If the /INT pin is used as flag, the other interrupt event should be disabled. Usually, the polling mode is used for ambient light sensor while /INT is used as flag of proximity sensing.

Interrupt mode

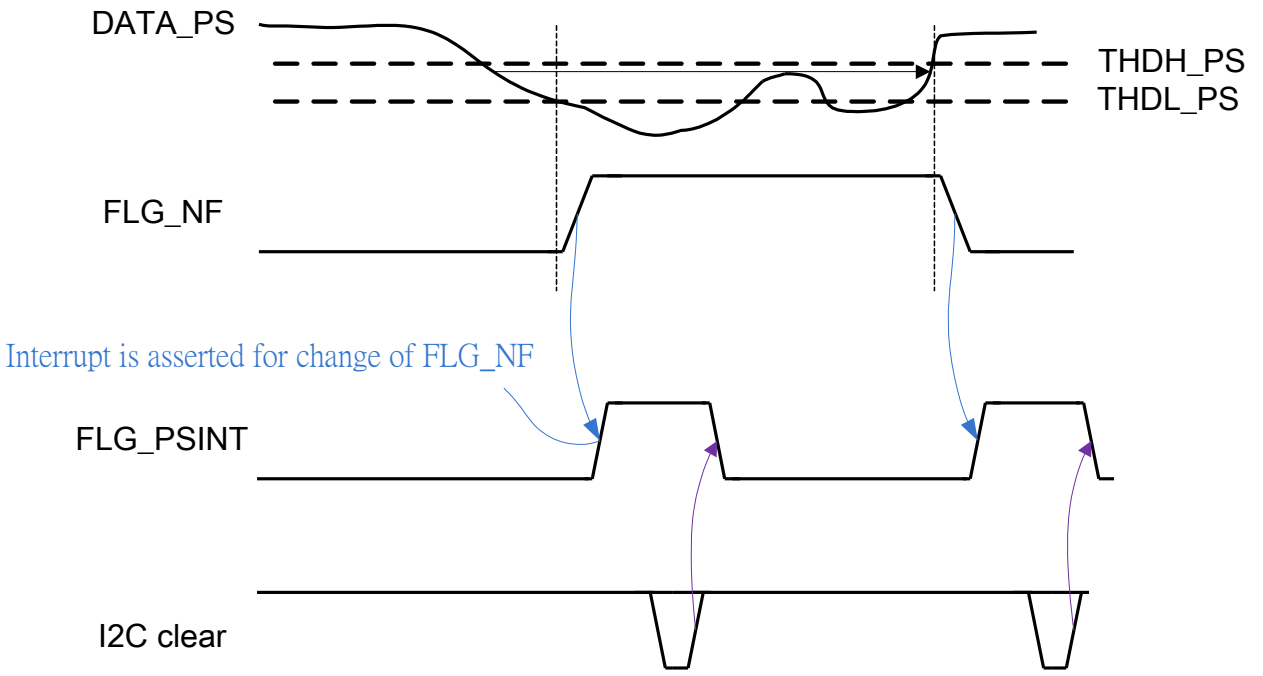
/INT is treated as interrupt signal when INT_PS[2:0] other than flag mode are selected. In these modes, the other interrupt source can share the same /INT pin to issue the interrupt event to host.

Out-of-Threshold interrupt mode

While INT_PS[2:0] is set to 3'b101/3'b110/3'b111, it is so-called "out-of-threshold interrupt". This interrupt scheme will issue continuous interrupt while the PS_DATA is higher or lower the threshold defined by THDH_PS[15:0] / THDL_PS[15:0].

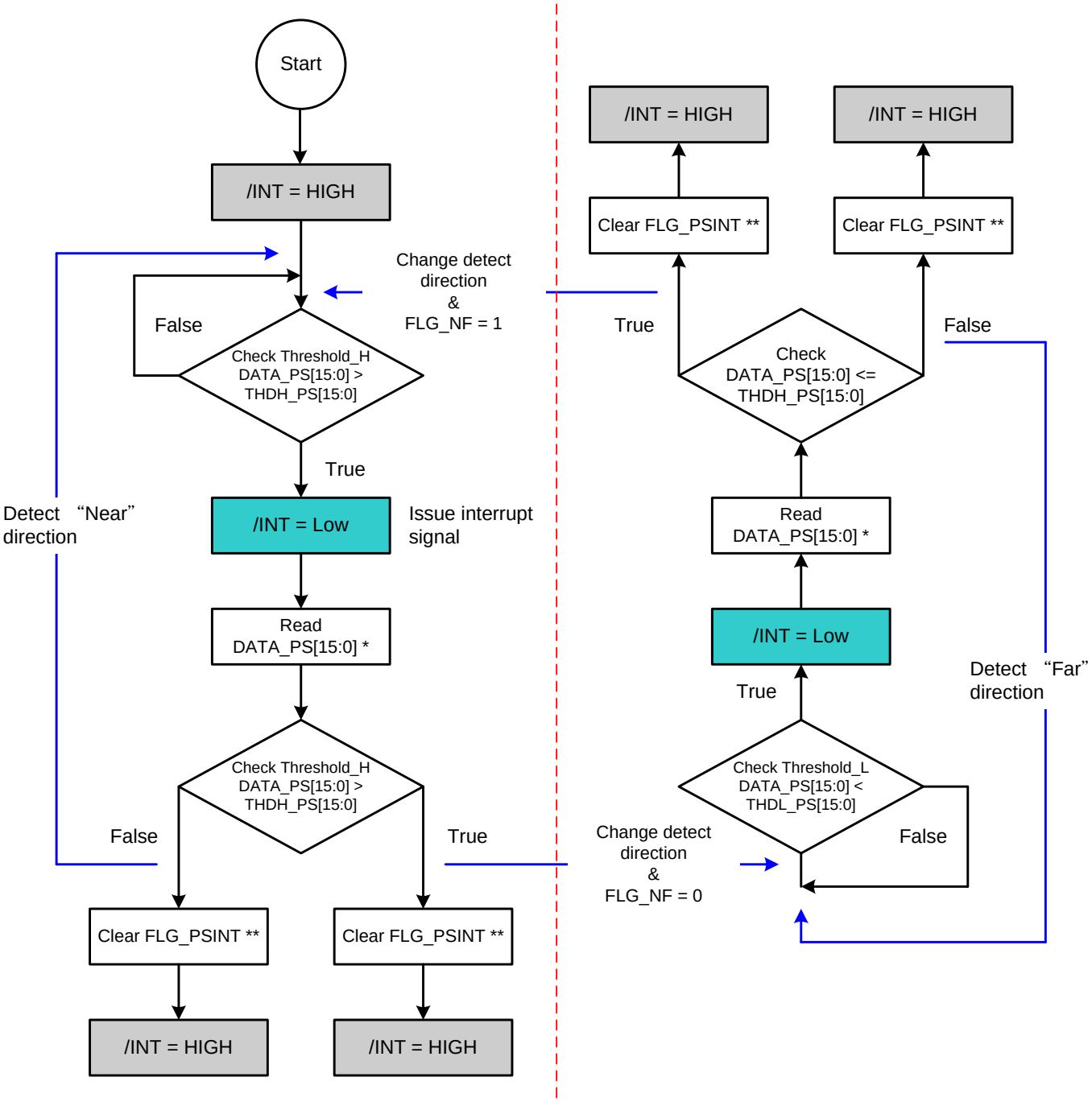
Recommended interrupt mode

The INT_PS[2:0] = 3'b001 is a new scheme which reduces the software's effort. The /INT is asserted only when proximity state (FLG_NF) is transient. Host just needs to handle the proximity sensor while /INT is asserted and no extra handling for interrupt.



Compatible interrupt mode

While INT_PS[2:0] = 3'b100, the interrupt mode is compatible with STK3171, STK3101 and STK3128. System pre-defined sequence is used to assert interrupt signal. Refer to the following state diagram.



Note : * read DATA_PS is driver's behavior and it will trigger IC's next action.
** clear FLG_PSINT is driver's behavior and it will let /INT pin = HIGH

2. INT_ALS (Bit[3]) :
INT_ALS = 0, disable ALS interrupt. INT_ALS = 1, enable ALS interrupt. STK3321 will issue an ALS interrupt if the actual count DATA_ALS are outside the user's programmed window defined in THDH_ALS and THDL_ALS. The user must write 0 to clear FLG_ALSINT

BIT 3	OPERATION
0	ALS interrupt Disable
1	ALS interrupt Enable

3. INT_CTRL (Bit[7]) :
This bit is used to control the interrupt mode.

BIT 7	OPERATION
0	Set /INT pin low if FLG_ALSINT or FLG_PSINT high (logical OR)
1	Set /INT pin low if FLG_ALSINT and FLG_PSINT high (logical AND)

WAIT Register (05h)

1. WAIT[7:0] (Bit[7:0]) :
The wait time among every PS and ALS operation can be adjusted via I^2C. The following table lists the possible values of wait time.

BIT [7:0]	WAIT TIME
00h	5.93 ms; wait time among every PS and ALS operation is 5.93 ms
01h	11.9 ms; wait time among every PS and ALS operation is 11.9 ms
02h	17.8 ms; wait time among every PS and ALS operation is 17.8 ms
…….	…….
FFh	1518 ms; wait time among every PS and ALS operation is 1518 ms

PS Threshold Register (06h, 07h, 08h ,09h)

A proximity interrupt event (FLG_PSINT) is governed by the high and low thresholds in register 06h, 07h, 08h and 09h respectively. The user write a high and low threshold value to these registers and the STK3321 will issue an PS interrupt depends on setting of INT_PS[2:0].

ALS Threshold Register (0Ah, 0Bh, 0Ch ,0Dh)

An ALS interrupt event (FLG_ALSINT) is governed by the high and low thresholds in register 0Ah, 0Bh, 0Ch and 0Dh respectively. The user write a high and low threshold value to these registers and the STK3321 will issue an ALS interrupt if the actual count DATA_ALS stored in registers 13h and 14h are outside the user's programmed window.

FLAG Register (10h)

1. FLG_NF (Bit[0]) :
The definition of FLG_NF depends on the setting of INT_PS[2:0].

INT_PS[2:0]	FLG_NF
000	Unused. FLG_NF is fixed to 1.
001	FLG_NF is 0 if object in near to sensor and FLG_NF is 1 if object is far to sensor. Refer to INT_PS[2:0] = 3'b001 in previous description.
010	FLG_NF is 0 if object in near to sensor and FLG_NF is 1 if object is far to sensor.
011	FLG_NF is 0 if object in near to sensor and FLG_NF is 1 if object is far to sensor.
100	FLG_NF is 0 if STK3321 detection direction is object move from near side to far side. FLG_NF is 1 if STK3321 detection direction is object move from far side to near side.
101	Unused. FLG_NF is fixed to 1.

110	Unused. FLG_NF is fixed to 1.
111	Unused. FLG_NF is fixed to 1.

2. FLG_IR_RDY (Bit[1]) :
FLG_IR_RDY default is 0 and will change to be 1 after IR sensing data updated. FLG_IR_RDY need to be cleared to 0 manually.

3. FLG_PSINT (Bit[4]) :
PS Interrupt flag. This is the status bit of the interrupt for PS. The bit is set to logic high when the interrupt thresholds have been triggered, and logic low when not yet triggered. Once triggered, /INT pin stays low and the status bit stays high. Both interrupt pin and the status bit are cleared by writing “0”.

BIT 4	OPERATION
0	Interrupt is cleared or not triggered yet
1	Interrupt is triggered

4. FLG_ALSINT (Bit[5]) :
ALS Interrupt flag. This is the status bit of the interrupt for ALS. The bit is set to logic high when the interrupt thresholds have been triggered, and logic low when not yet triggered. Once triggered, /INT pin stays low and the status bit stays high. Both interrupt pin and the status bit are cleared by writing “0”.

BIT 5	OPERATION
0	Interrupt is cleared or not triggered yet.
1	Interrupt is triggered.

5. FLG_PSDR (Bit[6]) :
PS Data Ready Flag. This flag is used to confirm whether the PS data in the PS data registers are read or not. The bit will be 1 when the refreshed data is not read. The bit is automatically cleared to zero by STK3321 after the PS data registers are read.

6. FLG_ALSDR (Bit[7]) :
ALS Data Ready Flag. This flag is used to confirm whether the ALS data in the ALS data registers are read or not. The bit will be 1 when the refreshed data is not read. The bit is cleared to zero after the ALS data registers are read.

PS Data Register (11 and 12 hex)
The STK3321 has two 8-bit read-only registers to hold the data from ADC of PS. The most significant bit (MSB) is accessed at register 11h, and the least significant bit (LSB) is accessed at register 12h. For 16-bit resolution, the data is from DATA_PS[15:0]. The registers are updated for every PS refresh time (conversion cycle).

ALS Data Register (13h and 14h)
The STK3321 has two 8-bit read-only registers to hold the data from ADC of ALS. The most significant bit (MSB) is accessed at register 13h, and the least significant bit (LSB) is accessed at register 14h. For 16-bit resolution, the data is from DATA_ALS[15:0]. The registers are updated for every ALS refresh time (conversion cycle).

Data Offset Register (15h and 16h)
Please refer to the description in state register (00h).

Data IR Register (17h and 18h)
Please refer to the description in state register (00h).

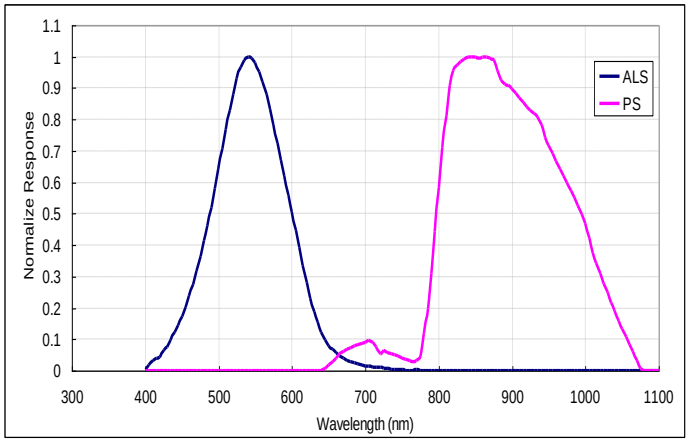
Product ID (3Eh)
Read Only; PDT_ID = Product ID to indicate the product information.

Reserved (3Fh)
Read Only; RSRVD = Reserved for engineering mode.

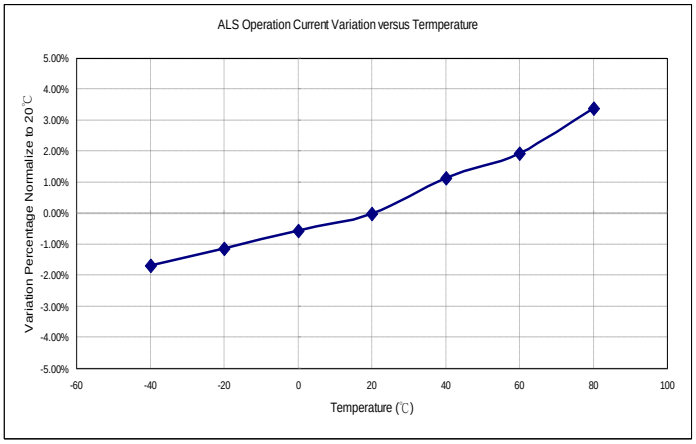
Soft reset (80h)

Write any data to this register will reset the chip.

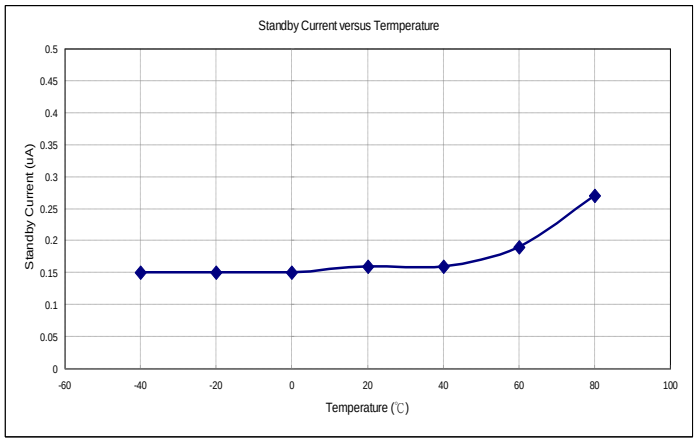
7. ALS RESPONSE CHARTS



Spectral Response

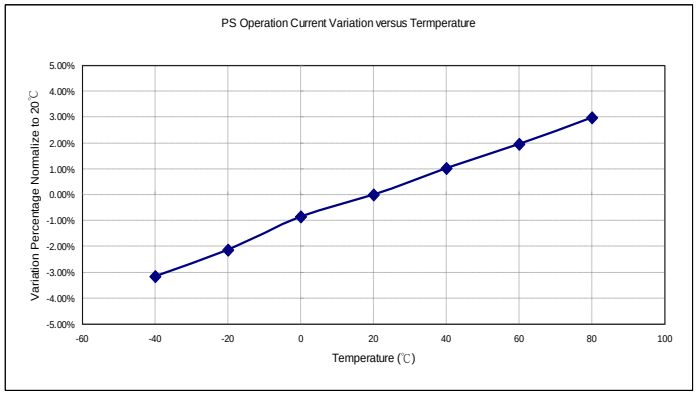


ALS I_{ACT} Variation versus Temperature
@ VDD = 2.8V, Halogen, ALS-IT = 94.85ms



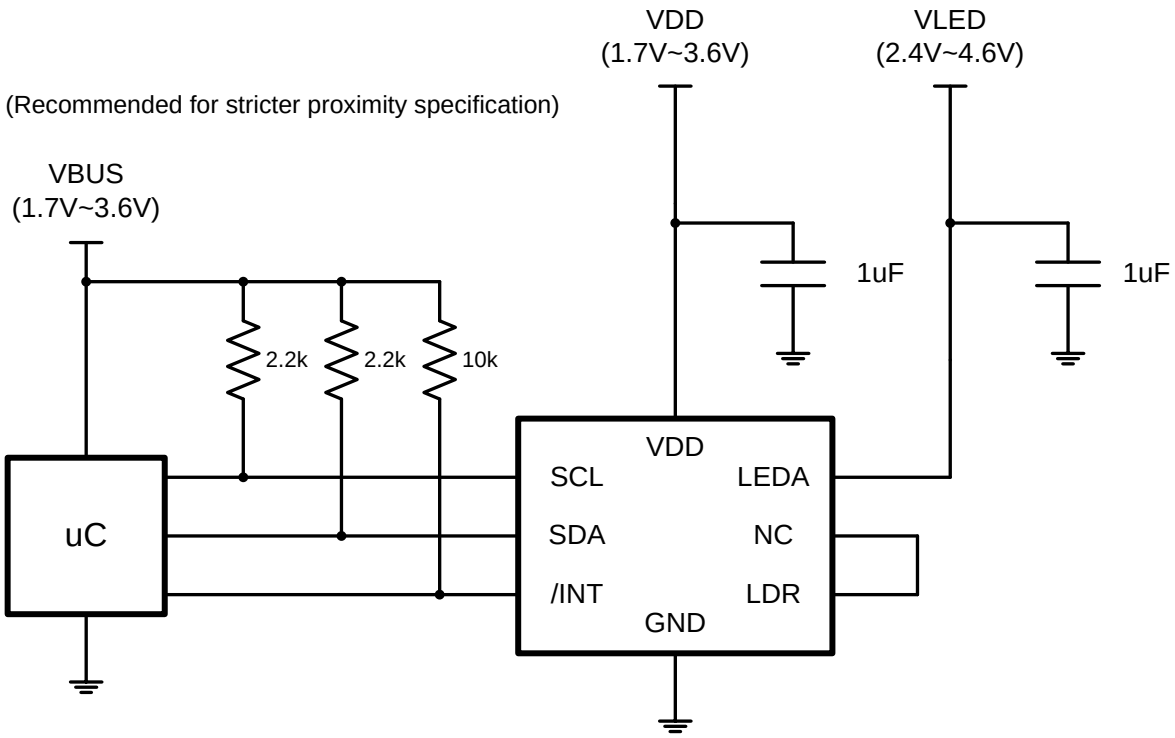
I_{SD} versus Temperature @ VDD = 2.8V, Halogen

8. PROXIMITY CHARACTERISTIC

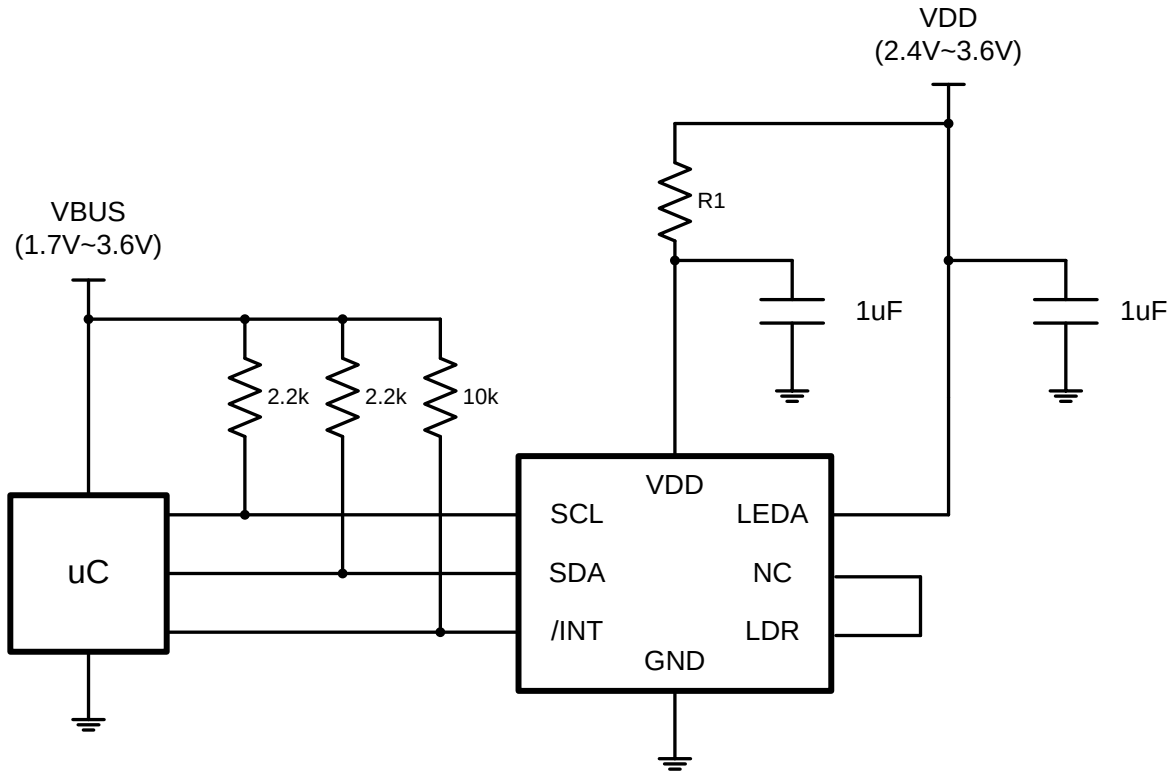


PS I_{ACT} Variation versus Temperature @ VDD = 2.8V, LED Driver Current = 100mA, PS-IT = 370us

9. APPLICATION NOTE



STK3321 Typical Application Circuit with Independent VDD and VLED Supply Voltage



STK3321 Typical Application Circuit with Only One Supply Voltage

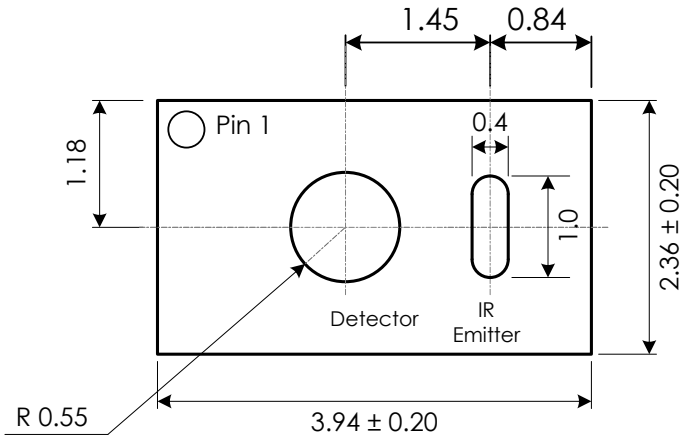
9.1 Power Noise Consideration

In order to reduce the switching noise come from the V_{LED}, it is suggested that IC power and V_{LED} comes from individual source to get the best performance of STK3321. If IC power and V_{LED} must be tied together due to system consideration, an R/C low pass filter should be added in the V_{DD} path of STK3321 to reduce the switching noise from V_{LED}. The recommended R1 value is 22 Ohm.

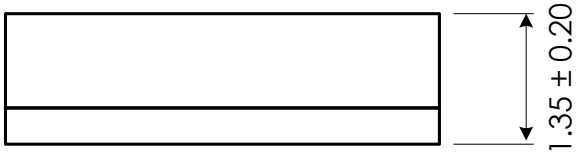
10. PACKAGE OUTLINE

STK3321

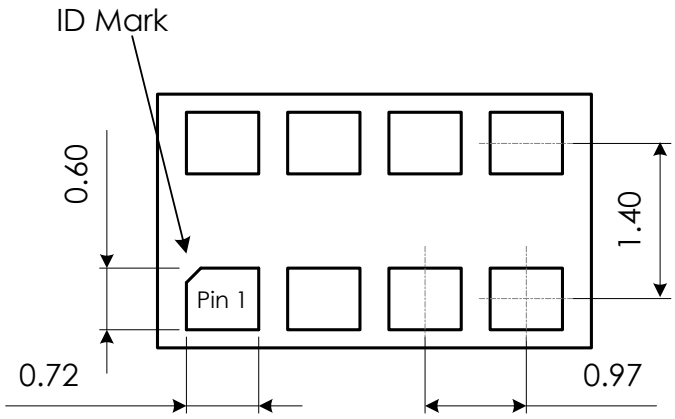
Top View



Side View



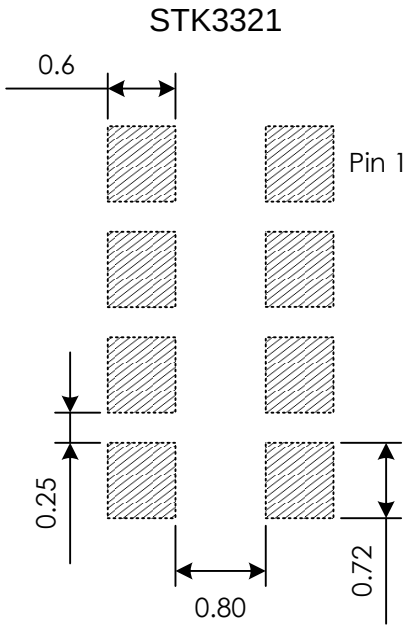
Bottom View

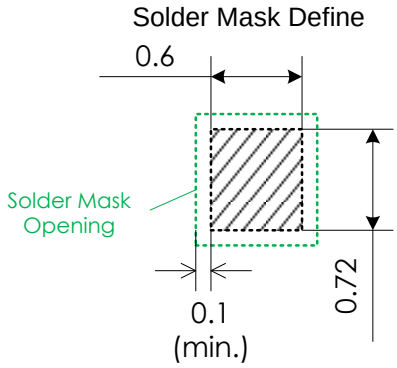


Dimension in Millimeters (mm)

PCB Pad Layout and Solder Mask Define Recommendation

Suggested PCB pad layout guidelines for the Dual Flat No-Lead surface mount package are shown below.



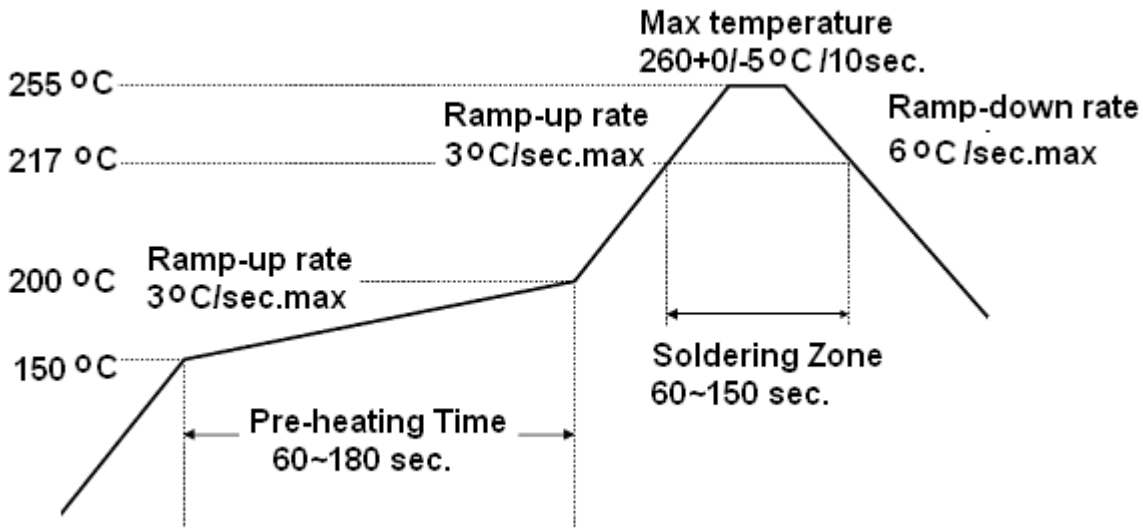


Notes: all linear dimensions are in mm.

11. SOLDERING INFORMATION

11.1 Soldering Condition

1. Pb-free solder temperature profile



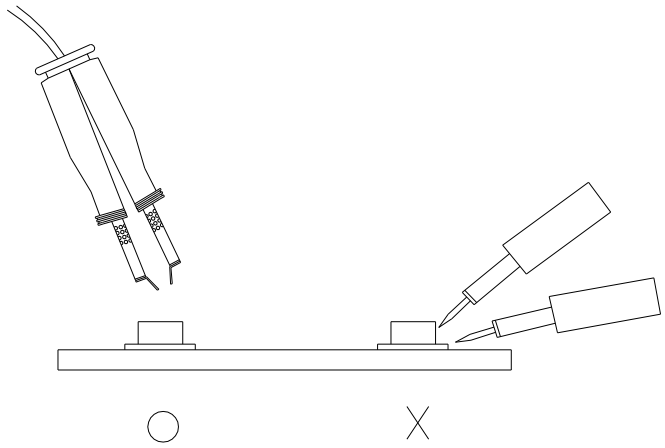
2. Reflow soldering should not be done more than three times.
3. When soldering, do not put stress on the ICs during heating.
4. After soldering, do not warp the circuit board.

11.2 Soldering Iron

Each terminal is to go to the tip of soldering iron temperature less than 350°C for 3 seconds within once in less than the soldering iron capacity 25W. Leave two seconds and more intervals, and do soldering of each terminal. Be careful because the damage of the product is often started at the time of the hand solder.

11.3 Repairing

Repair should not be done after the Ics have been soldered. When repairing is unavoidable, a double-head soldering iron should be used (as below figure). It should be confirmed beforehand whether the characteristics of the Ics will or will not be damaged by repairing.



12. STORAGE INFORMATION

12.1 Storage Condition

1. Devices are packed in moisture barrier bags (MBB) to prevent the products from moisture absorption during transportation and storage. Each bag contains a desiccant.
2. The delivery product should be stored with the conditions shown below:

Storage Temperature	10 to 30℃
Relatively Humidity	below 60%RH

12.2 Treatment After Unsealed

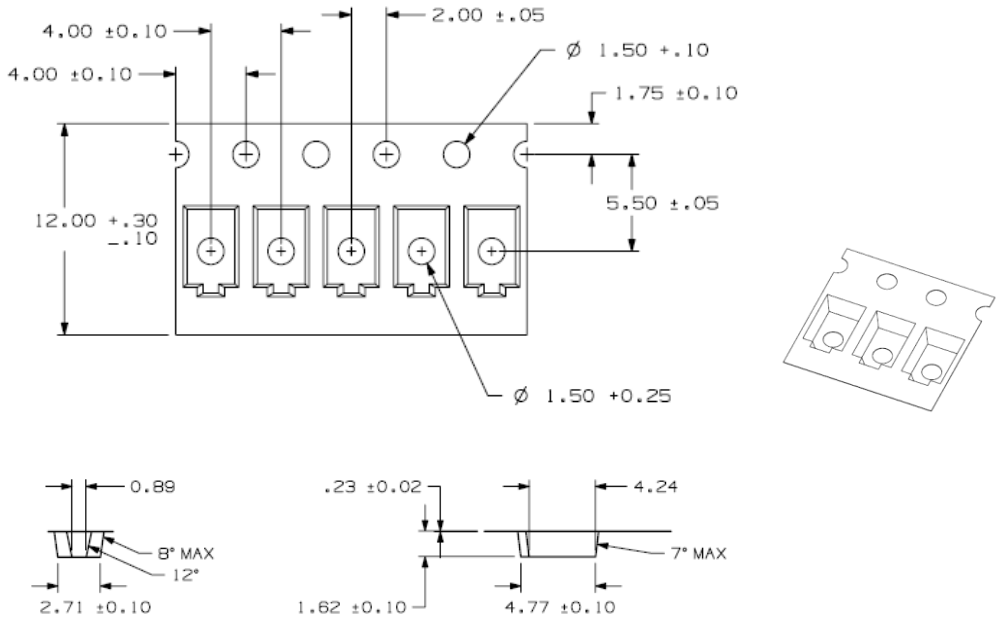
1. Floor life (time between soldering and removing from MBB) must not exceed the time shown below:

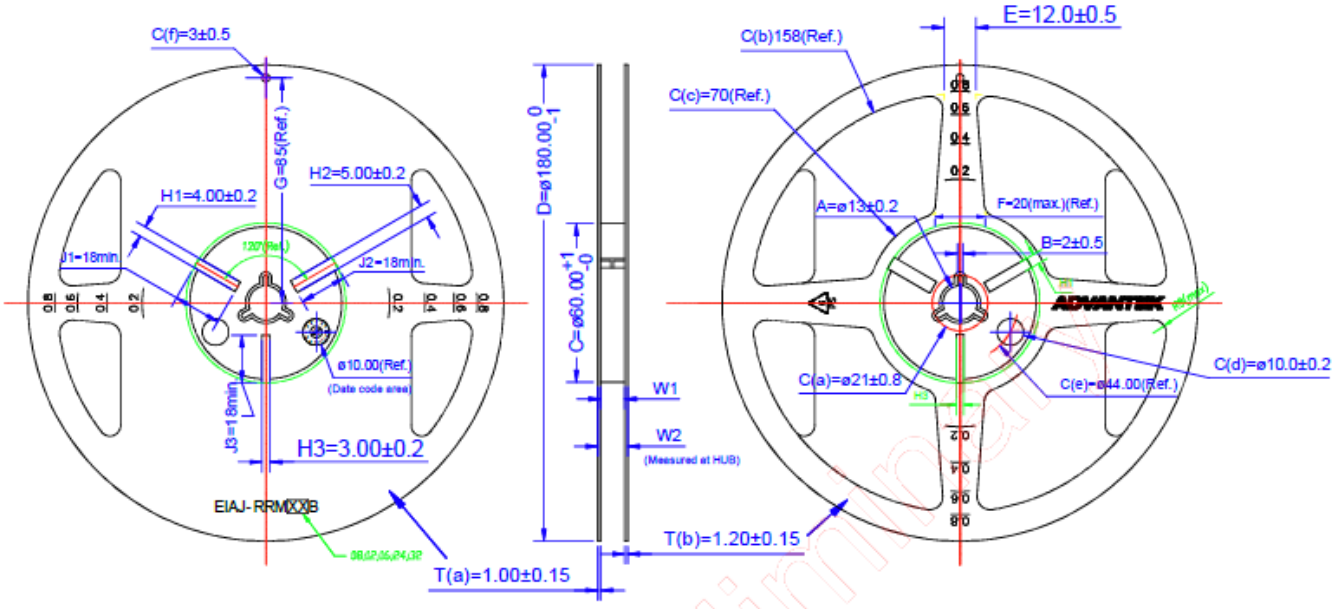
Floor Life	168 Hours
Storage Temperature	10 to 30℃
Relatively Humidity	below 60%RH

2. When the floor life limits have been exceeded or the devices are not stored in dry conditions, they must be re-baked before reflow to prevent damage to the devices. The recommended conditions are shown below

Temperature	60℃
Re-Baking Time	12 Hours

13. TAPE AND REEL DIMENSION





Notes: all linear dimensions are in mm.

Revision History

Date	Version	Modified Items
2016/7/27	0.9	Initial release.

