

## Features

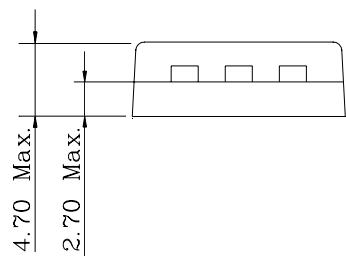
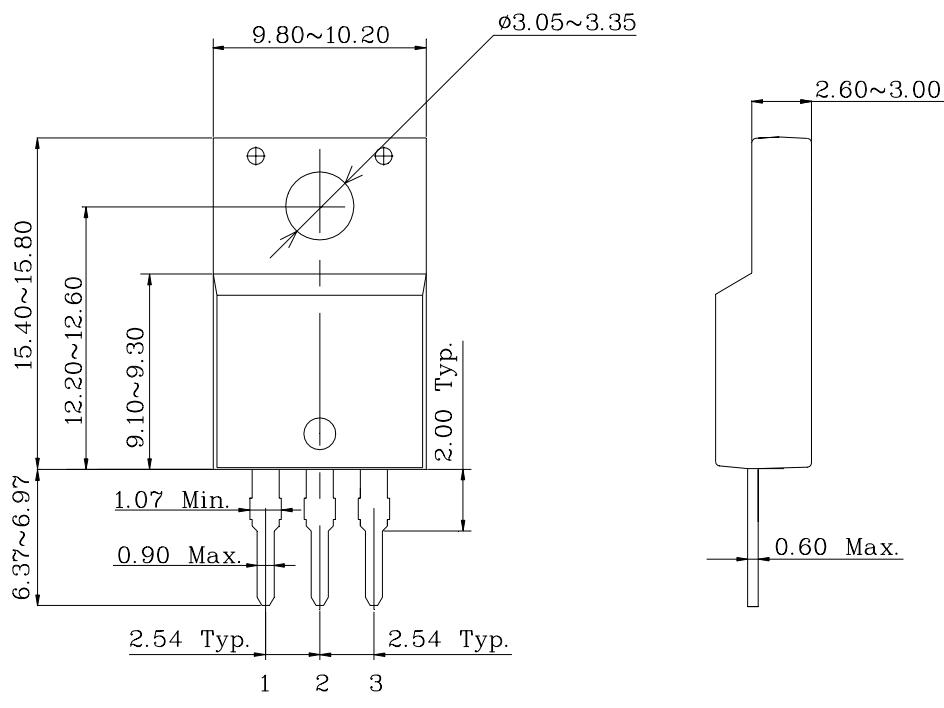
- Low Crss
- Low gate charge.
- Low leakage current

## Ordering Information

Type NO.	Marking	Package Code
STK0765FC	STK0765	TO-220F-3SL

## Outline Dimensions

unit : mm



**PIN Connections**  
 1. Gate  
 2. Drain  
 3. Source

**Absolute maximum ratings**(T<sub>C</sub>=25°C)

Characteristic	Symbol	Rating		Unit
Drain-source voltage	V <sub>DSS</sub>	650		V
Gate-source voltage	V <sub>GSS</sub>	±30		V
Drain current (DC) *	I <sub>D</sub>	T <sub>C</sub> =25°C	7	A
		T <sub>C</sub> =100°C	4.4	A
Drain current (Pulsed) *	I <sub>DP</sub>	28		A
Drain power dissipation (T <sub>c</sub> =25°C)	P <sub>D</sub>	40		W
Single pulsed avalanche energy ②	E <sub>AS</sub>	420		mJ
Avalanche current (Repetitive) ①	I <sub>AR</sub>	5.2		A
Repetitive avalanche energy ①	E <sub>AR</sub>	14.7		mJ
Peak diode recovery dv/dt ③	dv/dt	5.5		V/ns
Junction temperature	T <sub>J</sub>	150		°C
Storage temperature range	T <sub>stg</sub>	-55~150		°C

\* Limited by maximum junction temperature

**Thermal Resistance**

Characteristic	Symbol	Typ.	Max	Units
Thermal resistance junction-case	R <sub>th(J-C)</sub>	-	3.125	°C/W
Thermal resistance Junction-ambient	R <sub>th(J-A)</sub>	-	62.5	

**Electrical Characteristics**(T<sub>C</sub>=25°C)

Characteristic	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Drain-source breakdown voltage	V <sub>(BR)DSS</sub>	I <sub>D</sub> =250 μA, V <sub>GS</sub> =0	650	-	-	V
Gate threshold voltage	V <sub>GS(th)</sub>	I <sub>D</sub> =250 μA, V <sub>DS</sub> =V <sub>GS</sub>	2.0	-	4.0	V
Drain-source cut-off current	I <sub>DSS</sub>	V <sub>DS</sub> =650V, V <sub>GS</sub> =0	-	-	10	μA
Gate leakage current	I <sub>GSS</sub>	V <sub>DS</sub> =0V, V <sub>GS</sub> =±30V	-	-	±100	nA
Static drain-source on-resistance ④	R <sub>DS(on)</sub>	V <sub>GS</sub> =10V, I <sub>D</sub> =3.5A	-	-	1.2	Ω
Forward transfer conductance ④	g <sub>fs</sub>	V <sub>DS</sub> =5V, I <sub>D</sub> =3.5A	3.9	6.4	-	S
Input capacitance	C <sub>iss</sub>	V <sub>GS</sub> =0V, V <sub>DS</sub> =25V f=1 MHz	-	881	-	pF
Output capacitance	C <sub>oss</sub>		-	123	-	
Reverse transfer capacitance	C <sub>rss</sub>		-	19	-	
Turn-on delay time	t <sub>d(on)</sub>	V <sub>DD</sub> =325V, I <sub>D</sub> =7A R <sub>G</sub> =25Ω Fig. 13	-	18	-	ns
Rise time	t <sub>r</sub>		-	19	-	
Turn-off delay time	t <sub>d(off)</sub>		-	72	-	
Fall time	t <sub>f</sub>		-	28	-	
Total gate charge	Q <sub>g</sub>	V <sub>DS</sub> =520V, V <sub>GS</sub> =10V, I <sub>D</sub> =7A Fig. 12	-	49	-	nC
Gate-source charge	Q <sub>gs</sub>		-	8.4	-	
Gate-drain charge	Q <sub>gd</sub>		-	22.1	-	

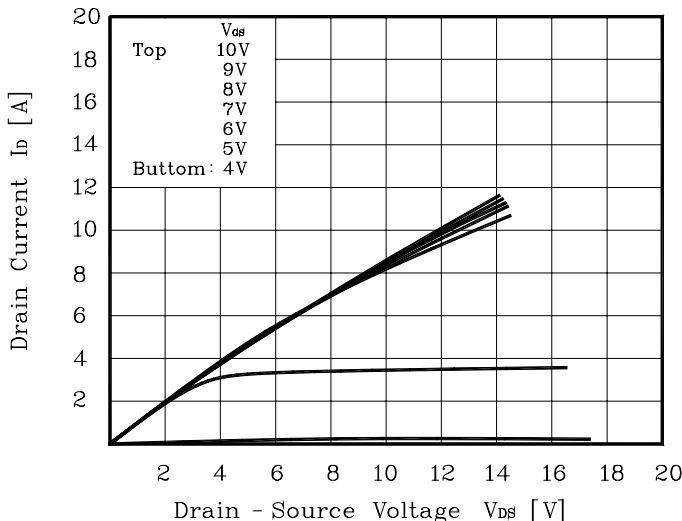
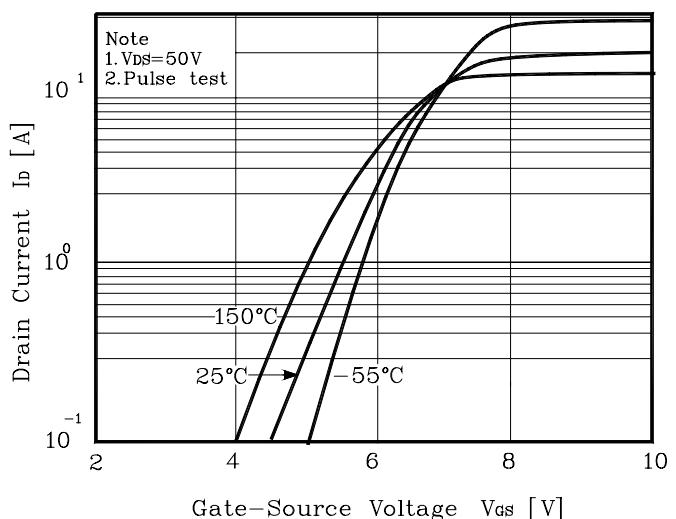
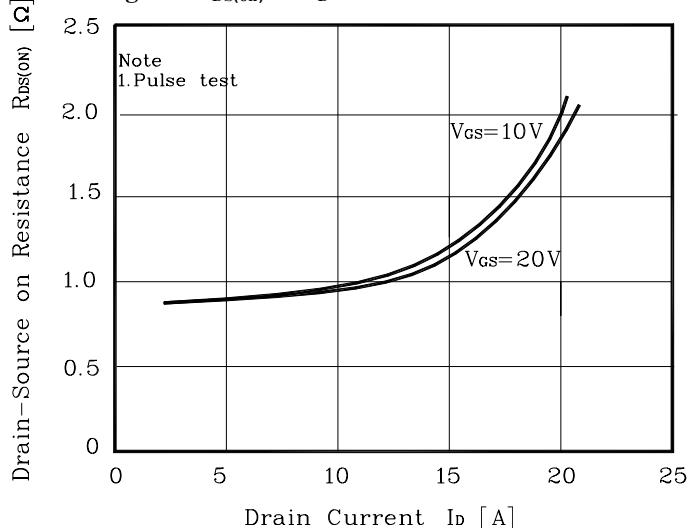
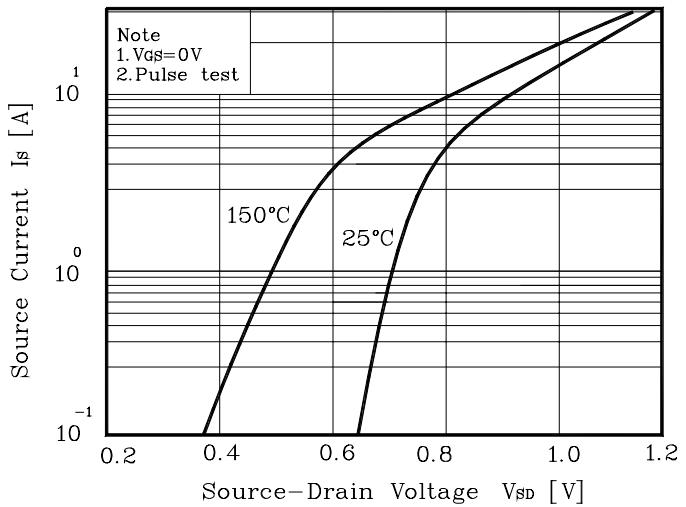
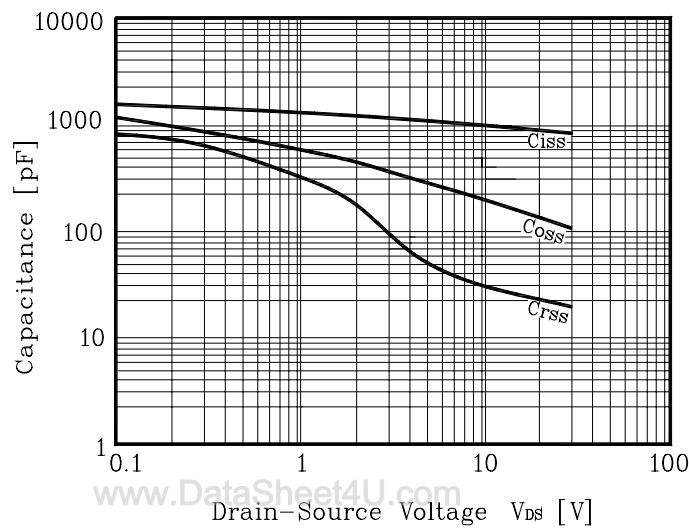
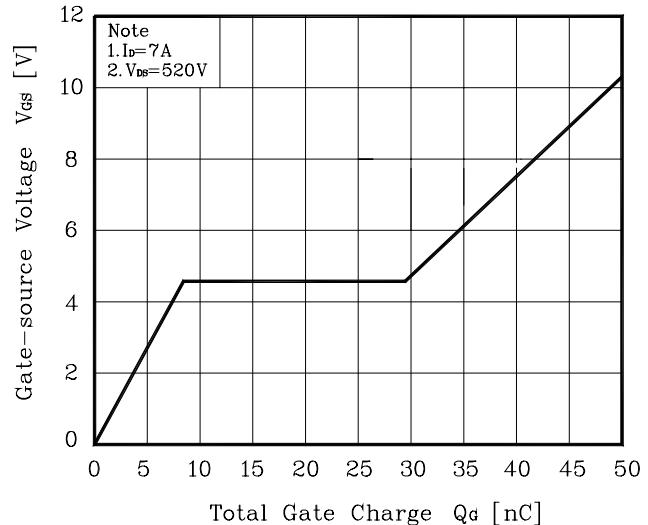
**Source-Drain Diode Ratings and Characteristics**(T<sub>C</sub>=25°C)

Characteristic	Symbol	Test Condition	Min	Typ	Max	Units
Source current (DC)	I <sub>S</sub>	Integral reverse diode in the MOSFET	-	-	7	A
Source current (Pulsed) ①	I <sub>SP</sub>		-	-	28	
Diode forward voltage ④	V <sub>SD</sub>	V <sub>GS</sub> =0V, I <sub>S</sub> =7A	-	-	1.4	V
Reverse recovery time	t <sub>rr</sub>	I <sub>S</sub> =7A dI <sub>S</sub> /dt=100A/μs	-	320	-	ns
Reverse recovery charge	Q <sub>rr</sub>		-	2.4	-	

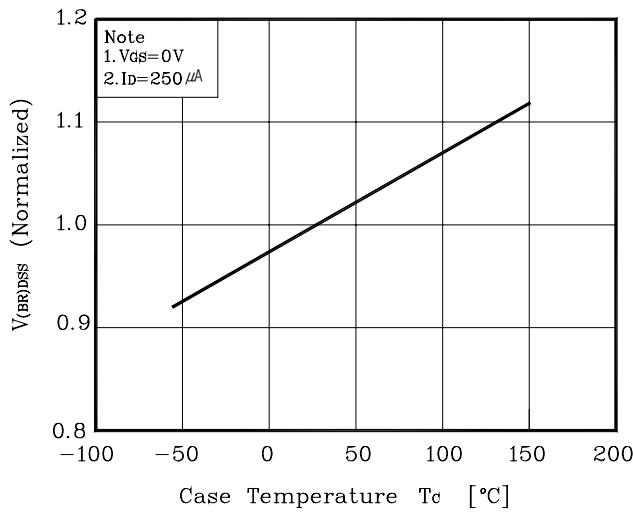
Note :

- ① Repetitive rating : Pulse width limited by maximum junction temperature
- ② L=15.7mH, I<sub>AS</sub>=7A, V<sub>DD</sub>=50V, R<sub>G</sub>=27Ω
- ③ I<sub>S</sub> ≤ 7A, di/dt≤ 300A/μs, V<sub>DD</sub>=100V
- ④ Pulse Test : Pulse width≤ 400 μs, Duty cycle≤ 2%
- ⑤ Essentially independent of operating temperature

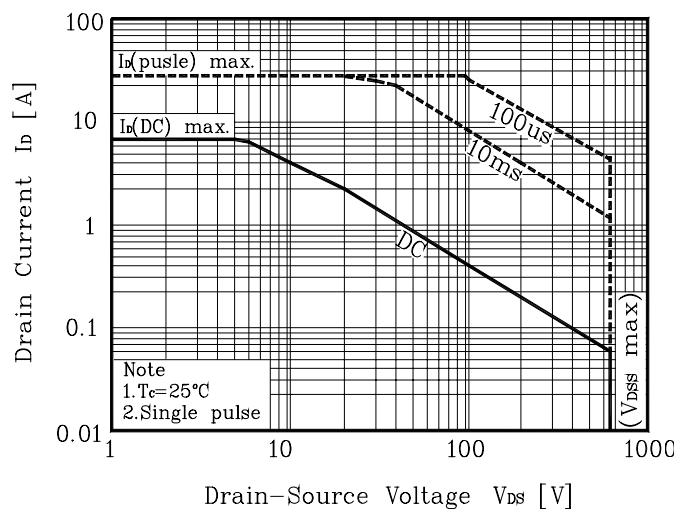
## Electrical Characteristic Curves

**Fig. 1**  $I_D$  -  $V_{DS}$ **Fig. 2**  $I_D$  -  $V_{GS}$ **Fig. 3**  $R_{DS(on)}$  -  $I_D$ **Fig. 4**  $I_S$  -  $V_{SD}$ **Fig. 5** Capacitance -  $V_{DS}$ **Fig. 6**  $V_{GS}$  -  $Q_G$ 

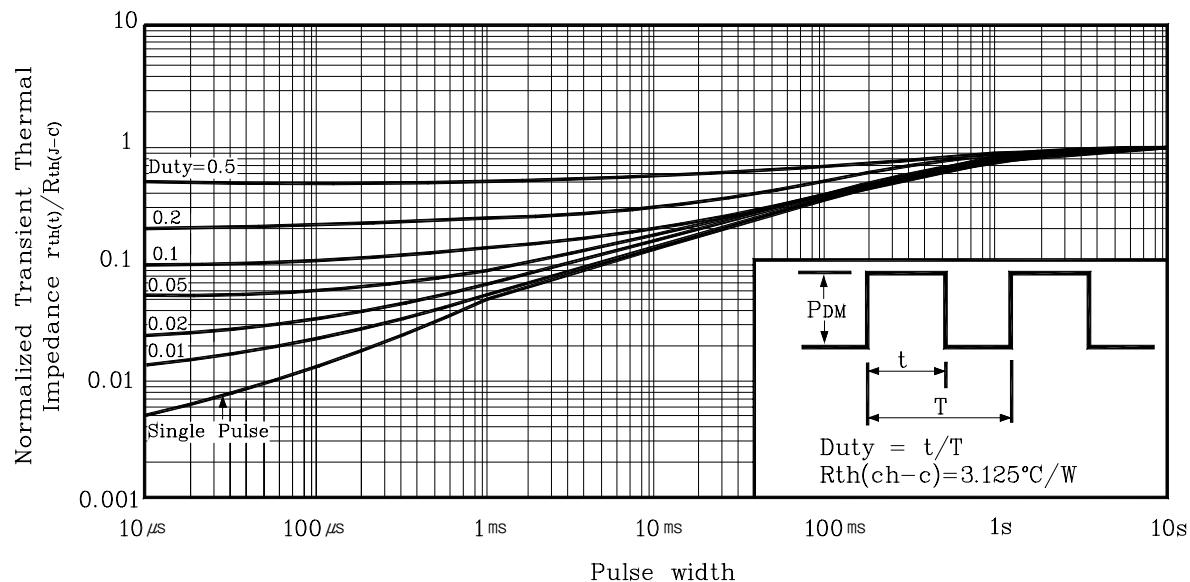
**Fig. 7**  $V_{(BR)DSS}$  -  $T_c$



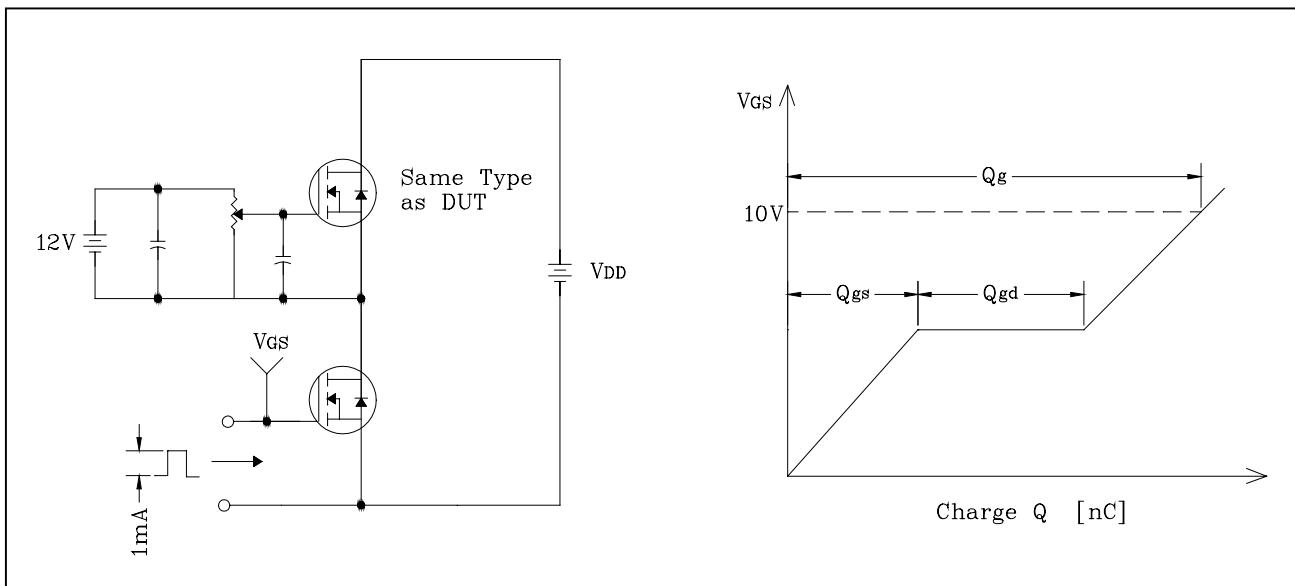
**Fig. 8** Safe Operating Area



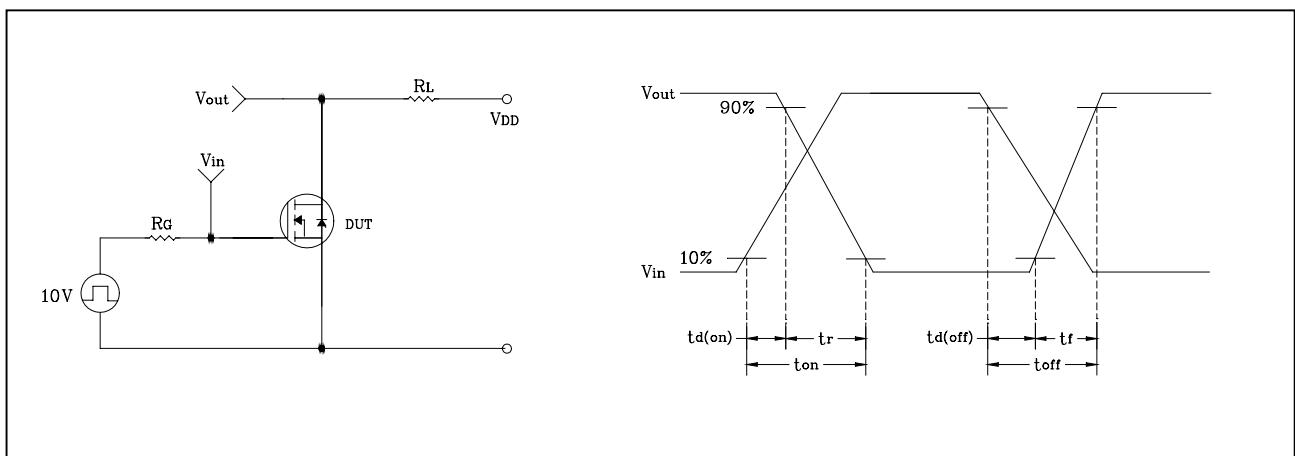
**Fig. 11 Thermal Response**



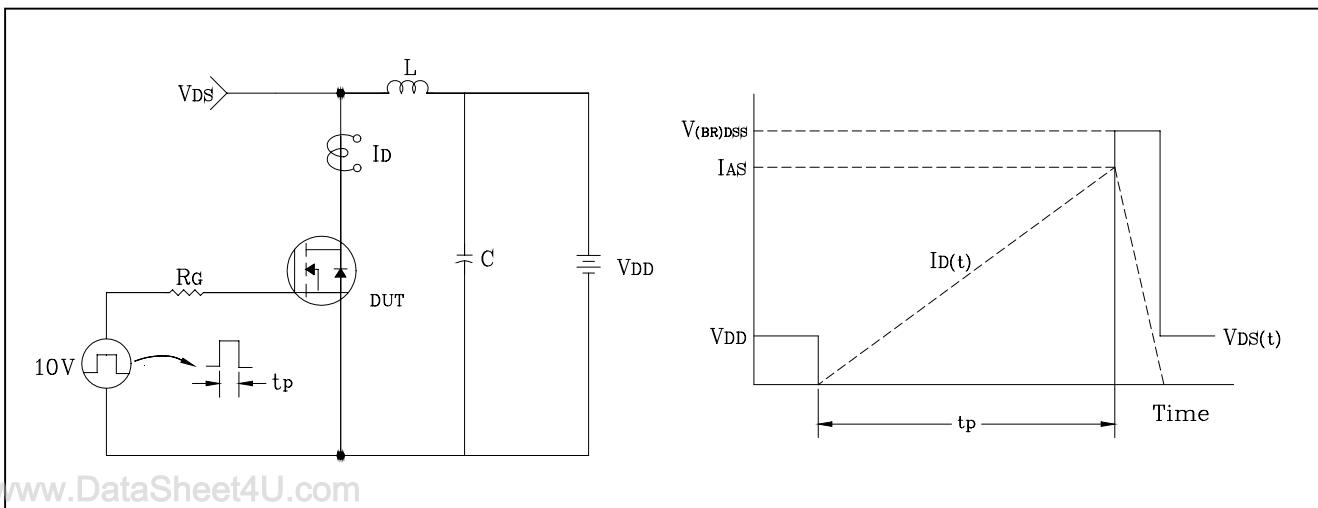
**Fig. 12 Gate Charge Test Circuit & Waveform**



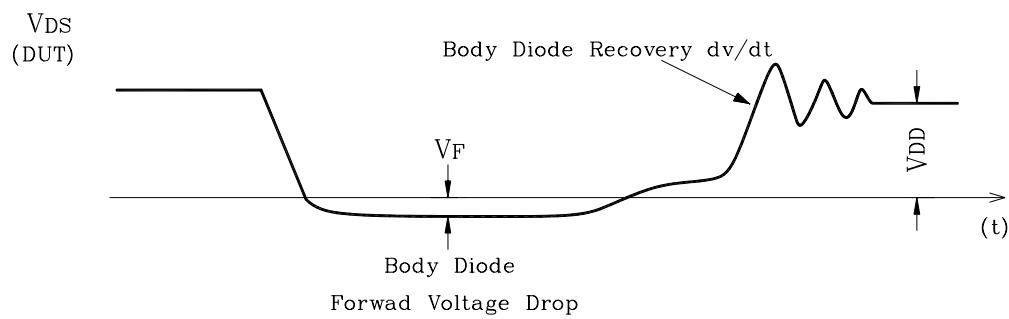
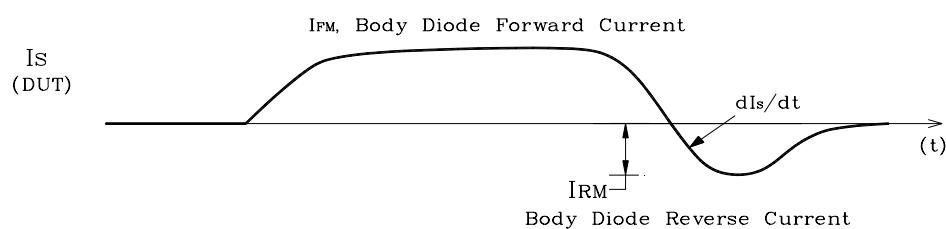
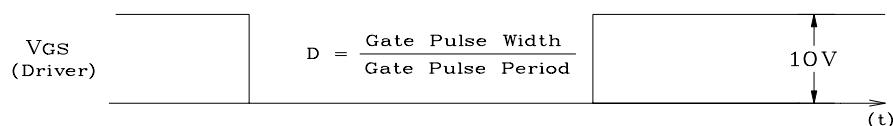
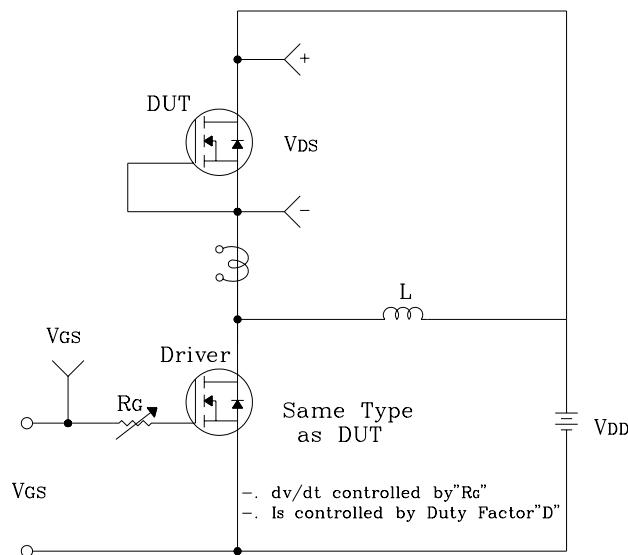
**Fig. 13 Switching Time Test Circuit & Waveform**



**Fig. 14 E<sub>AS</sub> Test Circuit & Waveform**



**Fig. 15 Peak Diode Recovery dv/dt Test Circuit & Waveform**



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