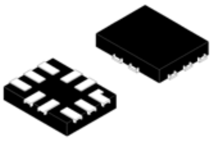
STG6684

High isolation dual SPDT analog switch

Features

- Ultra high off-isolation:
  -80 dB (typ) at 1 Mhz
- Ultra low power dissipation:
  I_{CC} = 0.2 µA (max.) at T_A = 85 °C
- R_{PEAK} on T_n = 1.30 Ω max (T_A = 25 °C) at V_{CC} = 4.3 V
- R_{PEAK} on S_n = 0.55 Ω max (T_A = 25 °C) at V_{CC} = 4.3 V
- Wide operating voltage range:
  V_{CC} (opr) = 1.65 to 4.3 V single supply
- 4.3 V tolerant and 1.8 V compatible threshold on digital control input at V_{CC} = 1.65 to 4.3 V
- Typical bandwidth (-3 dB) at 65 MHz on Sn channel, 58 MHz on the T_n channel
- Latch-up performance exceeds 100 mA per JESD 78, Class II
- ESD performance exceeds JESD22 2000-V Human body model (A114-A)



QFN10L (1.8 x 1.4 mm)

Description

The STG6684 is a high-speed CMOS low voltage dual analog SPDT (single pole dual throw) switch or 2:1 multiplexer/de-multiplexer switch fabricated in silicon gate C^2MOS technology.

The STG6684 is designed to operate from 1.65 to 4.3 V, making this device ideal for portable applications.

The SELn inputs are provided to control the switch operation. The switch Sn is ON (connected to common ports Dn) when the SELn input is held low and OFF (high impedance state exists between the two ports) when SELn is held high.

The switch Tn is “on” (connected to common port Dn) when the SELn input is held high and “off” (high impedance state exists between the two ports) when SELn is held low.

Additional key features are fast switching speed, break-before-make delay time and ultra low power consumption. All inputs and outputs are equipped with protection circuits against static discharge, giving them ESD immunity and transient excess voltage.

Table 1. Device summary

Order code	Package	Packaging
STG6684QTR	QFN10L (1.8 x 1.4 mm)	Tape and reel

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1 Pin settings

Figure 1. Pin connection (top through view)

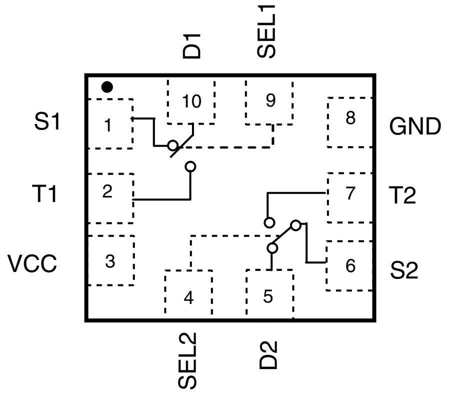


Table 2. Pin description

Pin number	Symbol	Name and function
1	S1	Independent channel
2	T1	Independent channel
3	V_{CC}	Positive supply voltage
4	SEL2	Selection control
5	D2	Common channel
6	S2	Independent channel
7	T2	Independent channel
8	GND	Ground (0 V)
9	SEL1	Selection control
10	D1	Common channel

2 Logic diagram

Figure 2. Logic block diagram

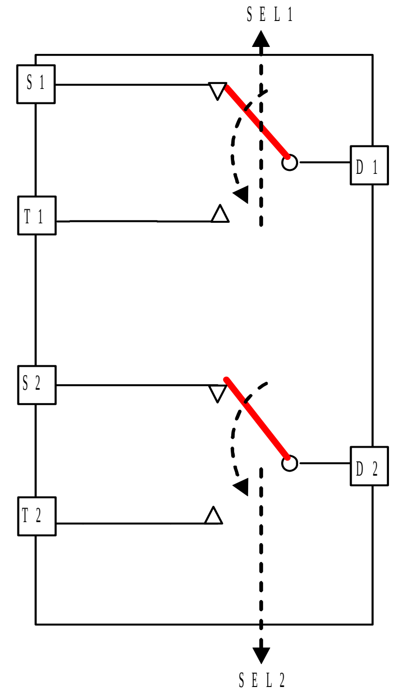


Table 3. Truth table

SELn	Switch Sn	Switch Tn
L	Sn is connected to Dn	OFF(1)
H	OFF(1)	Tn is connected to Dn

1. High impedance

3 Maximum rating

Stressing the device above the rating listed in the “Absolute maximum ratings” table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality documents.

Table 4. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage	-0.5 to 5.5	V
V_I	DC input voltage	-0.5 to V_{CC} + 0.5	V
V_{IC}	DC control input voltage	-0.5 to 5.5	V
V_O	DC output voltage	-0.5 to V_{CC} + 0.5	V
I_{IKC}	DC input diode current on control pin ($V_{SEL} < 0$ V)	–50	mA
I_{IK}	DC input diode current ($V_{SEL} < 0$ V)	±50	mA
I_{OK}	DC output diode current	±20	mA
I_O	DC output current	±300	mA
I_{OP}	DC output current peak (pulse at 1 ms, 10% duty cycle)	±500	mA
I_{CC} or I_{GND}	DC V_{CC} or ground current	±100	mA
P_D	Power dissipation at T_A=70 °C(1)	1120	mW
T_{STG}	Storage temperature	-65 to 150	°C
T_L	Lead temperature (10 sec)	300	°C

1. Derate above 70 °C by 18.5 mW/°C

3.1 Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter		Value	Unit
V_{CC}	Supply voltage		1.65 to 4.3	V
V_I	Input voltage		0 to V_{CC}	V
V_{IC}	Control input voltage		0 to 4.3	V
V_O	Output voltage		0 to V_{CC}	V
T_{op}	Operating temperature		-40 to 85	°C
dt/dv	Input rise and fall time control input	V_{CC} = 1.65 V to 2.7 V	0 to 20	ns/V
		V_{CC} = 3.0 V to 4.3 V	0 to 10	

4 Electrical characteristics

Table 6. DC specifications

Symbol	Parameter	V_{CC} (V)	Test condition	Value					Unit
				T_A = 25 °C			-40 to 85 °C		
				Min	Typ	Max	Min	Max	
V_{IH}	High level input voltage	1.65 –1.95		0.65 V_{CC}			0.65 V_{CC}		V
		2.3 –2.5		1.2			1.2		
		2.7 –3.0		1.3			1.3		
		3.3 –3.6		1.4			1.4		
		4.3		1.5			1.5		
V_{IL}	Low level input voltage	1.65 –1.95				0.25		0.25	V
		2.3 –2.5				0.25		0.25	
		2.7 –3.0				0.25		0.25	
		3.3 –3.6				0.30		0.30	
		4.3				0.40		0.40	
$R_{PEAK, Tn}$	Switch T_n ON resistance	4.3	V_S = 0 V to V_{CC} I_S = 100 mA		1.10	1.3		1.5	Ω
		3.6			1.15	1.4		1.6	
		3.0			1.25	1.5		1.8	
		2.7			1.35	1.6		1.9	
		1.8			2.20	2.9		3.5	
$R_{PEAK, Sn}$	Switch S_nON resistance	4.3	V_S = 0 V to V_{CC} I_S = 100 mA		0.45	0.55		0.62	Ω
		3.6			0.48	0.58		0.65	
		3.0			0.51	0.62		0.70	
		2.7			0.54	0.70		0.80	
		1.8			0.84	1.10		1.30	
$\Delta R_{ON, Tn}$	ON resistance match between Tn channels(1)	4.3	V_S at R_{PEAK} I_S = 100 mA		10				mΩ
		3.6			14				
		3.0			14				
		2.7			15				
		1.8			30				
$\Delta R_{ON, Sn}$	ON resistance match between Sn channels(1)	4.3	V_S at R_{PEAK} I_S = 100 mA		7				mΩ
		3.6			7				
		3.0			8				
		2.7			9				
		1.8			12				

Table 6. DC specifications

Symbol	Parameter	V_{CC} (V)	Test condition	Value					Unit
				T_A = 25 °C			-40 to 85 °C		
				Min	Typ	Max	Min	Max	
$R_{FLAT, Tn}$	ON resistance flatness for Tn channels(2)	4.3	V_S = 0 to V_{CC} I_S = 100 mA		0.45	0.50		0.55	Ω
		3.6			0.45	0.50		0.55	
		3.0			0.50	0.55		0.60	
		2.7			0.55	0.60		0.70	
		1.8			1.10	1.70		2.00	
$R_{FLAT, Sn}$	ON resistance flatness for Sn channels(2)	4.3	V_S = 0 to V_{CC} I_S = 100 mA		0.15	0.20		0.20	Ω
		3.6			0.15	0.20		0.20	
		3.0			0.15	0.20		0.20	
		2.7			0.15	0.20		0.20	
		1.8			0.35	0.55		0.66	
I_{OFF}	OFF state leakage current (Tn), (Sn), (Dn)	4.3	V_S = 0.3 or 4 V			±0.1		±1	µA
I_{SEL}	SEL leakage current	0 –4.3	V_{SEL} = 0 to 4.3 V			±0.05		±1	µA
I_{CC}	Quiescent supply current	1.65 –4.3	V_{SEL} = V_{CC} or GND			±0.05		±0.2	µA
I_{CCLV}	Quiescent supply current low voltage driving	4.3	V_{SEL} = 1.65 V		±37	±50		±100	µA
			V_{SEL} = 1.80 V		±33	±40		±50	
			V_{SEL} = 2.60 V		±12	±20		±30	

1. $\Delta R_{ON} = R_{ON(max)} - R_{ON(min)}$.
2. Flatness is defined as the difference between the maximum and minimum value of on-resistance as measured over the specified analog signal ranges.

Table 7. AC electrical characteristics (C_L = 35 pF, R_L = 50 Ω, $t_r = t_f \leq 5$ ns)

Symbol	Parameter	V_{CC} (V)	Test condition	Value					Unit
				T_A = 25 °C			-40 to 85 °C		
				Min	Typ	Max	Min	Max	
t_{PLH}, t_{PHL}	Propagation delay	1.65 —1.95			0.45				ns
		2.3 —2.7			0.45				
		3.0 —3.3			0.30				
		3.6 —4.3			0.30				
t_{ON}	Turn-ON time	1.65 —1.95	V_S = 0.8 V		120				ns
		2.3 —2.7	V_S = 1.5 V		65	85		90	
		3.0 —3.3			42	55		65	
		3.6 —4.3			40	55		65	
t_{OFF}	Turn-OFF time	1.65 —1.95	V_S = 0.8 V		45				ns
		2.3 —2.7	V_S = 1.5 V		18	30		40	
		3.0 —3.3			16	30		40	
		3.6 —4.3			15	30		40	
t_D	Break-before-make time delay	1.65 —1.95	C_L = 35 pF R_L = 50 Ω V_S = 1.5 V	2	18				ns
		2.3 —2.7		2	10				
		3.0 —3.3		2	8				
		3.6 —4.3		2	6				
Q	Charge injection	1.65 —1.95	C_L = 100 pF R_L = 1 MΩ V_{GEN} = 0 V R_{GEN} = 0 Ω		43				pC
		2.3 —2.7			51				
		3.0 —3.3			51				
		3.6 —4.3			49				

Table 8. Analog switch characteristics (C_L = 5 pF, R_L = 50 Ω, T_A = 25 °C)

Symbol	Parameter	V_{CC} (V)	Test condition	Value					Unit
				T_A = 25 °C			-40 to 85 °C		
				Min	Typ	Max	Min	Max	
OIRR$_{Tn}$	Off isolation for switch T1,T2	1.65 —4.3	V_S=1 V_{RMS}, f=1 MHz, R_L = 50 Ω		-80				dB
			V_S=1 V_{RMS}, f = 10 MHz, R_L = 50 Ω		-60				
OIRR$_{Sn}$	Off isolation for switch S1, S2	1.65 —4.3	V_S =1 V_{RMS}, f = 100 kHz RL = 50 Ω		-66				dB
			V_S=1 V_{RMS}, f = 1 MHz R_L = 50 Ω		-45				
Xtalk$_{Sn}$	Crosstalk between S1 and S2	1.65 — 4.3	V_S=1 V_{RMS}, f = 1 MHz Signal = 0 dBm		-90				dB
			V_S=1 V_{RMS}, f = 10 MHz Signal = 0 dBm		-69				dB
XtalkTn	Crosstalk between T1 and T2	1.65 — 4.3	V_S=1 V_{RMS}, f = 1 MHz Signal = 0 dBm		-85				dB
			V_S=1 V_{RMS}, f = 10 MHz Signal = 0 dBm		-74				
THD$_{Sn}$	Total harmonic distortion	2.3 — 4.3	f = 20 Hz to 20 kHz R_L= 600 Ω, C_L = 50 pF V_{IN} = 2 V_{P-P} V_{DC} = V_{CC}/2		0.01				%
BW$_{Tn}$	-3dB bandwidth for switch T1, T2	1.65 — 4.3	R_L = 50 Ω Signal = 0 dBm		58				MHz
BW$_{Sn}$	-3dB bandwidth for switch S1,S2	1.65 — 4.3	R_L = 50 Ω Signal = 0 dBm		65				MHz

Symbol	Parameter	V_{CC} (V)	Test condition	Value					Unit
				T_A = 25 °C			-40 to 85 °C		
				Min	Typ	Max	Min	Max	
C_{SEL}	Control pin input capacitance		V_{CC} = 0 V		9				pF
$C_{ON,Tn}$	Tn port capacitance when the switch is enabled	3.3	f = 1 MHz		113				
$C_{ON,Sn}$	Sn port capacitance when the switch is enabled	3.3	f = 1 MHz		88				
$C_{OFF,Tn}$	Tn port capacitance when the switch is disabled	3.3	f = 1 MHz		85				
$C_{OFF,Sn}$	Sn port capacitance when the switch is disabled	3.3	f = 1 MHz		40				

5 Test circuit

Figure 3. ON resistance

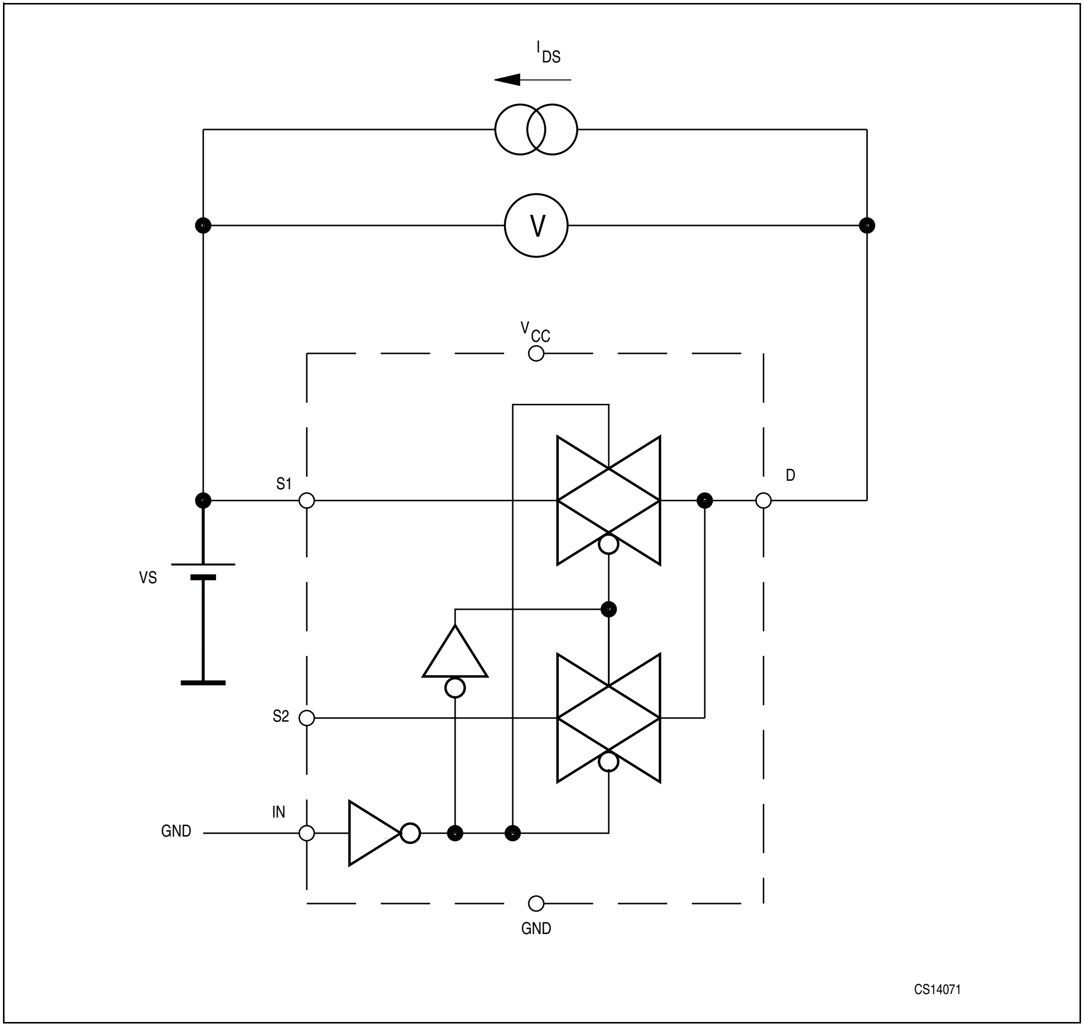


Figure 4. OFF leakage

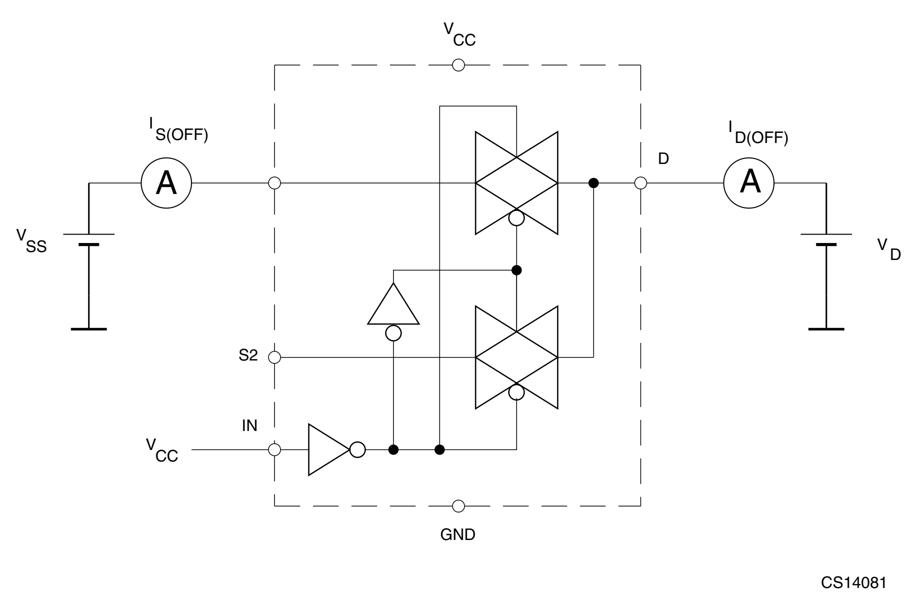


Figure 5. OFF isolation

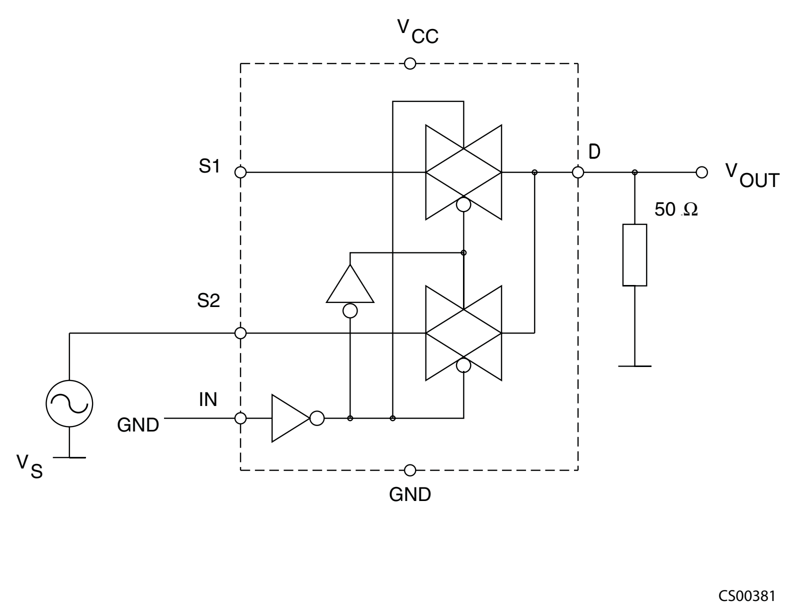


Figure 6. Bandwidth

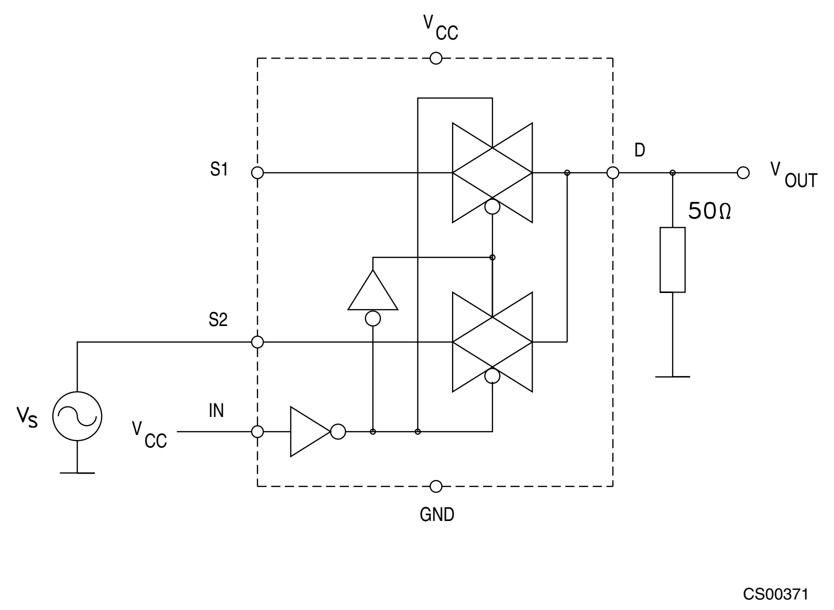


Figure 7. Switch-to-switch crosstalk

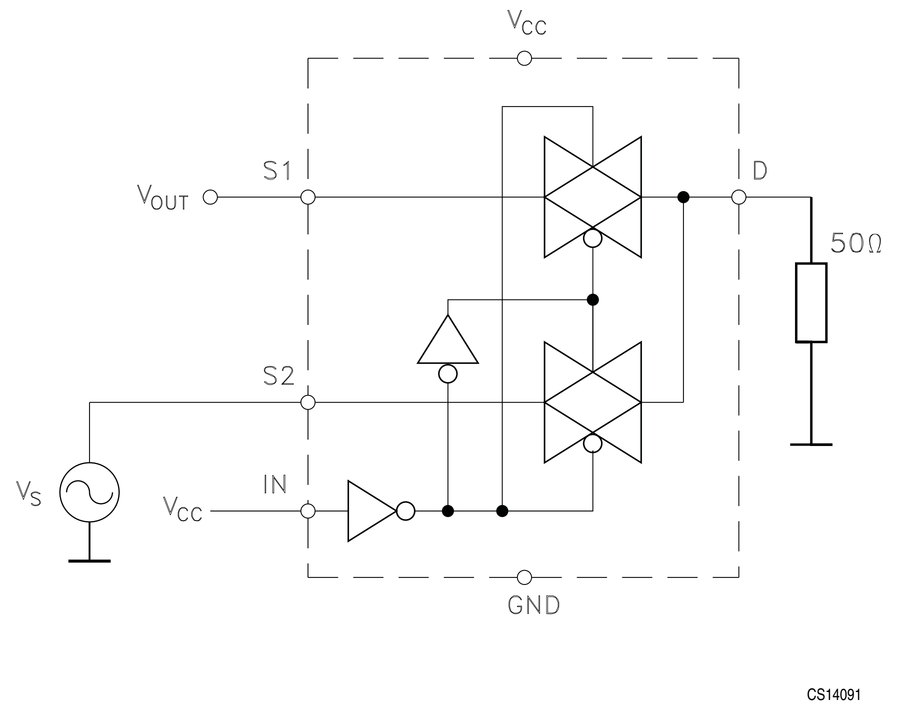
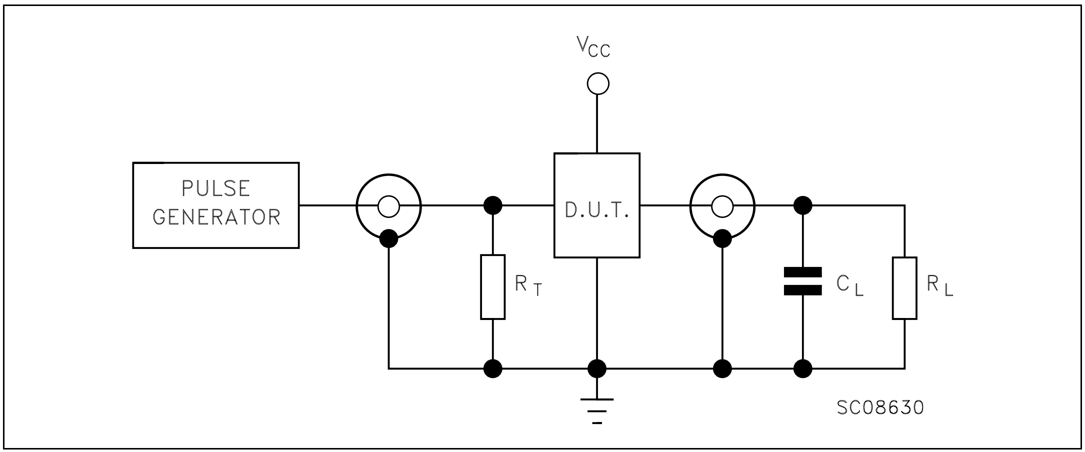


Figure 8. Test circuit



1. C_L = 5/35 pF or equivalent (includes jig and probe capacitance)
2. R_L = 50 Ω or equivalent
3. R_T = Z_{OUT} of pulse generator (typically 50 Ω)

Figure 9. Break-before-make time delay

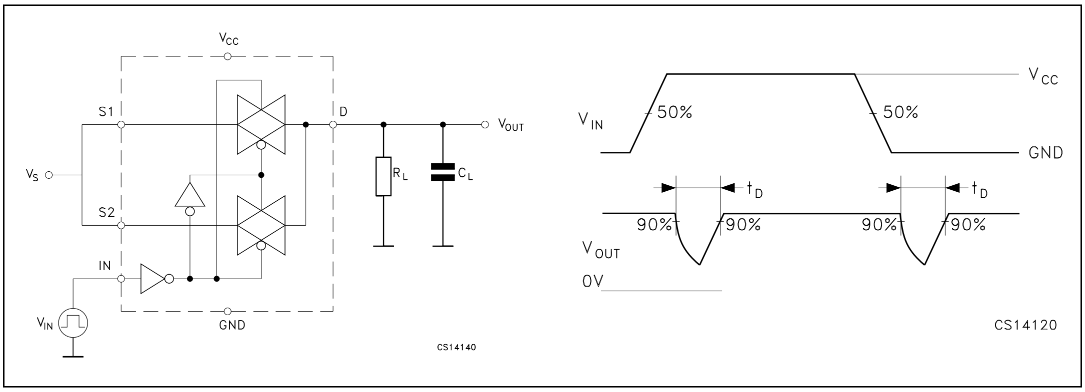


Figure 10. Switching time and charge injection ($V_{GEN} = 0$, $R_{GEN} = 0\ \Omega$, $R_L = 1\ M\Omega$, $C_L = 100\ pF$)

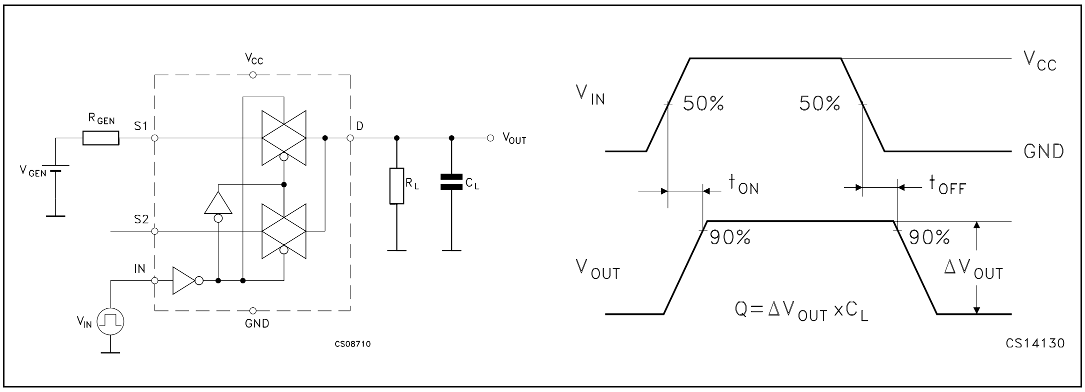
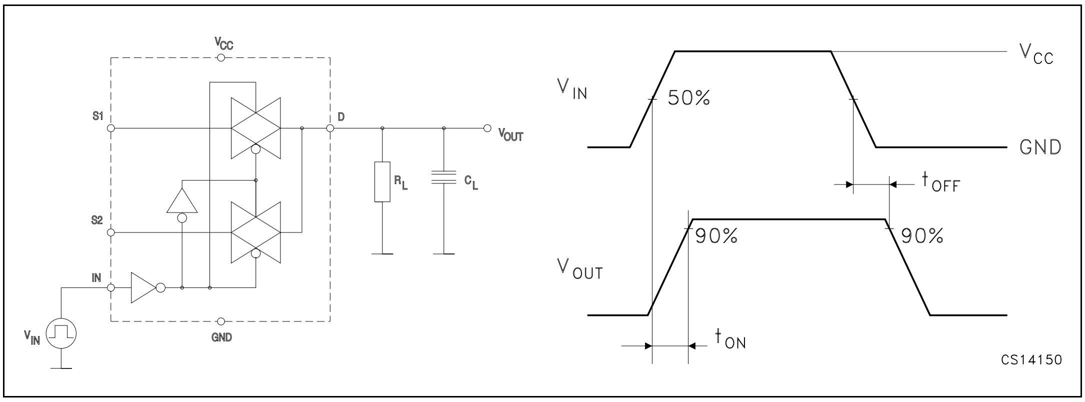


Figure 11. Turn on, turn off delay time



6 Application diagram

Figure 12. Application diagram

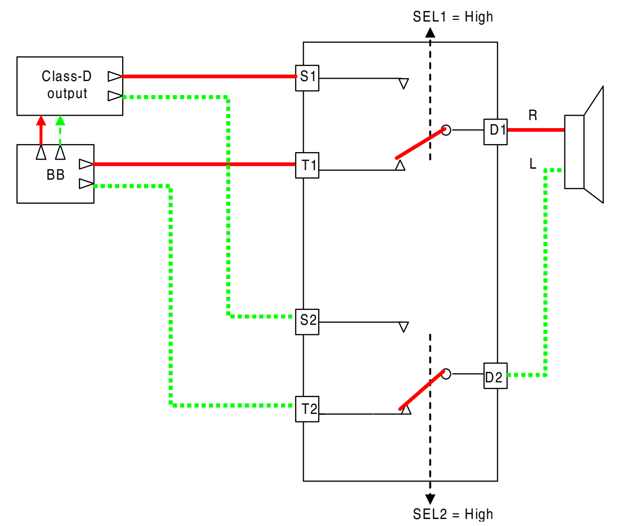
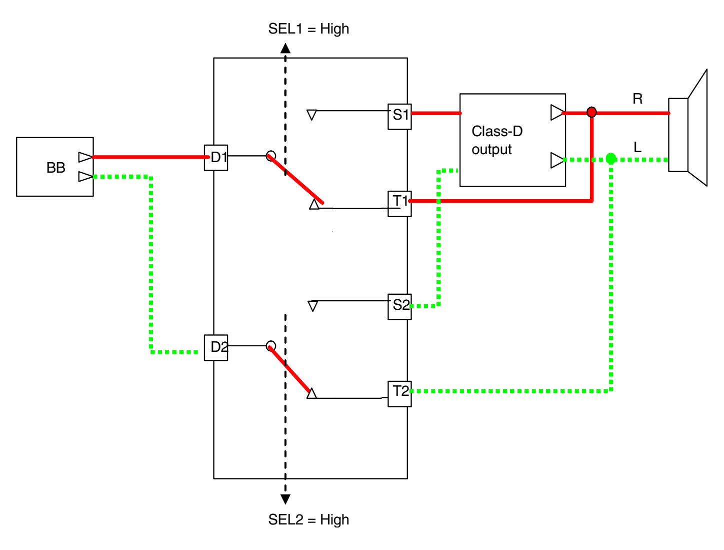


Figure 13. Application diagram



7 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com.

Figure 14. QFN10L (1.8 x 1.4 mm) package outline

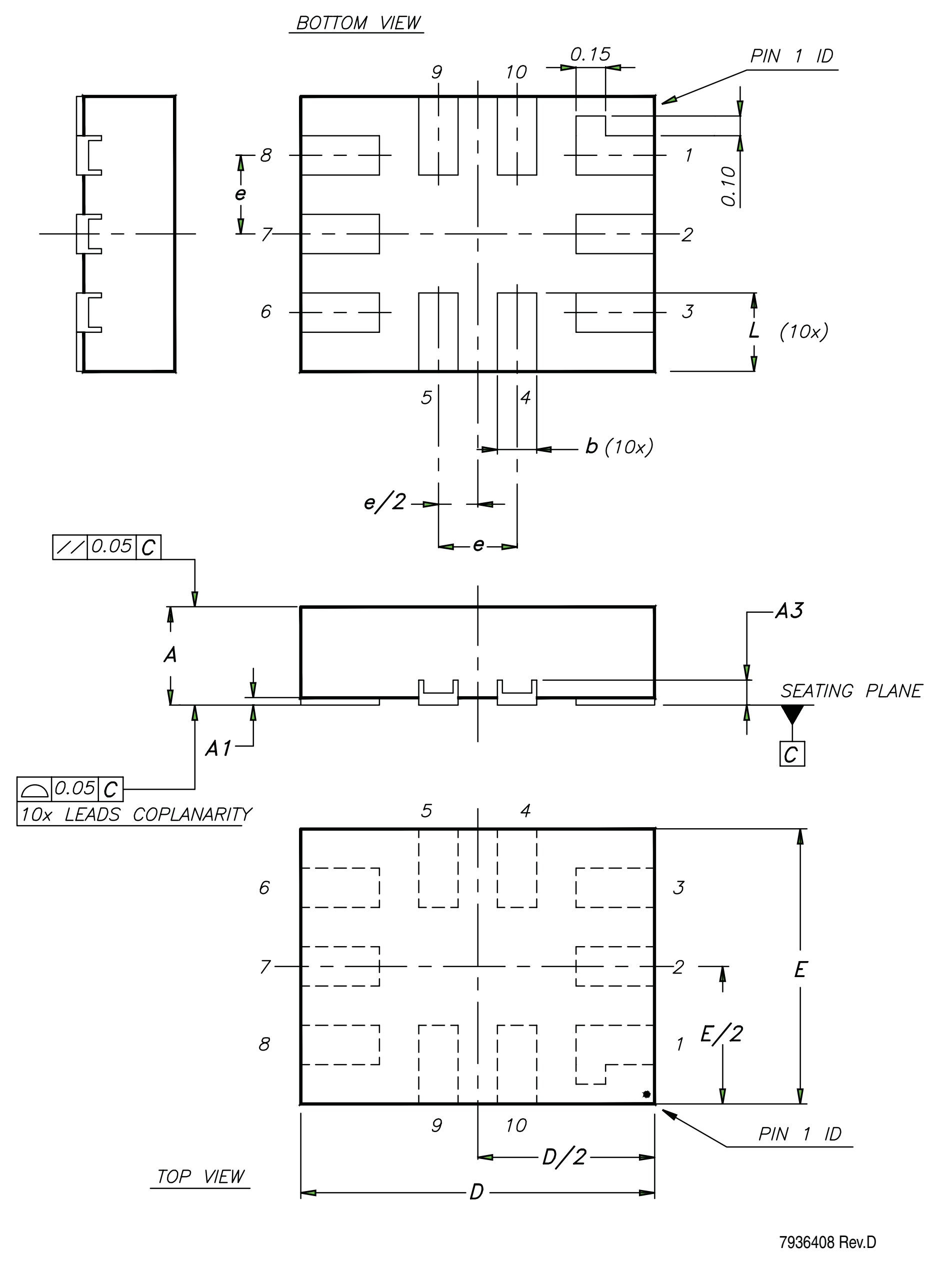


Table 2. QFN10L(1.8 x 1.4 mm) mechanical data

Symbol	Millimeters		
	Min	Typ	Max
A	0.45	0.50	0.55
A1	0	0.02	0.05
A3		0.127	
b	0.15	0.20	0.25
D	1.75	1.80	1.85
E	1.35	1.40	1.45
e		0.40	
L	0.35	0.40	0.45

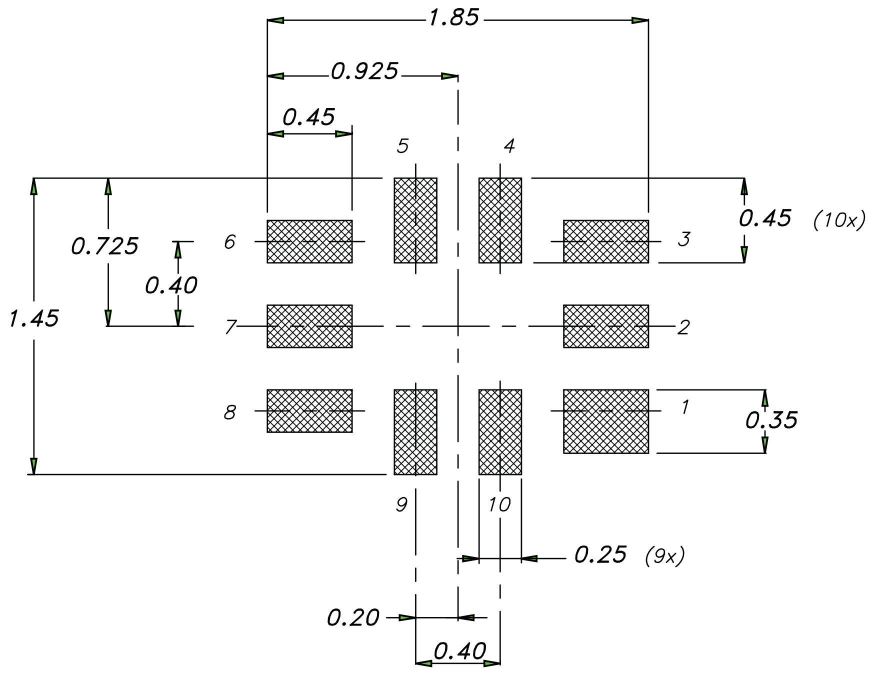
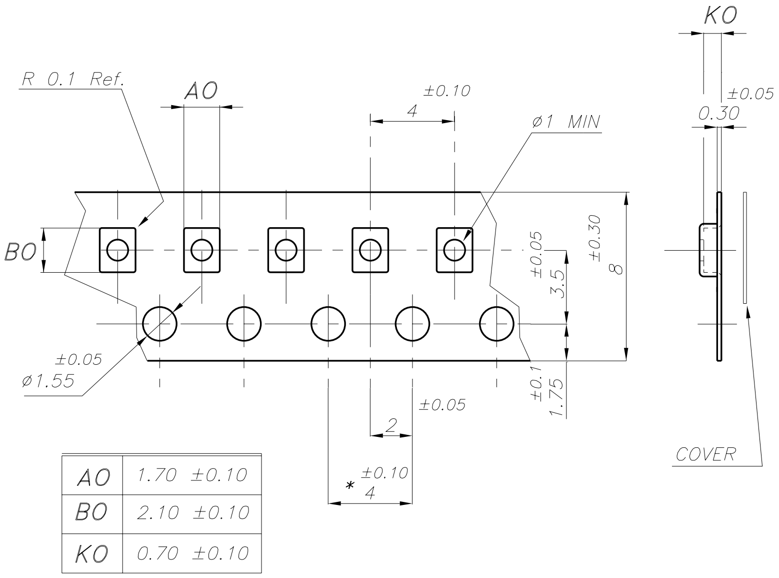


Figure 15. QFN10L (1.8 x 1.4 mm) footprint recommendations

Figure 16. QFN10L (1.8 x 1.4 mm) carrier tape



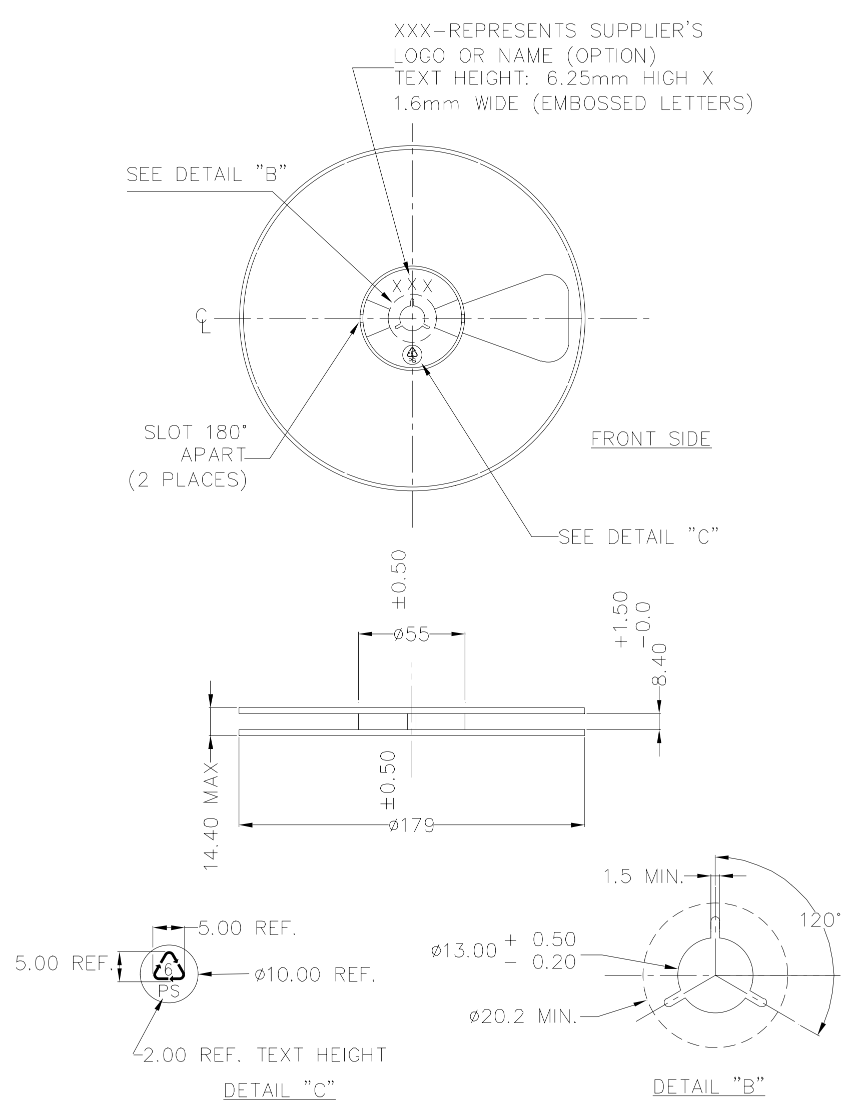
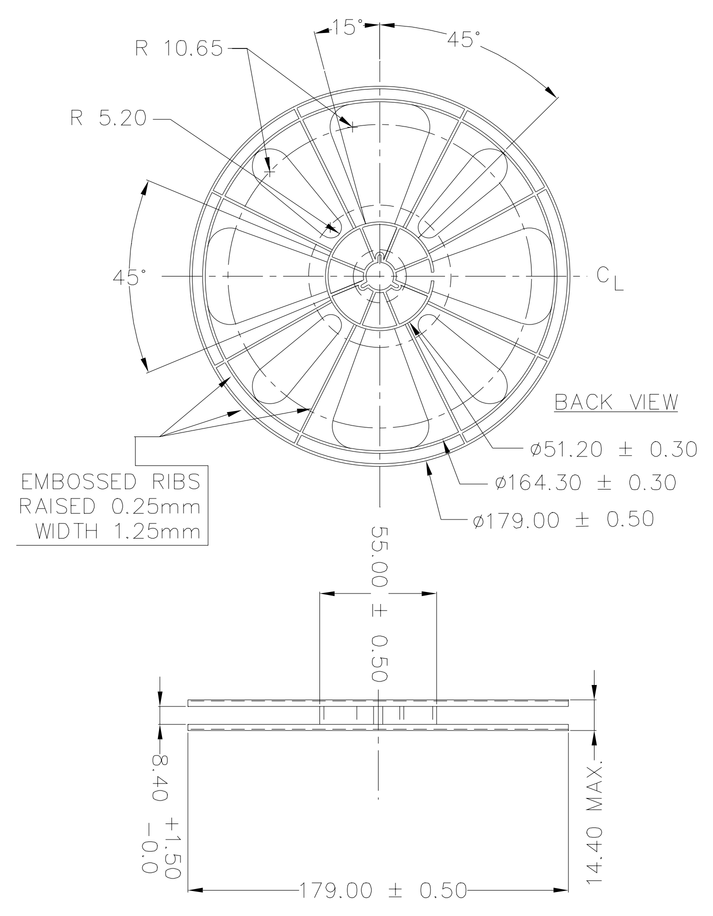


Figure 17. QFN10L (1.8 x 1.4 mm) reel information - front side

Figure 18. QFN10L(1.8 x 1.4 mm) reel information - back view



8 Revision history

Table 9. Document revision history

Date	Revision	Changes
9-Jan-2008	1	Initial release.

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