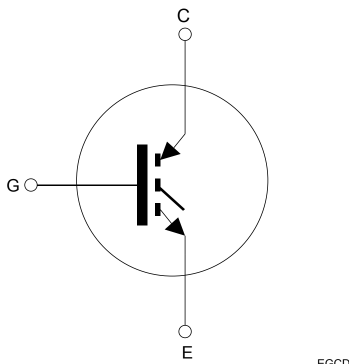
STG60H65FBD7

Datasheet

Trench gate field-stop 650 V, 60 A high-speed HB series IGBT die in D7 packing



Product status link
STG60H65FBD7

Product summary	
Order code	STG60H65FBD7
V_{CE}	6.32 x 4.90 mm
I_{CN}	60 A
Die size	6.32 x 4.90 mm
Packing	D7

Features

- Maximum junction temperature: T_J = 175 °C
- High speed switching series
- Minimized tail current
- Very low saturation voltage: $V_{CE(sat)}$ = 1.65 V (typ) @ I_C = 60 A
- Safe paralleling
- Tight parameter distribution

Applications

- Solar
- Welding
- High frequency converter

Description

This device is an IGBT developed using an advanced proprietary trench gate field-stop structure. The device is part of the new HB series of IGBTs, which represents an optimum compromise between conduction and switching loss to maximize the efficiency of any frequency converter. Furthermore, the slightly positive $V_{CE(sat)}$ temperature coefficient and very tight parameter distribution result in safer paralleling operation.

1 Mechanical parameters

Table 1. Mechanical parameters

<table>
<tr><th colspan="2">Symbol</th><th>Value</th><th>Unit</th></tr>
<tr><td colspan="2">Die size including scribe line</td><td>6.32 x 4.90</td><td>mm</td></tr>
<tr><td colspan="2">Wafer size</td><td>200</td><td>mm</td></tr>
<tr><td colspan="2">Maximum possible dice per wafer</td><td>844</td><td>dice</td></tr>
<tr><td colspan="2">Die thickness</td><td>70</td><td>µm</td></tr>
<tr><td colspan="2">Front side passivation</td><td colspan="2">Silicon nitride</td></tr>
<tr><td colspan="2">Emitter pad size</td><td>1.50 x 1.20</td><td>mm</td></tr>
<tr><td colspan="2">Gate pad size</td><td>0.50 x 0.30</td><td>mm</td></tr>
<tr><td rowspan="2">Front side metallization</td><td>composition</td><td colspan="2">AlCu</td></tr>
<tr><td>thickness</td><td>4.5</td><td>µm</td></tr>
<tr><td rowspan="2">Back side metallization</td><td>composition</td><td colspan="2">Al/Ti/NiV/Ag</td></tr>
<tr><td>thickness</td><td>0.80</td><td>µm</td></tr>
<tr><td colspan="2">Die bond</td><td colspan="2">Electrically conductive glue or soft solder</td></tr>
<tr><td colspan="2">Recommended wire bonding</td><td>≤ 500</td><td>µm</td></tr>
</table>

2 Electrical ratings

T_J = 25 °C unless otherwise specified.

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CES}	Collector-emitter voltage (V_{GE} = 0 V)	650	V
V_{GE}	Gate-emitter voltage	±20	V
I_C [(1)]	Continuous collector current at T = 100 °C	60	A
I_{CP} [(1)(2)]	Pulsed collector current	180	A
T_J	Operating junction temperature range	-55 to 175	°C

1. *Current level depends on the assembly thermal properties.*
2. *Pulse width is limited by maximum junction temperature.*

3 Electrical characteristics

T_J = 25 °C unless otherwise specified.

Table 3. Static characteristics (tested on wafer unless otherwise specified)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)CES}$	Collector-emitter breakdown voltage	I_C = 2 mA, V_{GE} = 0 V	650			V
$V_{CE(sat)}$	Collector-emitter saturation voltage	V_{GE} = 15 V, I_C = 15 A			2.2	V
$V_{GE(th)}$	Gate threshold voltage	V_{CE} = V_{GE}, I_C = 1 mA	5	6	7	V
I_{CES}	Collector cut-off current	V_{GE} = 0 V, V_{CE} = 650 V			25	µA
I_{GES}	Gate-emitter leakage current	V_{CE} = 0 V, V_{GE} = ±20 V			±250	nA

Table 4. Electrical characteristics (evaluated by design/characterization, not tested in production)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{CE(sat)}$	Collector-emitter saturation voltage	V_{GE} = 15 V, I_C = 60 A	-	1.65	-	V
		V_{GE} = 15 V, I_C = 60 A, T_J = 175 °C	-	1.85	-	
C_{ies}	Input capacitance	V_{CE} = 25 V, f = 1 MHz, V_{GE} = 0 V	-	7792	-	pF
C_{oes}	Output capacitance		-	262	-	pF
C_{res}	Reverse transfer capacitance		-	158	-	pF
Q_g	Total gate charge	V_{CC} = 520 V, I_C = 60 A, V_{GE} = 0 to 15 V	-	306	-	nC
Q_{ge}	Gate emitter charge		-	126	-	nC
Q_{gc}	Gate collector charge		-	58	-	nC

Table 5. Switching characteristics on inductive load (evaluated by design/characterization, not tested in production)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	V_{CE} = 400 V, I_C = 60 A, V_{GE} = 15 V, R_G = 5 Ω	-	51	-	ns
t_r	Current rise time		-	22	-	ns
$t_{d(off)}$	Turn-off delay time		-	160	-	ns
t_f	Fall time		-	18	-	ns
E_{off} (1)	Turn-off switching energy		-	0.63	-	mJ
$t_{d(on)}$	Turn-on delay time	V_{CE} = 400 V, I_C = 60 A, V_{GE} = 15 V, R_G = 5 Ω, T_J = 175 °C	-	50	-	ns
t_r	Current rise time		-	30	-	ns
$t_{d(off)}$	Turn-off delay time		-	184	-	ns
t_f	Fall time		-	117	-	ns
E_{off} (1)	Turn-off switching energy		-	1.02	-	mJ

1. *Including the tail of the collector current.*

Note: The aforementioned values are not tested at chip level and are strongly dependent on the package/module design and the mounting technology. These values refer to the characterization of the device STGW60H65DFB with a specific test circuit. For more information, please refer to the STGW60H65DFB device datasheet.

4 Die layout

Figure 1. Die drawing (dimensions are in mm)

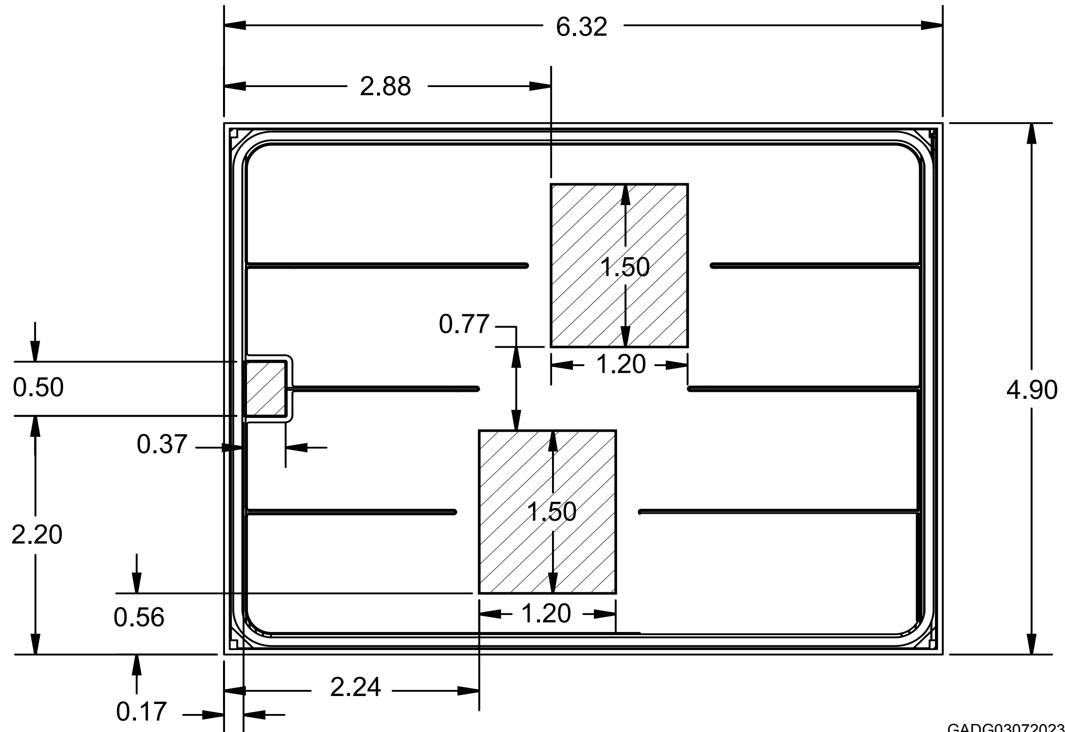
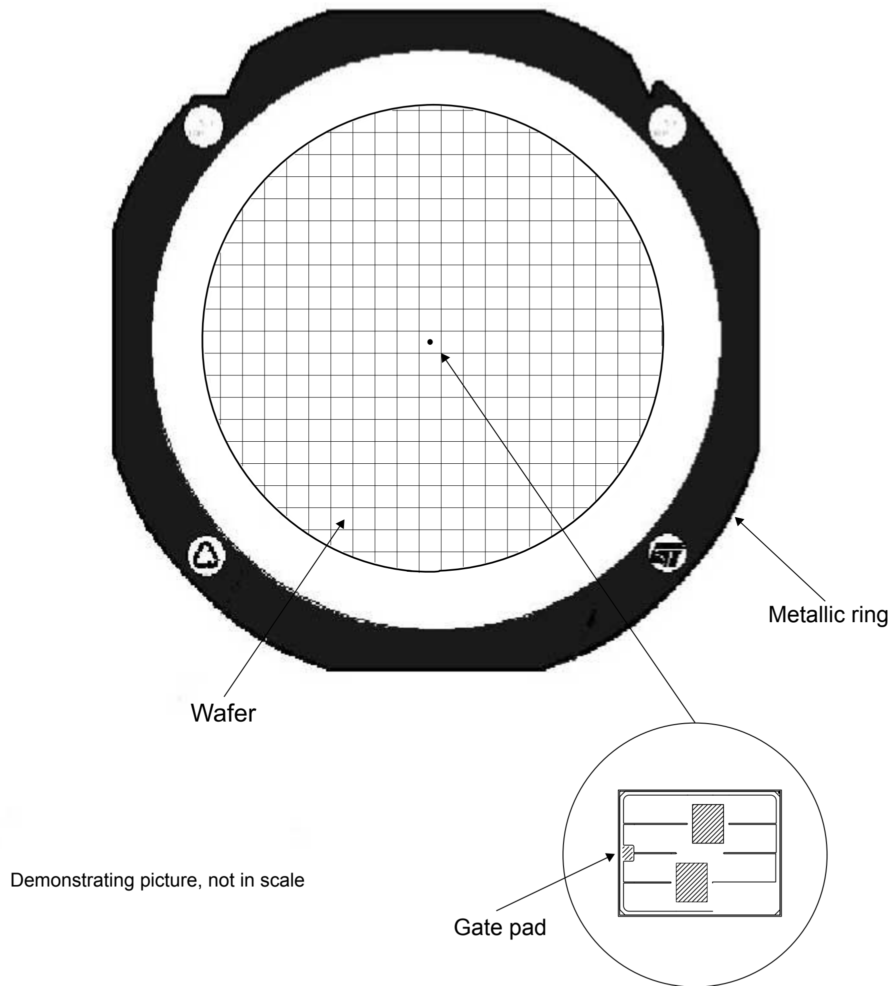


Table 6. Die delivery

Packing	Description	Details
D7	Wafer tested, inked, cut on sticky foil on metal ring 276 mm (see Figure 2. D7 drawing and die orientation)	Wafer is held by ring protected by two carton shells, inside a plastic envelope sealed under vacuum. Maximum number of wafers for each package is 25, weight is maximum 5 kg.

Figure 2. D7 drawing and die orientation



5 Additional information

5.1 Additional testing and screening

For customers requiring product supplied as known good die (KGD) or requiring specific die level testing (that is for dynamic and switching characterization), please contact the local ST sales office.

If KGD is requested, the shipping delivery is D8.

5.2 Shipping

Several shipping options are offered. Consult the local ST sales office for availability:

- Die on film-sticky foil - suffix on sales type D7
- Carrier tape - suffix on sales type D8

5.3 Handling

- Products must be handled only at ESD safe workstations. Standard ESD precautions and safe work environments are as defined in MIL-HDBK-263.
- Products must be handled only in a class 1000 or better-designated clean room environment.
- Singular die is not to be handled with tweezers. A vacuum wand with a nonmetallic ESD protected tip should be used.

5.4 Wafer/die storage

Once the packaging is opened, the wafer must be stored in a dry, inert atmosphere, such as nitrogen.

Optimum temperature for storage is 18 °C ±2 °C with as few variations as possible to avoid parasitic polymerization of the adhesive. Sawn wafers must be processed within 12 weeks after receipt by the customer.

After the customer opens the package, the customer is responsible for the products.

Revision history

Table 7. **Document revision history**

Date	Revision	Changes
13-Feb-2015	1	First release.
05-Mar-2015	2	Updated *Table 4.: Static characteristics (tested on wafer unless otherwise specified)* Minor text changes
06-Jul-2023	3	Updated Table 1. Mechanical parameters. Minor text changes.

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