STFW2N105K5

N-channel 1050 V, 6 Ω typ., 1.5 A Zener-protected SuperMESH™ 5 Power MOSFET in a TO-3PF package

Datasheet - preliminary data

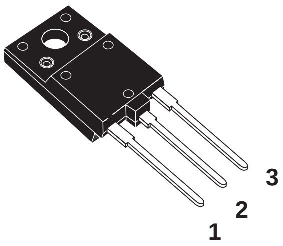
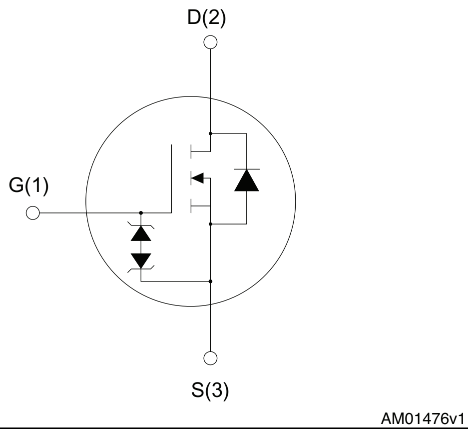


Figure 1. Internal schematic diagram



Features

Order code	V_{DS}	$R_{DS(on)}$ max	I_D	P_{TOT}
STFW2N105K5	1050 V	8 Ω	1.5 A	30 W

- Worldwide best FOM (figure of merit)
- Ultra low gate charge
- 100% avalanche tested
- Zener-protected

Applications

- Switching applications

Description

This N-channel Zener-protected Power MOSFET is designed using ST’s revolutionary avalanche-rugged very high voltage SuperMESH™ 5 technology, based on an innovative proprietary vertical structure. The result is a dramatic reduction in on-resistance, and ultra-low gate charge for applications which require superior power density and high efficiency.

Table 1. Device summary

Order code	Marking	Package	Packaging
STFW2N105K5	2N105K5	TO-3PF	Tube

This is preliminary information on a new product now in development or undergoing evaluation. Details are subject to change without notice.

Contents

1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{GS}	Gate- source voltage	30	V
I_D	Drain current (continuous) at T_C = 25 °C	2(1)	A
I_D	Drain current (continuous) at T_C = 100 °C	1.3(1)	A
I_{DM}	Drain current (pulsed)	6	A
P_{TOT}	Total dissipation at T_C = 25 °C	30	W
I_{AR}	Max current during repetitive or single pulse avalanche	0.5	A
E_{AS}	Single pulse avalanche energy (starting T_J = 25 °C, I_D=I_{AS}, V_{DD}= 50 V)	90	mJ
dv/dt (2)	Peak diode recovery voltage slope	4.5	V/ns
dv/dt(3)	MOSFET dv/dt ruggedness	50	V/ns
V_{ISO}	Insulation withstand voltage (RMS) from all three leads to external heat sink (t=1 s; TC=25 °C)	3500	V
T_j T_{stg}	Operating junction temperature Storage temperature	-55 to 150	°C

1. Pulse width limited by safe operating area.
2. $I_{SD} \leq 1.5$ A, di/dt $\leq$ 100 A/μs, $V_{Peak} \leq V_{(BR)DSS}$.
3. $V_{SD} \leq 840$ V

Table 3. Thermal data

Symbol	Parameter	Value	Unit
$R_{thj\text{-}case}$	Thermal resistance junction-case max	4.2	°C/W
$R_{thj\text{-}amb}$	Thermal resistance junction-ambient max	50	°C/W

2 Electrical characteristics

(Tcase =25 °C unless otherwise specified)

Table 4. On /off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	I_D = 1 mA, V_{GS} = 0	1050			V
I_{DSS}	Zero gate voltage, drain current (V_{GS} = 0)	V_{DS} = 1050 V			1	µA
		V_{DS} = 1050 V, T_C=125 °C			50	µA
I_{GSS}	Gate-body leakage current	V_{GS} = ± 20 V; V_{DS}=0			10	µA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 100 µA	3	4	5	V
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS} = 10 V, I_D = 0.75 A		6	8	Ω

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{DS} =100 V, f=1 MHz, V_{GS}=0	-	115	-	pF
C_{oss}	Output capacitance		-	15	-	pF
C_{rss}	Reverse transfer capacitance		-	0.5	-	pF
$C_{o(tr)}$(1)	Equivalent capacitance time related	V_{GS} = 0, V_{DS} = 0 to 840 V	-	17	-	pF
$C_{o(er)}$(2)	Equivalent capacitance energy related		-	6	-	pF
R_G	Intrinsic gate resistance	f = 1 MHz open drain	-	20	-	Ω
Q_g	Total gate charge	V_{DD} = 840 V, I_D = 1.5 A V_{GS} =10 V *(see Figure 16)*	-	10	-	nC
Q_{gs}	Gate-source charge		-	1.5	-	nC
Q_{gd}	Gate-drain charge		-	8	-	nC

1. Time related is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}
2. energy related is defined as a constant equivalent capacitance giving the same stored energy as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD} = 525 V, I_D = 0.75 A, R_G = 4.7 Ω, V_{GS} = 10 V *(see Figure 15)*	-	14.5	-	ns
t_r	Rise time		-	8.5	-	ns
$t_{d(off)}$	Turn-off-delay time		-	35	-	ns
t_f	Fall time		-	38.5	-	ns

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max	Unit
I_{SD}	Source-drain current		-		1.5	A
I_{SDM} (1)	Source-drain current (pulsed)		-		6	A
V_{SD} (2)	Forward on voltage	I_{SD} = 1.5 A, V_{GS} = 0	-		1.5	V
t_{rr}	Reverse recovery time	I_{SD} = 1.5 A, di/dt = 100 A/μs V_{DD}= 60 V *(see Figure 17)*	-	326		ns
Q_{rr}	Reverse recovery charge		-	1.19		μC
I_{RRM}	Reverse recovery current		-	7.3		A
t_{rr}	Reverse recovery time	I_{SD} = 1.5 A, di/dt = 100 A/μs V_{DD}= 60 V T_J = 150 °C *(see Figure 17)*	-	525		ns
Q_{rr}	Reverse recovery charge		-	1.83		μC
I_{RRM}	Reverse recovery current		-	7		A

1. Pulse width limited by safe operating area
2. Pulsed: pulse duration = 300 μs, duty cycle 1.5%

Table 8. Gate-source Zener diode

Symbol	Parameter	Test conditions	Min	Typ.	Max.	Unit
$V_{(BR)GSO}$	Gate-source breakdown voltage	I_{GS} = ± 1mA, I_D=0	30	-	-	V

The built-in back-to-back Zener diodes have specifically been designed to enhance the device's ESD capability. In this respect the Zener voltage is appropriate to achieve an efficient and cost-effective intervention to protect the device's integrity. These integrated Zener diodes thus avoid the usage of external components.

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

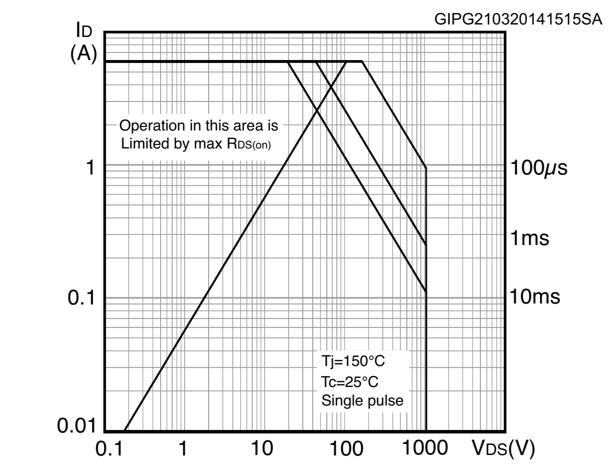


Figure 3. Thermal impedance

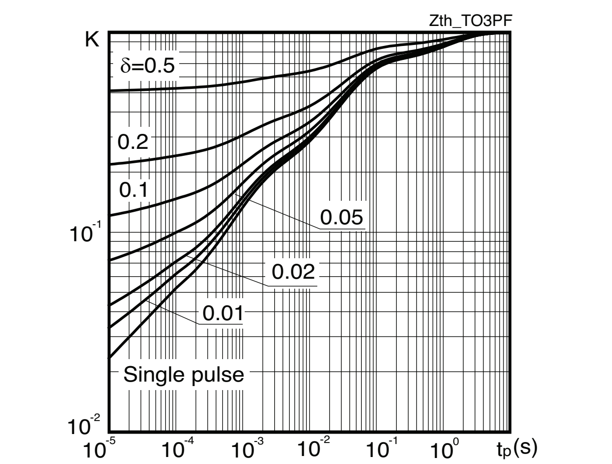


Figure 4. Output characteristics

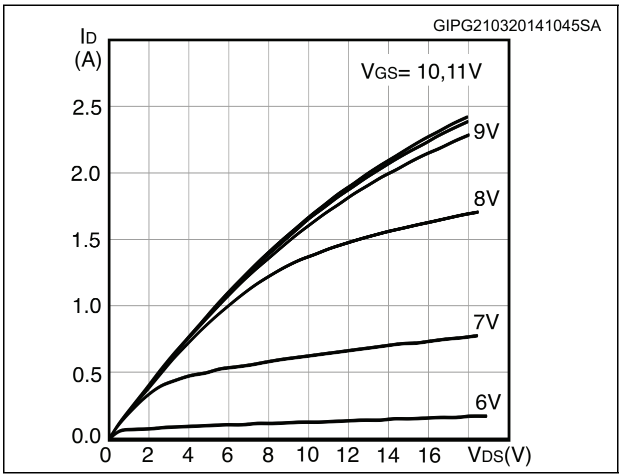


Figure 5. Transfer characteristics

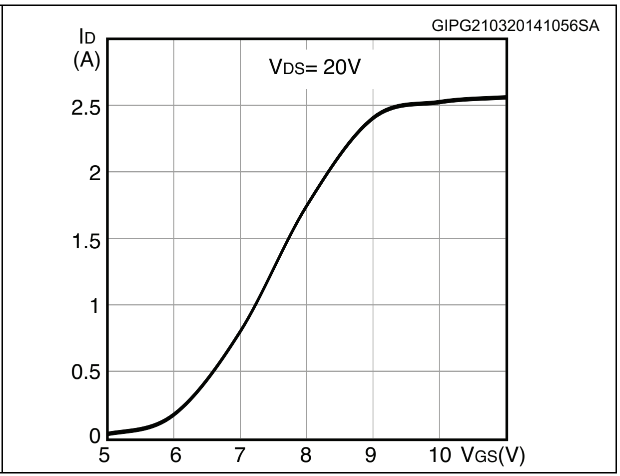


Figure 6. Gate charge vs gate-source voltage

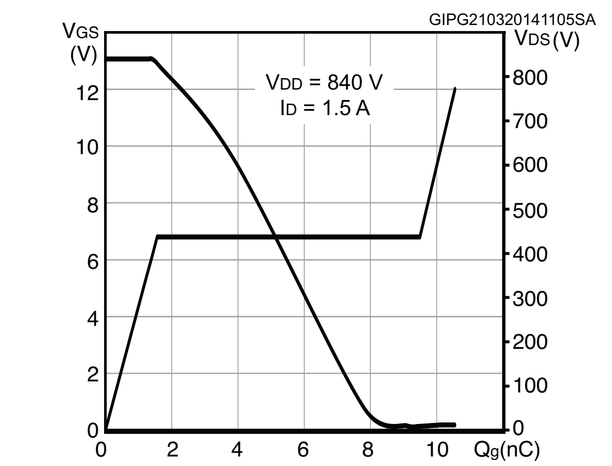


Figure 7. Static drain-source on-resistance

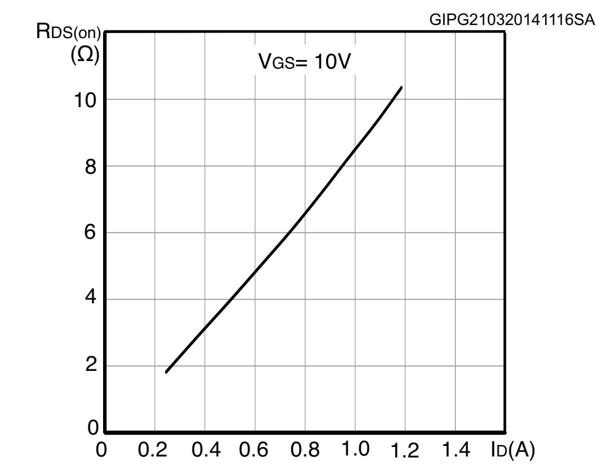


Figure 8. Capacitance variations

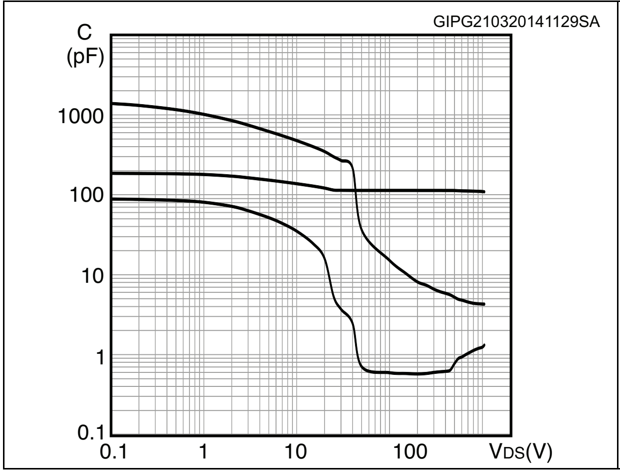


Figure 9. Output capacitance stored energy

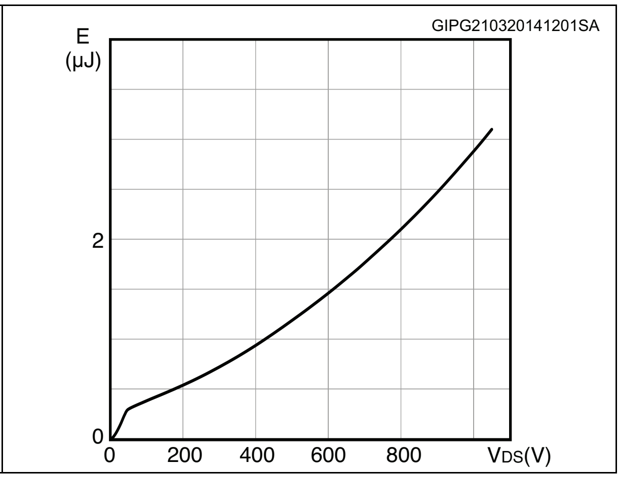


Figure 10. Normalized gate threshold voltage vs temperature

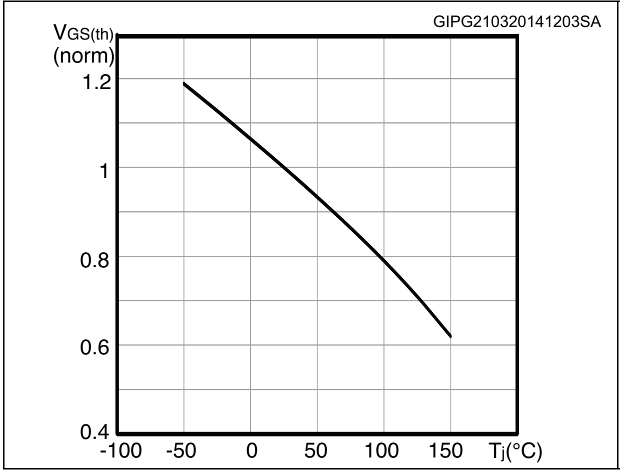


Figure 11. Normalized on-resistance vs temperature

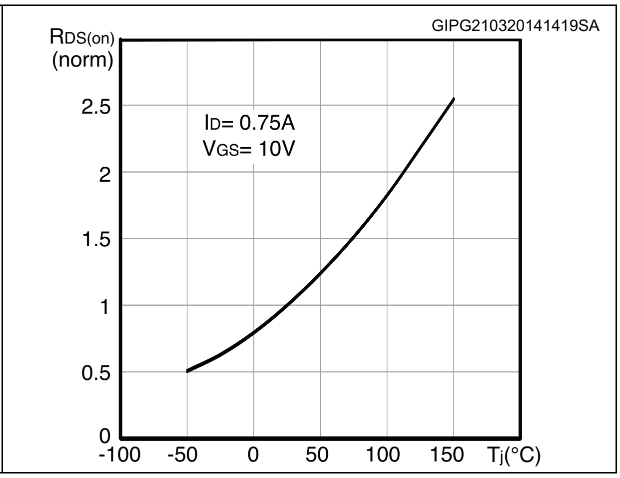


Figure 12. Source-drain diode forward characteristics

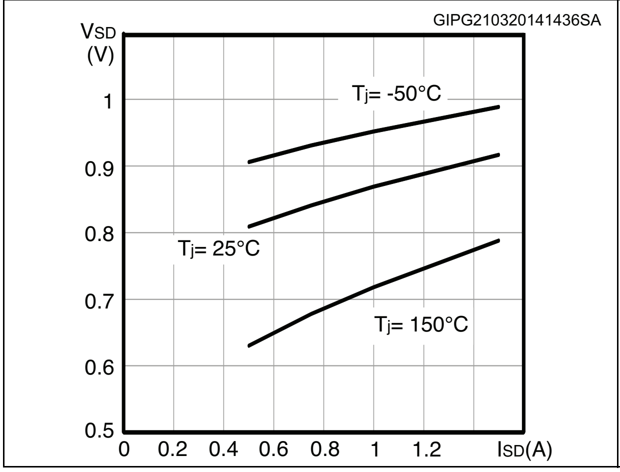


Figure 13. Normalized $V_{(BR)DSS}$ vs temperature

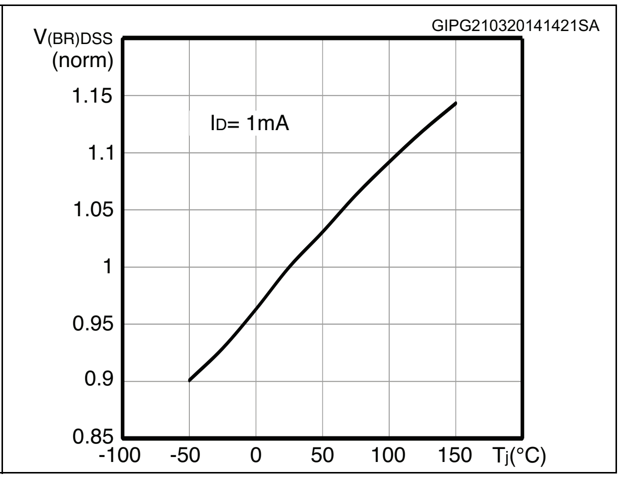
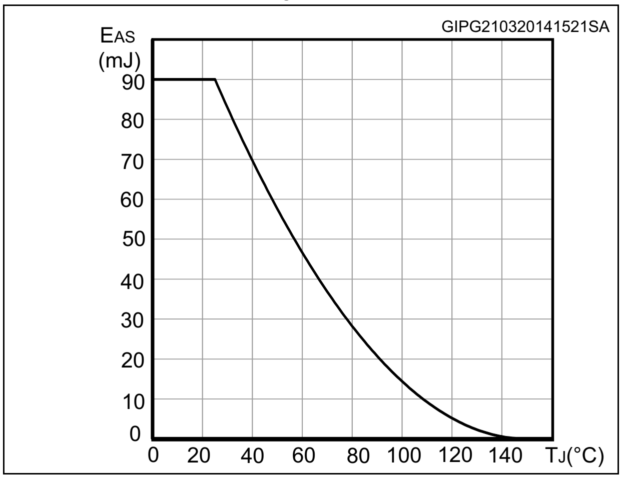


Figure 14. Maximum avalanche energy vs starting T_J



3 Test circuits

Figure 15. Switching times test circuit for resistive load

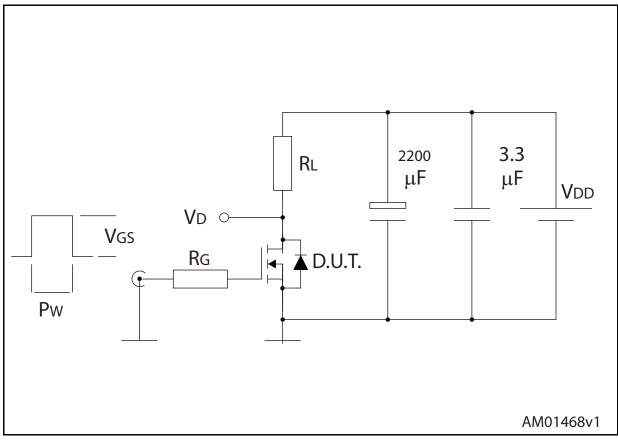


Figure 16. Gate charge test circuit

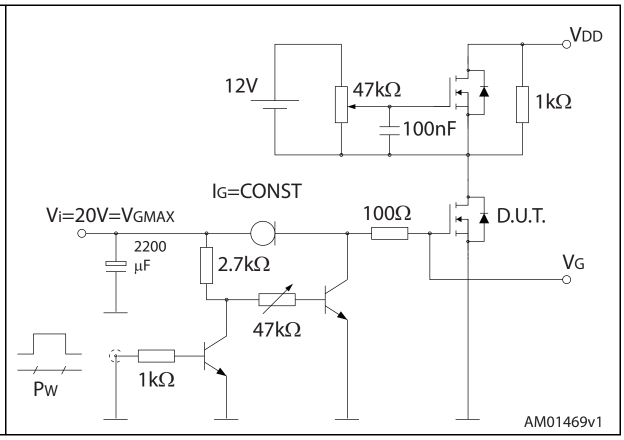


Figure 17. Test circuit for inductive load switching and diode recovery times

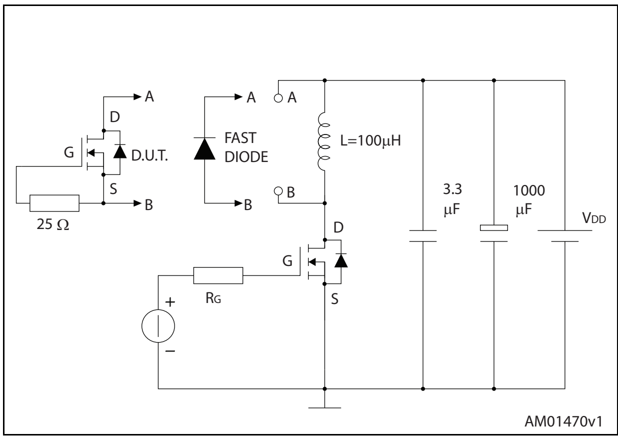


Figure 18. Unclamped inductive load test circuit

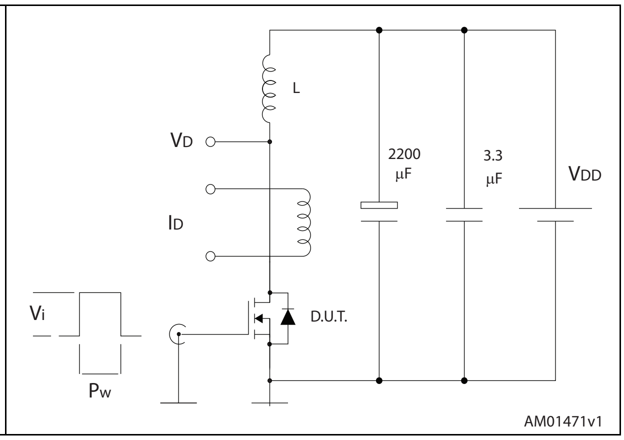


Figure 19. Unclamped inductive waveform

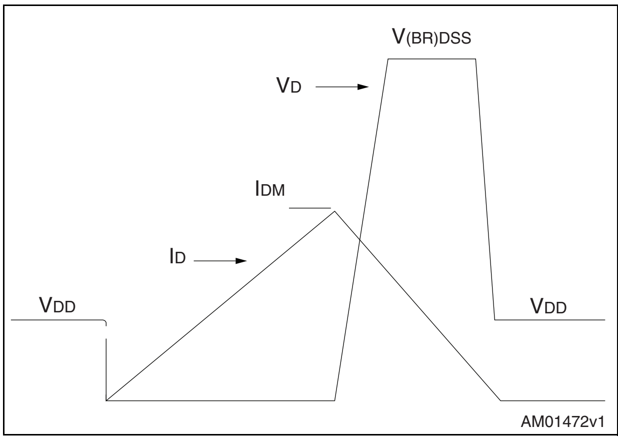
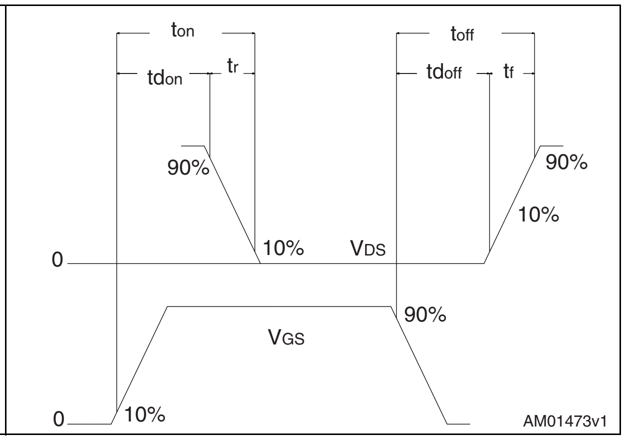


Figure 20. Switching time waveform



4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

Figure 21. TO-3PF drawing

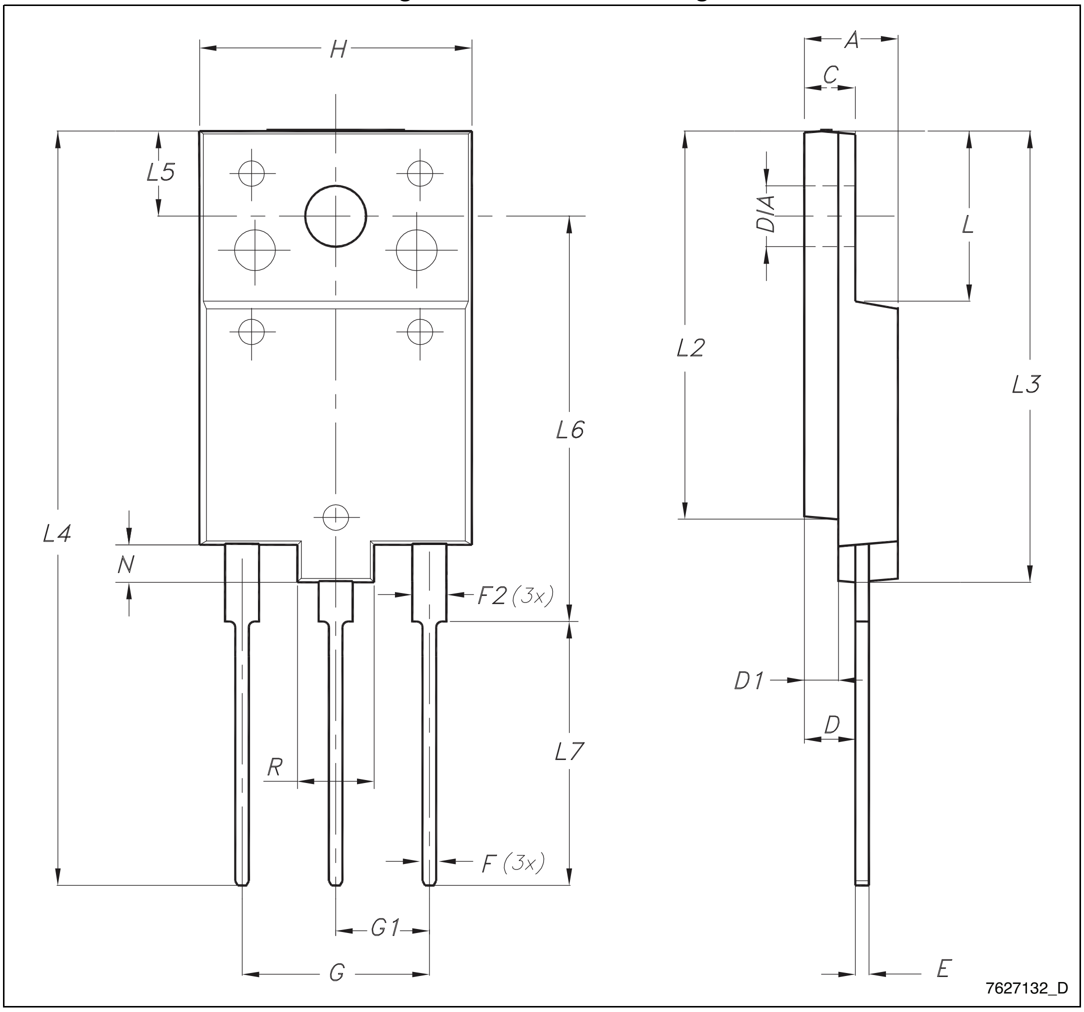


Table 9. TO-3PF mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	5.30		5.70
C	2.80		3.20
D	3.10		3.50
D1	1.80		2.20
E	0.80		1.10
F	0.65		0.95
F2	1.80		2.20
G	10.30		11.50
G1		5.45	
H	15.30		15.70
L	9.80	10	10.20
L2	22.80		23.20
L3	26.30		26.70
L4	43.20		44.40
L5	4.30		4.70
L6	24.30		24.70
L7	14.60		15
N	1.80		2.20
R	3.80		4.20
Dia	3.40		3.80

5 Revision history

Table 10. Document revision history

Date	Revision	Changes
08-May-2014	1	First release.