



STE140NF20D

N-channel 200 V, 0.010 Ω, 140 A, ISOTOP
STripFET™ II with fast recovery diode Power MOSFET

Preliminary Data

Features

Type	V _{DSS}	R _{DS(on)} max	I _D
STE140NF20D	200 V	< 0.012 Ω	140 A

- Exceptional dv/dt capability
- Low gate charge
- 100% avalanche tested

Application

- Switching applications

Description

This Power MOSFET is produced using STMicroelectronics' unique STripFET™ process, which is specifically designed to minimize input capacitance and gate charge. The STE140NF20D offers extremely fast switching performance thanks to the intrinsic fast body diode, making the device ideal for hard switching topologies.

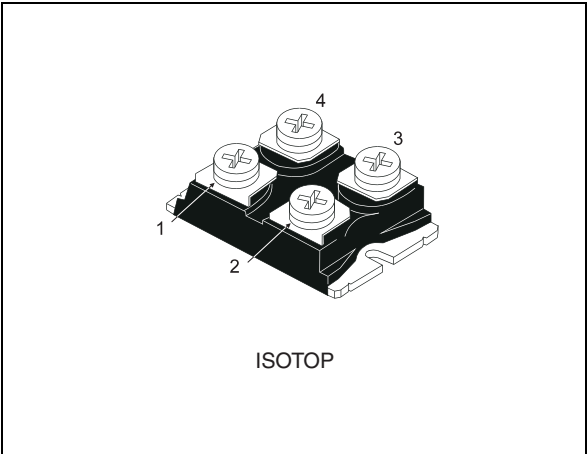


Figure 1. Internal schematic diagram

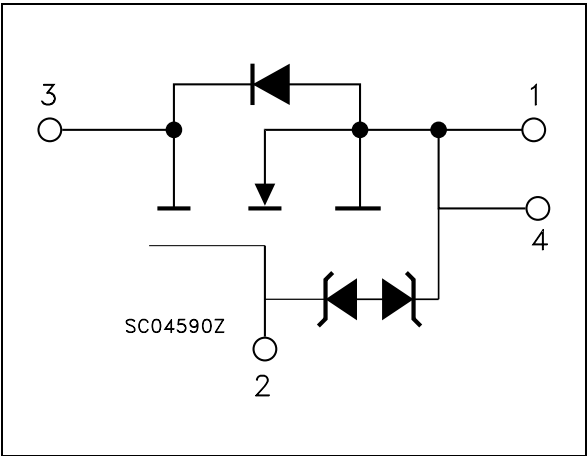


Table 1. Device summary

Order code	Marking	Package	Packaging
STE140NF20D	140NF20D	ISOTOP	Tube

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1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage ($V_{GS} = 0$)	200	V
V_{GS}	Gate-source voltage	± 20	V
$I_D^{(1)}$	Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$	140	A
$I_D^{(1)}$	Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$	260	A
$I_{DM}^{(2)}$	Drain current (pulsed)	560	A
$P_{TOT}^{(2)}$	Total dissipation at $T_C = 25\text{ }^\circ\text{C}$	500	W
	Derating factor	4	W/ $^\circ\text{C}$
$dv/dt^{(3)}$	Peak diode recovery voltage slope	25	V/ns
T_J T_{stg}	Operating junction temperature Storage temperature	- 55 to 150	$^\circ\text{C}$

1. The value is rated according $R_{thj-pcb}$
2. Pulse width limited by safe operating area
3. $I_{SD} \leq 30\text{ A}$, $di/dt \leq \text{TBD A}/\mu\text{s}$, $V_{DD} \leq 80\% V_{(BR)DSS}$

Table 3. Thermal resistance

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case	0.25	$^\circ\text{C}/\text{W}$
$R_{thj-amb}$	Thermal resistance junction-ambient	40	$^\circ\text{C}/\text{W}$

Table 4. Avalanche data

Symbol	Parameter	Value	Unit
I_{AR}	Avalanche current, repetitive or not repetitive ⁽¹⁾	TBD	A
E_{AS}	Single pulse avalanche energy ⁽²⁾	TBD	mJ

1. Pulse width limited by T_{jmax}
2. Strating $T_j = 25\text{ }^\circ\text{C}$, $I_D = I_{AR}$, $V_{DD} = 50\text{ V}$

2 Electrical characteristics

($T_{CASE} = 25\text{ }^{\circ}\text{C}$ unless otherwise specified)

Table 5. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = 1\text{ mA}$, $V_{GS} = 0$	200			V
I_{DSS}	Zero gate voltage drain current ($V_{GS} = 0$)	$V_{DS} = \text{max rating}$, $V_{DS} = \text{max rating @ } 125\text{ }^{\circ}\text{C}$			10 100	μA μA
I_{GSS}	Gate body leakage current ($V_{DS} = 0$)	$V_{GS} = \pm 21\text{ V}$			± 100	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$, $I_D = 250\text{ }\mu\text{A}$	2	3	4	V
$R_{DS(on)}$	Static drain-source on resistance	$V_{GS} = 10\text{ V}$, $I_D = 70\text{ A}$		0.010	0.012	Ω

Table 6. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
g_{fs}	Forward transconductance	$I_D = 140\text{ A}$, $V_{DS} = 150\text{ V}$		TBD		
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	$V_{DS} = 25\text{ V}$, $f = 1\text{ MHz}$, $V_{GS} = 0$		9900 2000 450		pF pF pF
Q_g Q_{gs} Q_{gd}	Total gate charge Gate-source charge Gate-drain charge	$V_{DD} = 480\text{ V}$, $I_D = 140\text{ A}$ $V_{GS} = 4.5\text{ V}$ (see Figure 3)		390 TBD TBD		nC nC nC

Table 7. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 100\text{ V}$, $I_D = 70\text{ A}$, $R_G = 4.7\ \Omega$, $V_{GS} = 10\text{ V}$ (see Figure 2)		TBD		ns
t_r	Rise time			TBD		ns
$t_{d(off)}$	Turn-off delay time			TBD		ns
t_f	Fall time			TBD		ns

Table 8. Source drain diode

Symbol	Parameter	Test conditions	Min	Typ.	Max	Unit
I_{SD}	Source-drain current				140	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)				560	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 70\text{ A}$, $V_{GS} = 0$			1.6	V
t_{rr}	Reverse recovery time	$I_{SD} = 70\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$, $V_{DD} = 100\text{ V}$, $T_j = 150\text{ }^\circ\text{C}$		TBD		ns
Q_{rr}	Reverse recovery charge			TBD		nC
I_{RRM}	Reverse recovery current			TBD		A

1. Pulse width limited by safe operating area
2. Pulsed: pulse duration=300 μs , duty cycle 1.5%

Test circuit

3 Test circuit

Figure 2. Switching times test circuit for resistive load

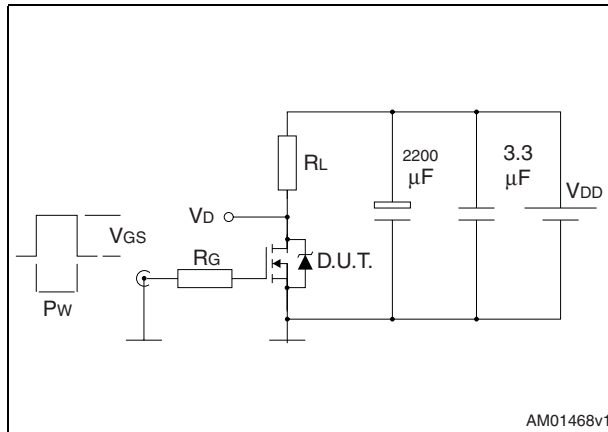


Figure 3. Gate charge test circuit

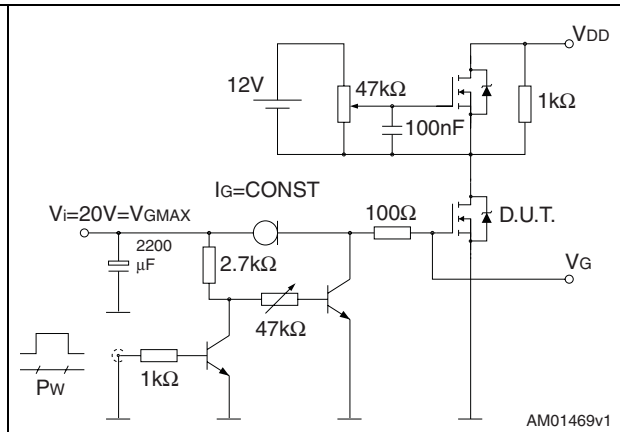


Figure 4. Test circuit for inductive load switching and diode recovery times

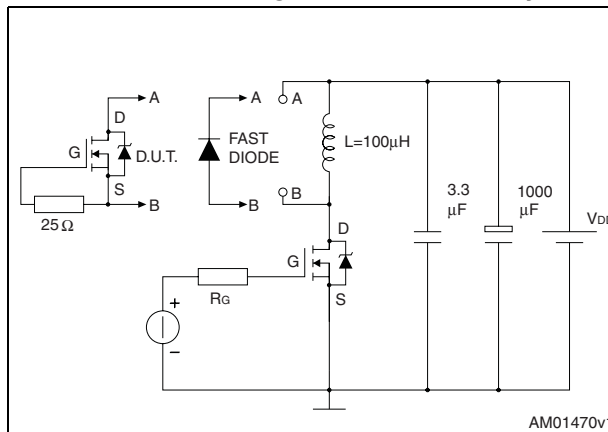


Figure 5. Unclamped inductive load test circuit

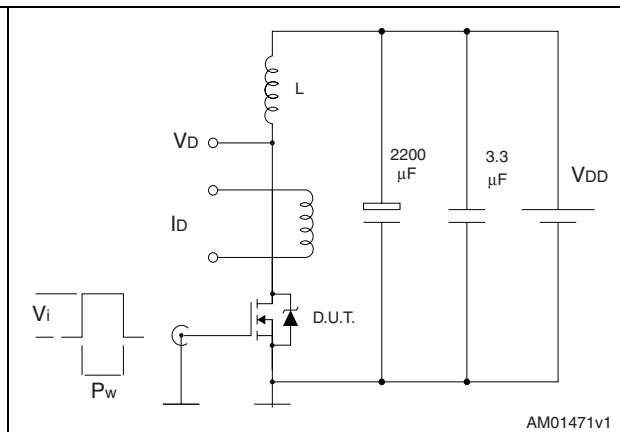


Figure 6. Unclamped inductive waveform

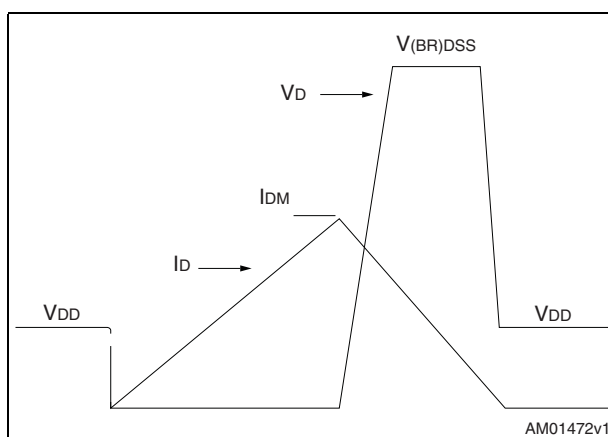
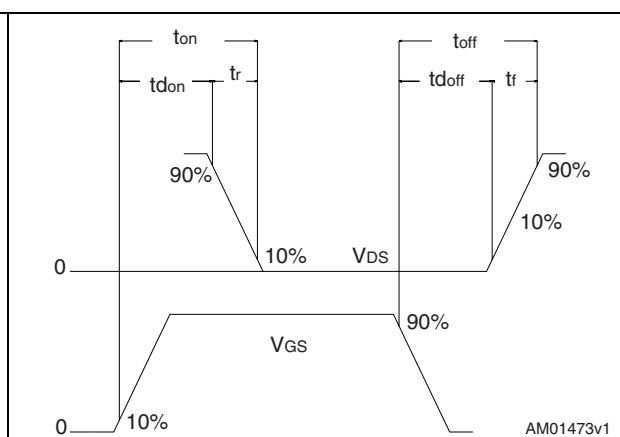


Figure 7. Switching time waveform



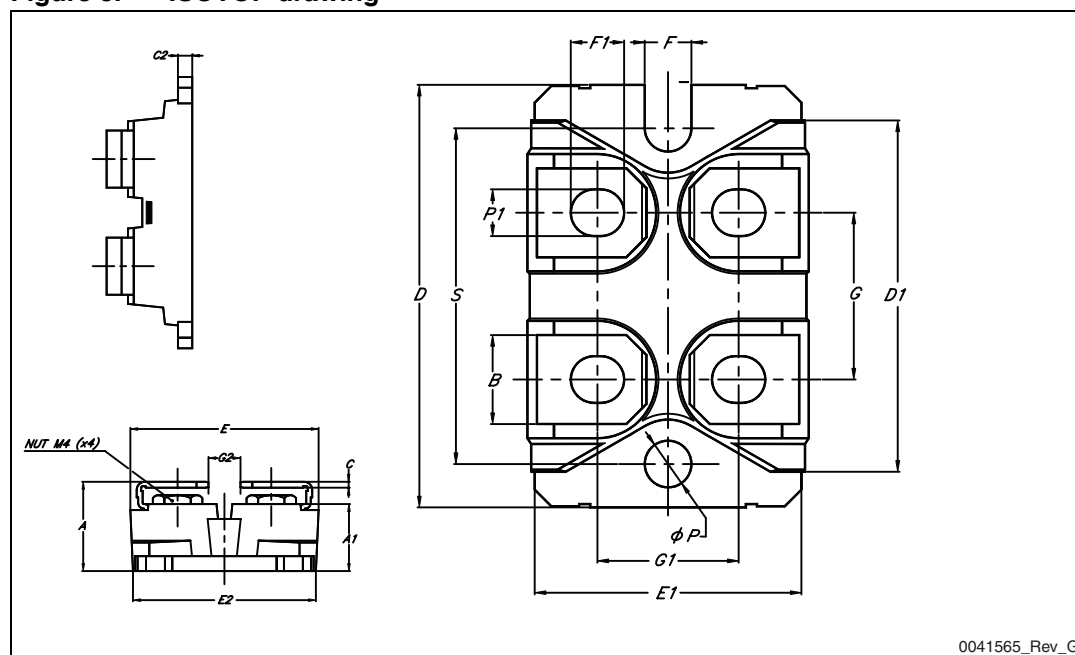
4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

Table 9. ISOTOP mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	11.80		12.20
A1	8.90		9.10
B	7.80		8.20
C	0.75		0.85
C2	1.95		2.05
D	37.80		38.20
D1	31.50		31.70
E	25.15		25.50
E1	23.85		24.15
E2		24.80	
G	14.90		15.10
G1	12.60		12.80
G2	3.50		4.30
F	4.10		4.30
F1	4.60		5
ϕP	4		4.30
P1	4		4.40
S	30.10		30.30

Figure 8. ISOTOP drawing



5 Revision history

Table 10. Document revision history

Date	Revision	Changes
27-Jan-2009	1	First release

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