STDP3150
DisplayPort to VGA converter

Datasheet

Rev F

MegaChips

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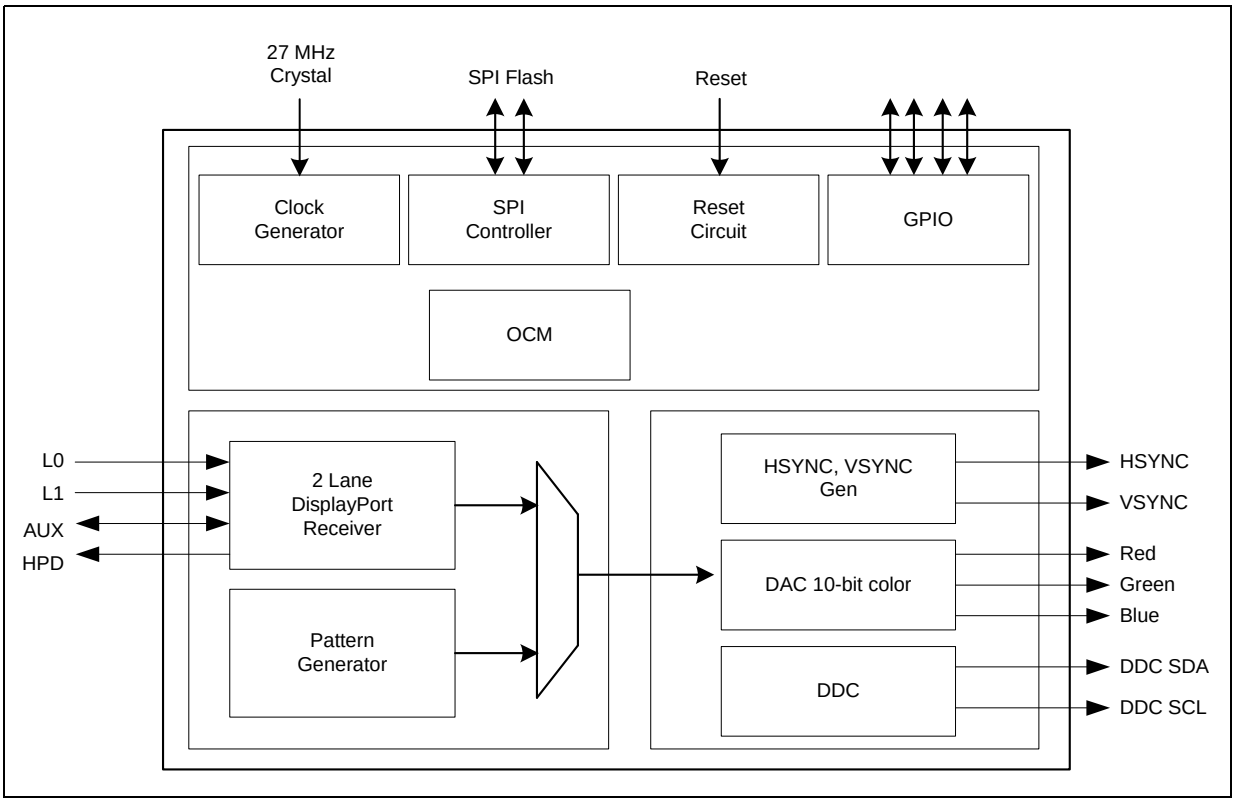
Features

- Two lane DisplayPort® 1.2a receiver
- Triple 10-bit video DAC
  - 162 MSPS throughput rate
  - VSIS compatible
  - RGB output with 0 to 700 mV range
- 3.3 V HSYNC, VSYNC
- Resolution through WUXGA
- EDID, MCCS pass-through support
- 3.3 V DDC output signals
- Sink detection logic
- Low power operation – Active 400 mW, standby mode 15 mW
- Package: 64-pin QFN, 6 x 6 mm

Applications

- DisplayPort to VGA dongle as an attachment to notebook and desktop PCs
- DisplayPort to VGA conversion for notebook and desktop PC motherboard applications



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1. Description

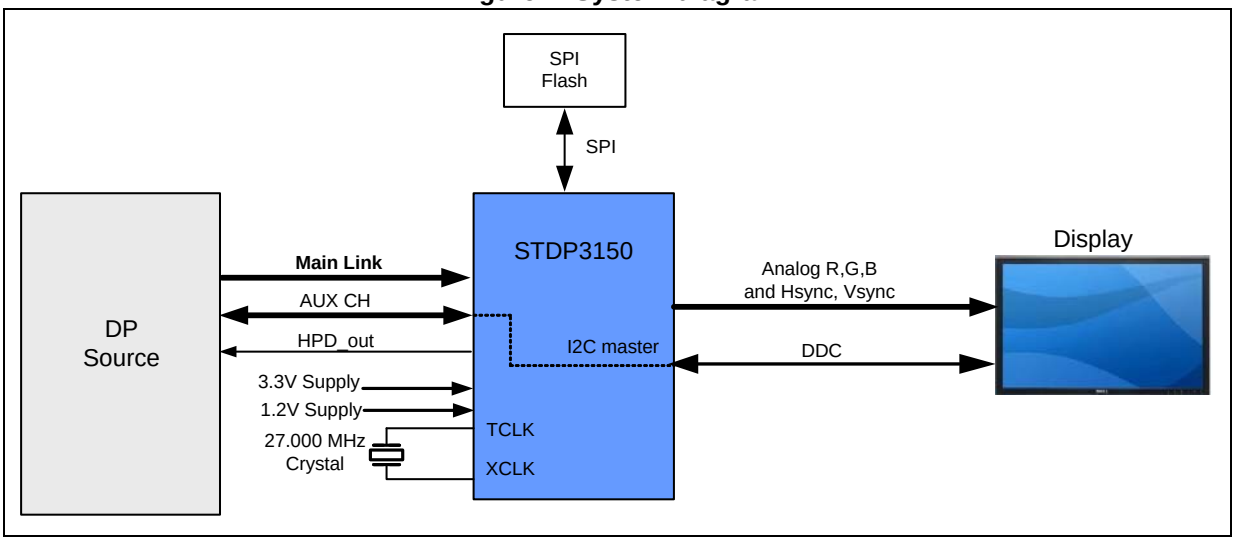
STDP3150 is a DisplayPort to VGA signal format converter for interfacing DisplayPort based PC, notebook, tablet, and smart phones with conventional VGA displays. DisplayPort offers a unified, scalable, and cost effective interface for embedded and external display applications. As desktop and notebook PCs are increasingly transitioning from conventional analog type interfaces to DisplayPort, STDP3150 facilitates the transition by offering seamless connectivity between new DisplayPort PC, notebooks, and the installed base VGA monitors and projectors. Besides the dongle application, STDP3150 is also a perfect fit for the notebook and desktop motherboard designs based on new generation Intel, AMD CPU/GPU architecture. STDP3150 is a highly integrated converter featuring a DisplayPort receiver, video DAC, clock form generator, test pattern generator, and sink detection block. In addition, STDP3150 includes EDID and MCCS pass-through features, forming a fully transparent operation between the PC and display. Active power consumption of this device is as low as 400 mW, and thus it can be powered by the DisplayPort source when used in a dongle application. The device has a built-in sink detection feature that determines the active and standby state. The device enters into standby (low power) state whenever the VGA cable is disconnected and returns to normal operation when the cable is connected back.

STDP3150 supports video resolutions from VGA through WUXGA. The input DisplayPort interface consists of two main lanes, AUX channel, and HPD signal that maps directly to a standard DisplayPort connector via two layers PCB. The output interface consists of analog R, G, B video, Hsync, Vsync, and DDC signals. Analog video signal amplitude ranges from 0 to 700 mV from a 10-bit video DAC with maximum sampling frequency of 162 MHz. The VGA output signal interface conforms to the VSIS standards with separate Hsync and Vsync control signals. The DDC_SDA and DDC_CLK signals are driven from an I2C master, which controls I2C traffic between the DisplayPort AUX channel and external slave device.

2. Application overview

MegaChips offers an STDP3150 designers kit with complete reference hardware and firmware.

Figure 1. System diagram



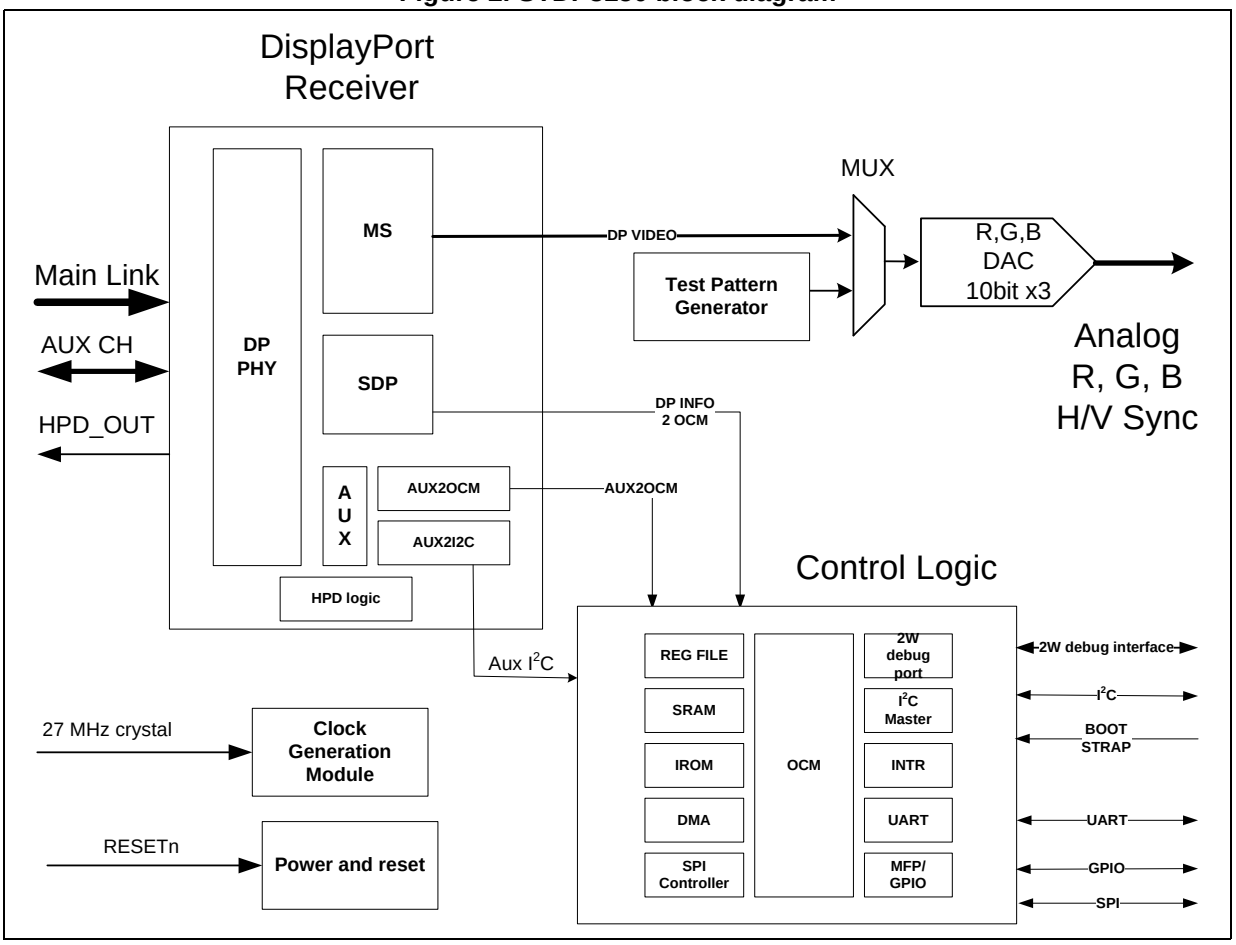
3. Feature attributes

- Production-proven DisplayPort receiver from the DisplayPort leader
- Comprehensive feature set for DisplayPort to VGA dongle and for notebook embedded application
- Proven interoperability with DisplayPort sources from all major graphics vendors
- Cost savings due to optimized BOM, low power, low EMI, and small form factor
- DisplayPort CTS compliant
- Windows based software tool for factory/field upgrade – programs over DP AUX channel
- DisplayPort 1.2a compliant receiver offering 5.4 Gbps bandwidth over two lanes
- Integrated triple 10-bit, 162 MHz video DAC for analog VGA signal output
- Supports up to 1080p, 1920 x 1200 reduced blanking video resolution
- EDID and MCCS pass-through from PC source to display
- Spread spectrum (de-spreading) for EMI reduction
- Automatic sink detection
- Low power standby mode operation initiated based on sink detection status
- SPI interface with external Serial Flash for storing firmware and system configuration data for customization purposes
- Optional two-wire host interface for device configuration using external controller
- UART interface for chip debug and development purpose
- ISP over DP AUX channel
- General-purpose I/O pins for system usage
- Powered from DisplayPort source
- 3.3 V IO, 1.2 V Core
- 64-pin QFN (6 x 6 mm) package

4. Functional block description

4.1 Block diagram

Figure 2. STDP3150 block diagram



4.2 Power sequence

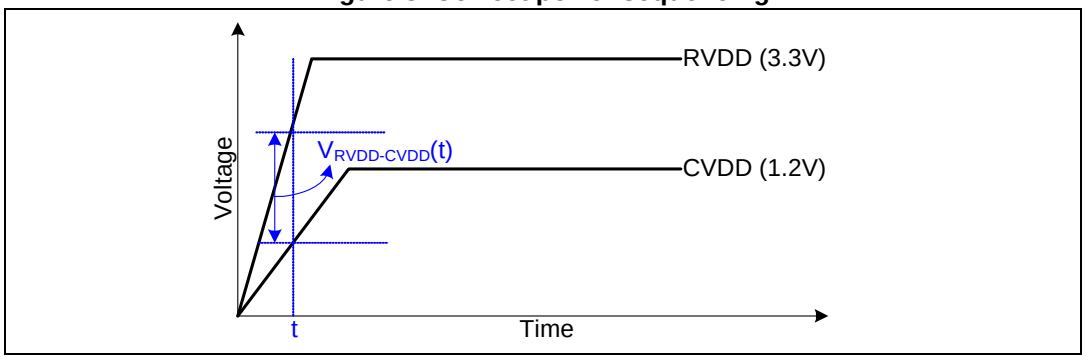
When using linear regulators for the 3.3 V and 1.2 V supplies, precautions must be taken in designing the power supply system to meet the following requirements.

At any time during the power-up sequence, the actual voltage of the 3.3 V ring VDD (RVDD) power supply should always be equal to or higher than the actual voltage of the 1.2 V core VDD (CVDD). In mathematical terms, VRVDD >= VCVDD at all times.

Table 1. Power sequencing requirements

Parameter	Min	Typ	Max
VRVDD-VCVDD (for all t>0)	0 V	1.50 V	-

Figure 3. Correct power sequencing



4.3 Power-on reset

The STDP3150 device has an integrated reset pulse generator. The internal reset pulse generator performs hardware reset under the following conditions:

- During system power-up, after the RVDD_3V3 voltage has reached reset threshold voltage V_T
- In the event RVDD_3V3 voltage drops below threshold V_T for more than approximately 150 ns
- Manually holding the RESETn pin low for a minimum of 1 ms

The active-low reset pulse on the RESETn pin generated by the internal reset pulse generator is described in the table below. During the reset period, all internal circuits and logic are reset to the default power-on state. To ensure proper chip operation, TCLK (generated by crystal oscillator or from the external clock source) must be applied during and after the reset.

The following figure shows the relationship between RVDD_3V3 and RESETn during system power-up.

Figure 4. Power-up reset sequence between RVDD_3.3V and RESETn pin

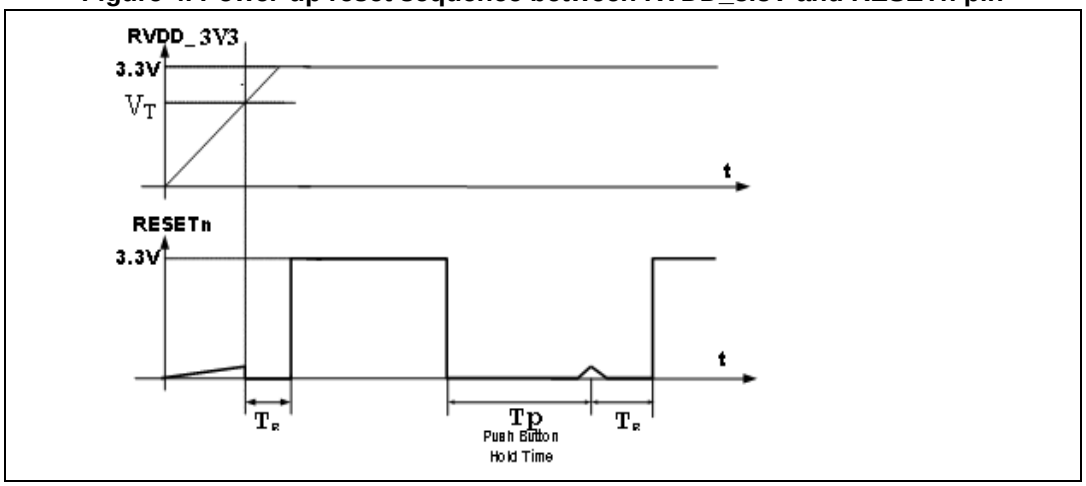


Table 2. Power-on reset characteristics

Description	Symbol	Min	Typ	Max
Power-on reset threshold voltage	V_T	2.60 V	2.70 V	2.80 V
Reset pulse duration	T_R	150 ms	160 ms	250 ms
Push-button hold time	T_P	1 ms	-	-

The glitch filter inside the internal reset pulse generator ignores the RVDD_3V3 power line glitch if the duration of the glitch is shorter than approximately 150 ns. However, if RVDD_3V3 voltage drops below the threshold V_T for more than 150 ns in duration, reset is asserted and RESETn signal goes low. The following figure illustrates the RVDD_3V3 glitch.

Figure 5. RVDD_3V3 glitch

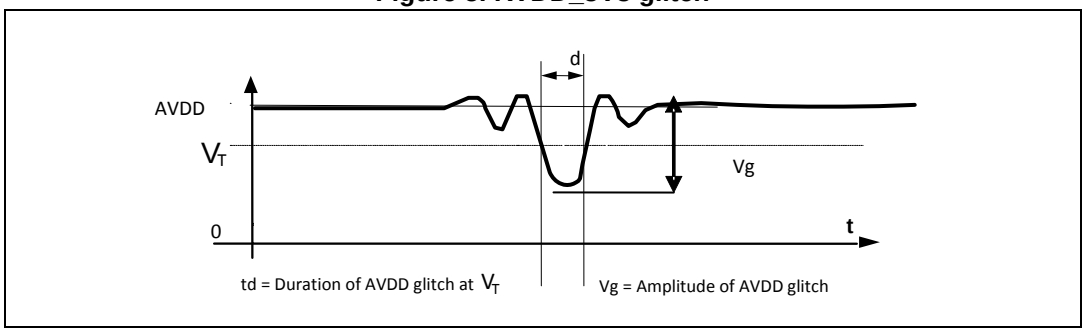


Table 3. RVDD_3.3V glitch-Induced reset specifications

Description	Symbol	Min	Typ	Max
RVDD_3V3 glitch duration	tg	150 ns		
RVDD_3V3 glitch amplitude	Vg	0.9 V(1)		1.2 V(1)

1. The RESETn pin must connect to RVDD with a pull-up resistor of 2.7 K.

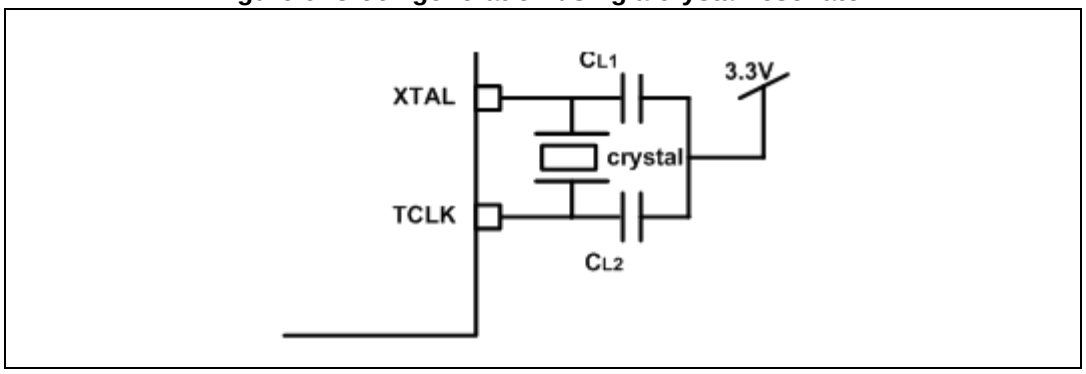
The RVDD_3V3 voltage must fall by more than Vg below the supply voltage (3.3 V nominal) for the reset to assert (RESETn becomes low). For example, RVDD_3V3 voltage level must fall below at least 2.4 V (3.3 V - 0.9 V) in order for reset to assert.

4.4 Clock generation

TCLK is the main timing clock for this device. All other internal clocks are generated from the TCLK. The TCLK oscillator circuitry is a custom designed circuit to support the use of an external oscillator (27 MHz) or a crystal resonator (27 MHz) to generate a reference frequency source, as shown in the figure below.

The internal oscillator circuit is designed to provide a very low jitter and low harmonic clock to the internal circuitry of the STDP3150, using an external crystal. The internal oscillator circuit also minimizes the overdrive of the crystal, which reduces the aging of the crystal. An Automatic Gain Control (AGC) circuit insures proper startup and operation over a wide range of conditions.

Figure 6. Clock generation using a crystal resonator

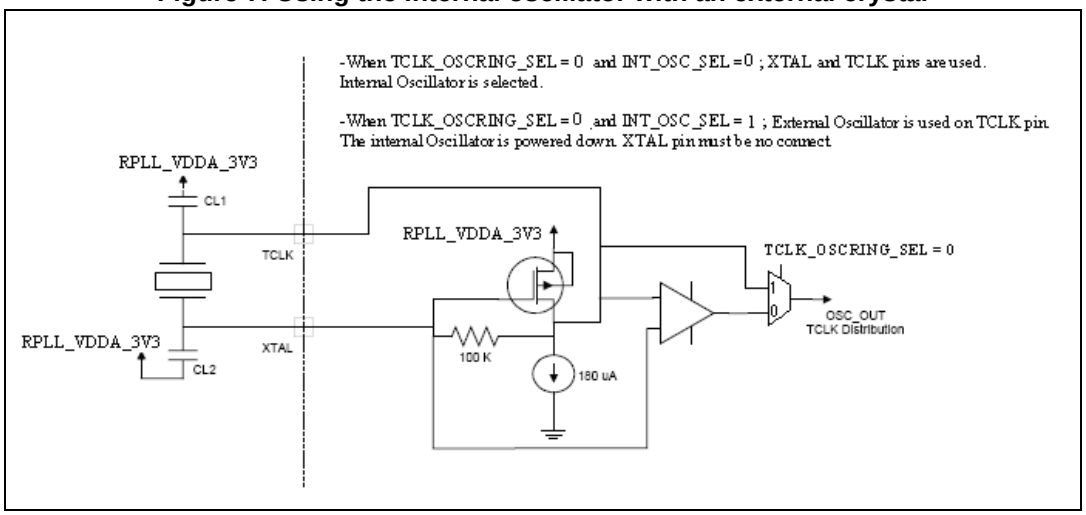


4.4.1 Internal crystal oscillator operation

When the STDP3150 chip is in reset, the state of the bootstrap TCLK_OSCRING_SEL pin and INT_OSC_SEL pin are sampled. If both the bootstrap pins are pulled LOW (by connecting the pin to VSS through a pull-down resistor), the internal oscillator is enabled. The maximum value of the pull-down resistor is 15 K (typical value 4.7 K) ohm. In this mode, a crystal resonator is connected between the XTAL pin and the TCLK pin with the appropriately sized loading capacitors CL1 and CL2.

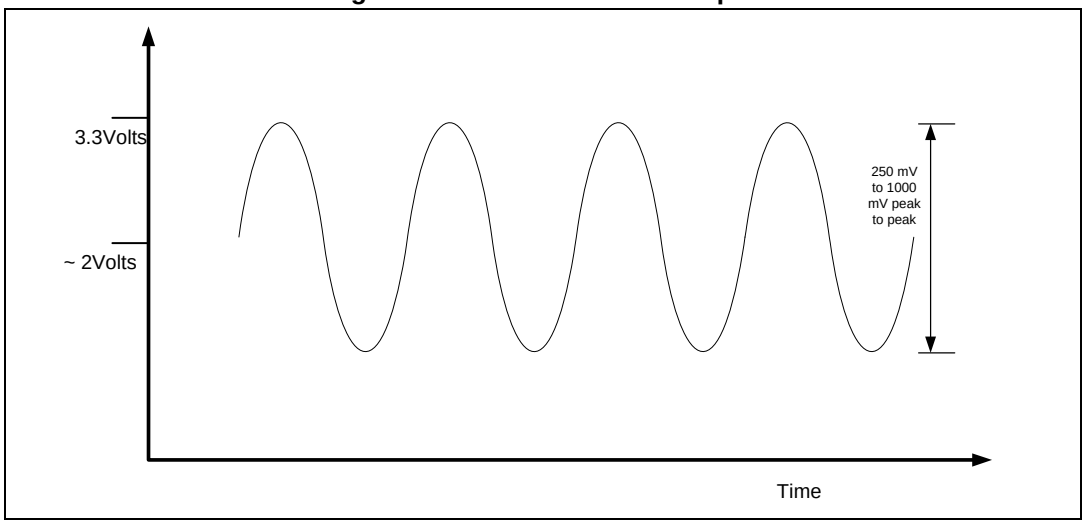
Note: The size of CL1 and CL2 are determined from the crystal manufacturer's specification and by compensating for the parasitic capacitance of the device and the printed circuit board traces. The loading capacitors are terminated to the RPLL_VDDA_3V3 power supply. This connection increases the power supply rejection ratio when compared to terminating the loading capacitors to ground.

Figure 7. Using the internal oscillator with an external crystal



The internal oscillator circuit is a Pierce Oscillator circuit and a simplified schematic is shown in the above figure. The output of the oscillator circuit, measured at the TCLK pin, is an approximate sine wave with a bias of about 2 volts above ground (see figure below). The peak-to-peak voltage of the output can range from 250 mV to 1000 mV, depending on the specific characteristics of the crystal and variation in the oscillator characteristics. The output of the oscillator feeds to a comparator that converts the sine wave to a square wave. The comparator requires a minimum signal level of about 50-mV peak to peak to function correctly. Comparator output is buffered and the signal is distributed to the rest of STDP3150 circuits.

Figure 8. Internal oscillator output



One of the design parameters that must be given some consideration is the value of the loading capacitors used with the crystal, as shown below. The loading capacitance (C_{load}) on the crystal is the combination of CL1 and CL2 and is calculated by C_{load} = ((CL1 * CL2)/(CL1 + CL2)) + C_{shunt}. The shunt capacitance C_{shunt} is the effective capacitance between the XTAL and TCLK pins. For STDP3150, this is approximately 9 pF. CL1 and CL2 are a parallel combination of the external loading capacitors (Cex), the PCB board capacitance (C_{pcb}), the pin capacitance (C_{pin}), the pad capacitance (C_{pad}), and the ESD protection capacitance (C_{esd}). The capacitances are symmetrical so that CL1 = CL2 = C_{ex} + C_{PCB} + C_{pin} + C_{pad} + C_{ESD}. The correct value of Cex must be calculated based on the values of the load capacitances.

CPCB ~ Layout dependent. Approximately 2 pF to 10 pF

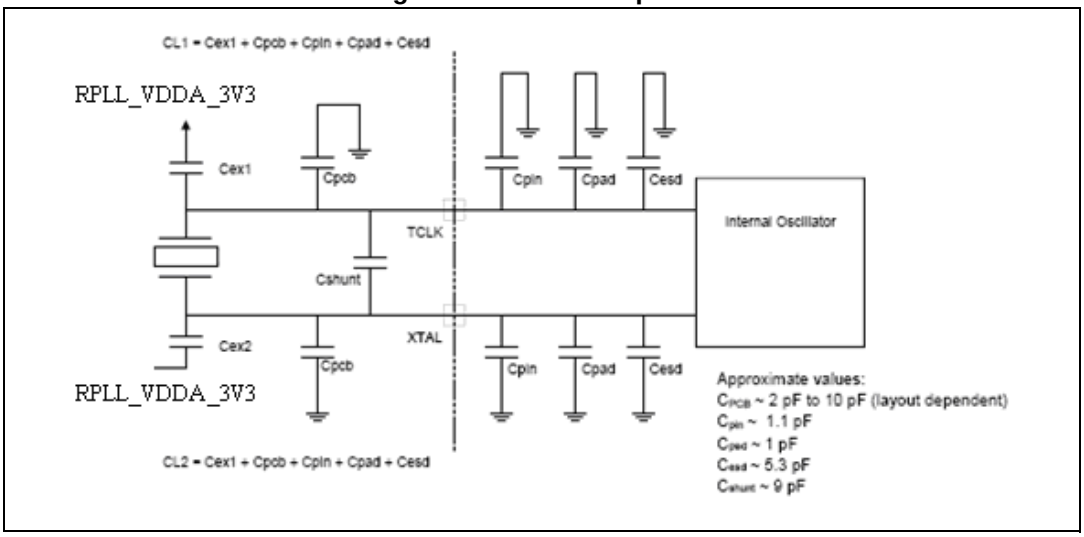
Cpin ~ 1.1 pF

Cpad ~ 1 pF

CESD ~ 5.3 pF

Cshunt ~ 9 pF

Figure 9. Parasitic capacitance sources



Some attention must be given to the details of the oscillator circuit when used with a crystal resonator. The PCB traces should be as short as possible. The value of C_{load} that is specified by the manufacturer should not be exceeded to avoid potential start-up problems with the oscillator. Additionally, the crystal should be a fundamental AT-cut and the value of the equivalent series resistance must be less than 80 Ω.

4.4.2 General recommendations for crystal specifications

While the selection of a crystal mainly depends on the specific PCB layout and the crystal manufacturer's specifications, the following are general recommendations.

Table 4. Recommended crystal specifications

Paremeters	Specifications
Frequency	27.000 MHz
Operation mode	Fundamental
Operating temperature	-10 °C to +70 °C
Frequency tolerance @25 ^{0}C	+/- 50 ppm max
Frequency stability over temperature	+/- 100 ppm max
Load capacitance CL Shunt capacitance C0	8 pF to 18 pF 0.5 pF to 7 pF
Equivalent series resistance	< 80 ohms
Crystal cut	AT-cut

4.5 Master I2C interface

The STDP3150 device includes a set of I2C pins for DisplayPort AUX channel interface with external system devices. The DisplayPort AUX channel transports I2C commands in addition to native AUX commands. The I2C commands received through the AUX channel are sent to the external device through the AUX to I2C port. This port comprises the M_I2C_SDA and M_I2C _SCL pins. This interface is used for reading downstream sink EDID and for transferring MCCS commands from source to sink. AUX to I2C is an I2C master port, but it simply acts as a message transfer port between AUX channel and external I2C device. This port does not generate device address or issue read, write commands on its own. Instead, the I2C commands are originated from the DisplayPort PC source connected by the DisplayPort cable.

M_I2C_SCL and M_I2C_SDA pins are connected to the DDC lines of the output VGA connector. During the PC boot up, or any time during normal operation, the source can issue an EDID read. The STDP3150 will read EDID from VGA monitor through I2C port if cable is connected, and pass the EDID content directly to the PC source. In addition, the STDP3150 supports EDID caching feature, where it stores the sink (monitor) EDID in internal memory, and presents the EDID data to the PC source whenever there is an EDID read request from the PC source. This mode of operation is available by a configuration option and internal register settings. The EDID caching mode of operation is used to avoid potential time-out conditions particularly with legacy EDID devices, which supports only block read. EDID caching also avoids delay and failure in reading EDID in situations where there are periodic read requests from the source. The STDP3150 supports six I2C speeds (100 Kbps, 50 Kbps, 25 Kbps, 10 Kbps, 3 Kbps, and 1 Kbps). The PC source generally sets the desired I2C speed for EDID reads.

4.6 DisplayPort receiver

DisplayPort receiver decodes serialized DisplayPort streams into 30-bit video streams. Physical interface to DisplayPort receiver consists of two main lanes, an auxiliary channel, and an HPD output signal. The main lanes are unidirectional, AC-coupled, doubly terminated differential pairs. The video streams are received over the main lanes. The STDP3150 supports two bit rates: 2.7 Gbps per lane (referred to as "high bit rate") and 1.62 Gbps per lane (referred to as "low bit rate" or "reduced bit rate"). The receiver locks to one bit rate after negotiating with the transmitter.

The DisplayPort Aux channel is a bidirectional, AC-coupled, doubly terminated differential signal pair. It is capable of transmitting and receiving data at 1 Mbps. The Aux channel is for link management and device control purposes. The Aux channel in the STDP3150 handles the following functions:

- Link training/Link management
- Native AUX and I2C-over-AUX communication

The HPD output signal serves as a cable-plug event indicator, as well as an interrupt request to the source device. The HPD_out signal is in low state as long as the receiver is inactive. Once the sink device is ready to receive data, it sets the HPD_out signal to an active high state. This indicates to the source device that the sink is ready to receive data over the DisplayPort interface. When the receiver wants to interrupt the source, it momentarily brings the HPD_out signal to low state. Refer to HPD-IRQ event described in the DisplayPort 1.2a specification.

4.7 Digital-to-Analog converter (DAC)

The STDP3150 has an integrated 3.3 V triple 10-bit DAC The DAC transforms the graphics digital data from the DisplayPort to analog Red, Green, and Blue data for the analog CRT monitor. The DAC can be operated at a maximum Pixel clock frequency of 162 MHz. It supports up to 1600 x 1200 resolution in 8 bpc mode at 60 Hz or 1920 x 1080p resolution in 10 bpc mode at 60 Hz. The peak-to-peak voltage range on the RGB output is 700 mV.

4.8 Highest video resolution modes supported

Table 5. Resolution modes supported

Resolution	Refresh	Color depth	Reduced blanking	Freq.	Input port(s)	DPRX lane	Output port(s)
1920 x 1200 (WUXGA-R)	60 Hz	8 bpc	RB	154 MHz	DP	2L	Analog R,G,B port
1920 x 1080p	60 Hz	10 bpc		144 MHz	DP	2L	Analog R,G,B port
1600 x 1200	60 Hz	8 bpc		162 MHz	DP	2L	Analog R,G,B port
1680 x 1050	60 Hz	6 bpc	RB	119 MHz	DP	1L	Analog R,G,B port

4.9 On-chip microcontroller (OCM)

This device includes an on-chip microcontroller. When the chip is powered, OCM configures various internal hardware blocks for the proper operation of the device. OCM includes on-chip RAM, timers, Interrupt controller, UART handler and SPI controller. The OCM executes firmware from both internal ROM (iROM) and external serial Flash ROM. The STDP3150 supports many commercially available serial Flash ROMs of size from 512 KBits to 4 MBits. Contact MegaChips for the list of SPI Flash devices supported in the ISP driver tool.

4.10 Serial peripheral interface for SPI Flash ROM

The SPI interface between STDP3150 and a serial Flash ROM is as follows:

SPI_CSn <-> CE# of SPI memory

SPI_CLK <-> SCK of SPI memory

SPI_DO <-> SI of SPI memory

SPI_DI <-> SO of SPI memory

Pins of WP# and HOLD# of SPI ROM are options for controlling the SPI ROM. WP# if pulled low will disable writing to the ROM. HOLD# is used when multiple devices are used in daisy-chain configuration. They can be pulled-high all the time to disable their functions or they can be controlled with GPIOs for more flexibility. Refer to SPI ROM specifications for details. SPI port pins also share functionality with general-purpose output. During power up, the bootstrap selection SPI_FUNC_SEL decides whether the port pins are used as SPI interface or something else.

4.11 Test, debug, and development

The following sections are useful for chip test, debug, and development purposes.

4.11.1 Two-wire debug interface

The STDP3150 has a two-wire debug port. This port is intended for development/debug purposes from an external micro. This mode of operation is not recommended for production environment. The OCM and its peripherals, such as UART and SPI blocks are not operational when the two-wire interface is active. Pin description of two-wire interface is not shown in this document. Contact MegaChips for further details.

4.11.2 UART interface

The OCM has an integrated Universal Asynchronous Receiver and Transmitter (UART) port that can be used as a factory debug port. The UART interface is optional and described only to give information for developmental/debug purposes. In particular, the UART can be used to 1) read/write chip registers; 2) In-System-Programming of the SPI Flash. The UART_RX and UART_TX pins also share functionality with GPO. During power up, bootstrap status on UART_FUN_SEL determines whether the pins are configured for UART function or for general-purpose output. The UART baud rate is set to 19200 baud.

4.11.3 In-system-programming (ISP) of external Flash ROM

It is possible to program the serial ROM devices via the standard UART or through DisplayPort AUX channel. The embedded boot firmware performs the programming of external Flash ROM. However, ISP requires an external hardware and software tool (GProbe). Contact MegaChips for the ISP tool and procedure.

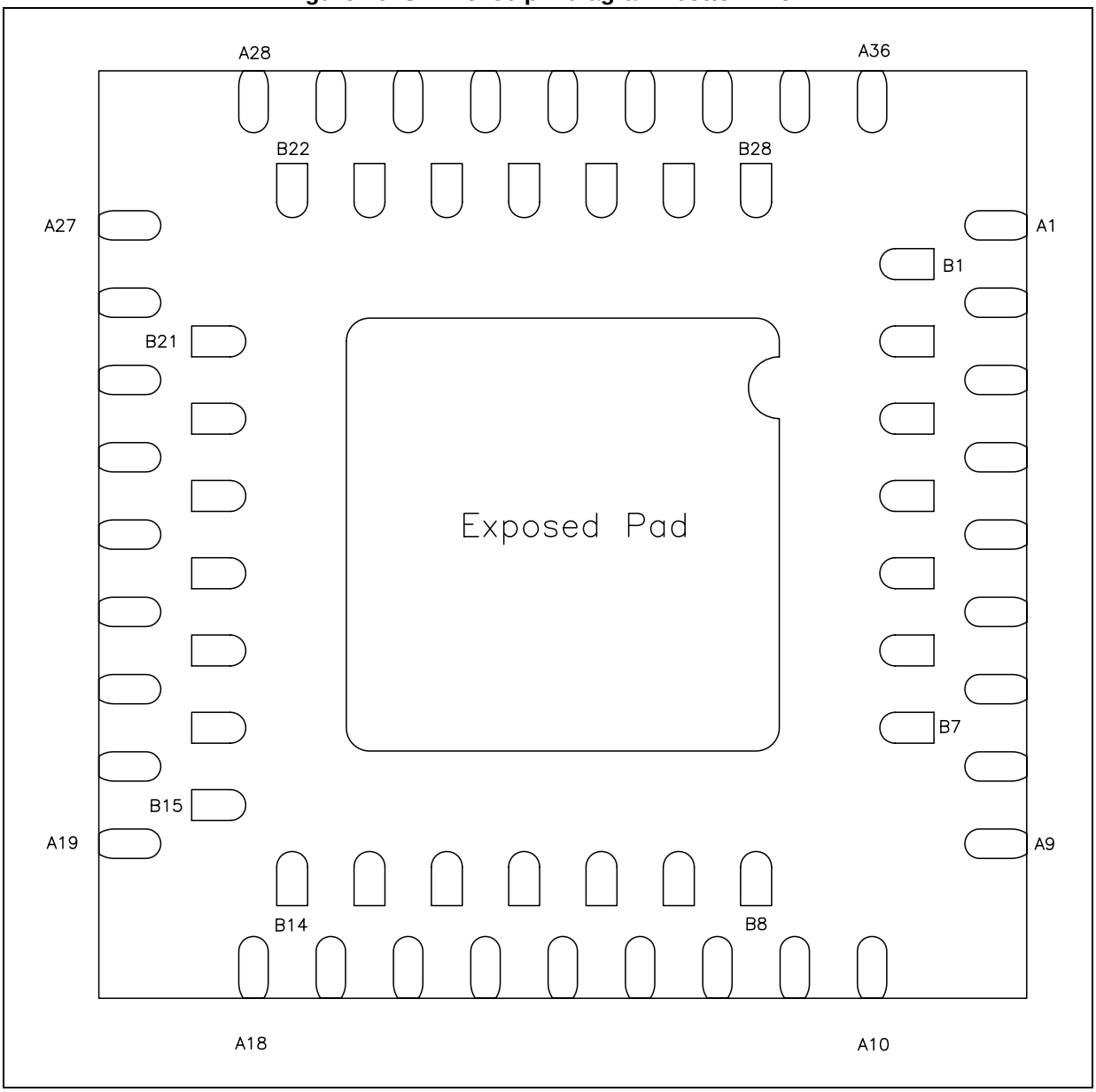
4.11.4 Internal test pattern generator

The STDP3150 has an on-chip test pattern generator that is useful for system debug.

5. Pin diagram

The STDP3150 is available in a 64-pin QFN package.

Figure 10. STDP3150 pin diagram: bottom view



5.1 Full pin list sorted by pin number

Table 6. Pin list

Pin number	Net name
A1	DAC_VDD_1V2
A2	BLUEN
A3	BLUEP
A4	GREENN
A5	GREENP
A6	REDN
A7	REDP
A8	COMP
A9	REF_R
A10	DNC
A11	DNC
A12	STI_TM2
A13	GPIO_25
A14	UART_RX
A15	SPI_CSn/GPIO_8
A16	SPI_DI/GPIO_10
A17	GPIO_0
A18	GPIO_1
A19	DPRX_AUXP
A20	DNC
A21	DPRX_REXT
A22	DPRX_ML_L0P
A23	DPRX_ML_L0N
A24	DPRX_ML_L1P
A25	DPRX_ML_L1N
A26	RPLL_VBUFC
A27	XTAL
A28	RPLL_VDDA_3V3
A29	RESETn
A30	M_I2C_SDA/ GPIO_12
A31	M_I2C_SCL/ GPIO_13
A32	GPIO_30
A33	GPIO_27

Table 6. Pin list (continued)

Pin number	Net name
A34	GPIO_14
A35	VSYNC
A36	HSYNC
B1	DNC
B2	DAC_VDDA_1V2
B3	RGB_VDDA_3V3
B4	DNC
B5	RGB_VDDA_3V3
B6	RGB_VDDA_3V3
B7	DNC
B8	CVDD_1V2
B9	RVDD_3V3
B10	GPIO_31
B11	UART_TX
B12	SPI_CLK/GPIO_9
B13	SPI_DO/GPIO_11
B14	DPRX_HPD_OUT
B15	DPRX_AUXN
B16	DPRX_VDD_1V2
B17	DPRX_VDDA_1V2
B18	DNC
B19	DNC
B20	DPRX_VDDA_1V2
B21	RPLL_VDD_1V2
B22	TCLK
B23	RVDD_3V3
B24	CVDD_1V2
B25	DNC
B26	GPIO_5
B27	GPIO_26
B28	GPIO_15

6. Connections

6.1 Pin list

I/O Legend: A = Analog = Input; O = Output; P = Power; G = Ground

Note: Some pins can have multiple functionalities, which are configured under register control. The alternate functionality for each pin is listed in the Description column.

Table 7. DisplayPort receiver pins

Pin Name	No	I/O	Description
DPRX_HPD_OUT	B14	O	DisplayPort Receiver Hot Plug Detect Output. This is a digital output with an 8mA output drive.
DPRX_AUXN	B15	AIO	DisplayPort Receiver Auxiliary channel Negative analog input/output.
DPRX_AUXP	A19	AIO	DisplayPort Receiver Auxiliary channel Positive analog input/output.
DPRX_VDD_1V2	B16	P	DisplayPort Receiver Digital 1.2 V power supply. Must be bypassed with a 0.1uF capacitor to digital ground plane on board.
DPRX_REXT	A21	AI	DisplayPort Receiver External termination resistor. A 287 Ohm 1% Pull-high resistor should be connected from this pin to 1.2V analog power supply.
DPRX_VDDA_1V2	B17	AP	DisplayPort Receiver Analog 1.2 V power supply. Must be bypassed with a 0.1uF capacitor to analog ground plane on board.
DPRX_ML_L0P	A22	AI	DisplayPort Receiver Main Link Lane 0 Positive analog input.
DPRX_ML_L0N	A23	AI	DisplayPort Receiver Main Link Lane 0 Negative analog input.
DPRX_ML_L1P	A24	AI	DisplayPort Receiver Main Link Lane 1 Positive analog input.
DPRX_ML_L1N	A25	AI	DisplayPort Receiver Main Link Lane 1 Negative analog input.
DPRX_VDDA_1V2	B20	AP	DisplayPort Receiver Analog 1.2 V power supply. Must be bypassed with a 0.1uF capacitor to analog ground plane on board.

Table 8. Digital to analog converter (DAC) pins

Pin Name	No	I/O	Description
REF_R	A9	AI	This is an external reference resistor for setting video DAC current. It controls magnitude of the full-scale video signal. Connect a 3.38 K Ohm 1% pull down resistor to this pin and VSS pin.
COMP	A8	AI	This is a compensation pin for internal reference amplifier. Connect a 0.01uF capacitor between COMP pin and analog 3.3 V power. Use a Ferrite Bead to isolate from other supplies.
RGB_VDDA_3V3	B6	AP	Analog 3.3 V power pin for RGB DACs. Must be bypassed with a 0.1uF capacitor to analog ground plane on board. Use a Ferrite Bead to isolate from other supplies.
REDP	A7	AO	RED Output. It can drive 37.5 ohm equivalent load (e.g. 75 ohm resistor on the board, in parallel with a 75 ohm CRT load). Note: All three outputs should have similar output loads whether or not they are all being used.

Table 8. Digital to analog converter (DAC) pins

Pin Name	No	I/O	Description
REDN	A6	AO	Differential RED Output. This signal is used to provide noise immunity. Complementary RGB outputs should be tied to ground if not required.
RGB_VDDA_3V3	B5	AP	Analog 3.3 V power pin for RGB DACs. Must be bypassed with a 0.1uF capacitor to analog ground plane on board. Use a Ferrite Bead to isolate from other supplies.
GREENP	A5	AO	GREEN Output. It can drive 37.5 ohm equivalent load (e.g. 75 ohm resistor on the board, in parallel with a 75 ohm CRT load). Note: All three outputs should have similar output loads whether or not they are all being used.
GREENN	A4	AO	Differential GREEN Current Output. This signal is used to provide noise immunity. Complementary RGB outputs should be tied to ground if not required.
RGB_VDDA_3V3	B3	AP	Analog 3.3V power pin for RGB DACs. Must be bypassed with a 0.1uF capacitor to analog ground plane on board. Use a Ferrite Bead to isolate from other supplies.
BLUEP	A3	AO	BLUE Output. It can drive 37.5 ohm equivalent load (e.g. 75 ohm resistor on the board, in parallel with a 75 ohm CRT load). Note: All three outputs should have similar output loads whether or not they are all being used.
BLUEN	A2	AO	Differential BLUE Current Output. This signal is used to provide noise immunity. Complementary RGB outputs should be tied to ground if not required.
DAC_VDDA_1V2	B2	AP	1.2 V - Analog power pin for the DAC switching logic. Must be bypassed with a 0.1uF capacitor to analog ground plane on board. Use a Ferrite Bead to isolate from other supplies.
DAC_VDD_1V2	A1	P	1.2 V- Digital power pin for the DAC. Must be bypassed with a 0.1uF capacitor to digital ground plane on board

Table 9. Vsync/Hsync pins

Pin Name	No	I/O	Sync Current/ Output Drive	Tolerance	Internal or External Pull-up/ Pull-down	Description
VSYNC	A35	I/O	8 mA drive	5 V Tol.		VSYNC - Vertical Sync output. This signal is generated at 3.3 V. External level shifting buffer is required for 5 V VSYNC output.
HSYNC	A36	I/O	8 mA drive	5 V Tol.		HSYNC - Horizontal Sync output. This signal is generated at 3.3 V. External level shifting buffer is required for 5 V HSYNC output.

Table 10. Reference clock pins

Pin Name	No	I/O	Description
RPLL_VBUFC	A26	AO	Analog test pin for internal clocks. Do not connect.
RPLL_VDD_1V2	B21	P	Digital 1.2 V power supply for RCLK PLL core. Bypass to digital ground plane on the board with a 0.1 uF capacitor.
XTAL	A27	AO	27 MHz Oscillator input port. Do not connect this pin when TTL Oscillator input is used on TCLK pin. Connect to 27.00 MHz external Crystal.
TCLK	B22	AI	27 MHz Oscillator output port, or TTL oscillator input port (refer to figure 8). Connect to 27.00 MHz external Crystal or an Oscillator.
RPLL_VDDA_3V3	A28	AP	Analog 3.3 V power supply for the reference DDS PLL. Bypass with a 0.1 uF capacitor to VSS pin.

Table 11. Multi-function and system interface pins

Pin Name	No	I/O	Sync Current/ Output Drive	Tolerance	Internal or External Pull-up/ Pull-down	Description
STI_TM2	A12	I	8 mA	5 V		Test pin. For normal operation, tie it to ground. When this pin is pulled high, it is in test mode.
GPIO_31	B10	I/O	8 mA	5 V		GPIO_31 - General Purpose Input/Output 31.
GPIO_25	A13	I/O	8 mA	5 V	50 K Internal Pull-down.	GPIO_25 - General Purpose Input/Output 25. This pin may be used as DDC return line on VGA connector (DB15 pin 10). It may be used for both plug and unplug detection of VGA sink. Refer to the register specifications for configuring this pin as GPIO_25.
UART_RX	A14	I/O	8 mA	5 V	50K Internal Pull-up	UART_RX - UART Receive (data input). This signal is used for debug and development only. Refer to the Bootstrap option for configuring this pin for UART_RX.
UART_TX	B11	I/O	8 mA	5 V		UART_TX - UART Transmit (data output). This signal is used for debug and development only. Refer to the Bootstrap table for configuring this pin for UART_TX.
SPI_CSn/GPIO_8	A15	I/O	8 mA	5 V		SPI_CSn - SPI ROM Chip Select. Please refer to the Bootstrap configuration table for configuring this pin as a SPI_CSn. GPIO_8 - General Purpose Input/Output 5. This pin is GPIO_8 if not configured as a SPI_CSn.

Table 11. Multi-function and system interface pins

Pin Name	No	I/O	Sync Current/ Output Drive	Tolerance	Internal or External Pull-up/ Pull-down	Description
SPI_CLK/GPIO_9	B12	I/O	8 mA	5 V	50 K Internal Pull-down.	SPI_CLK - SPI ROM Clock output. Please refer to the Bootstrap configuration table for configuring this pin as a SPI_CLK. GPIO_9 - General Purpose Input/Output 9. This pin is GPIO_9 if not configured as a SPI_CLK.
SPI_DI/GPIO_10	A16	I/O	8 mA	5 V	50 K Internal Pull-down	SPI_DI - SPI ROM Data Input. Please refer to the Bootstrap configuration table for configuring this pin as a SPI_DI. GPIO_10 - General Purpose Input/Output 10. This pin is GPIO_10 if not configured as a SPI_DI.
SPI_DO/GPIO_11	B13	I/O	8 mA	5 V	50 K Internal Pull-down.	SPI_DO - SPI ROM Data Output. Please refer to the Bootstrap configuration table for configuring this pin as a SPI_DO. GPIO_11 - General Purpose Input/Output 11. This pin is GPIO_11 if not configured as a SPI_DO.
GPIO_0	A17	I/O	8 mA	5 V	50 K Internal Pull-down.	GPIO_0 - General Purpose Input/Output 0.
GPIO_1	A18	I/O	8 mA	5 V		GPIO_1 - General Purpose Input/Output 1. This pin may be used for Sense Source detect for embedded application to force the STDP3150 to wake up and establish link irrespective of VGA Sink detect.
RESETn	A29	I	8 mA	5 V	External 2.7 K Pull high required	RESETn - Reset (active low) signal. Connect to RVDD_3V3 with a 2.7K ohm pull-high resistor.
M_I2C_SDA / GPIO_12	A30	I/O	8 mA	5 V	50 K Internal Pull-up.	M_I2C_SDA - I2C Serial Data for Master I2C port. This signal is used for DDC interface. Connect it to the VGA connector. Refer to the register specifications for configuring this pin as M_I2C_SDA. GPIO_12 - General Purpose Input/Output 12. Refer to the register specifications for configuring this pin as GPIO_12.

Table 11. Multi-function and system interface pins

Pin Name	No	I/O	Sync Current/ Output Drive	Tolerance	Internal or External Pull-up/ Pull-down	Description
M_I2C_SCL/ GPIO_13	A31	I/O	8 mA	5 V	50 K Internal Pull-up.	M_I2C_SCL - I2C Serial Clock for Master I2C port. This signal is used for DDC interface. Connect it to the VGA connector. Refer to the register specifications for configuring this pin as M_I2C_SCL. GPIO_13 - General Purpose Input/Output 13.
GPIO_30	A32	I/O	8 mA	5 V		GPIO_30 - General Purpose Input/Output 30. This pin is used for DP cable detect.
GPIO_5	B26	I/O	8 mA	5 V	50 K Internal Pull-down.	GPIO_5 - General Purpose Input/Output 5.
GPIO_27	A33	I/O	8 mA	5 V	50 K Internal Pull-up.	GPIO_27 - General Purpose Input/Output 27.
GPIO_26	B27	I/O	8 mA	5 V	50 K Internal Pull-up.	GPIO_26 - General Purpose Input/Output 26.
GPIO_14	A34	I/O	8 mA	5 V		GPIO_14 - General Purpose Input/Output 14.
GPIO_15	B28	I/O	8 mA	5 V		GPIO_15 - General Purpose Input/Output 15.

Table 12. Power and ground pins

Pin Name	No	I/O	Description
CVDD_1V2	B8	P	Core VDD. Connect to digital 1.2 V with 0.1uF bypass capacitor to system ground.
CVDD_1V2	B24	P	Core VDD. Connect to digital 1.2 V with 0.1uF bypass capacitor to system ground.
RVDD_3V3	B9	P	Ring (I/O) VDD. Connect to digital 3.3 V with 0.1uF bypass capacitor to system ground.
RVDD_3V3	B23	P	Ring (I/O) VDD. Connect to digital 3.3 V with 0.1uF bypass capacitor to system ground.
CRVSS	EP	G	Core and Ring (I/O) VSS. Must be directly connected to the system ground.

Table 13. Reserved pins

Pin	Assignment	Description
A10, A11, A20, B1, B4, B7, B18, B19, B25	DNC	Reserved. Do not connect

6.2 Bootstrap configuration

During hardware reset, on the rising edge of RESETn, logic high or low configuration on Bootstrap pins are latched and stored. 4.7 K pull-up or pull-down resistors must be installed to indicate logic '1' or '0' status on the bootstrap pins. Bootstrap operation is only guaranteed with external pull-up or pull-down resistors. There are sixteen Bootstrap pins available on STDP3150. Some bootstraps may not be available for normal use.

Table 14. Bootstrap configuration

Pin#	Pin Name	Function
B10	SPI_FUNC_SEL	SPI_FUN_SEL: This is used to select the functionality of SPI interface pins 0 = SPI Pins are disabled for interfacing external Flash device 1 = SPI Pins are enabled for interfacing external Flash device
A13	SW_BS_4	Reserved
B11	SW_BS_2	Reserved
A15	SW_BS_5	Enable/Disable VGA Load sensor circuit 0 = Disable VGA load sensor circuit to detect the VGA cable. 1 = Enable load sensor circuit to detect the VGA cable for both plug and unplug event.
B26	INT_OSC_SEL	TCLK Source selection: TCLK_OSCRING_SEL: INT_OSC_SEL 00 - XTAL PAD OSC (Internal Oscillator). Use external crystal on TCLK and XCLK pins 01 - TCLK INPUT (External Oscillator). Use external TTL oscillator. Connect to TCLK pin. Do not connect XTAL pin 1x - Reserved.
B12	TCLK_OSCRING_SEL	
B13	JTAG_TEST_MODE	Test Mode selection 0 = Test mode of Operation; 1 = Normal mode of Operation
A17	UART_FUN_SEL	UART_FUN_SEL: This bootstrap enable UART RX & TX Function on UART_RX and UART_TX pins 0 = UART Interface Disabled. Pin is used for GPIO. 1 = UART Interface Enabled.
A18	SW_BS_3	Reserved
A32	SW_BS_6	Reserved
A33	INTERFACE_SEL_0	INTERFACE_SEL[1:0]- Selects interfaces for debug 00 - Reserved 01 - Two wire Interface 10 - Reserved 11 - Normal operation
B27	INTERFACE_SEL_1	

Table 14. Bootstrap configuration

Pin#	Pin Name	Function
A34	OCM_BOOT_SEL	Bootstrap pin for selecting OCM Boot Option 0 = OCM boot will be from internal ROM code. (Internal ROM is 'ON' and mapped to top 32 K of OCM address range). External ROM is not needed for production design. 1 = OCM boot is from external ROM/FLASH code (Internal ROM is 'OFF' and external ROM/FLASH mapped to top 512 K of OCM address range)
B28	SW_BS_7	Reserved
A35	SW_BS_1	DisplayPort Bit rates select: 0 = DisplayPort high bit rate (2.7Gbps) or Low Bit rate (1.62Gbps) 1 = Reserved
A36	SW_BS_0	VGA Plug/unplug detect 0 = Default state. Disable programmable frequency VGA plug/unplug detect for load sensor circuit 1 = Enable programmable frequency VGA plug/unplug detect for load sensor circuit When enabled configures load sensor circuit scheduler for VGA sink detection circuit. This scheduling applies to both normal and power saving mode. It can be used to control the response time of the system.

6.3 General-purpose input/output (GPIO) pins

The STDP3150 offers sixteen general-purpose input/output (GPIO) pins: GPIO_0, GPIO_1, GPIO_5, GPIO_8, GPIO_9, GPIO_10, GPIO_11, GPIO_12, GPIO_13, GPIO_14, GPIO_15, GPIO_25, GPIO_26, GPIO_27, GPIO_30, and GPIO_31. Some GPIO pins may not be available for targeted application due to the shared functionality of these pins. The general-purpose input/output pins can be used for interfacing with system components. Each GPIO has independent direction control and open drain enable for reading and writing.

Refer to the pin definition table for detailed functionality of the GPIO pins for their shared functions.

7. Package specifications

Package type: 64-pin QFN, 6 x 6 mm

7.1 Package drawing

Figure 11. Package drawing: bottom view

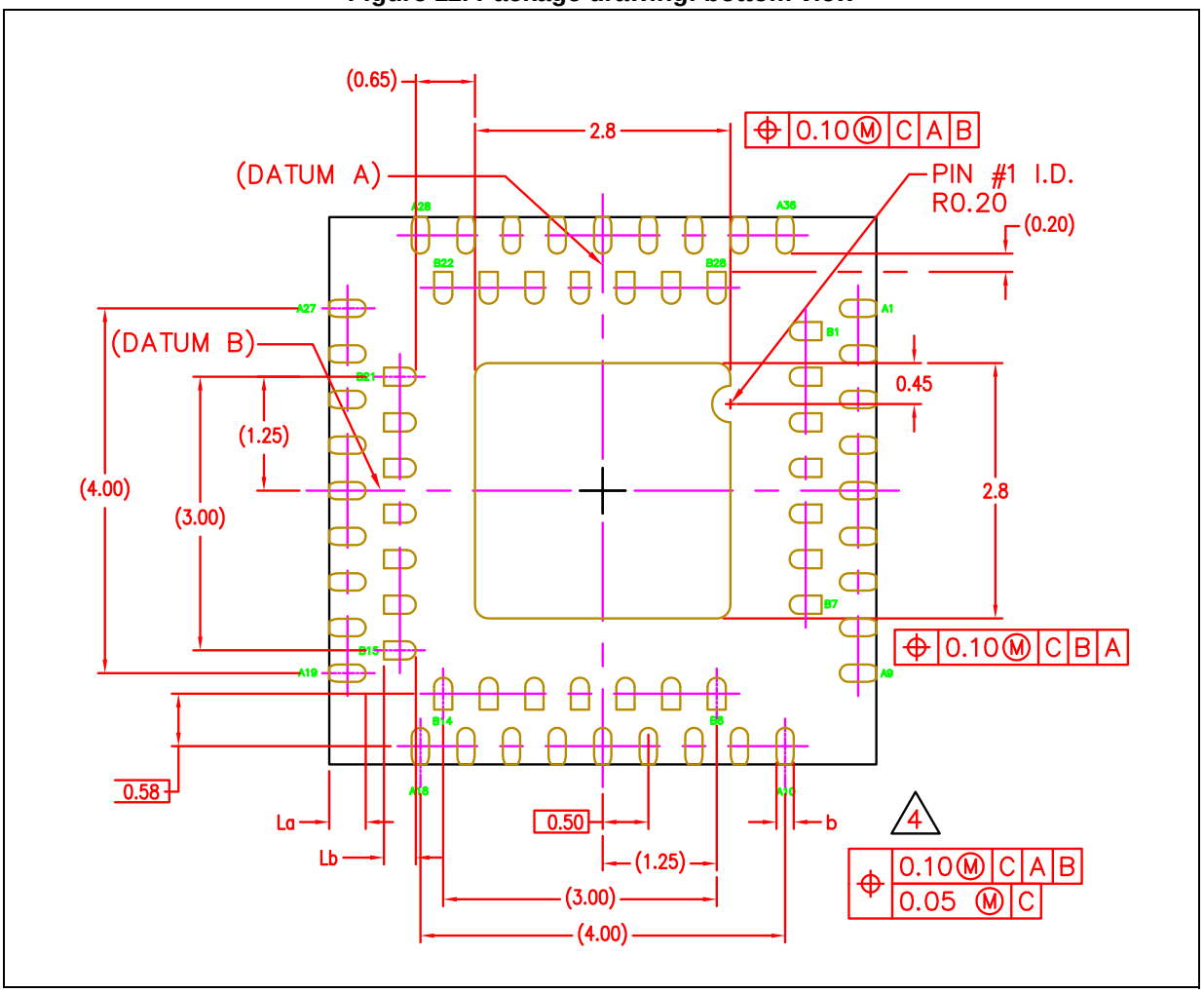


Figure 12. Package drawing: top and side views

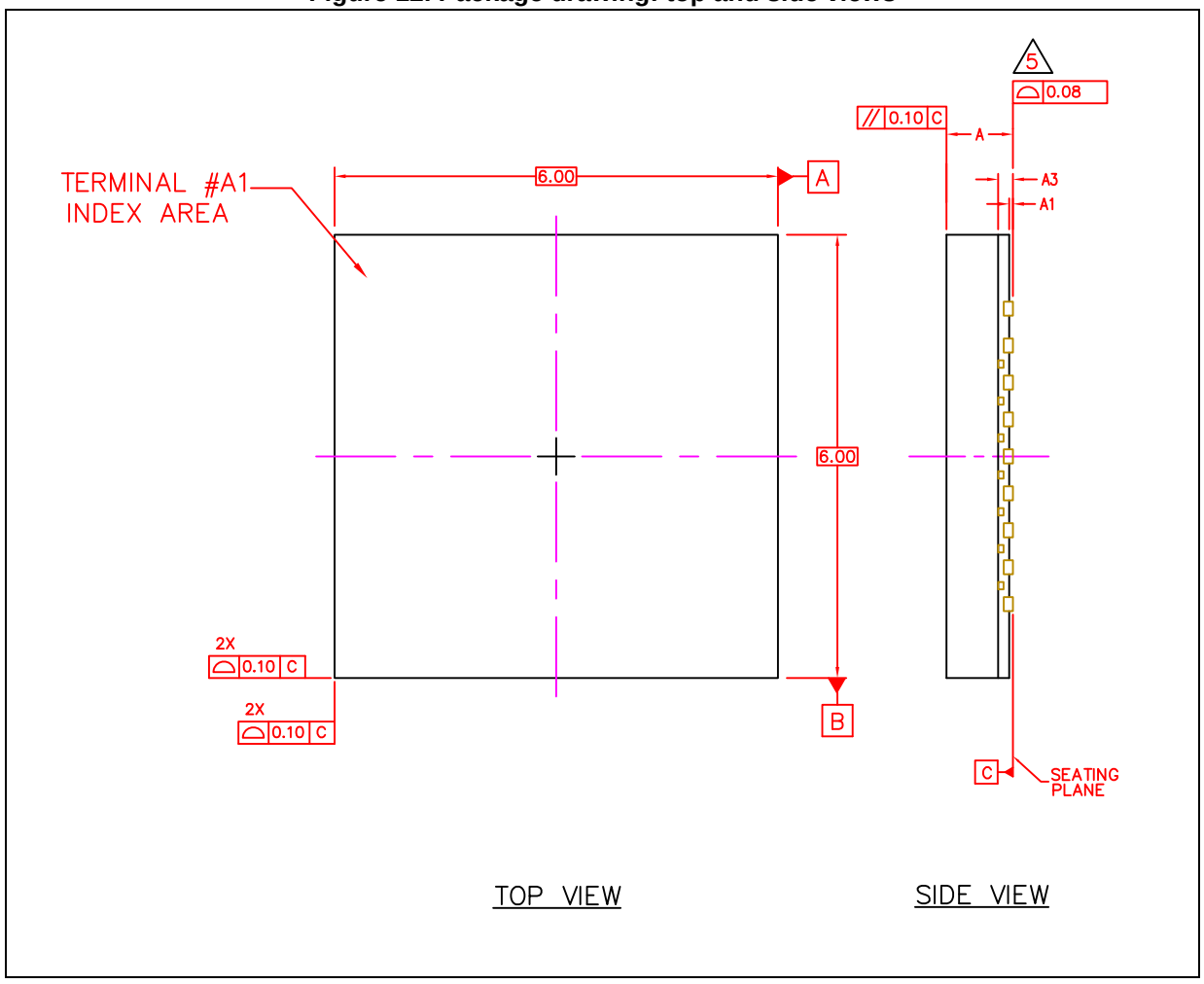


Figure 13. Package drawing: dimensions

	DIMENSIONS			
	DATABOOK (mm)			
REF.	MIN.	TYP.	MAX.	NOTES
A	0.80	0.85	0.90	
A1	0.00	0.02	0.05	(5)
A3		0.152 REF.		
N		64		(3)
Na		36		(3)
Nb		28		(3)
La	0.30	0.40	0.50	
Lb	0.30	0.35	0.40	(4)
b	0.15	0.20	0.25	(4)

NOTES:

1. - VQFN stands for **V**ery Thin **Q**uad **F**lat **N**o Lead package.
   Low Profile: The total profile height (Dim A) is measured from the seating plane to the top of the component
   Body size 6x6 not yet referenced inside JEDEC standard

2. – All dimensions are in millimeters
   Decimal
   X.X ±0.1
   X.XX ±0.05
   X.XXX ±0.030

3. – N is the total number of terminals
   Na is the number of terminals in outer land &
   Nb is the number of terminals in inner land

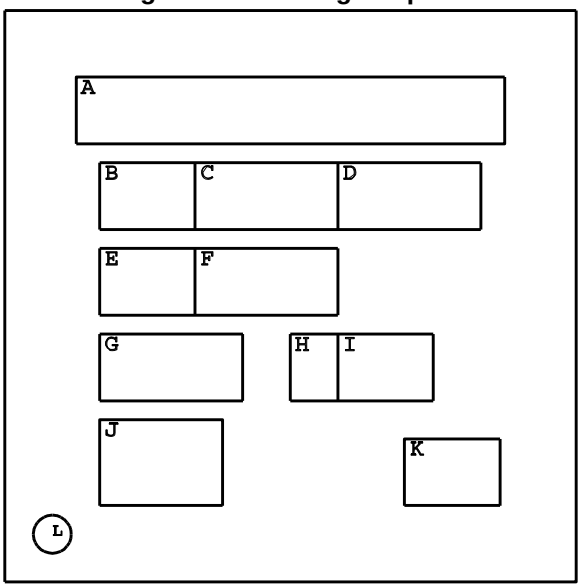
4. – Dimension b applies to plated terminal and is measured between 0.10 and 0.20mm from terminal tip.

5. – Unilateral coplanarity zone applies to the exposed pad as well as the terminals.

7.2 Marking field template and descriptors

The STDP3150 marking template is shown below.

Figure 14. Marking template



Field descriptors are shown below.

Table 15.Field descriptors

Field	Description	Marking
A	Product code	STDP3150
B	2-character diffusion plant code	9R
C	3-digit wafer start date	“YWW”
D	3-character FE sequence code	“ABC”
E	2-character assembly plant code	AP
F	3-character BE sequence code	“XYZ”
G	3-character country of origin code	TWN
H	1-digit assembly year	“Y”
I	2-digit assembly week	“WW”
J	Standard MegaChips logo	M
K	2-character version code	AB
L	Ball A1 identifier	a DOT

7.3 Classification reflow profile

Please refer to the DisplayPort Application Note: Classification reflow profile for SMD devices (C0353-APN-06) for reflow diagram and details.

8. Electrical specifications

8.1 Absolute maximum ratings

Applied conditions greater than those listed under “Absolute maximum ratings” may cause permanent damage to the device. The device should never exceed absolute maximum conditions since it may affect device reliability.

Table 16. Absolute maximum ratings

Parameter	Symbol	Min	Typ	Max	Units
3.3 V supply voltages (1) (2)	$V_{VDD\_3.3}$	-0.3	3.3	3.6	V
1.2 V supply voltages (1) (2)	$V_{VDD\_1.2}$	-0.3	1.2	1.26	V
Input voltage (5 V tolerant inputs)(1) (2)	$V_{IN5Vtol}$	-0.3	-	5.5	V
Input voltage (non-5 V tolerant inputs)(1) (2)	$V_{IN3V3tol}$	-0.3	-	3.6	V
ESD - Human Body Model (HBM)(3)	V_{ESD}	-	-	±2.0	kV
ESD - Charged Device Model (CDM)(3)	V_{ESD}	-	-	±500	V
Latch-up	I_{LA}	-	-	±200	mA
Ambient operating temperature	T_A	0	-	70	°C
Storage temperature	T_{STG}	-40	-	150	°C
Operating junction temperature	T_J	0	-	125	°C
Thermal resistance (Junction to Air) natural convection(4)	θ_{JA_2L}	-	-	TBD	°C/W
	θ_{JA_4L}	-	-	TBD	°C/W
Thermal resistance (Junction to Case) convection(4)	θ_{JC_2L}	-	-	TBD	°C/W
	θ_{JC_4L}	-	-	TBD	°C/W
Peak IR reflow soldering temperature	T_{SOL}	-	-	260	°C
Active power dissipation		-	415	434	mW
Standby power dissipation		-	-	16	mW

1. All voltages are measured with respect to GND.
2. Absolute maximum voltage ranges are for transient voltage excursions.
3. Electrostatic Discharge (ESD): Integrated ESD diodes are provided to protect the device during handling. The ESD result shown is not applicable for reserved pins. For additional ESD protection, external diodes are recommended on the DisplayPort input and VGA output traces (refer to RD schematics).
4. These are simulated results under following conditions - Two layer/Four Layer PCB, No heat spread, Air flow = 0 m/s.

8.2 Maximum speed of operation

System clocks

Crystal clock = 27 MHz typical

SPI_CLK = TCLK/2

I2C CLK = 100 KHz

Internal OCM clock = 27 MHz max

DisplayPort receiver bit rate

Main link

Min: 1.62 Gbps/lane

Max: 2.7 Gbps/lane

Auxiliary channel: 1 Mbps

Pixel clock

Max: 162 MHz

8.3 DC characteristics

Table 17. DC characteristics

Input/output ports	**Maximum power dissipation mW**	Measurement conditions: RVDD_3V3, RGB_VDDA_3V3, , RPLL_VDDA_3V3 at 3.3 V CVDD_1V2, DPRX_VDD_1V2, DPRX_VDDA_1V2, DAC_VDD_1V2, DAC_VDDA_1V2, RPLL_VDD_1V2 at 1.2 V Ambient temperature 25 °C
Sleep mode ->	16	Only I2C, AUX monitoring active
Input: DP-2L Output: VGA Port	415	1600 x 1200, 60 Hz, 8 bpc @162 MHz Running ON/OFF Patterns
Input: DP-2L Output: VGA Port	415	1920 x 1200 (WUXGA-R), 60 Hz, 8 bpc, RB @154 MHz Running ON/OFF Patterns
Input: DP-2L Output: VGA Port	415	1920 x 1080p, 60 Hz, 10 bpc @144 MHz Running ON/OFF Patterns
Input: DP-1L Output: VGA Port	370	1680 x 1050, 60 Hz, RB, 6 bpc @119 MHz Running ON/OFF Patterns

Parameter	Symbol	Min	Typ	Max	Units
3.3 V supply voltages (analog and digital)	VVDD_3.3	2.97	3.3	3.6	V
1.2 V supply voltages (analog and digital)	VVDD_1.2	1.14	1.2	1.26	V
Supply current – 1.2 V digital supply – 1.2 V analog supply – 3.3 V digital supply – 3.3 V analog supply Note: 1600x1200, 60Hz, 8bpc @162MHz. ON/OFF patterns running.	 IVDD_1.2 IAVDD_1.2 IVDD_3.3 IAVDD_3.3	-	-	 72 64 10 65	mA

8.4 AC characteristics

8.4.1 DisplayPort receiver

Table 18. DisplayPort receiver characteristics

Symbol	Parameter	Min	Typ	Max	Unit	Comments
UI_High_Rate	Unit interval for high bit rate (2.7 Gbps/lane)		370		ps	DisplayPort link RX does not require local crystal for link clock generation
UI_Low_Rate	Unit interval for reduced bit rate (1.62 Gbps/lane)		617		ps	
Down spread tracking	Link clock down spreading	0.0		0.5	%	Modulation frequency range of 30 kHz to 33 kHz
$V_{RX-DIFFp-p}$	Differential peak-to-peak input voltage at package pins	120			mV	
Rx horizontal eye specification for high bit rate						
T_{RX-EYE_CONN}	Minimum receiver eye width at Rx-side connector pins	0.51			UI	
T_{RX-EYE_CHIP}	Minimum receiver eye width at Rx package pins	0.47			UI	
$T_{RX-EYE-MEDIAN-to-MAX-JITTER\_CHIP}$	Maximum time between the jitter median and maximum deviation from the median at Rx package pins			0.265	UI	$T_{RX-EYE-MEDIAN-to-MAX-JITTER}$ specifies the total allowable DJ
Rx horizontal eye specification for reduced bit rate						
T_{RX-EYE_CONN}	Minimum receiver eye width at Rx-side connector pins	0.46			UI	
T_{RX-EYE_CHIP}	Minimum receiver eye width at Rx package pins	0.42			UI	(1- T_{RX-EYE_CONN}) specifies the allowable TJ

Table 18. DisplayPort receiver characteristics

Symbol	Parameter	Min	Typ	Max	Unit	Comments
$T_{RX\text{-}EYE\text{-}MEDIAN\text{-}to\text{-}MAX\text{-}JITTER\_CHIP}$	Maximum time between the jitter median and maximum deviation from the median at Rx package pins			0.29	UI	$T_{RX\text{-}EYE\text{-}MEDIAN\text{-}to\text{-}MAX\text{-}JITTER}$ specifies the total allowable DJ
$V_{RX\text{-}DC\text{-}CM}$	RX DC common mode voltage	0		VDD	V	Common mode voltage is equal to Vbias_Rx voltage. VDD is the receiver input power supply voltage and 3.6 V maximum
$I_{RX\text{-}SHORT}$	RX short circuit current limit			60	mA	Total short circuit current when a differential input pin is shorted to ground
$RL_{RX\text{-}DIFF}$	Differential return loss at 0.675 GHz			12	dB	Straight loss line between 0.675 GHz and 1.35 GHz
	Differential loss at 1.35 GHz			9	dB	
$R_{RX\text{-}HIGH\text{-}IMP\text{-}DC}$	Powered down DC input resistance	200 k			Ω	
$L_{RX\text{-}SKEW\text{-}INTER\_CHIP}$	Lane-to-lane skew at RX package pins			5200	ps	Maximum skew limit between different RX lanes of a DisplayPort link
Intra-pair skew specification for high bit rate						
$L_{RX\text{-}SKEW\text{-}INTRA\_CHIP\_High\text{-}Bit\text{-}Rate}$	Lane intra-pair skew at RX package pins			100	ps	Maximum skew limit between D+ and D- of the same lane
Intra-pair skew specification for reduced bit rate						
$L_{RX\text{-}SKEW\text{-}INTRA\_CHIP\_Reduced\text{-}Bit\text{-}Rate}$	Lane intra-pair skew at RX package pins			300	ps	Maximum skew limit between D+ and D- of the same lane
$F_{RX\text{-}TRACKING\text{-}BW}$	Jitter tracking bandwidth	20			MHz	Minimum CDR tracking bandwidth at the receiver

8.4.2 DAC characteristics

Table 19. DAC characteristics

Parameters	Min	Typ	Max	Unit	Comments
Max Luminance Voltage					
Input Data =3FFh	0.665	0.716	0.720 + 0.07	Volts	+0.070/ -0.035 Volts
Min Luminance voltage					
Input Data = 00h	0.0			Volts	
Video Channel Rise/Fall Time Max		25%	50%	ns	25% of minimum pixel clock period
Maximum Settling Time after overshoot/undershoot			30	%	% of minimum pixel clock period averaged over 100 waveforms to 5% final full-scale value
Integral Linearity Error	-1.5		+2.2	LSB	For 10-bit operation
Differential Linearity Error	-0.275		+0.275	LSB	For 8-bit operation
Differential Linearity Error	-1.1		+1.1	LSB	For 10-bit operation
Video Channel to Video Channel Mismatch			6	%	% of any video output voltage over the full voltage range
Video Noise injection ratio			+/- 2.5	%	% of Max Luminance Voltage
Video Channel to Video Channel Output Skew		25	50	%	% of minimum pixel clock period
Overshoot/Undershoot			+/- 12	%	% of step function voltage level over the full voltage range

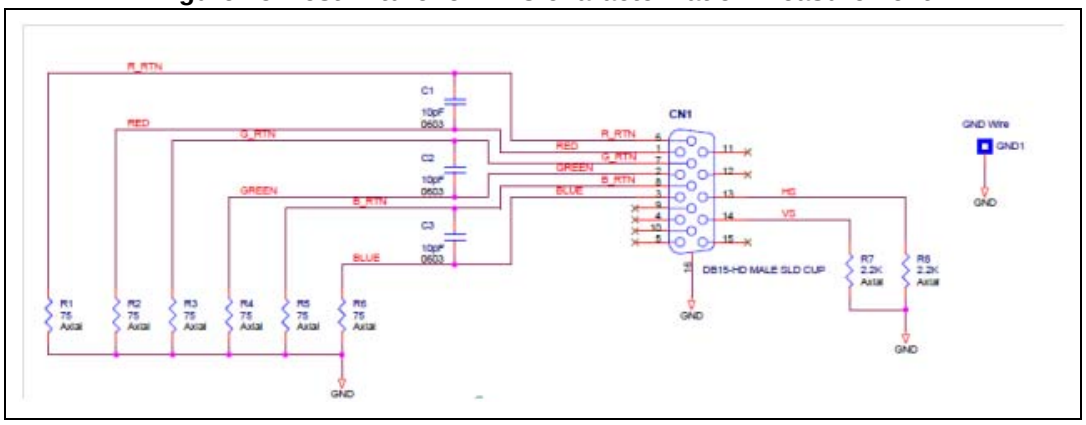
Monotonic	Yes
Resolution	1 LSB

Note: The STDP3150 DAC meets output characteristics as specified by the VESA Video Signal Standard specifications (VSIS) version 1 rev 1 in 8-bit operation. In 10-bit operation, INL and DNL values exceed VESA spec, as shown in the table above.

Note: The measurements for the VESA specification are supposed to be conducted with a test fixture that provides the VGA plug and 75 ohm termination resistors. The 10 pf load needs to be added in parallel to the 75 ohm termination resistor on the test fixture (see figure below) in order to slow down the rise and fall times of the DAC output which in-turn reduces the

over-shoot and under-shoot." Please refer to the VESA specifications for the details and measuring conditions.

Figure 15. Test fixture for DAC characterization measurement



8.4.3 Hsync and Vsync specifications

Table 20. Hsync and Vsync specifications

Parameters	Min	Typ	Max	Unit	Comments
Driver Logic level "1"	2.4		3.6	Volts	STDP3150 generates HSYNC and VSYNC signals at 3.3 V. External level shifting buffer is needed to achieve 5 V level.
Driver Logic level "0"	0.0		0.5	Volts	
Driver High Level Output Current	8			mA	
Driver Low Level Output Current	8			mA	
Fall Time Max			80	%	% of minimum pixel clock period
Rise Time Max			80	%	% of minimum pixel clock period
Monotonic Rise/Fall Voltage range	0.5-2.4			Volts	
Overshoot/Undershoot			30	%	% of high level signal voltage range. No signal excursions allowed in the 0.5-2.4 volt voltage range
Jitter (Measured between Hsync pulses)			15	%	Over the frequency spectrum: One half of the difference between the maximum and minimum interval between Hsync pulses measured over 100,000 intervals shall be less than 15% of the pixel clock. 0 Hz to Max. horizontal refresh rate at all image formats, worst-case screen patterns.

Note: The STDP3150 DAC meets output characteristics as specified by the VESA Video Signal Standard specifications (VSIS) version 1 rev 2. Please refer to these specifications for the details and measuring conditions.

8.4.4 I2C interface timing

Table 21. I2C interface timing

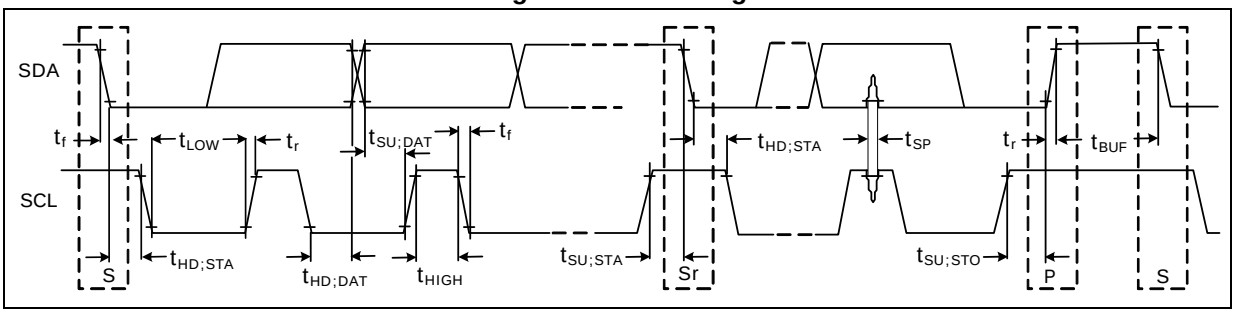
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{SCL}	SCL clock rate	Fast mode	0	50	100	kHz
t_{HD-STA}	Hold time START	After this period, the 1st clock starts	4.0	-	-	µs
t_{LOW}	Low period of clock	SCL	4.7	-	-	µs

Table 21. I2C interface timing

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{HIGH}	High period of clock	SCL	4.0	-	-	µs
$T_{su;STA}$	Setup time for a repeated START		4.7	-	-	µs
$t_{HD;DAT}$	Data hold time	For master	5	-	-	µs
$t_{SU;DAT}$	Data setup time		250	-	-	ns
T_{BUF}	Bus free time between STOP and START		4.7	-	-	µs
C_b	Capacitance load for each bus line		-	-	400	pF
t_r	Rise time		-	-	1000	ns
t_f	Fall time		-	-	300	ns
V_{nh}	Noise margin at high level		0.2 VDD	-	-	V
V_{nl}	Noise margin at low level		0.1 VDD	-	-	V

Note: The maximum $t_{HD;DAT}$ only has to be met if the device does not stretch the low period t_{LOW} of the SCL signal. In the diagram below, S = start, P = stop, Sr = Repeated start, and SP= Repeated stop conditions.

Figure 16. I²C timing



8.4.5 SPI interface timing

Table 22. SPI interface timing, VDD = 3.3 V

Symbol	Parameter	Min	Max	Units
F_{CLK}	Serial clock frequency	-	13.5	MHz
T_{SCKH}	Serial clock high time	20	-	ns
T_{SCKL}	Serial clock low time	20	-	ns
T_{SCKR}	Serial clock rise time	-	5	ns
T_{SCKF}	Serial clock fall time	-	5	ns
T_{CES}	CE# active setup time	20	-	ns

Table 22. SPI interface timing, VDD = 3.3 V

T_{CEH}	CE# active hold time	20	-	ns
T_{CHS}	CE# not active setup time	10	-	ns
T_{CHH}	CE# not active hold time	10	-	ns
T_{CPH}	CE# high time	100	-	ns
T_{CHZ}	CE# high to high-Z output	-	20	ns
T_{CLZ}	SCK low to low-Z output	0	-	ns
T_{DS}	Data in setup time	4	-	ns
T_{DH}	Data in hold time	5	-	ns
T_{OH}	Output hold from SCK change	0	-	ns
T_V	Output valid from SCK	-	23	ns

Figure 17. SPI output or serial interface SPI ROM input timing

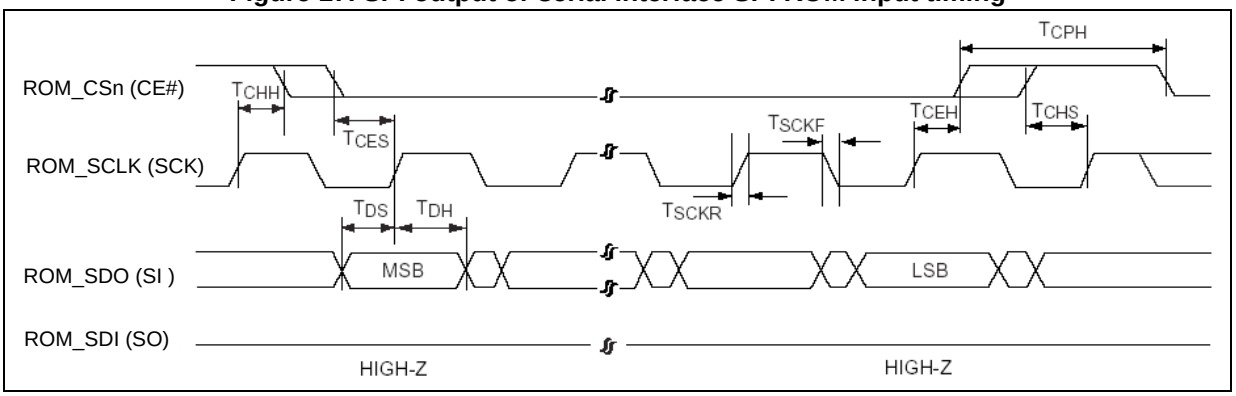
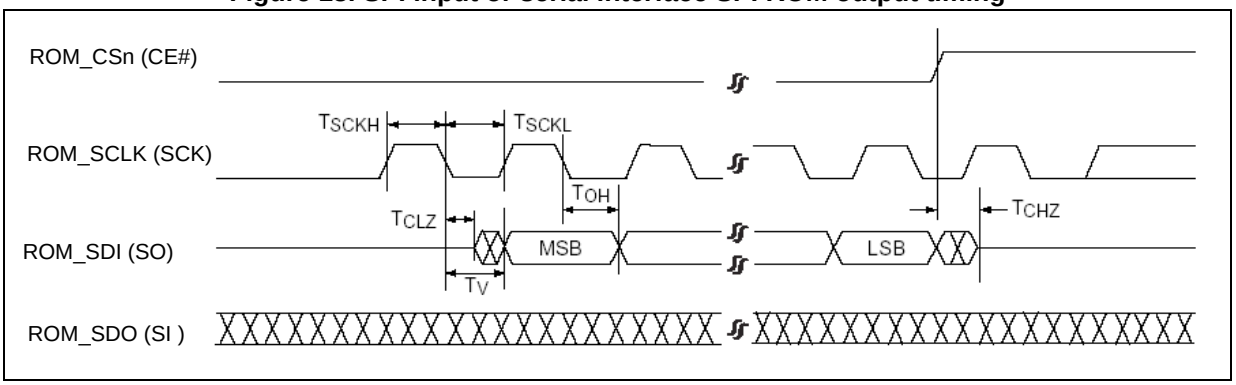


Figure 18. SPI input or serial interface SPI ROM output timing



9. Ordering information

Table 23. Order codes

Part number	Description
STDP3150-AB	64-pin QFN, 6 x 6 mm

10. Revision history

Table 24. Document revision history

Date	Revision	Changes
19-Jul-2012	A	Initial version.
22-Nov-2012	B	Page 12, Table 2 DisplayPort receiver pins: B17 I/O changed to AG. Chapter 8, package diagrams and dimensions updated (changed from QFN Ts-CSP2 type to QFN DRMLF type)
23-Jan-2013	C	Page 9, updated pin diagram. All instances of DisplayPort 1.1a changed to DisplayPort 1.2a. Solder profile content removed and relocated to “DisplayPort application note: Classification reflow profile” (C0353-APN-06).
08-May-2014	D	Updated to comply with MegaChips documentation style/formatting.
22-Aug-2014	E	Added Section 7.2 Marking field template and descriptors.
29-Aug-2014	F	Corrected marking diagram and descriptors.

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