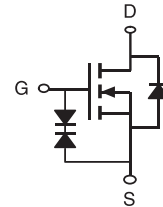


**N-Channel Logic Level Enhancement Mode Field Effect Transistor****PRODUCT SUMMARY**

V _{DSS}	I _D	R _{DS(ON)} (mΩ) Typ
60V	16A	64 @ V _{GS} =10V
		81 @ V _{GS} =4.5V

FEATURES

- Super high dense cell design for low R_{DS(ON)}.
- Rugged and reliable.
- Surface Mount Package.
- ESD Protected.

**ABSOLUTE MAXIMUM RATINGS (T_C=25°C unless otherwise noted)**

Symbol	Parameter	Limit	Units
V _{DS}	Drain-Source Voltage	60	V
V _{GS}	Gate-Source Voltage	±20	V
I _D	Drain Current-Continuous ^a T _A =25°C	16	A
I _{DM}	-Pulsed ^b	46.8	A
I _{AS}	Avalanche Current ^c	9	A
E _{AS}	Avalanche Energy ^c	20.25	mJ
P _D	Maximum Power Dissipation ^a T _A =25°C	60	W
T _J , T _{STG}	Operating Junction and Storage Temperature Range	-55 to 175	°C

THERMAL CHARACTERISTICS

R _{θJC}	Thermal Resistance, Junction-to-Case	2.5	°C/W
R _{θJA}	Thermal Resistance, Junction-to-Ambient	50	°C/W

STU/D616S

Ver1.1

ELECTRICAL CHARACTERISTICS (T_C=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
OFF CHARACTERISTICS						
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V , I _D =250uA	60			V
BV _{DSS}	Drain-Source Breakdown Voltage ^e	V _{GS} =0V , I _D =10mA	65			V
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} =48V , V _{GS} =0V			1	A
I _{GSS}	Gate-Body leakage current	V _{GS} = ±20V , V _{DS} =0V			±10	uA
ON CHARACTERISTICS ^a						
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =250uA	1	1.8	3	V
R _{DS(ON)}	Drain-Source On-State Resistance	V _{GS} =10V , I _D =8A		64	77	m ohm
		V _{GS} =4.5V , I _D =6A		81	99	m ohm
g _{FS}	Forward Transconductance	V _{DS} =5V , I _D =8A		13.5		S
DYNAMIC CHARACTERISTICS ^b						
C _{ISS}	Input Capacitance	V _{DS} =20V,V _{GS} =0V f=1.0MHz		780		pF
C _{OSS}	Output Capacitance			58.5		pF
C _{RSS}	Reverse Transfer Capacitance			46.5		pF
SWITCHING CHARACTERISTICS ^b						
t _{D(ON)}	Turn-On DelayTime	V _{DD} =30V I _D =1A		14		ns
t _r	Rise Time			13		ns
t _{D(OFF)}	Turn-Off DelayTime	V _{GS} =10V R _{GEN} = 6 ohm		38		ns
t _f	Fall Time			9.4		ns
Q _g	Total Gate Charge	V _{DS} =30V,I _D =8A,V _{GS} =10V		13.5		nC
		V _{DS} =30V,I _D =8A,V _{GS} =4.5V		6.7		nC
Q _{gs}	Gate-Source Charge	V _{DS} =30V,I _D =8A,		1.88		nC
Q _{gd}	Gate-Drain Charge	V _{GS} =10V		3.71		nC
DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS						
I _S	Maximum Continuous Drain-Source Diode Forward Current				1.5	A
V _{SD}	Diode Forward Voltage	V _{GS} =0V,I _S =1.5A		0.8	1.3	V
Notes						
a.Pulse Test:Pulse Width ≤ 300us, Duty Cicle ≤ 2%.						
b.Guaranteed by design, not subject to production testing.						
c.Starting T _J =25° C,L=0.5mH,R _G =25Ω,I _{AS} =9A,V _{DD} ≤ V _(BR) DSS.(See Figure13)						
e.Pulse Test : Pulse Width < 1us,Duty Cycle < 1%.						

Feb,12,2010

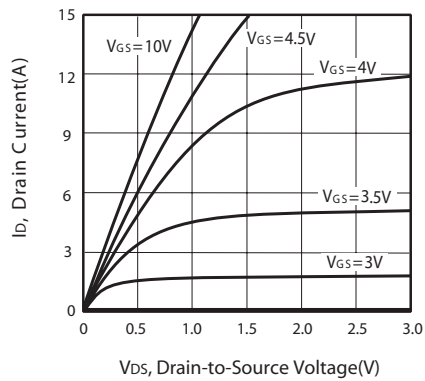


Figure 1. Output Characteristics

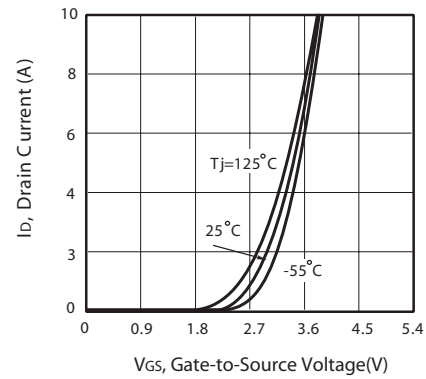


Figure 2. Transfer Characteristics

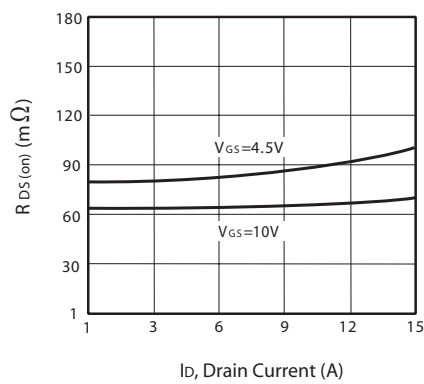


Figure 3. On-Resistance vs. Drain Current and Gate Voltage

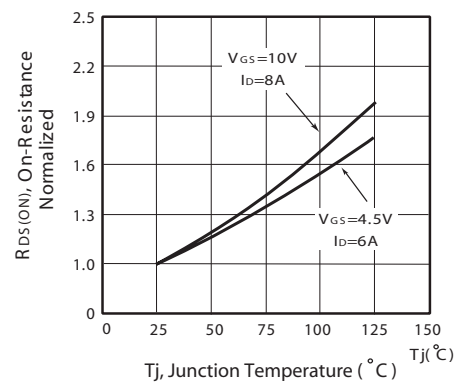


Figure 4. On-Resistance Variation with Drain Current and Temperature

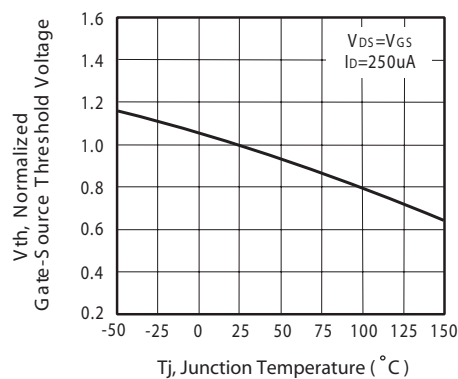


Figure 5. Gate Threshold Variation with Temperature

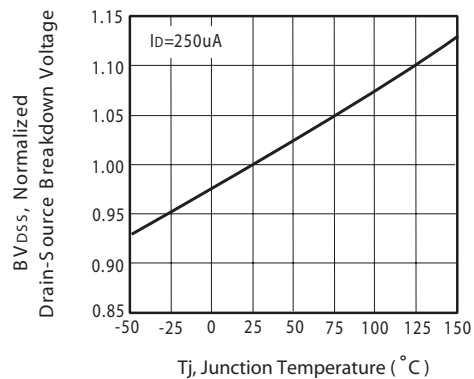


Figure 6. Breakdown Voltage Variation with Temperature

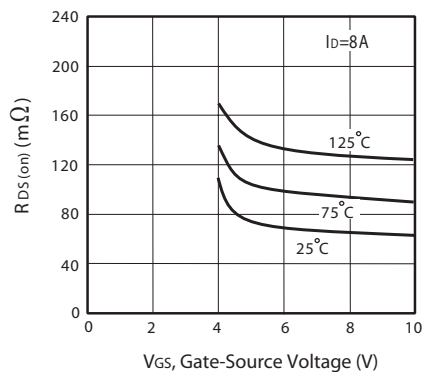


Figure 7. On-Resistance vs. Gate-Source Voltage

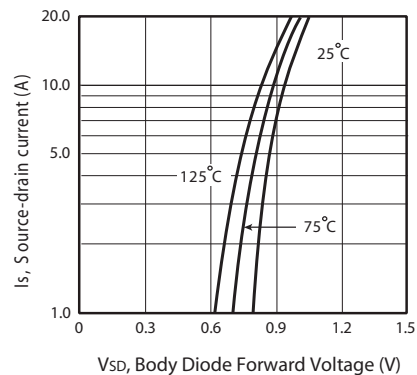


Figure 8. Body Diode Forward Voltage Variation with Source Current

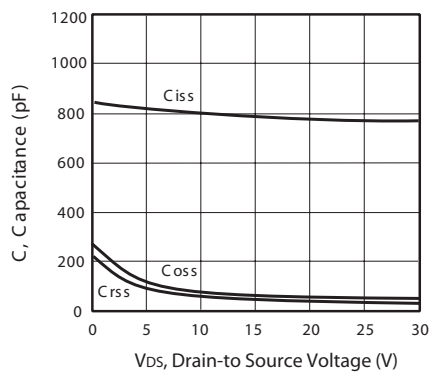


Figure 9. Capacitance

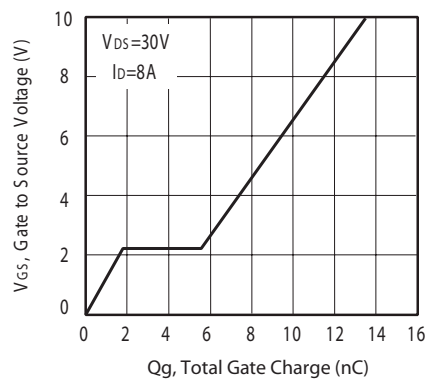


Figure 10. Gate Charge

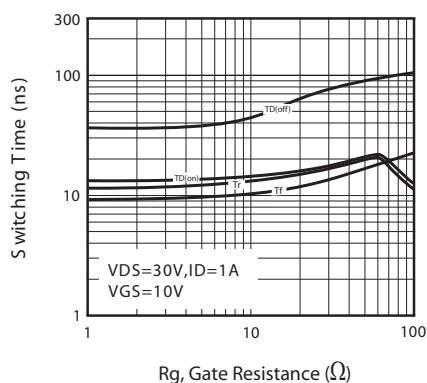


Figure 11. Switching Characteristics

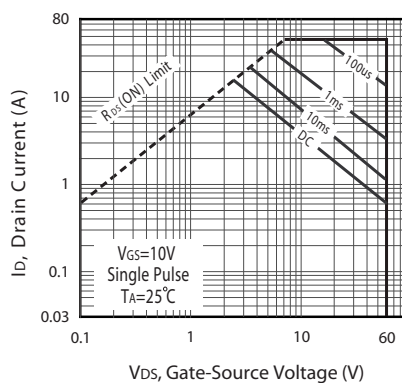
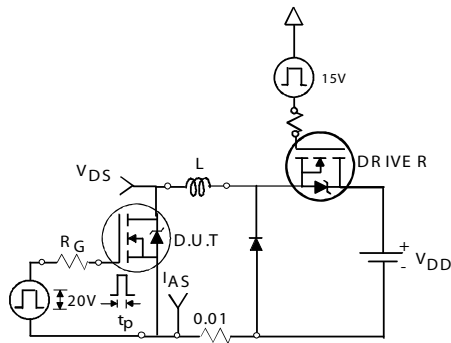
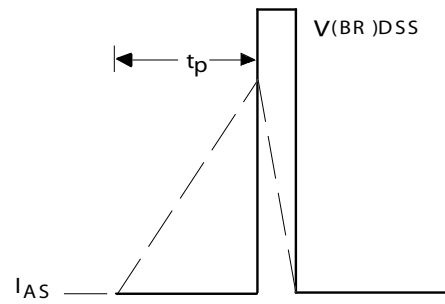


Figure 12. Maximum Safe Operating Area



Unclamped Inductive Test Circuit

Figure 13a.



Unclamped Inductive Waveforms

Figure 13b.

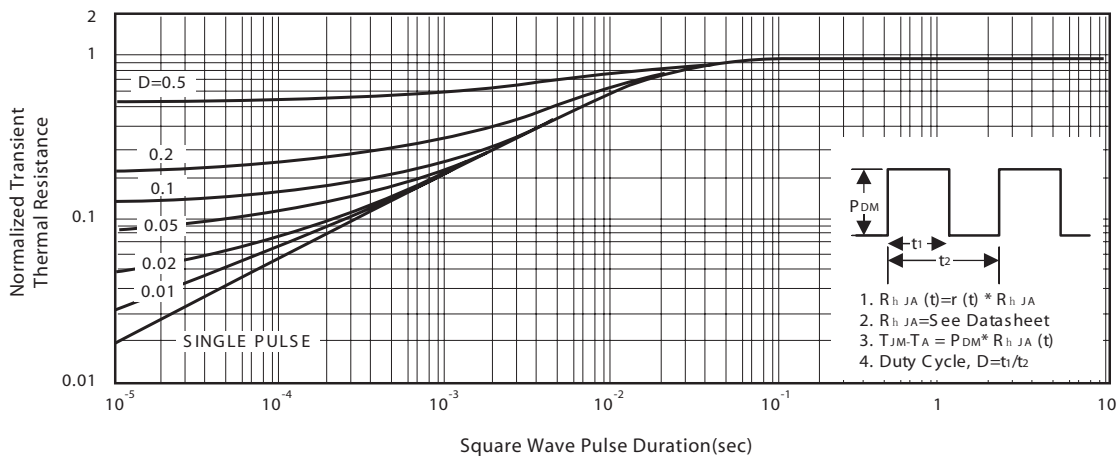


Figure 14. Normalized Thermal Transient Impedance Curve

PACKAGE OUTLINE DIMENSIONS

