STD3PK50Z

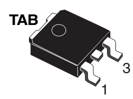
P-channel 500 V, 3 Ω typ., 2.8 A Zener-protected SuperMESH™ Power MOSFET in a DPAK package

Datasheet — production data

Features

Order code	V_{DSS}	$R_{DS(on)}$max	I_D	P_{TOT}
STD3PK50Z	500 V	< 4Ω	2.8 A	70 W

- Gate charge minimized
- Extremely high dv/dt capability
- 100% avalanche tested
- Very low intrinsic capacitance
- Improved ESD capability



DPAK

Applications

- Switching applications

Description

This device is a P-channel Zener-protected Power MOSFET developed using STMicroelectronics' SuperMESH™ technology, achieved through optimization of ST's well established strip-based PowerMESH™ layout. In addition to a significant reduction in on-resistance, this device is designed to ensure a high level of dv/dt capability for the most demanding applications.

Figure 1. Internal schematic diagram

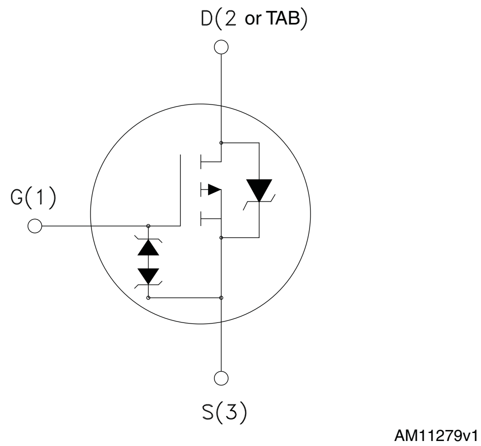


Table 1. Device summary

Order code	Marking	Package	Packaging
STD3PK50Z	3PK50Z	DPAK	Tape and reel

Note: For the P-channel Power MOSFETs actual polarity of voltages and current has to be reversed.

Contents

1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain source voltage	500	V
V_{GS}	Gate- source voltage	± 30	V
I_D	Drain current (continuous) at T_C = 25 °C	2.8	A
I_D	Drain current (continuous) at T_C = 100 °C	1.8	A
I_{DM} (1)	Drain current (pulsed)	11	A
P_{TOT}	Total dissipation at T_C = 25 °C	85	W
I_{AR}	Max current during repetitive or single pulse avalanche (pulse width limited by T_{jmax})	2.8	A
E_{AS}	Single pulse avalanche energy (starting T_J = 25 °C, I_D=I_{AS}, V_{DD}= 50 V)	200	mJ
dv/dt (2)	Peak diode recovery voltage slope	40	V/ns
ESD	Gate-source human body model (R = 1,5 k, C = 100 pF)	3	kV
T_j T_{stg}	Operating junction temperature Storage temperature	- 55 to 150	°C

1. Pulse width limited by safe operating area.
2. I_{SD} ≤ 2.8 A, di/dt ≤ 200 A/µs, V_{Peak} ≤ $V_{(BR)DSS}$

Table 3. Thermal data

Symbol	Parameter	Value	Unit
Rthj-case	Thermal resistance junction-case max	1.47	°C/W
Rthj-pcb	Thermal resistance junction-pcb max	50	°C/W

Note: For the P-channel Power MOSFETs actual polarity of voltages and current has to be reversed.

2 Electrical characteristics

(T_{CASE} = 25 °C unless otherwise specified)

Table 4. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	I_D = 1 mA, V_{GS}= 0	500			V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = 500 V, V_{DS} = 500 V,Tc=125 °C			1 100	µA µA
I_{GSS}	Gate body leakage current (V_{DS} = 0)	V_{GS} = ± 25 V			±10	µA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 100 µA	3	3.75	4.5	V
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS} = 10 V, I_D= 1.4 A		3	4	Ω

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} =50 V, f=1 MHz, V_{GS}=0	-	530 50 25	-	pF pF pF
$C_{o(tr)}$(1)	Equivalent capacitance time related	V_{GS} = 0, V_{DS} = 0 to 400 V	-	32	-	pF
$C_{o(er)}$(2)	Equivalent capacitance energy related		-	23	-	pF
R_G	Intrinsic gate resistance	f = 1MHz open drain	-	4.7	-	Ω
Q_g Q_{gs} Q_{gd}	Total gate charge Gate-source charge Gate-drain charge	V_{DD} = 400 V, I_D = 2.8 A V_{GS} =10 V *(see Figure 14)*	-	29 4.3 15	-	nC nC nC

1. Time related is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}
2. energy related is defined as a constant equivalent capacitance giving the same stored energy as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}

Note: For the P-channel Power MOSFETs actual polarity of voltages and current has to be reversed.

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$ t_r $t_{d(off)}$ t_f	Turn-on delay time Rise time Turn-off delay time Fall time	V_{DD} = 250 V, I_D = 1.4 A, R_G=4.7 Ω, V_{GS}=10 V *(see Figure 13)*	-	16 15 46 26	-	ns ns ns ns

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD} I_{SDM}	Source-drain current Source-drain current (pulsed)		-		2.8 11.2	mA A
V_{SD}(1)	Forward on voltage	I_{SD}= 2.8 A, V_{GS}=0	-		1.5	V
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	I_{SD}= 2.8 A, V_{DD}= 60 V di/dt = 100 A/µs, *(see Figure 15)*	-	220 1600 14		ns nC A
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	I_{SD}= 2.8 A,V_{DD}= 60 V di/dt=100 A/µs, Tj=150 °C *(see Figure 15)*	-	280 2100 15		ns nC A

1. Pulsed: pulse duration = 300µs, duty cycle 1.5%

Table 8. Gate-source Zener diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
BV_{GSO}	Gate-source breakdown voltage	Igs ± 1mA, (open drain)	30	-		V

The built-in back- to-back Zener diodes have specifically been designed to enhance not only the device's ESD capability, but also to make them safely absorb possible voltage transients that may occasionally be applied from gate to source. In this respect the Zener voltage is appropriate to achieve an efficient and cost-effective intervention to protect the device's integrity. These integrated Zener diodes thus avoid the usage of external components.

Note: For the P-channel Power MOSFETs actual polarity of voltages and current has to be reversed.

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

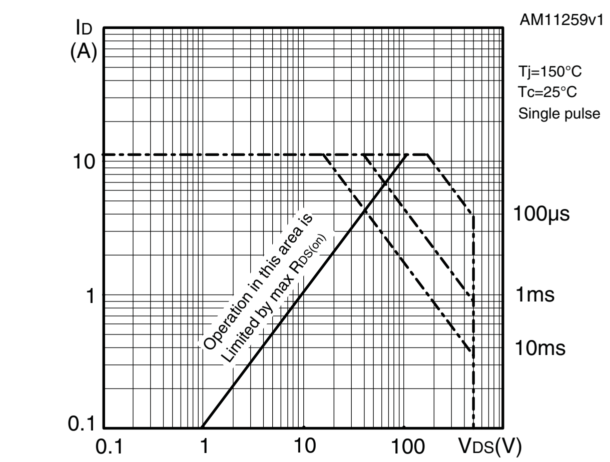


Figure 3. Thermal impedance

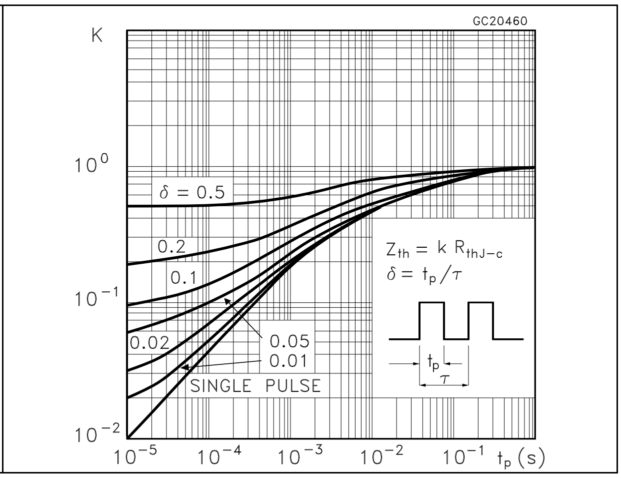


Figure 4. Output characteristics

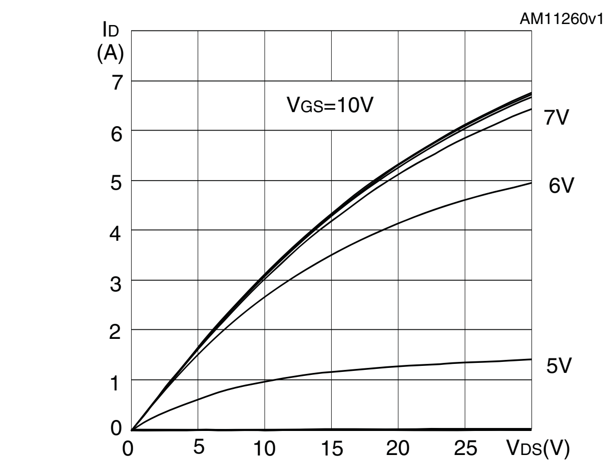


Figure 5. Transfer characteristics

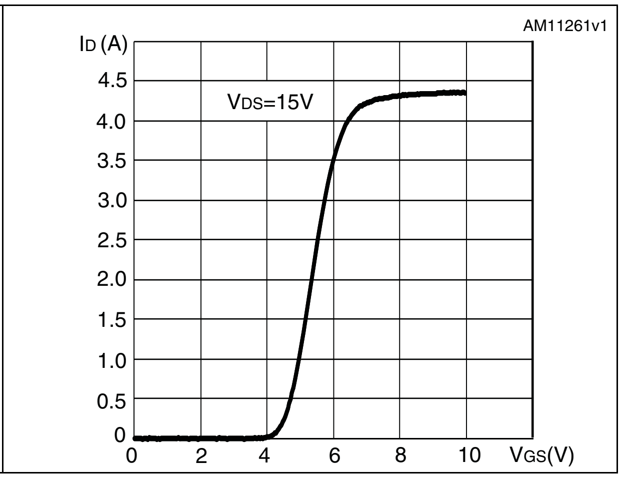


Figure 6. Normalized B_{VDSS} vs temperature

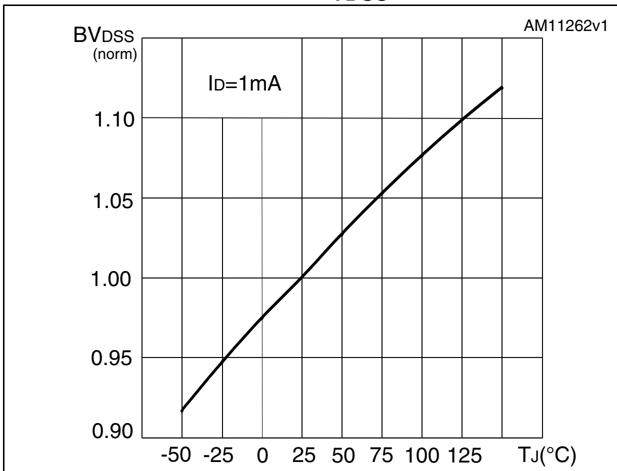


Figure 7. Static drain-source on-resistance

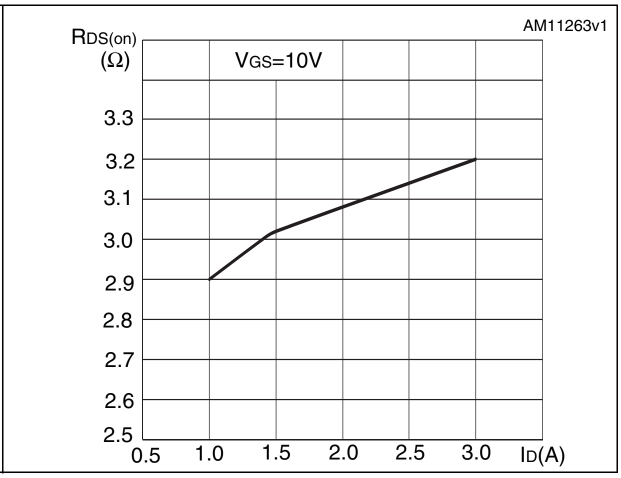


Figure 8. Gate charge vs gate-source voltage

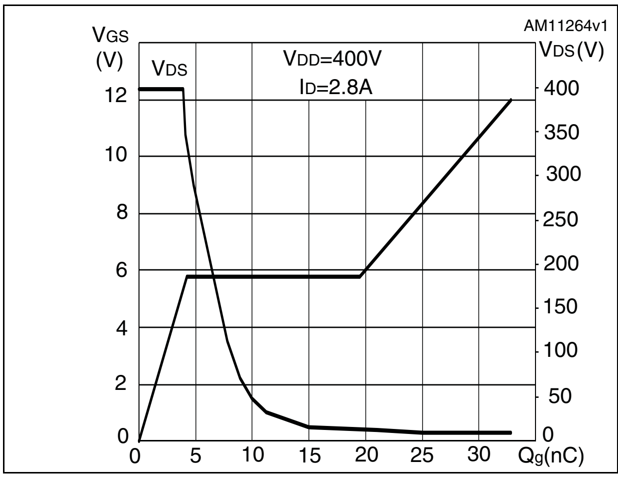


Figure 9. Capacitance variations

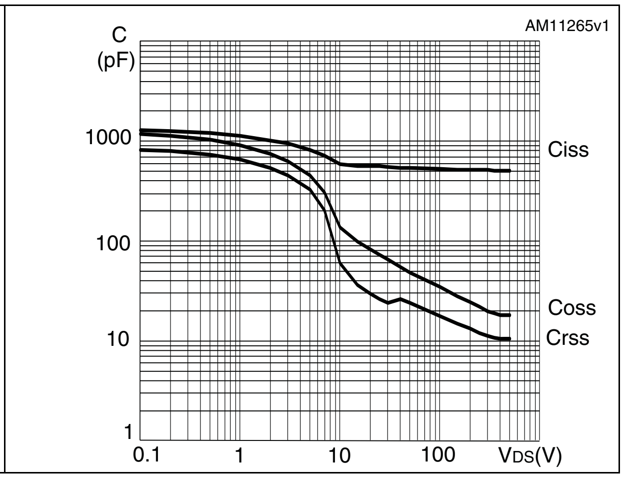


Figure 10. Normalized gate threshold voltage vs temperature

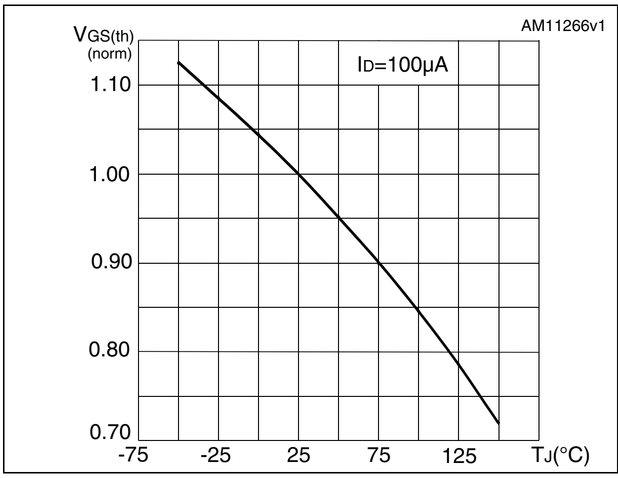


Figure 11. Normalized on-resistance vs temperature

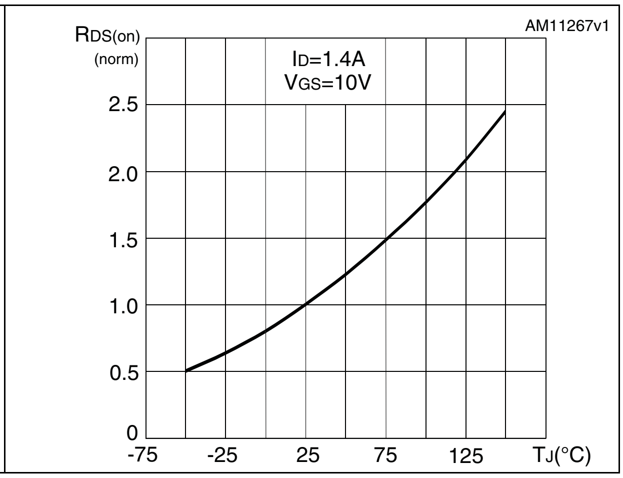
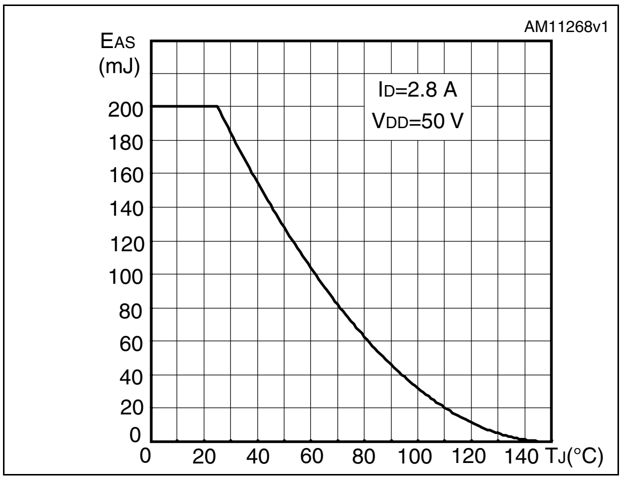


Figure 12. Maximum avalanche energy vs starting Tj



3 Test circuits

Figure 13. Switching times test circuit for resistive load

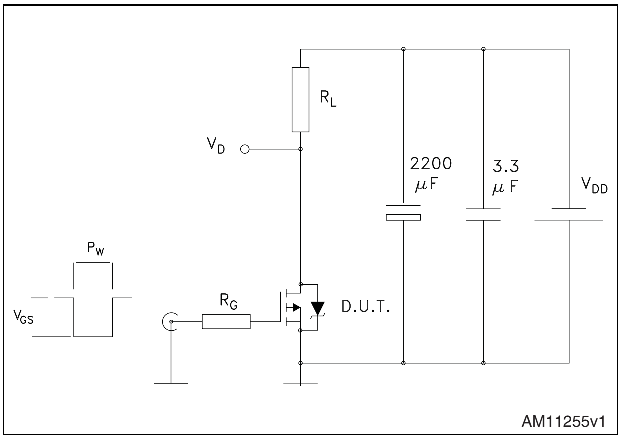


Figure 14. Gate charge test circuit

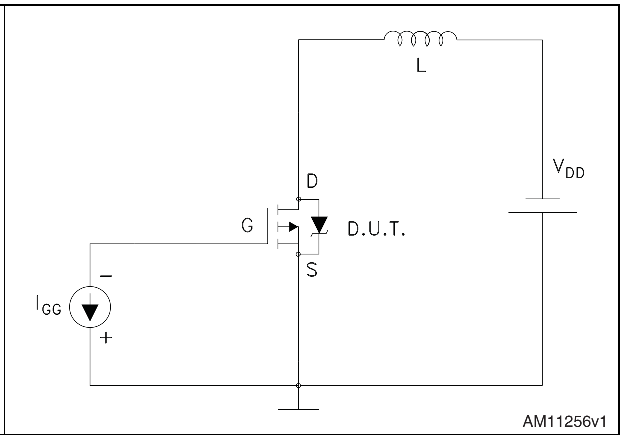
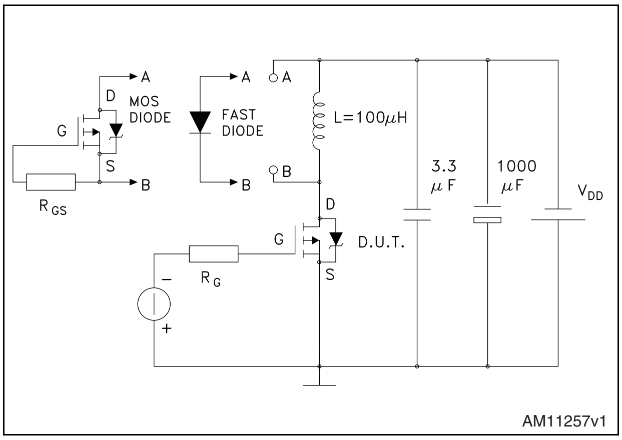


Figure 15. Test circuit for diode recovery behavior



4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

Table 9. DPAK (TO-252) mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	2.20		2.40
A1	0.90		1.10
A2	0.03		0.23
b	0.64		0.90
b4	5.20		5.40
c	0.45		0.60
c2	0.48		0.60
D	6.00		6.20
D1		5.10	
E	6.40		6.60
E1		4.70	
e		2.28	
e1	4.40		4.60
H	9.35		10.10
L	1		1.50
L1		2.80	
L2		0.80	
L4	0.60		1
R		0.20	
V2	0°		8°

Figure 16. DPAK (TO-252) drawing

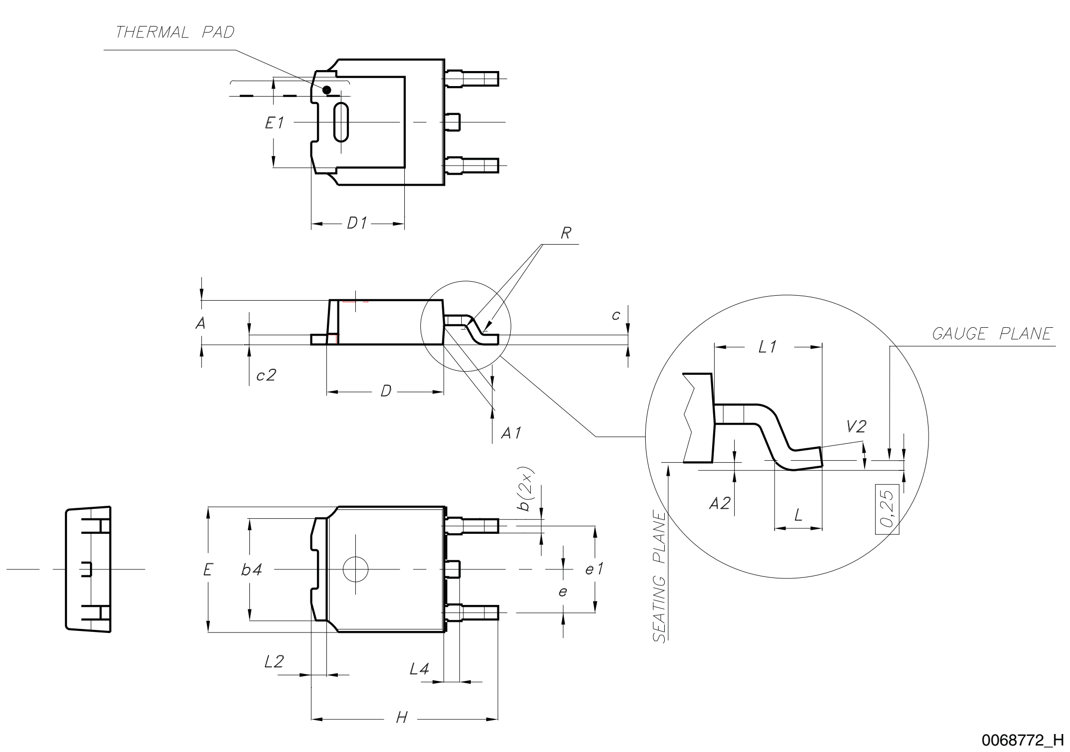
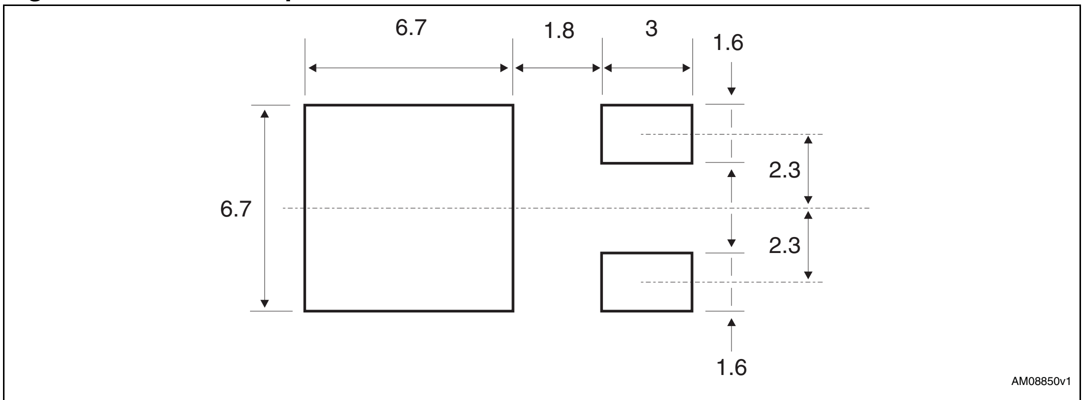


Figure 17. DPAK footprint[a]



a. All dimensions are in millimeters

5 Packaging mechanical data

Table 10. DPAK (TO-252) tape and reel mechanical data

Tape			Reel		
Dim.	mm		Dim.	mm	
	Min.	Max.		Min.	Max.
A0	6.8	7	A		330
B0	10.4	10.6	B	1.5	
B1		12.1	C	12.8	13.2
D	1.5	1.6	D	20.2	
D1	1.5		G	16.4	18.4
E	1.65	1.85	N	50	
F	7.4	7.6	T		22.4
K0	2.55	2.75			
P0	3.9	4.1	Base qty.		2500
P1	7.9	8.1	Bulk qty.		2500
P2	1.9	2.1			
R	40				
T	0.25	0.35			
W	15.7	16.3			

Figure 18. Tape for DPAK (TO-252)

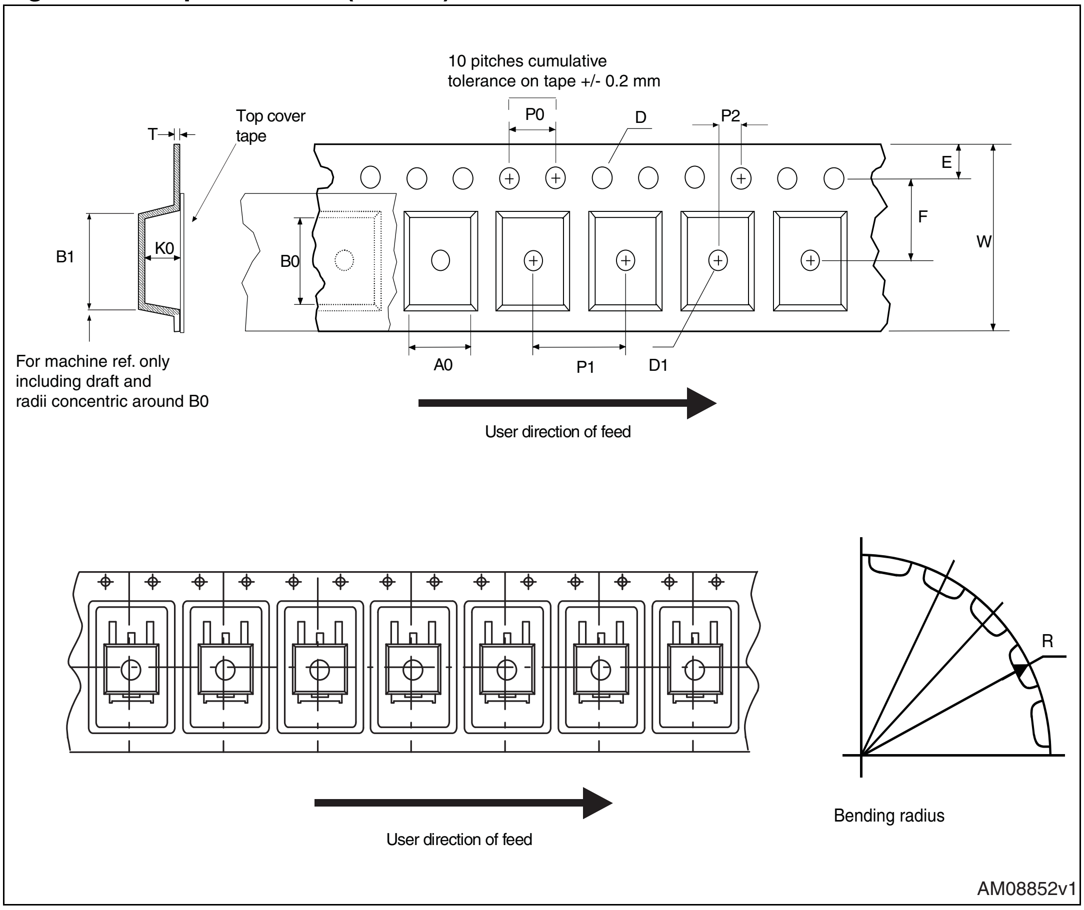
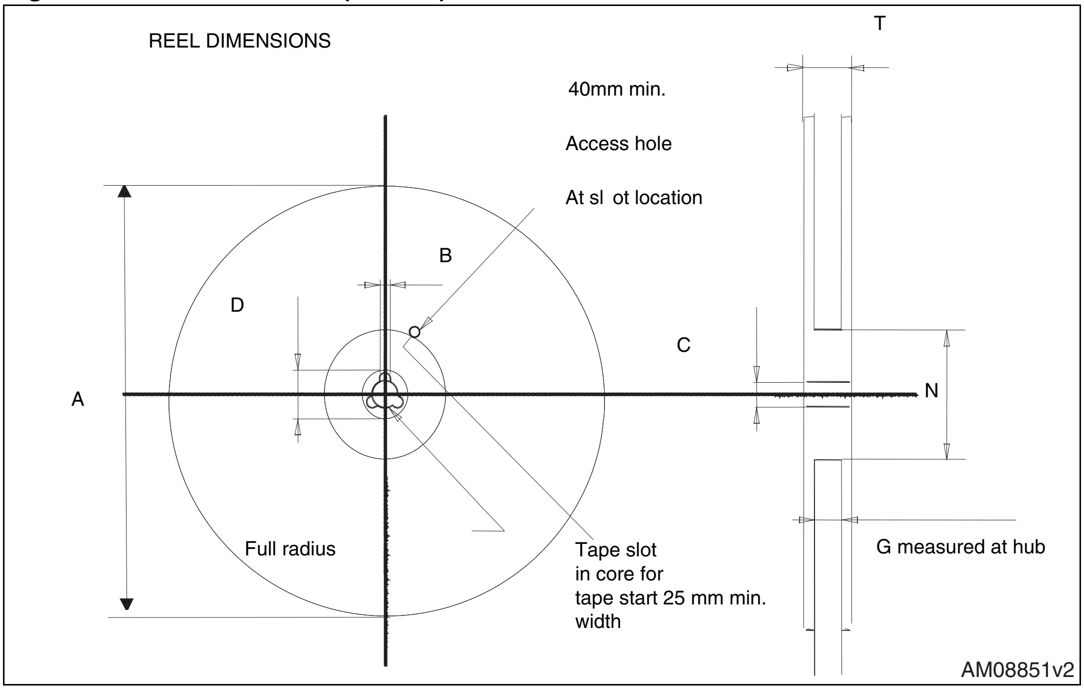


Figure 19. Reel for DPAK (TO-252)



6 Revision history

Table 11. Document revision history

Date	Revision	Changes
26-Nov-2010	1	First release.
31-Aug-2012	2	Document status promoted from preliminary data to production data. Minor text changes on the cover page.