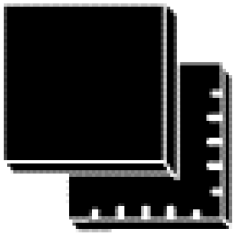
STBLW35

Datasheet

Ultra-low power and wide input range buck-boost converter



VFQFPN 3 x 3 x 1 mm 20L

Features

- Seamless transition from Buck-Boost to Boost and vice versa working mode
- Up to 70 mA output current
- Four fully integrated MOSFETs
- Enable pin
- 2.6 V to 5.3 V trimmable overvoltage level (± 1% accuracy)
- 2.2 V to 3.6 V trimmable undervoltage level (± 1% accuracy)
- Two fully independent LDOs (1.8 V and 3.3 V output)
- Enable/disable LDO control pins
- Load disconnect function at first switch-on
- Embedded pass transistor status and DC-DC status open drain indication pins

Application

- WSN, building and home automation, industrial control, security, surveillance
- Wearable and biomedical sensors, fitness
- Battery charging

Description

The STBLW35 is an ultra-low power and high-efficiency buck-boost DC-DC converter which can work as boost or buck-boost according to the selected hardware configuration. When in buck-boost the DC-DC can seamlessly switch between the two working modes depending on operating conditions.

The IC shows very low power losses either in active or disable mode and provides an average output current between 33 mA to 70 mA, suitable to guarantee load minimum current constraints or to faster charge a battery. The device also allows the charge of any battery by tightly monitoring the end-of-charge and the minimum battery voltage in order to avoid overdischarge and to preserve battery life.

The power manager covers the input voltage range from 150 mV up to 18 V and guarantees high efficiency in both buck-boost and boost configuration.

Furthermore, the STBLW35 device shows very high flexibility thanks also to the trimming capability of the overvoltage and the undervoltage protection voltages.

In order to optimize the power consumption during system operation, the device can be driven in standby mode thanks to the high impedance Enable pin.

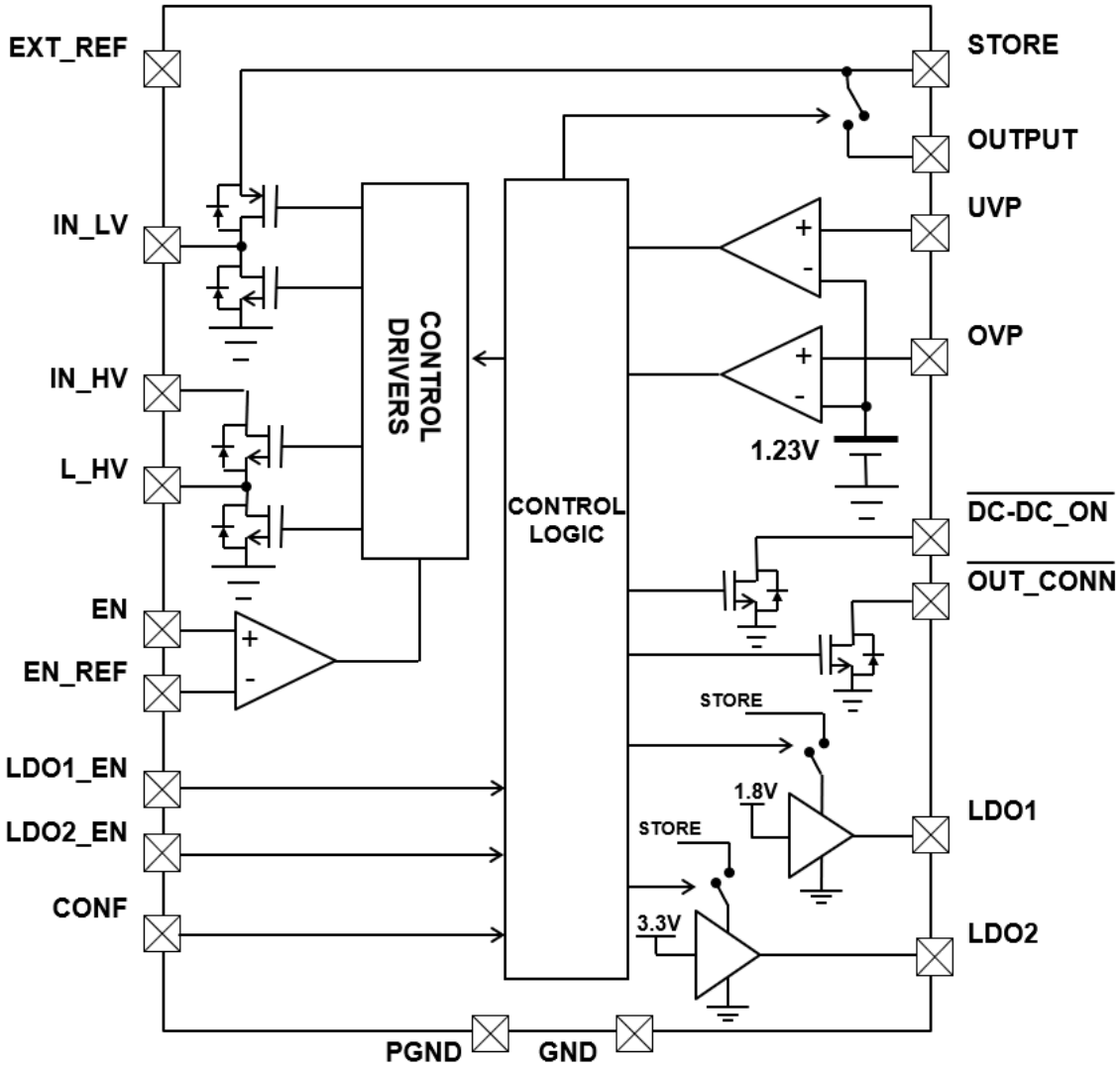
An unregulated voltage output is available (to supply a transceiver for instance), while two fully independent LDOs are embedded for powering sensors and other companion chips. Both LDOs (1.8 V and 3.3 V) can be independently enabled through dedicated pins.

Product status link
STBLW35

Product label
SUSTAINABLE TECHNOLOGY

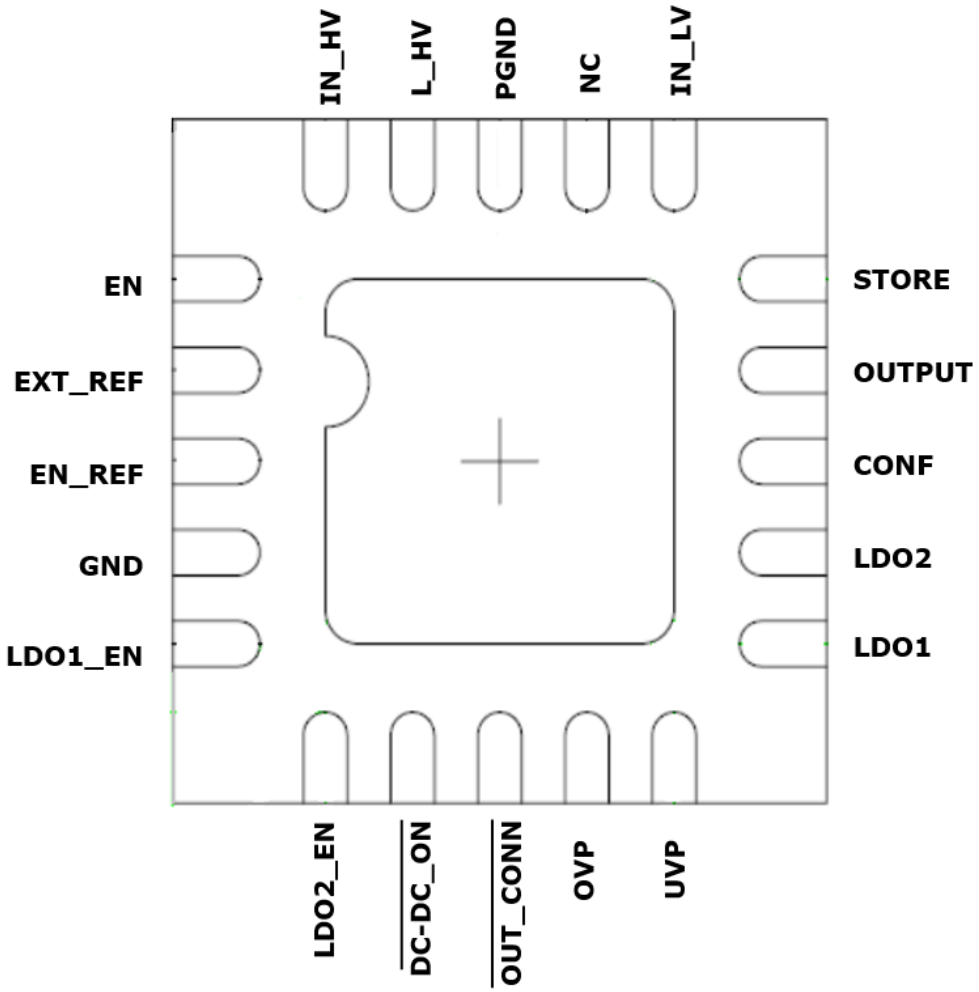
1 Block Diagram

Figure 1. **Block diagram**



2 Pin configuration

Figure 2. Pin out (top through view)



3 Pin description

Table 1. Pin description

Pin no.	Name	Type	Description
1	EN	I	Enable/disable switching pin. Connected to the supply voltage (directly or by a resistor partitioning, see Section 6 Functional description, Section 6.2 Boost configuration and Section 6.3 Buck-boost configuration).
2	EXT_REF	I	Connect this pin (by a short or by a 1 kΩ resistor) to an external voltage reference or to STORE pin.
3	EN_REF	I	Connect this pin to an external voltage reference: the DC-DC switches when $V_{EN} > V_{EN\_REF}$ and stops switching when $V_{EN} \leq V_{EN\_REF}$. Connecting this pin to ground enables continuous switching of the DC-DC converter provided that enough power is available at the source and other protections (e.g. overvoltage) are not active.
4	GND	GND	Signal ground pin.
5	LDO1_EN	I	If high, enables LDO1.
6	LDO2_EN	I	If high, enables LDO2.
7	$\overline{\text{DC-DC\_ON}}$	O	DC-DC ON output flag pin (open drain). If low, it indicates that the DC-DC is switching. If high, it indicates that the DC-DC is not switching.
8	$\overline{\text{OUT\_CONN}}$	O	Embedded pass transistor connection status pin (open drain). If high, it indicates that the pass transistor between the STORE and OUTPUT pins is open (load disconnected). If low, it indicates that the pass transistor between the STORE and OUTPUT pins is closed (load connected).
9	OVP	I	Output overvoltage protection pin. To be connected to the STORE pin through a resistor divider. Internal DC-DC stops/restarts switching when the voltage at OVP pin is higher/lower than the internal bandgap voltage. Also, at startup (internal pass transistor between STORE and OUTPUT is still open) and while V_{STORE} is increasing, the triggering of the internal bandgap voltage makes the internal pass transistor close.
10	UVP	I	Output undervoltage protection pin. To be connected to the STORE pin through a resistor divider. Internal pass transistor between STORE and OUTPUT pins opens when the voltage at UVP pin goes below the internal bandgap voltage.
11	LDO1	O	1.8 V regulated output voltage pin.
12	LOD2	O	3.3 V regulated output voltage pin.
13	CONF	I	DC-DC converter configuration pin. Boost configuration: CONF pin connected to the input supply source (see Figure 4. Boost configuration). Buck-boost configuration: CONF pin connected to ground (see Figure 11. Buck-boost configuration).
14	OUTPUT	I/O	Load connection pin.
15	STORE	I/O	Tank capacitor connection pin.
16	IN_LV	I	Low voltage input source. It has to be connected to the inductor for both boost and buck-boost configuration. See Figure 4. Boost configuration and Figure 11. Buck-boost configuration.
17	NC	I	Not connected.
18	PGND	PGND	Power ground pin.
19	L_HV	I	Input pin for buck-boost configuration. Boost configuration: to be connected to ground. Buck-boost configuration: to be connected to the inductor (see Figure 11. Buck-boost configuration).

Pin no.	Name	Type	Description
20	IN_HV	I	High voltage input source. Boost configuration: to be connected to ground. Buck-boost configuration: to be connected to the voltage supply source (see Figure 11. Buck-boost configuration).

4 Maximum ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
IN_LV	Analog input	V_{STORE} + 0.3	V
IN_HV	Analog input	20	V
L_HV	Analog input	IN_HV + 0.3	V
CONF	Analog input	5.5	V
EN	Analog input	5.5	V
EXT_REF	Analog input	5.5	V
EN_REF	Analog input	5.5	V
OUTPUT	Analog input/output	5.5	V
STORE	Analog input/output	5.5	V
UVP	Analog input	V_{STORE} + 0.3	V
OVP	Analog input	V_{STORE} + 0.3	V
$\overline{OUT\_CONN}$	Digital output	5.5	V
$\overline{DC\text{-}DC\_ON}$	Digital output	5.5	V
LDO1_EN	Digital input	V_{STORE} + 0.3	V
LDO2_EN	Digital input	V_{STORE} + 0.3	V
LDO1	Analog output	V_{STORE} + 0.3	V
LDO2	Analog output	V_{STORE} + 0.3	V
PGND	Power ground	0	V
GND	Signal ground	-0.3 to 0.3	V
T_J	Junction temperature	-40 to 125	°C
$T_{STORAGE}$	Storage temperature	150	°C

Table 3. Thermal data

Symbol	Parameter	Value	Unit
$R_{th(JC)}$	Thermal resistance junction-case	7.5	°C/W
$R_{th(JA)}$ (1)	Thermal resistance junction-ambient	49	°C/W

1. *Measured on 2-layer application board FR4, Cu thickness = 17 um with total exposed pad area = 16 mm^2.*

5 Electrical characteristics

V_{STORE} = 4 V; -40 °C < T_J < 85 °C, unless otherwise specified. Voltage with respect to GND, unless otherwise specified.

Table 4. Electrical characteristics

Symbol	Parameter	Test conditions		Min.	Typ.	Max.	Unit
Output operating range							
I_{OUT}	Maximum output current	Boost configuration		-	-	70	mA
		Buck-boost configuration		33	35	-	
V_{OUT}	OUTPUT pin voltage range			2.2	-	5.3	V
R_{OUT}	Pass transistor resistance			6	7	8	Ω
Bandgap							
V_{BG}	Internal reference voltage			-	1.23	-	V
	Accuracy			-1	-	+1	%
UVP							
$V_{STORE(UVP)}$	V_{STORE} undervoltage protection range	(V_{UVP} + UVP_{HYS}) < (V_{OVP} - OVP_{HYS})		2.2	-	3.6	V
UVP_{HYS}	UVP hysteresis	V_{STORE} rising		-	5	-	%
OVP							
$V_{STORE(OVP)}$	V_{STORE} end-of-charge voltage range	(V_{UVP} + UVP_{HYS}) < (V_{OVP} - OVP_{HYS})		2.6	-	5.3	V
OVP_{HYS}	OVP hysteresis	V_{STORE} falling		-	-1	-	%
STORE							
V_{STORE}	STORE pin voltage operating range			$V_{STORE(UVP)}$	-	$V_{STORE(OVP)}$	V
Static current consumption							
I_{SD}	Shutdown current	Shutdown mode: before first startup or $\overline{OUT\_CONN}$ high T_{AMB} < 60 °C		-	-	1	nA
I_{SB}	Standby current	Standby mode: $\overline{OUT\_CONN}$ low, $\overline{DC\text{-}DC\_ON}$ high, V_{STORE} = 5.3 V and LDO1,2_EN low T_{AMB} = 25 °C		-	0.8	-	µA
I_{OP}	Operating current in open load	Operating mode: LDOs in open load $\overline{OUT\_CONN}$ low, $\overline{DC\text{-}DC\_ON}$ high T_{AMB} = 25 °C	LDO1_EN = 1 or LDO2_EN = 1	-	1.7	-	µA
			LDO1_EN = 1 and LDO2_EN = 1	-	2.6	-	
DC-DC converter							

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{IN-SU}	Minimum input voltage to startup	Boost configuration $\overline{OUT\_CONN}$ high or at first startup	-	0.55	0.58	V
		Buck-boost configuration $\overline{OUT\_CONN}$ high or at first startup	-	2.6	2.8	
I_{SU}	Start-up input current	Boost configuration	-	30	-	µA
		Buck-boost configuration	-	5	-	
V_{IN_LV}	Operating input voltage range	Boost configuration	0.15	-	V_{EOC}	V
V_{IN_HV}		Buck-boost configuration	0.15	-	18	
V_{EN}	EN pin voltage range		0.075		V_{UVP}	V
$R\text{-}ON_B$	Low-side MOS resistance	Boost configuration	0.5	1.0	1.5	Ω
$SR\text{-}ON_B$	Synchronous rectifier MOS resistance		0.5	1.0	1.5	
$R\text{-}ON_{BB}$	Low-side MOS resistance	Buck-boost configuration	1	1.5	2	Ω
$SR\text{-}ON_{BB}$	Synchronous rectifier MOS resistance		1	1.5	2	
f_{SW}	Maximum allowed switching frequency	Boost and buck-boost configurations	-	-	1	MHz
$UVLO_H$	Undervoltage lockout activation threshold	V_{STORE} rising	-	2.6	2.8	V
$UVLO_L$	Undervoltage lockout deactivation threshold	V_{STORE} falling	2	2.1	-	V
LDO						
$V_{LDO1,2}$	LDO1,2 adjusted output voltage	LDO1_EN = 1		1.8		V
		LDO2_EN = 1		3.3		
$\Delta V_{LDO1,2}$	LDO1 dropout	V_{UVP} + 200 mV < V_{OUT} ≤ 5.3 V; I_{LDO1} = 100 mA			0.5	%
	LDO2 dropout	3.3 < V_{UVP} + 200 mV < V_{OUT} ≤ 5.3 V; I_{LDO2} = 100 mA			0.5	
t_{LDO}	LDO1,2 START-up time	$\overline{OUT\_CONN}$ = low; $C_{LDO1,2}$ = 100 nF	-	-	1	ms
$I_{LDO1,2}$[1]	I_{OUT} max. from LDO1		-	-	200	mA
	I_{OUT} max. from LDO2		-	-	200	mA
$V_{LDO1,2\_EN\_H}$	LDO1,2 enable input HIGH		1	-	-	V
$V_{LDO1,2\_EN\_L}$	LDO1,2 enable input LOW		-	-	0.5	V
Digital output						
$V_{\overline{OUT\_CONN}\_L}$	$V_{\overline{OUT\_CONN}}$ = low	1 mA sink current	40	70	150	mV
$V_{\overline{DC\text{-}DC\_ON}\_L}$	$V_{\overline{DC\text{-}DC\_ON}}$ = low	1 mA sink current	40	70	150	mV

1. *Guaranteed by design, not tested in production.*

6 Functional description

The STBLW35 integrates a DC-DC converter stage that can be configured as boost or buck-boost by tying the CONF pin to positive rail of the supply or to ground, respectively (see Figure 4. Boost configuration and Figure 11. Buck-boost configuration).

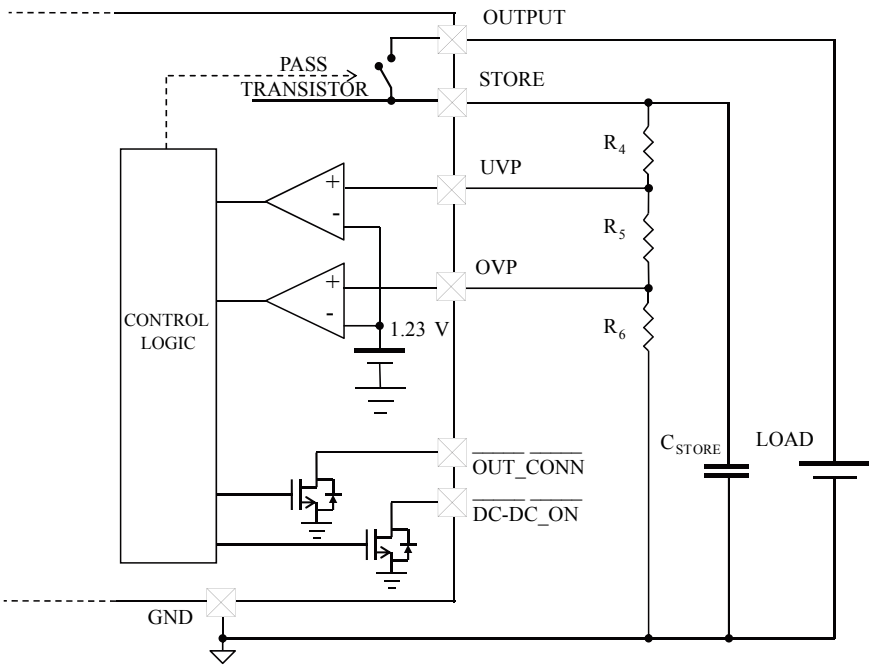
In normal operation the IC works with the EN pin connected to the input supply rail (directly or by a resistor partitioning according to voltage range of the supply source, operating range and absolute maximum rating of the EN pin), EXT_REF pin connected to the STORE pin and by EN_REF pin connected to a voltage reference. After the first startup (see Figure 5. Boost startup and Section 6.3 Buck-boost configuration) the DC-DC converter switches until the voltage at EN pin (V_{EN}) is higher than the voltage at EN_REF pin (V_{EN_REF}) and until the voltage at OUTPUT pin remains below the overvoltage threshold (see Section 6.1 Output voltage control).

In case of low impedance source, the EN_REF is normally connected to GND: the IC switches at the highest duty cycle. In case of high impedance source (by means, with limited current capability, i.e. the source is unable to sustain the continuous switching at the maximum duty cycle), the EN_REF pin can be connected to a proper voltage reference ($V_{IN(MIN)}$) such that the IC stops switching when $V_{EN} > V_{IN(MIN)}$. This voltage reference can be set through a resistor ladder connected to STORE rail or to any other voltage reference available in the application.

6.1 Output voltage control

In order to guarantee the lifetime and safety of the load (e.g. a battery), the IC controls an integrated pass transistor (with $R_{DS(ON)} = R_{BATT}$) between the STORE and OUTPUT pins and implements both the undervoltage and the overvoltage protection thresholds. These thresholds are respectively controlled by the pins UVP and OVP, normally connected to the STORE pin by a resistor partitioning. The respective voltages (V_{UVP} and V_{OVP}) are compared with the IC internal voltage reference ($V_{BG(TYP)}$ = 1.23 V).

Figure 3. Output voltage control section



Before the first startup the pass transistor is open, so that the leakage from the output is lower than 1 nA. The pass transistor is closed once the voltage on the STORE pin rises such that the overvoltage threshold is triggered ($V_{OVP} > V_{BG}$). An internal hysteresis (OVP_{HYS}) sets the restart voltage level for DC-DC converter. The IC also offers the undervoltage protection threshold: the pass transistor is opened once the voltage on the STORE pin decreases down to the undervoltage threshold ($V_{UVP} < V_{BG}$). For some applications (battery charging) it may be necessary to implement a reactivation hysteresis after undervoltage event: it can be easily implemented by a diode (or by a p-channel MOSFET driven by $\overline{OUT\_CONN}$) between STORE and OUTPUT pins. Referring to Figure 3. Output voltage control section, the design rules to set up the R4, R5 and R6 are the following:

Equation 1:

- $V_{BG} = V_{UVP} \times (R5 + R6) / (R4 + R5 + R6)$

Equation 2:

- $V_{BG} = V_{OVP} \times R6 / (R4 + R5 + R6)$

In order to minimize the leakage due to the output resistor partitioning it has to be typically:

Equation 3:

- $10M\Omega \leq R4 + R5 + R6 \leq 20M\Omega$

In addition, the IC provides two open drain digital outputs to an external microcontroller:

- **$\overline{OUT\_CONN}$**

  This pin is pulled down when the pass transistor is closed. It is released once the pass transistor is opened (e.g. triggering of V_{UVP}). If used, this pin must be pulled up to the STORE by a 10 MΩ (typical) resistor.

- **$\overline{DC\text{-}DC\_ON}$**

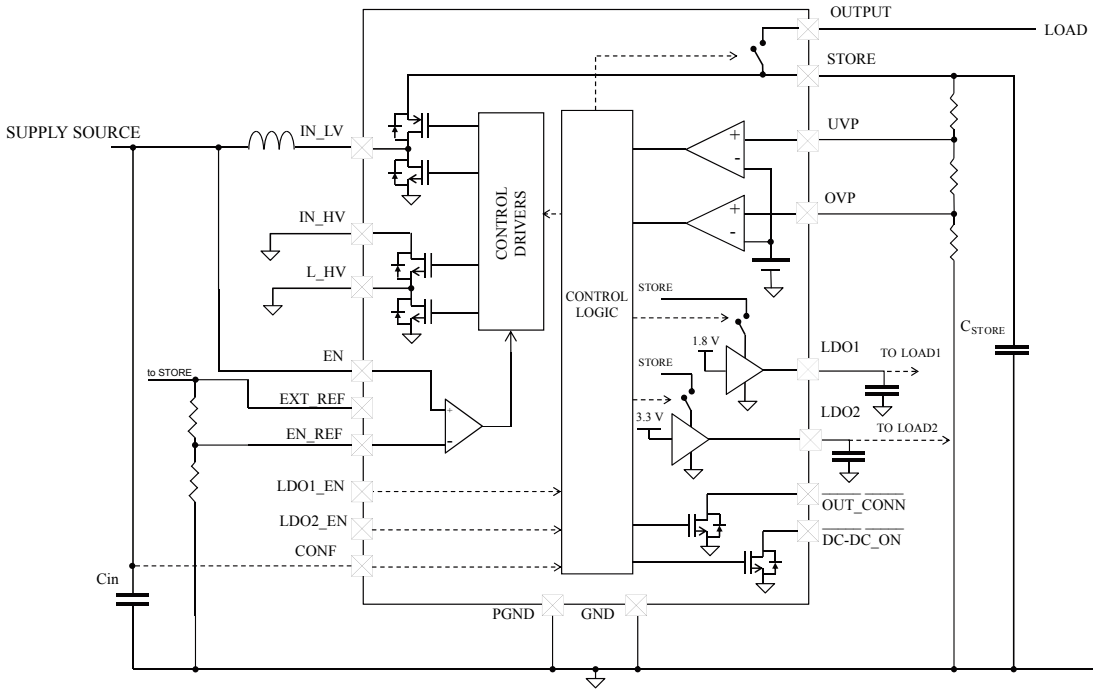
  This pin is pulled down when the DC-DC converter is switching, while it's released when it is not switching, i.e. when the OVP threshold is triggered until the voltage on the STORE pin drops at V_{OVP} - OVP_{HYS} or when the UVLO threshold is triggered. If used, this pin must be pulled up to the STORE by a 10 MΩ (typical) resistor.

Note that the output current causes a voltage drop over the R_{BATT} of the internal pass transistor, consequently, voltages at STORE (where the resistor partitioning to OVP and UVP pins are connected) and OUTPUT may slightly differ. If high precision is required for the output voltage regulation thresholds, then some application workaround may be necessary. For example, two p-channel MOSFETs in back-to-back, both driven by $\overline{OUT\_CONN}$ could be placed between STORE and OUTPUT pins.

6.2 Boost configuration

Figure 4. Boost configuration below shows an example of boost application circuit. In this example, the EN pin is shorted to input supply rail: a resistor partitioning may be required if the voltage range of the supply source goes above the limits of EN pin (see Table 2. Absolute maximum ratings and Table 4. Electrical characteristics).

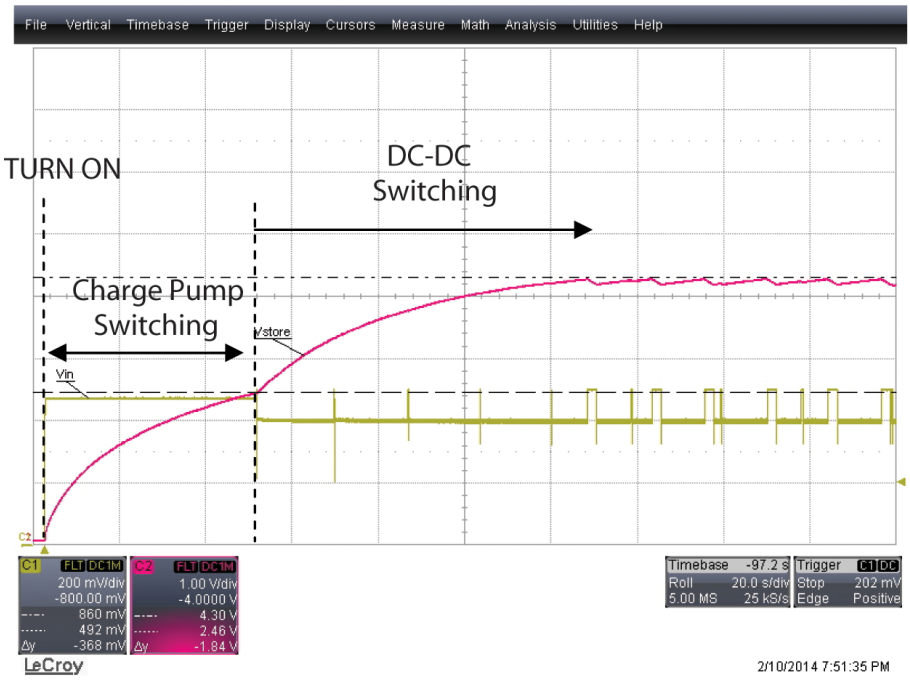
Figure 4. Boost configuration



In case of boost configuration, once the source is connected, the IC starts boosting the voltage on the STORE pin. In the range of $0 \leq V_{STORE} < 2.6$ V the voltage boost is carried on by an integrated high-efficiency charge pump, while the DC-DC converter stage remains OFF.

Figure 5. Boost startup shows the behavior of input voltage V_{IN} and V_{STORE} at the startup.

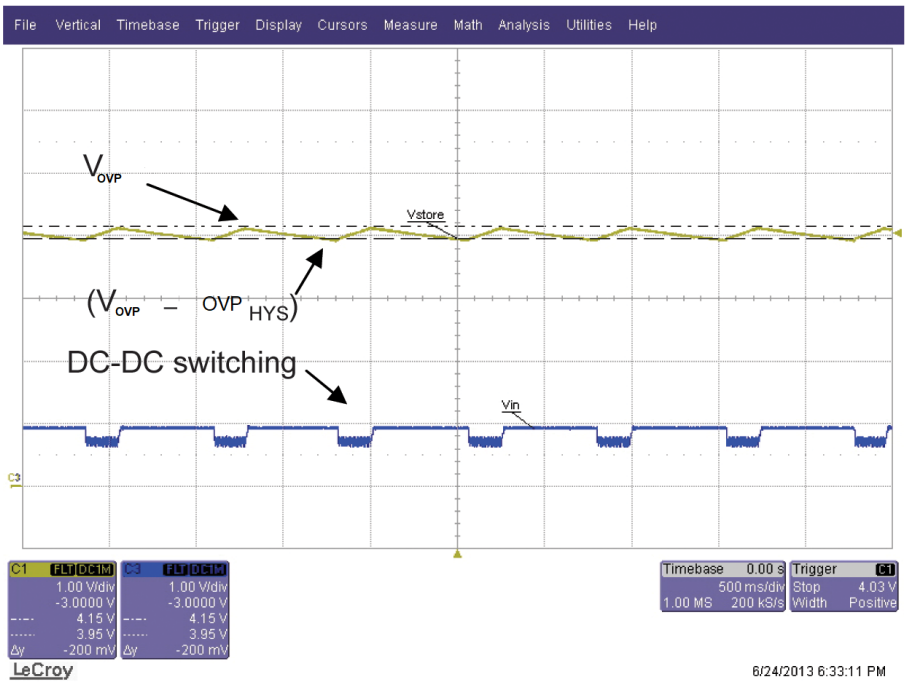
Figure 5. Boost startup



In the range $V_{STORE} \geq 2.6$ V and until $V_{OVP} < V_{BG}$ the V_{STORE}voltage is boosted by the DC-DC converter. In this voltage range DC-DC switches until $V_{EN} > V_{EN\_REF}$.

Once the voltage at STORE pin triggers the overvoltage threshold ($V_{OVP} = V_{BG}$) the switching of the DC-DC converter is stopped until V_{STORE} decrease below the level defined by the internal hysteresis (OVP_{HYS}).

Figure 6. Triggering of V_{OVP} (BATT pin floating)



The following plots (Figure 7. Efficiency vs. input current; V_{IN} = 0.85 V, Figure 8. Efficiency vs. input current; V_{IN} = 1.25 V, Figure 9. Efficiency vs. input current; V_{IN} = 1.65 V, Figure 10. Efficiency vs. input current; V_{IN} = 2.05 V) show the power efficiency of the DC-DC converter configured in boost mode at T_{AMB} = 25 °C in some typical use cases at different input voltages:

Figure 7. Efficiency vs. input current; V_{IN} = 0.85 V

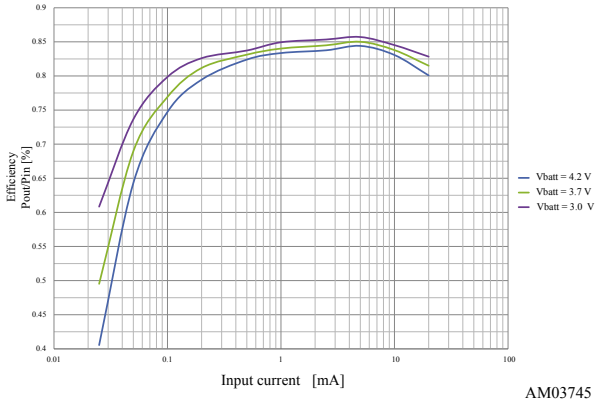


Figure 8. Efficiency vs. input current; V_{IN} = 1.25 V

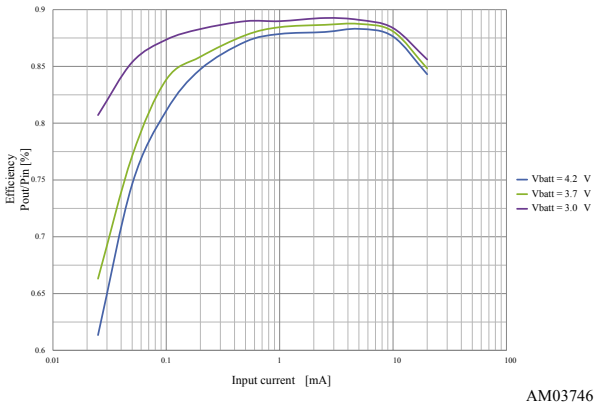


Figure 9. Efficiency vs. input current; V_{IN} = 1.65 V

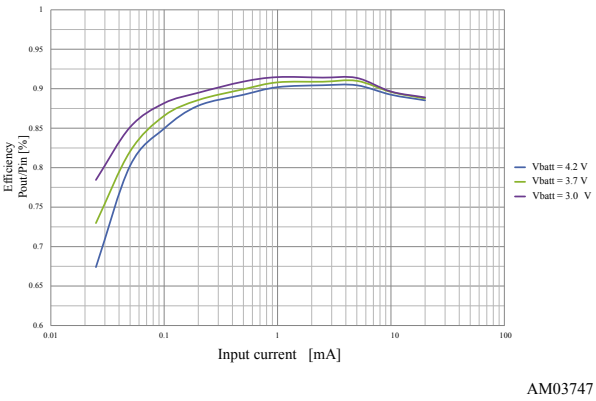
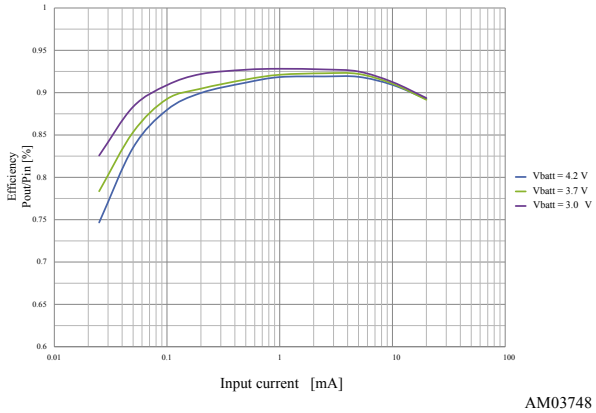


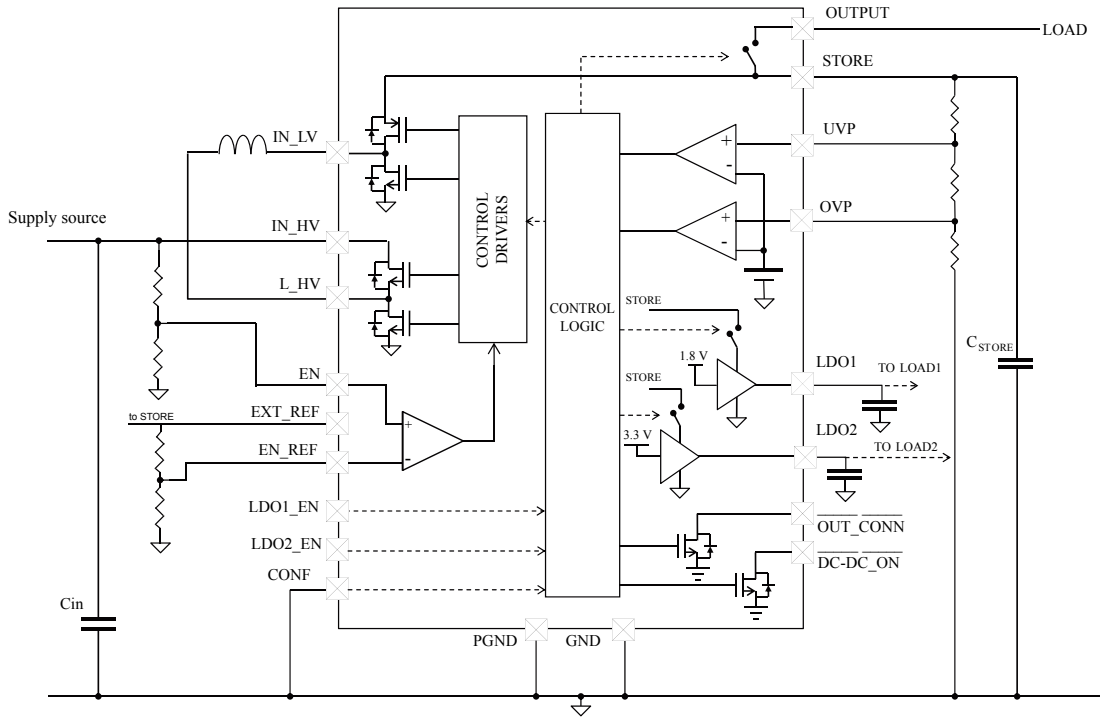
Figure 10. Efficiency vs. input current; V_{IN} = 2.05 V



6.3 Buck-boost configuration

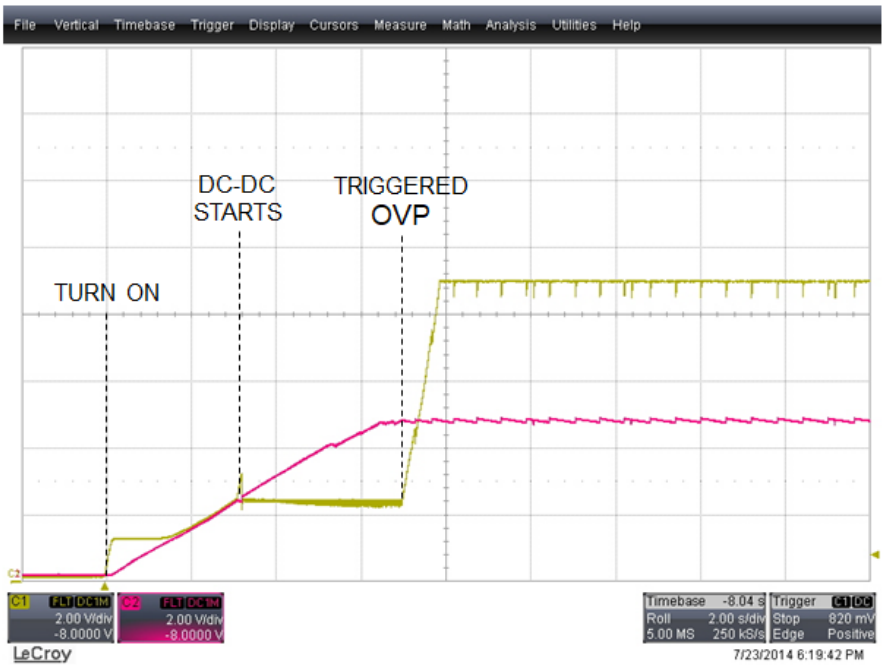
Figure 11. Buck-boost configuration shows an example of buck-boost application circuit.

Figure 11. Buck-boost configuration



In case of buck-boost configuration, once the source is connected, the IN_HV and STORE pins are internally shorted until V_{STORE} < 2.6 V. Figure 12. Buck-boost startup (I_{IN} = 5 µA) shows the behavior of the input voltage V_{IN_HV} and V_{STORE} at the startup.

Figure 12. Buck-boost startup (I_{IN} = 5 µA)



In the range V_{STORE} ≥ 2.6 V and below the overvoltage protection (V_{OVP} < V_{BG}) the integrated DC-DC converter starts switching until V_{EN} > V_{EN_REF}. For the supply sources providing voltages above the allowed range for EN and EN_REF then a resistor partitioning connected between the source and these pins is necessary.

The following plots (Figure 13. Efficiency vs. input current - V_{IN} = 5 V , Figure 14. Efficiency vs. input current - V_{IN} = 7.5 V , Figure 15. Efficiency vs. input current - V_{IN} = 10 V , Figure 16. Efficiency vs. input current - V_{IN} = 12.5 V) show the power efficiency of the DC-DC converter configured in buck-boost mode at T_{AMB} = 25 °C in some typical use cases:

Figure 13. Efficiency vs. input current - V_{IN} = 5 V

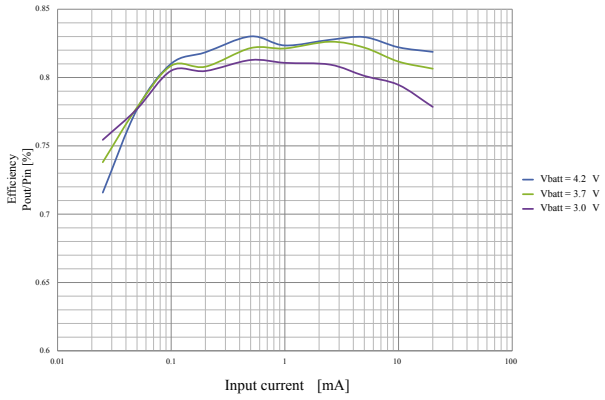


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Figure 14. Efficiency vs. input current - V_{IN} = 7.5 V

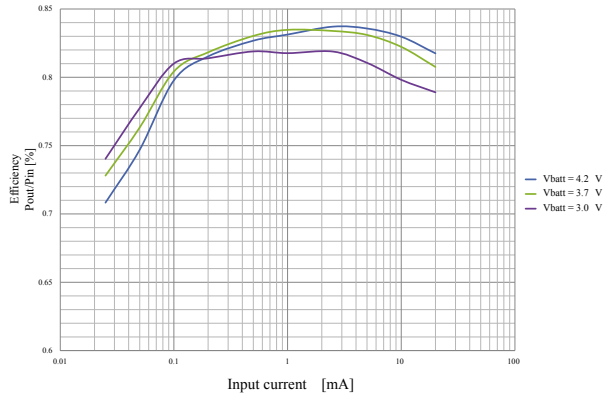

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Figure 15. **Efficiency vs. input current - V_{IN} = 10 V**

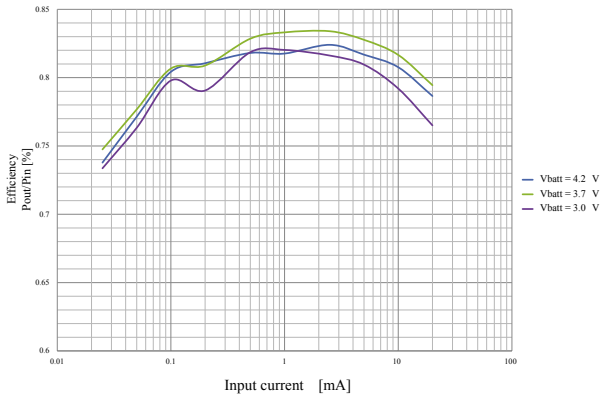

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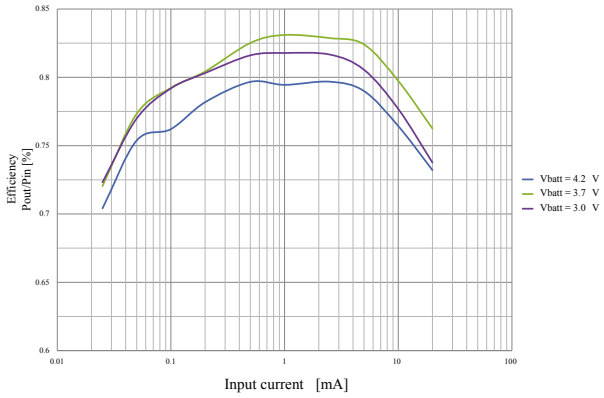
Figure 16. **Efficiency vs. input current - V_{IN} = 12.5 V**



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6.4 Power manager

The IC works as a power manager also by providing one unregulated output voltage on the STORE pin and two regulated voltages on the LDO1 (1.8 V) and LDO2 (3.3 V) pins.

Each LDO can be selectively enabled or disabled by driving the related enable/disable pins LDO1_EN and LDO2_EN. The performances of the LDOs can be optimized by selecting a proper capacitor between the LDO output pin and ground. A 100 nF for each LDO pin is suitable for the most typical use cases. Figure 17. LDO1 turn-on with 100 mA load and Figure 18. LDO2 turn-on with 100 mA load show the behavior of the LDOs when a 100 mA load is connected.

Figure 17. **LDO1 turn-on with 100 mA load**

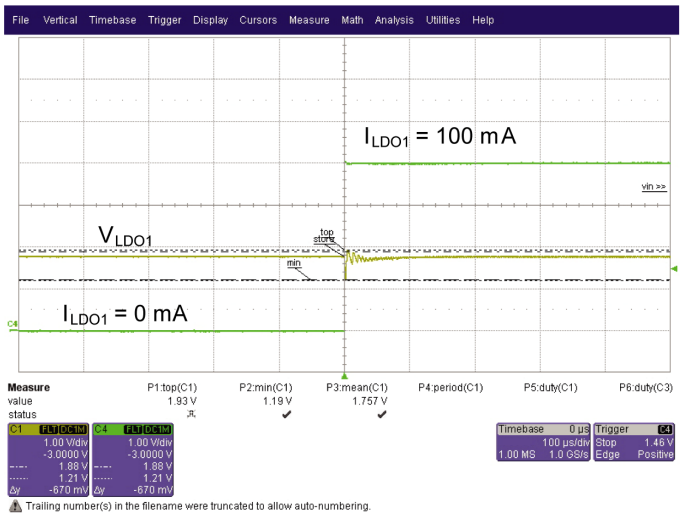
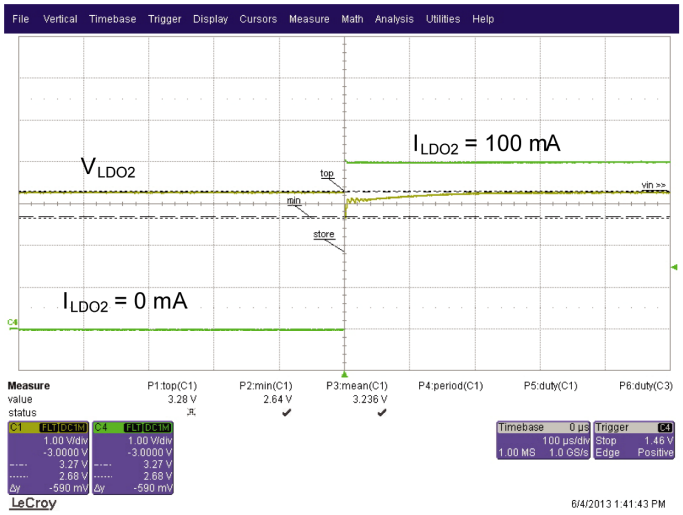


Figure 18. **LDO2 turn-on with 100 mA load**



7 Package and packing information

Figure 19. **VFQFPN20 3 x 3 x 1 mm - 20-lead pitch 0.4 package outline**

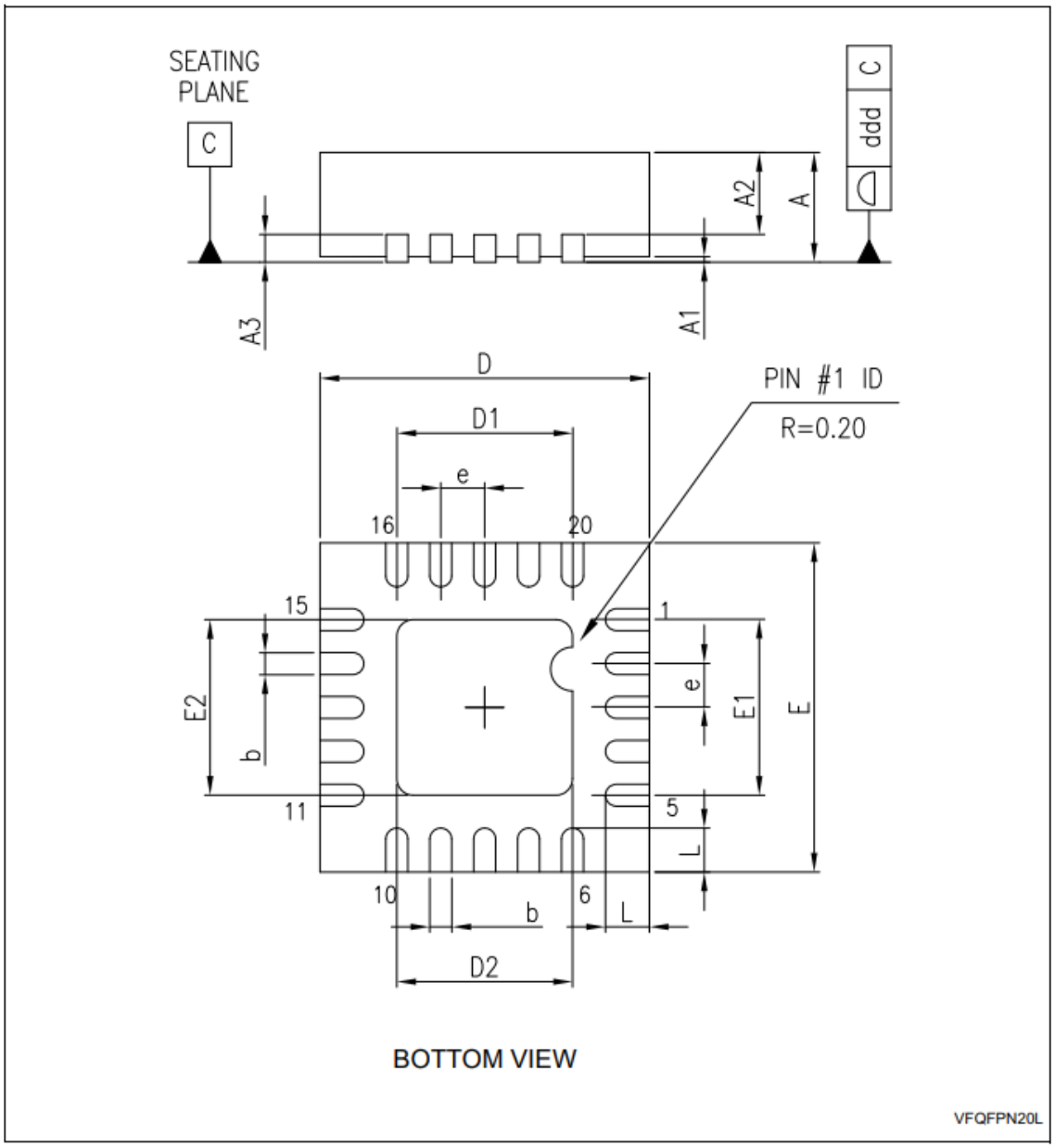


Table 5. **VFQFPN20 3 x 3 x 1 mm - 20-lead pitch 0.4 package mechanical data**

Symbol	Dimensions [mm](1)		
	Min.	Typ.	Max.
A	0.80	0.90	1.0
A1	-	0.02	0.05
A2	-	0.65	1.00

Symbol	Dimensions [mm](1)		
	Min.	Typ.	Max.
A3	-	0.20	-
b	0.15	0.20	0.25
D	2.85	3.00	3.15
D1	-	1.60	-
D2	1.50	1.60	1.70
E	2.85	3.00	3.15
E1	-	1.60	-
E2	1.50	1.60	1.70
e	0.35	0.40	0.45
L	0.30	0.40	0.50
ddd	-	-	0.07

1. *"VFQFPN" stands for "Thermally Enhanced Very thin Fine pitch Quad Packages No lead". Very thin: 0.80 < A ≤ 1.00 mm / fine pitch: e < 1.00 mm.*

Figure 20. Reccomended footprint of VFQFPN20 3 x 3 x 1 mm - 20-lead pitch 0.4

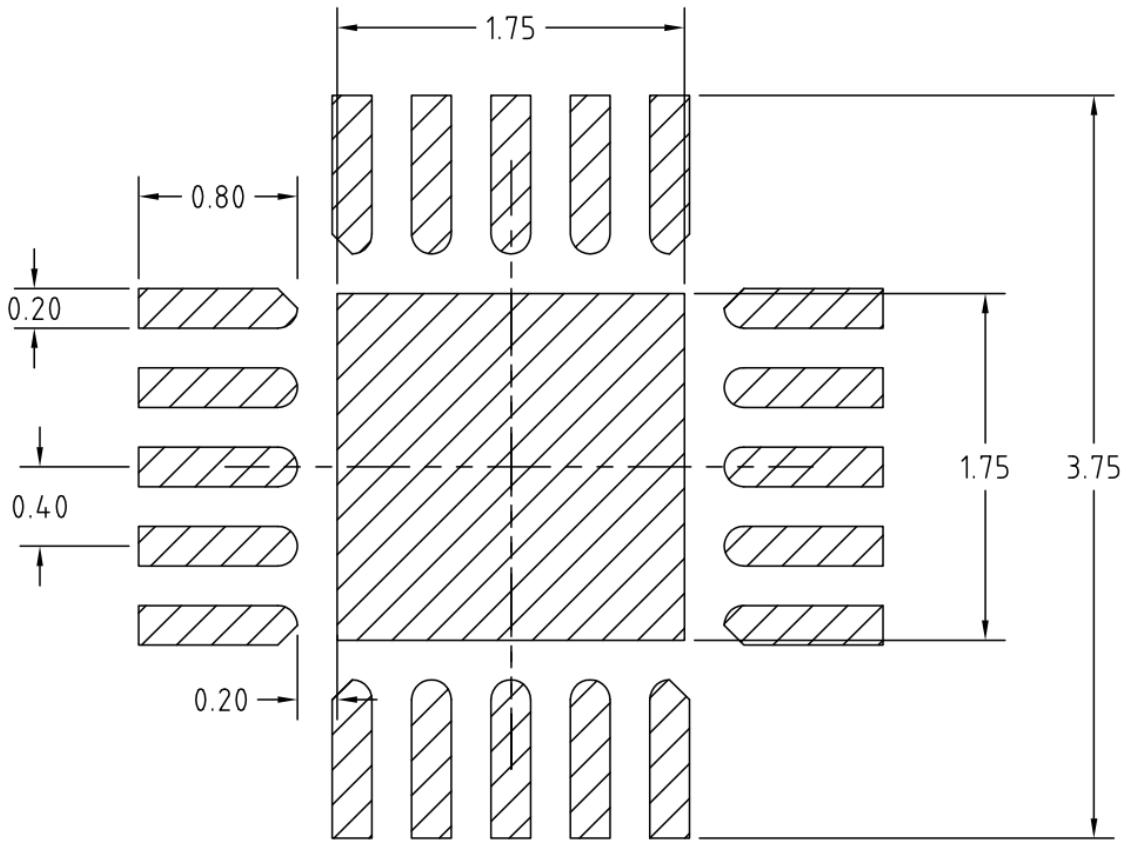
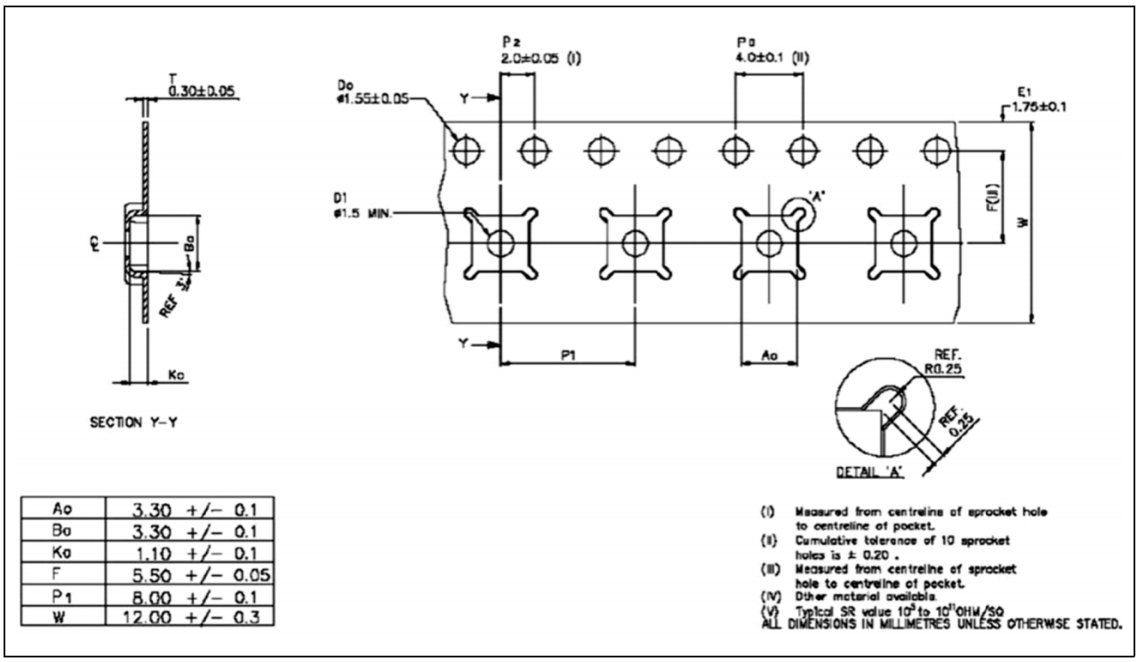


Figure 21. **Tape and reel design**



Ao	3.30 +/- 0.1
Bo	3.30 +/- 0.1
Ko	1.10 +/- 0.1
F	5.50 +/- 0.05
P1	8.00 +/- 0.1
W	12.00 +/- 0.3

8 Ordering information

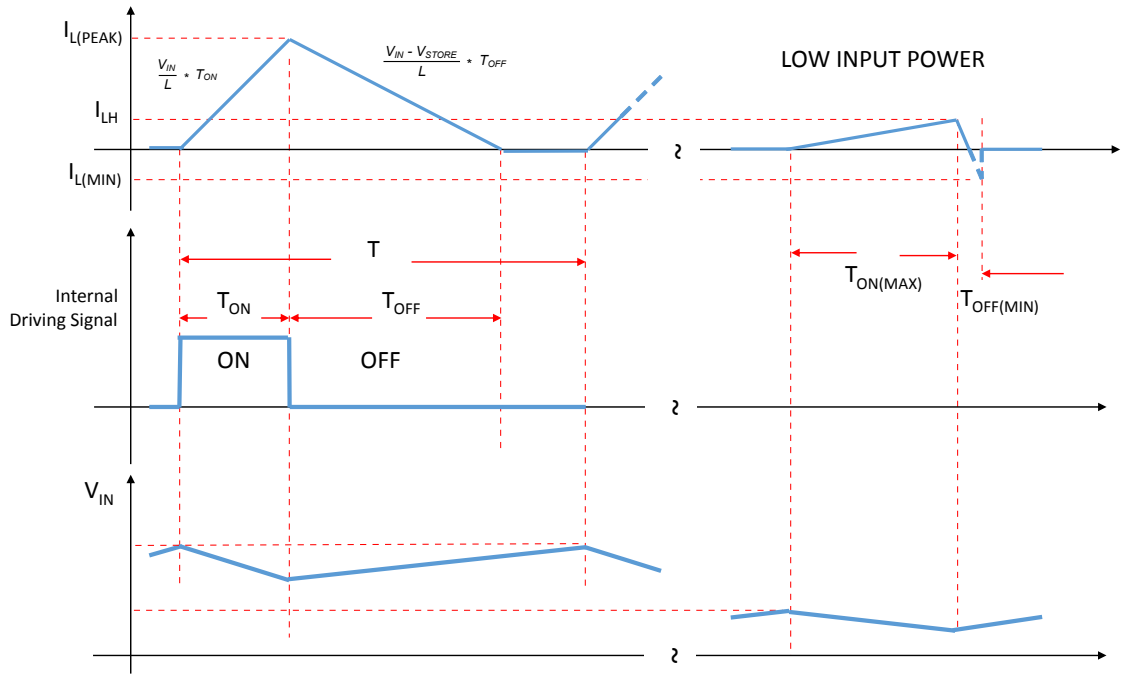
Table 6. **Order code**

Order code	Op. temp. range [°C]	Package	Packing
STBLW35TTR	-40 to 85	VFQFPN 3 x 3 x 1 20L	Tape and reel

Appendix A Application tips

In DC-DC converters the energy is transferred from the input to the output through the inductor. During the ON phase of the duty cycle, the inductor stores energy while during the OFF phase of the duty cycle, the energy is released toward the output stage.

Figure 22. Inductor current and input voltage waveforms



The IC controls the duty cycle of the driving signal by comparing the voltages on the EN and EN_REF pins. When V_{EN} rises higher than V_{EN_REF}, the IC switches ON and the inductor is loaded for T_{ON} until one of the following events occurs:

- V_{STORE} triggers the overvoltage threshold
- The inductor current (I_L) triggers the internal threshold $I_{L(PEAK)}$ (= 140 mA, typ.)
- $T_{ON(MAX)}$ = 10 µs elapses

The energy stored in the inductor is released to the output stage during the OFF phase. During T_{OFF}, I_L decreases to 0 mA (all energy has been released). According to the internal controls of the IC, $T_{OFF(MIN)}$ = 0.2 µs then, in order to prevent I_L becoming negative, the application must be designed such that the energy stored in the inductor during T_{ON} is always greater or equal to the energy released during T_{OFF}. The application has to guarantee $I_{L(MIN)} > 0$:

Equation 10:

- $I_{L(MIN)} = I_H - (V_{STORE} - V_{IN}) \times (T_{OFF(MIN)}/L) > 0$

Equation 11:

- $I_{L(MIN)} = (V_{IN}/L) \times T_{ON(MAX)} - (V_{STORE} - V_{IN}) \times (T_{OFF(MIN)}/L) > 0$

leading

Equation 12:

- $V_{IN} > V_{STORE} \times (T_{OFF(MIN)}/(T_{ON(MAX)} + T_{OFF(MIN)})$

A resistor partitioning can be used between input rail, EN and EN_REF pins purposing the IC switch-off before $I_{L(MIN)} \leq 0$. As worst case for the above equation it can be considered: V_{STORE} at overvoltage level, V_{EN} at the minimum operating voltage ($V_{IN(MIN)}$).

Revision history

Table 7. **Document revision history**

Date	Version	Changes
15-Jul-2021	1	Initial release.

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