

40V 4A DOUBLE POWER HALF BRIDGE

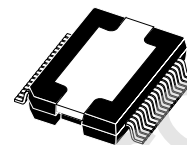
- MINIMUM INPUT OUTPUT PULSE WIDTH DISTORTION
- 200mΩ R_{dsON} COMPLEMENTARY DMOS OUTPUT STAGE
- CMOS COMPATIBLE LOGIC INPUTS
- THERMAL PROTECTION
- THERMAL WARNING OUTPUT
- UNDER VOLTAGE PROTECTION

DESCRIPTION

STA502 is a monolithic dual half bridge stage in Multipower BCD Technology.

The device is particularly designed to make the output stage of a mono All-Digital High Efficiency

MULTIPOWER BCD TECHNOLOGY

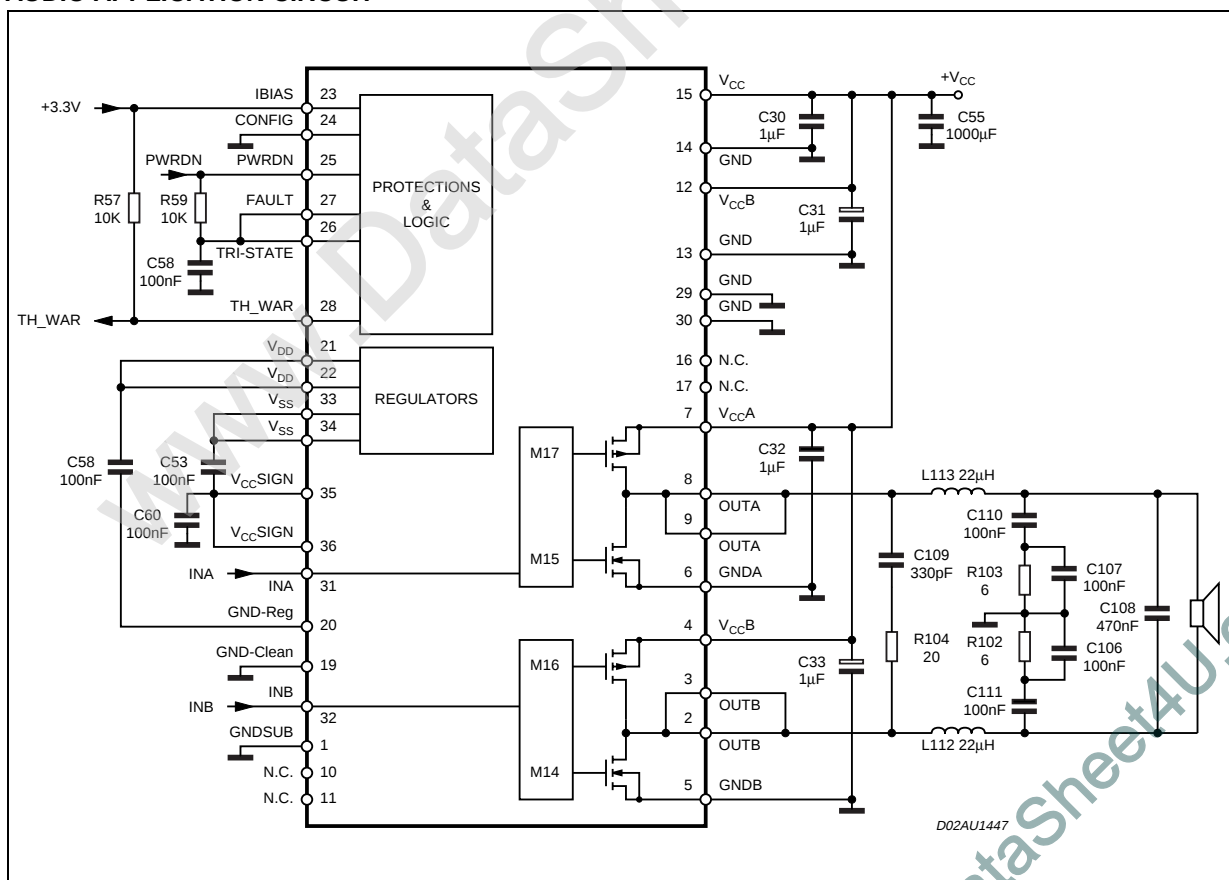


PowerSO36

ORDERING NUMBER: STA502

(DDX™) amplifier capable to deliver 60W @ THD = 10% at V_{CC} 32V output power on 8Ω load. The input pins have threshold proportional to I_{bias} pin voltage.

AUDIO APPLICATION CIRCUIT



PIN FUNCTION

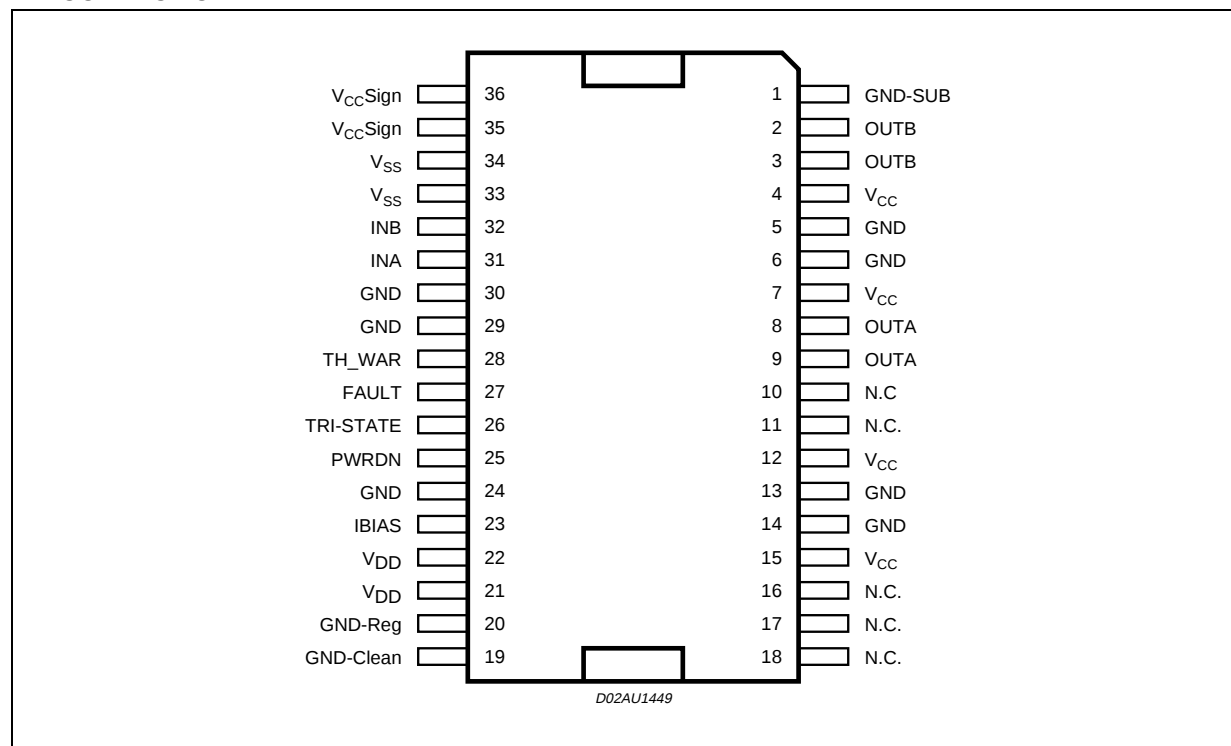
N°	Pin	Description
1	GND-SUB	Substrate ground
35 ; 36	Vcc Sign	Signal Positive supply
15	V _{CC}	Positive Supply
12	V _{CC}	Positive Supply
7	V _{CC}	Positive Supply
4	V _{CC}	Positive Supply
14	GND	Negative Supply
13	GND	Negative Supply
6	GND	Negative Supply
5	GND	Negative Supply
16 ; 17	N.C.	
10 ; 11	N.C.	
8 ; 9	OUTA	Output half bridge
2 ; 3	OUTB	Output half bridge
29	GND	
30	GND	
31	INA	Input of half bridge
32	INB	Input of half bridge
21 ; 22	V _{dd}	5V Regulator referred to ground
33 ; 34	V _{SS}	5V Regulator referred to + V _{CC}
25	PWRDN	Stand-by pin
26	TRI-STATE	Hi-Z pin
27	FAULT	Fault pin advisor
24	GND	
28	TH-WAR	Thermal warning advisor
19	GND-Clean	Logical ground
23	IBIAS	High logical state setting voltage
18	NC	Not connected
20	GND-Reg	Ground for regulator V _{dd}

FUNCTIONAL PIN STATUS

PIN NAME	Logical value	IC -STATUS
FAULT	0	Fault detected (Short circuit, or Thermal ..)
FAULT *	1	Normal Operation
TRI-STATE	0	All powers in Hi-Z state
TRI-STATE	1	Normal operation
PWRDN	0	Low absorption
PWRDN	1	Normal operation
THWAR	0	Temperature of the IC =130°C
THWAR*	1	Normal operation

* : The pin is open collector. To have the high logic value, it needs to be pulled up by a resistor.

PIN CONNECTION



THERMAL DATA

Symbol	Description	Value	Unit
R _{th j-case}	Thermal Resistance Junction-case	max 1.5	°C/W

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CE}	DC Supply Voltage (Pin 4,7,12,15)	40	V
V_{max}	Maximum Voltage on pins 23 to 32	5.5	V
P_{tot}	Power Dissipation ($T_{case} = 70^{\circ}C$)	50	W
T_{op}	Operating Temperature Range	0 to 70	$^{\circ}C$
T_{stg}, T_j	Storage and Junction Temperature	-40 to 150	$^{\circ}C$

THERMAL DATA

Symbol	Parameter	Min.	Typ.	Max.	Unit
T_{j-case}	Thermal Resistance Junction to Case (thermal pad)			2.5	$^{\circ}C/W$
T_{jSD}	Thermal shut-down junction temperature		150		$^{\circ}C$
T_{warn}	Thermal warning temperature		130		$^{\circ}C$
t_{hSD}	Thermal shut-down hysteresis		25		$^{\circ}C$

ELECTRICAL CHARACTERISTICS ($I_{bias} = 3.3V$; $V_{CC} = 30V$; $T_{amb} = 25^{\circ}C$ unless otherwise specified)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
R_{dsON}	Power Pchannel/Nchannel MOSFET R_{dsON}	$I_d=1A$;		200	270	$m\Omega$
I_{dss}	Power Pchannel/Nchannel leakage I_{dss}	$V_{CC}=35V$;			50	μA
g_N	Power Pchannel R_{dsON} Matching	$I_d=1A$;	95			%
g_P	Power Nchannel R_{dsON} Matching	$I_d=1A$;	95			%
Dt_s	Low current Dead Time (static)	see test circuit no.1; see fig. 1		10	20	ns
Dt_d	High current Dead Time (dynamic)	$L=22\mu H$; $C = 470nF$; $R_l = 8 \Omega$ $I_d=3.5A$; see fig. 3			50	ns
$t_{d ON}$	Turn-on delay time	Resistive load			100	ns
$t_{d OFF}$	Turn-off delay time	Resistive load			100	ns
t_r	Rise time	Resistive load; as fig.1			25	ns
t_f	Fall time	Resistive load; as fig. 1			25	ns
V_{CC}	Supply voltage operating voltage		10		36	V
V_{IN-H}	High level input voltage				$I_{bias}/2 + 300mV$	V
V_{IN-L}	Low level input voltage		$I_{bias}/2 - 300mV$			V
I_{IN-H}	Hi level Input current	Pin voltage = I_{bias}		1		μA

ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I _{IN-L}	Low level input current	Pin voltage = 0.3V		1		μA
I _{PWRDN-H}	Hi level PWRDN pin input current	I _{bias} = 3.3V		35		μA
V _L	Low logical state voltage V _L (pin PWRDN, TRISTATE) (note 1)	I _{bias} = 3.3V	0.8			V
V _H	High logical state voltage V _H (pin PWRDN, TRISTATE) (note 1)	I _{bias} = 3.3V			1.7	V
I _{VCC-PWRDN}	Supply current from V _{cc} in Power Down	PWRDN = 0			3	mA
I _{FAULT}	Output Current pins FAULT -TH-WARN when FAULT CONDITIONS	V _{pin} = 3.3V		1		mA
I _{VCC-hiz}	Supply current from V _{cc} in Tri-state	Tri-state=0;		22		mA
I _{VCC}	Supply current from V _{cc} in operation (both channel switching)	Input pulse width = 50% Duty; Switching Frequency = 384KHz; No LC filters;		80		mA
I _{VCC-q}	I _{sc} (short circuit current limit)		4	6	8	A
V _{OUT-SH}	Undervoltage protection threshold			7		V
V _{OV}	Output minimum pulse width	No Load	70		150	ns

Notes: 1. The following table explains the V_L, V_H variation with I_{bias}

I _{bias}	V _{Lmin}	V _{Hmax}	Unit
2.7	0.7	1.5	V
3.3	0.8	1.7	V
5	0.85	1.85	V

LOGIC TRUTH TABLE (see fig. 2)

TRI-STATE	INA	INB	Q1	Q2	Q3	Q4	OUTPUT MODE
0	x	x	OFF	OFF	OFF	OFF	Hi-Z
1	0	0	OFF	OFF	ON	ON	DUMP
1	0	1	OFF	ON	ON	OFF	NEGATIVE
1	1	0	ON	OFF	OFF	ON	POSITIVE
1	1	1	ON	ON	OFF	OFF	Not used

Figure 1. Test Circuit.

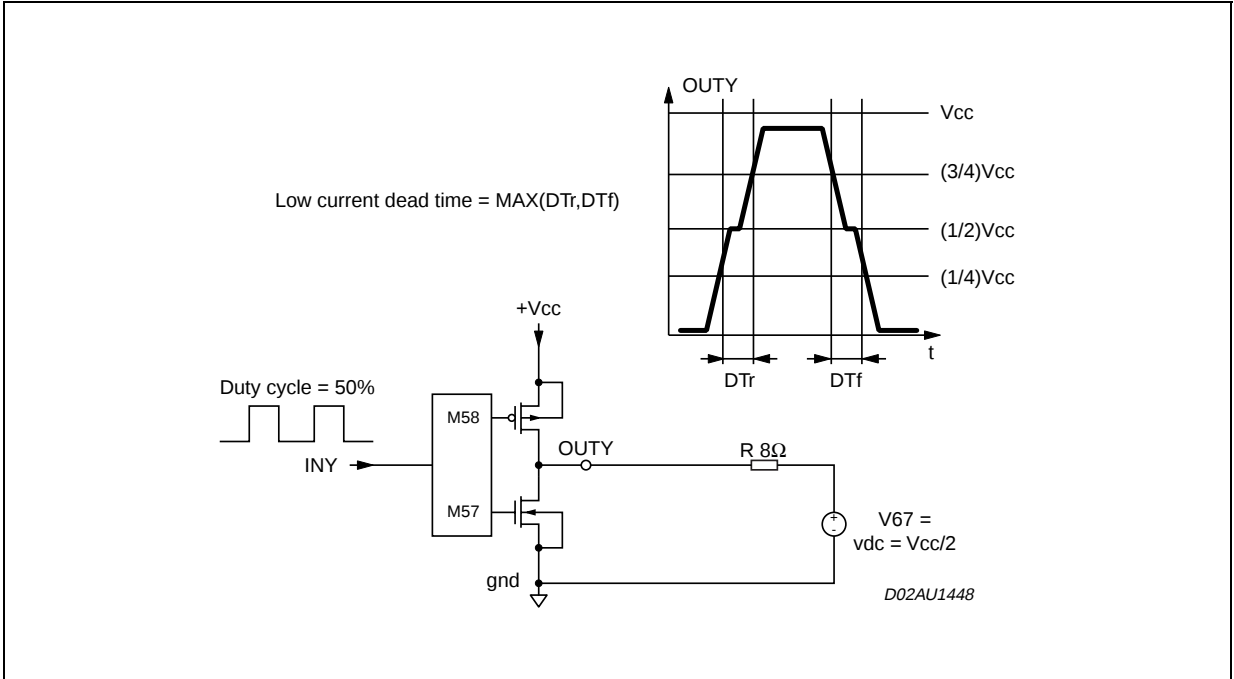


Figure 2.

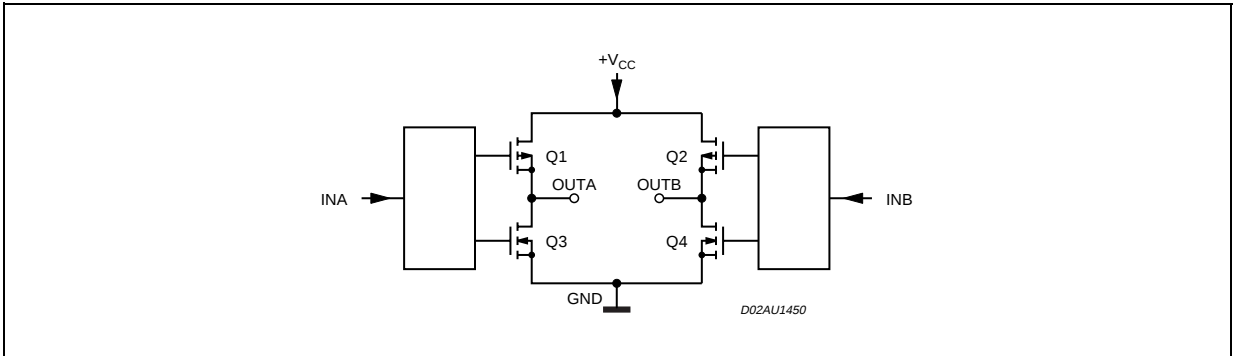
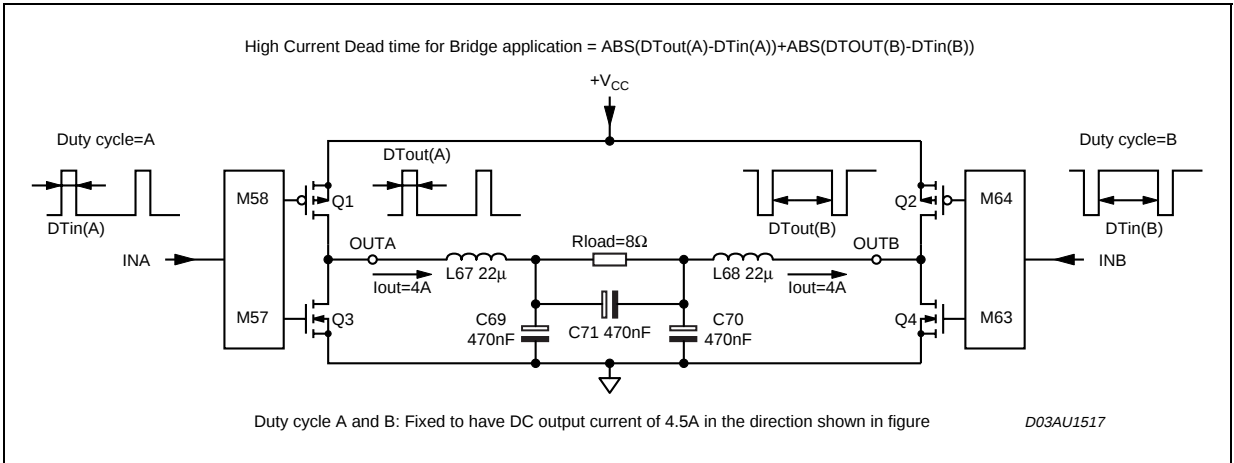


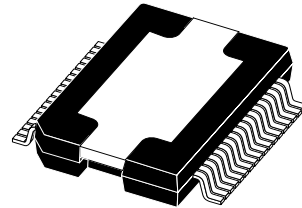
Figure 3.



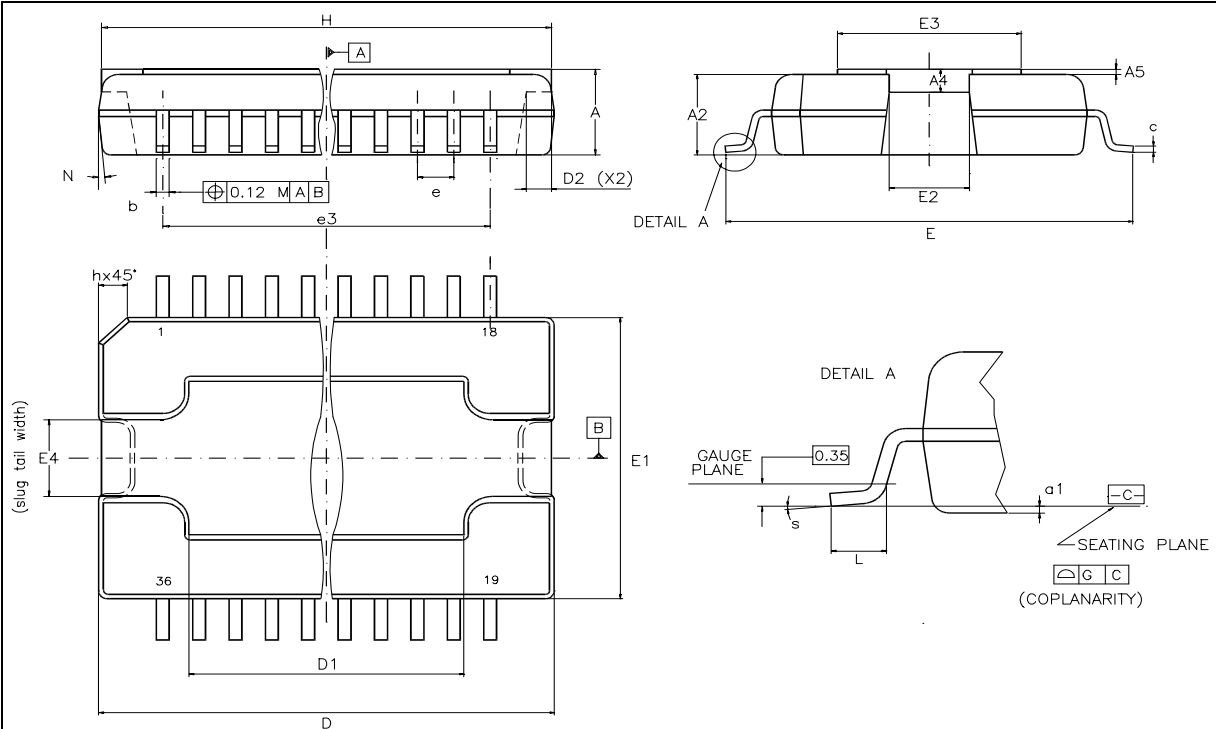
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	3.25		3.5	0.128		0.138
A2			3.3			0.13
A4	0.8		1	0.031		0.039
A5		0.2			0.008	
a1	0		0.075	0		0.003
b	0.22		0.38	0.008		0.015
c	0.23		0.32	0.009		0.012
D	15.8		16	0.622		0.630
D1	9.4		9.8	0.37		0.38
D2		1			0.039	
E	13.9		14.5	0.547		0.57
E1	10.9		11.1	0.429		0.437
E2			2.9			0.114
E3	5.8		6.2	0.228		0.244
E4	2.9		3.2	0.114		1.259
e		0.65			0.026	
e3		11.05			0.435	
G	0		0.075	0		0.003
H	15.5		15.9	0.61		0.625
h			1.1			0.043
L	0.8		1.1	0.031		0.043
N	10° (max)					
s	8° (max)					

- (1) "D and E1" do not include mold flash or protusions.
Mold flash or protusions shall not exceed 0.15mm (0.006")
- (2) No intrusion allowed inwards the leads.

OUTLINE AND MECHANICAL DATA



PowerSO36 (SLUG UP)



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