



ST8024S

COM/SEG LCD Driver

Datasheet

Version 0.39

2008/05/05

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1. FEATURES

- Number of LCD drive outputs: 240
- Supply voltage for LCD drive: +15.0 to +30.0 V
- Supply voltage for the logic system: +2.5 to +5.5 V
- Low power consumption
- Low output impedance

(Segment mode)

- Shift clock frequency
 - 20MHz(MAX.): $V_{DD} = +5.0 \pm 0.5 \text{ V}$
 - 15MHz(MAX.): $V_{DD} = +3.0 \text{ to } +4.5 \text{ V}$
 - 12MHz(MAX.): $V_{DD} = +2.5 \text{ to } +3.0 \text{ V}$
- Adopts a data bus system
- 4-bit/8-bit parallel input modes are selectable with a mode (MD) pin
- Automatic transfer function of an enable signal
- Automatic counting function which, in the chip selection mode, causes the internal clock to be stopped by automatically counting 240 bits of input data
- Line latch circuits are reset when /DISPOFF active

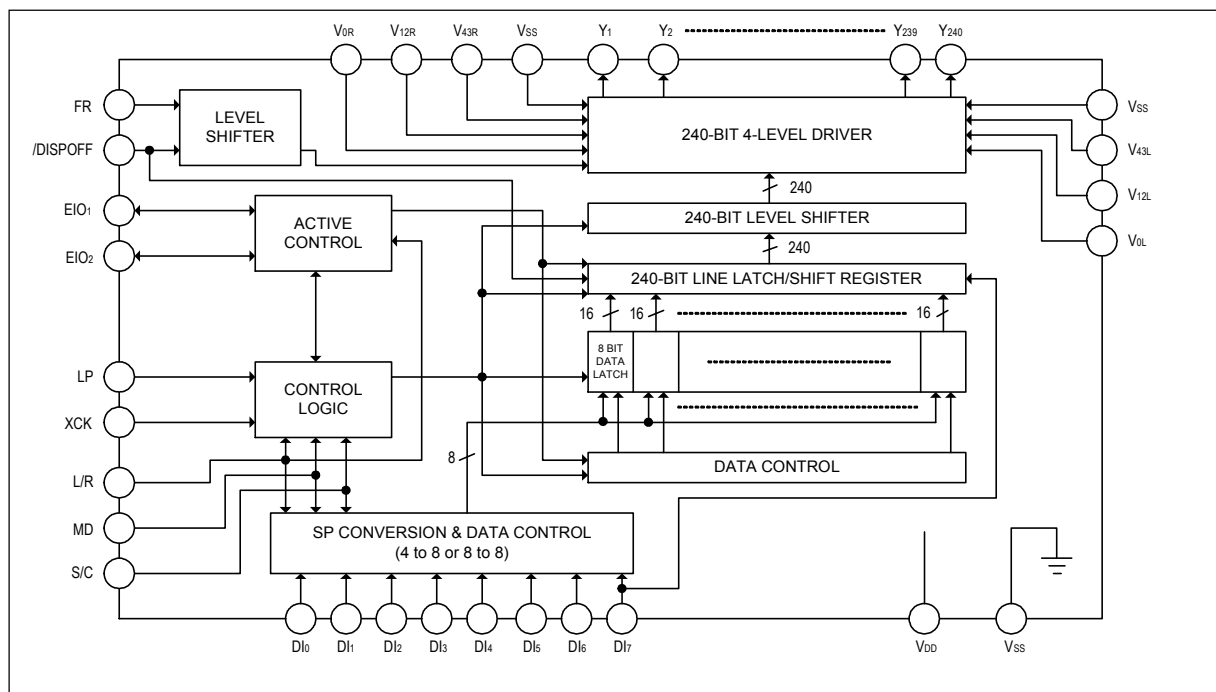
(Common mode)

- Shift clock frequency: 4 MHz (MAX.)
- Built-in 240-bit bi-directional shift register (divisible into 120 bits x 2)
- Available in a single mode (240-bit shift register) or in a dual mode (120-bit shift register x 2)
 - Y1->Y240 Single mode
 - Y240->Y1 Single mode
 - Y1->Y120, Y121->Y240 Dual mode
 - Y240->Y121, Y120->Y1 Dual modeThe above 4 shift directions are in-selectable
- Shift register circuits are reset when /DISPOFF active

2. DESCRIPTION

The ST8024S is a 240-output segment/common driver IC suitable for driving large/medium scale dot matrix LCD panels, and is used in personal computers/work stations. The ST8024S is good both as a segment driver and a common driver, and it can create a low power consuming, high-resolution LCD.

3. BLOCK DIAGRAM



4. FUNCTIONAL OPERATIONS OF EACH BLOCK

BLOCK	FUNCTION
Active Control	In case of segment mode, controls the selection or non-selection of the chip. Following an LP signal input, and after the chip selection signal is input, a selection signal is generated internally until 240 bits of data have been read in. Once data input has been completed, a selection signal for cascade connection is output, and the chip is non-selected. In case of common mode, controls the input/output data of bi-directional pins.
SP Conversion & Data Control	In case of segment mode, keeps input data which are 2 clocks of XCK at 4-bit parallel input mode in latch circuit, or keeps input data which are 1 clock of XCK at 8-bit parallel input mode in latch circuit; after that they are put on the internal data bus 8 bits at a time.
Data Latch Control	In case of segment mode, selects the state of the data latch which reads in the data bus signals. The shift direction is controlled by the control logic. For every 16 bits of data read in, the selection signal shifts one bit based on the state of the control circuit.
Data Latch	In case of segment mode, latches the data on the data bus. The latch state of each LCD drive output pin is controlled by the control logic and the data latch control; 240 bits of data are read in 30 sets of 8 bits.
Line Latch/Shift Register	In case of segment mode, all 240 bits which have been read into the data latch are simultaneously latched at the falling edge of the LP signal, and are output to the level shifter block. In case of common mode, shifts data from the data input pin at the falling edge of the LP signal.
Level Shifter	The logic voltage signal is level-shifted to the LCD drive voltage level, and is output to the driver block.
4-Level Driver	Drives the LCD drive output pins from the line latch/shift register data, and selects one of 4 levels (V0, V12, V43 or Vss) based on the S/C, FR and /DISPOFF signals.
Control Logic	Controls the operation of each block. In case of segment mode, when an LP signal has been input, all blocks are reset and the control logic waits for the selection signal output from the active control block. Once the selection signal has been output, operation of the data latch and data transmission is controlled, 240 bits of data are read in, and the chip is non-selected. In case of common mode, controls the direction of data shift.

5. INPUT/OUTPUT CIRCUITS

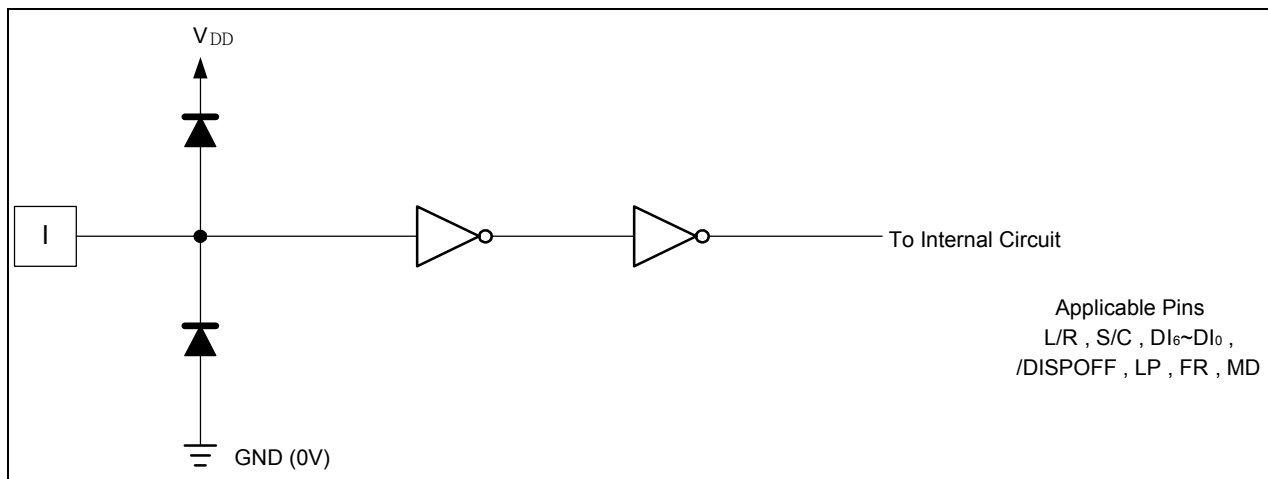


Figure 1 Input Circuit (1)

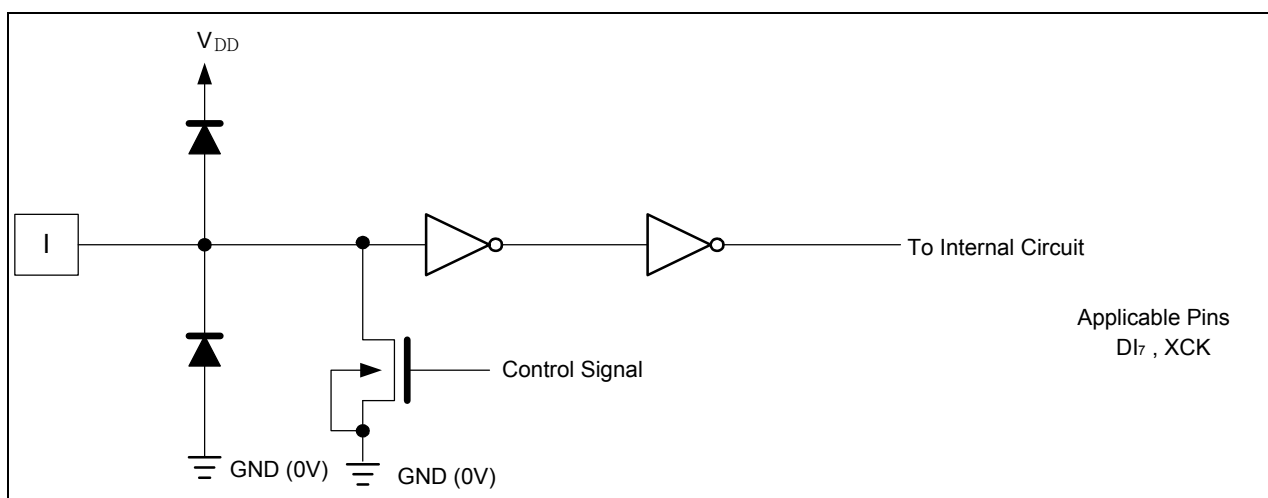


Figure 2 Input Circuit (2)

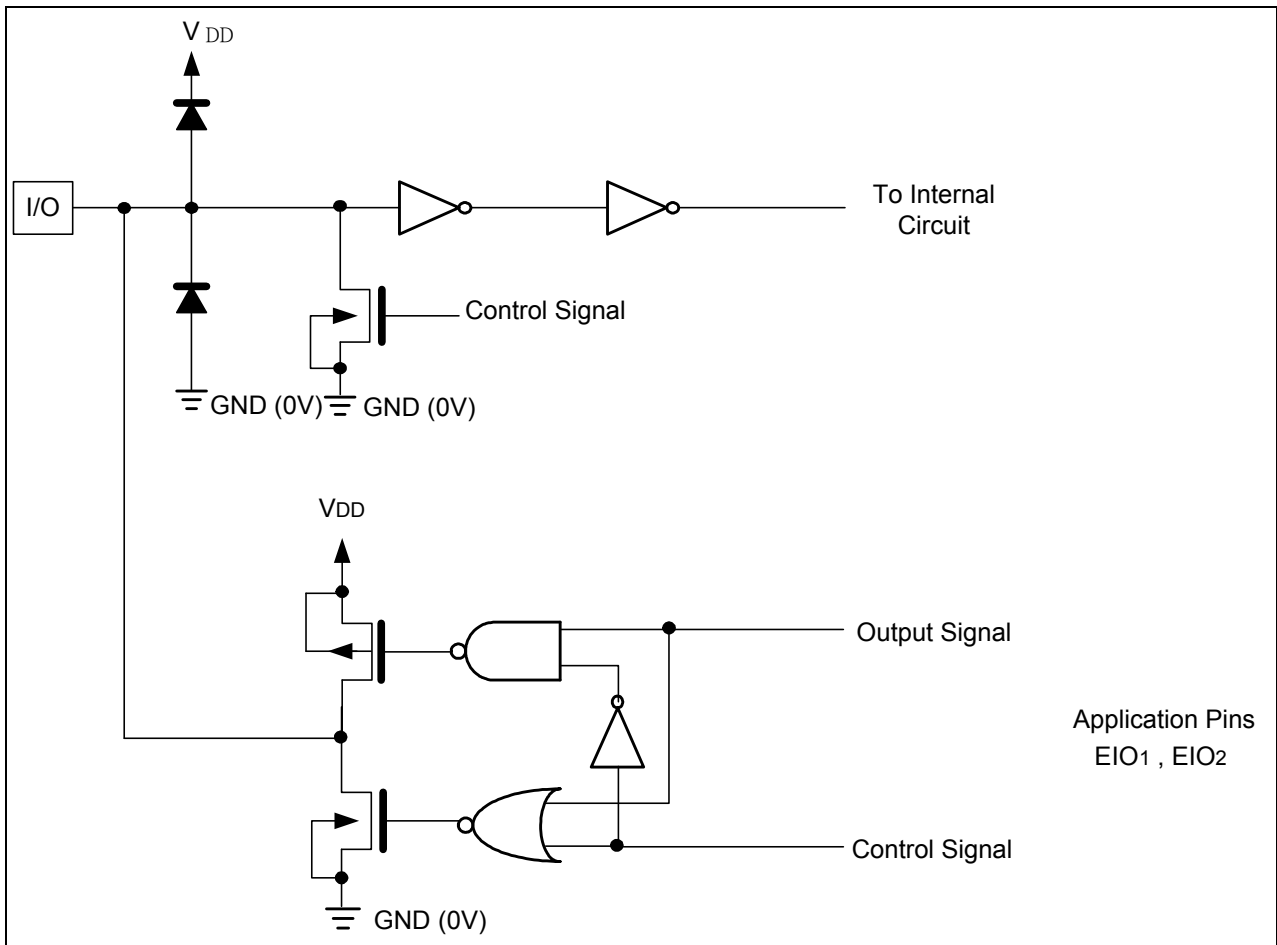


Figure 3 Input/Output Circuit

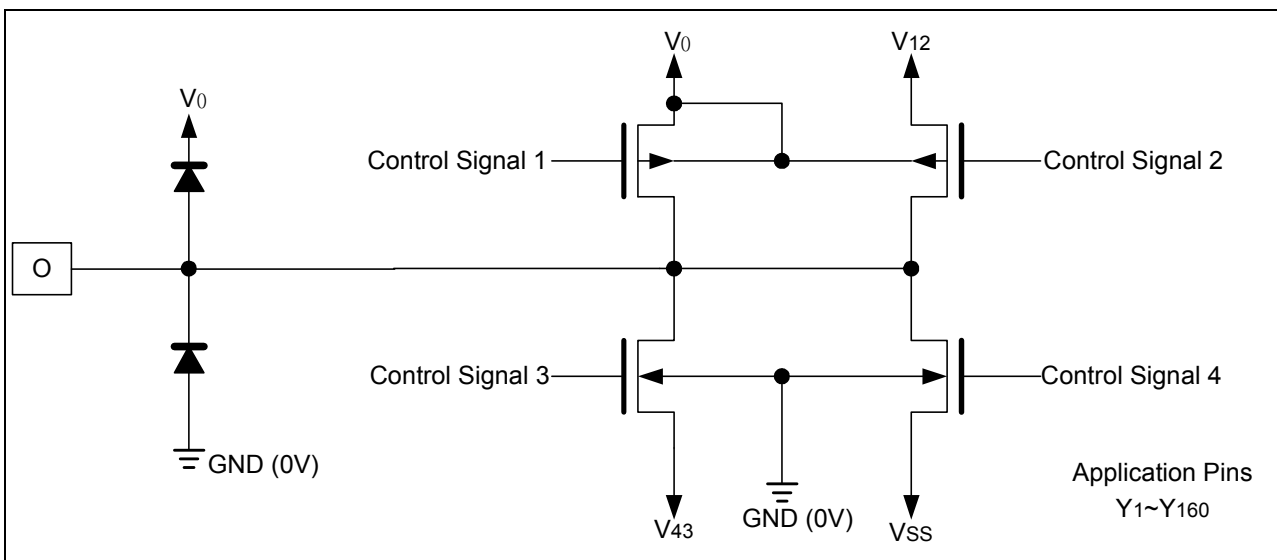


Figure 4 LCD Drive Output Circuit

6. FUNCTIONAL DESCRIPTION

6.1 Pin Functions

(Segment mode)

SYMBOL	FUNCTION
V _{DD}	Logic system power supply pin, • Connected to +2.5 to +5.5 V.
GND	Ground pin
LGND	Logic ground pin • Do not short LGND with GND and V _{SS} by ITO on LCD panel • Connect it to GND on PCB or FPC.
V _{SS}	Connect to GND by ITO on LCD panel.
V _{0L} , V _{0R} V _{12L} , V _{12R} V _{43L} , V _{43R}	Bias power supply pins for LCD drive voltage • Normally use the bias voltages set by a resistor divider • Ensure that voltages are set such that V _{SS} < V ₄₃ < V ₁₂ < V ₀ . • V _{iL} and V _{iR} (i = 0, 12, 43) must connect to an external power supply, and supply regular voltage which is assigned by specification for each power pin
DI7-DI0	Input pins for display data • In 4-bit parallel mode, DI3-DI0 are the display data input pins, and DI7-DI4 must be connected to LGND or V _{DD} . • In 8-bit parallel mode, All DI7-DI0 pins are the display data input pins. • Refer to section 6.2.2.
XCK	Clock input pin for taking display data • Data is read at the falling edge of the clock pulse.
LP	Latch pulse input pin for display data • Data is latched at the falling edge of the clock pulse.
L/R	Input pin for selecting the reading direction of display data • When set to LGND level "L", data is read sequentially from Y ₂₄₀ to Y ₁ . • When set to V _{DD} level "H", data is read sequentially from Y ₁ to Y ₂₄₀ . Refer to section 6.2.2.
/DISPOFF	Control input pin for output of non-select level • The input signal is level-shifted from logic voltage level to LCD drive voltage level, and controls the LCD drive circuit. • When set to LGND level "L", the LCD drive output pins (Y ₁ -Y ₂₄₀) are set to level V _{SS} . • When set to "L", the contents of the line latch are reset, but the display data are read in the data latch regardless of the condition of /DISPOFF. When the /DISPOFF function is canceled, the driver outputs non-select level (V ₁₂ or V ₄₃), then outputs the contents of the data latch at the next falling edge of the LP. At that time, if /DISPOFF removal time does not correspond to what is shown in AC characteristics, it can not output the reading data correctly. • Table of truth values is shown in "TRUTH TABLE" in Functional Operations.
FR	AC signal input pin for LCD drive waveform • The input signal is level-shifted from logic voltage level to LCD drive voltage level, and controls the LCD drive circuit. • Normally it inputs a frame inversion signal. • The LCD drive output pins' output voltage levels can be set using the line latch output signal and the FR signal. • Table of truth values is shown in "TRUTH TABLE" in Functional Operations.
MD	Mode selection pin • When set to LGND level "L", 8-bit parallel input mode is set. • When set to V _{DD} level "H", 4-bit parallel input mode is set. • Refer to section 6.2.2.
S/C	Segment mode/common mode selection pin • When set to V _{DD} level "H", segment mode is set.
EIO ₁ , EIO ₂	Input/output pins for chip selection • When L/R input is at LGND level "L", EIO ₁ is set for output, and EIO ₂ is set for input. • When L/R input is at V _{DD} level "H", EIO ₁ is set for input, and EIO ₂ is set for output. • During output, set to "H" while LP • XCK is "H" and after 240 bits of data have been

	read, set to "L" for one cycle (from falling edge to failing edge of XCK), after which it returns to "H". During input, the chip is selected while EI is set to "L" after the LP signal is input. The chip is non-selected after 240 bits of data have been read.
Y ₁ -Y ₂₄₀	LCD drive output pins - Corresponding directly to each bit of the data latch, one level (V₀, V₁₂, V₄₃, or V_{SS}) is selected and output. - Table of truth values is shown in "TRUTH TABLE" in Functional Operations.

(Common mode)

SYMBOL	FUNCTION
V _{DD}	Logic system power supply pin, connected to +2.5 to +5.5 V.
GND	Ground pin
LGND	Logic ground pin - Do not short LGND with GND and V_{SS} by ITO on LCD panel - Connect it to GND on PCB or FPC.
V _{SS}	Connect to GND by ITO on LCD panel.
V _{0L} , V _{0R} V _{12L} , V _{12R} V _{43L} , V _{43R}	Bias power supply pins for LCD drive voltage - Normally use the bias voltages set by a resistor divider. - Ensure that voltages are set such that V_{SS} < V₄₃ < V₁₂ < V₀. - V_{iL} and V_{iR} (i = 0, 12, 43) must connect to an external power supply, and supply regular voltage which is assigned by specification for each power pin.
EIO ₁	Shift data input/output pin for bi-directional shift register - Output pin when L/R is at LGND level "L", input pin when L/R is at V_{DD} level "H". - When L/R = H, EIO₁ is used as input pin, it will be pulled down. - When L/R = L, EIO₁ is used as output pin, it won't be pulled down. - Refer to section 6.2.2.
EIO ₂	Shift data input/output pin for bi-directional shift register - Input pin when L/R is at LGND level "L", output pin when L/R is at V_{DD} level "H". - When L/R = L, EIO₂ is used as input pin, it will be pulled down. - When L/R = H, EIO₂ is used as output pin, it won't be pulled down. - Refer to section 6.2.2.
LP	Shift clock pulse input pin for bi-directional shift register Data is shifted at the falling edge of the clock pulse.
L/R	Input pin for selecting the shift direction of bi-directional shift register - Data is shifted from Y₂₄₀ to Y₁ when set to LGND level "L", and data is shifted from Y₁ to Y₂₄₀ when set to V_{DD} level "H". - Refer to section 6.2.2.
/DISPOFF	Control input pin for output of non-select level - The input signal is level-shifted from logic voltage level to LCD drive voltage level, and controls the LCD drive circuit. - When set to LGND level "L", the LCD drive output pins (Y₁-Y₂₄₀) are set to level LGND. - When set to "L", the contents of the shift register are reset to not reading data. When the /DISPOFF function is canceled, the driver outputs non-select level (V₁₂ or V₄₃), and the shift data is read at the next falling edge of the LP. At that time, if /DISPOFF removal time does not correspond to what is shown in AC characteristics, the shift data is not read correctly. - Table of truth values is shown in "TRUTH TABLE" in Functional Operations.
FR	AC signal input pin for LCD drive waveform - The input signal is level-shifted from logic voltage level to LCD drive voltage level, and controls the LCD drive circuit. - Normally it inputs a frame inversion signal. - The LCD drive output pins' output voltage levels can be set using the shift register output signal and the FR signal. - Table of truth values is shown in "TRUTH TABLE" in Functional Operations.
MD	Mode selection pin When set to LGND level "L", single mode operation is selected; when set to V_{DD} level

	"H" dual mode operation is selected. • Refer to section 6.2.2.
DI ₇	Dual mode data input pin • According to the data shift direction of the data shift register, data can be input starting from the 121st bit. When the chip is used in dual mode, DI ₇ will be pulled down. When the chip is used in single mode, DI ₇ won't be pulled down. • Refer to section 6.2.2.
S/C	Segment mode/common mode selection pin • When set to LGND level "L", common mode is set.
DI ₆ -DI ₀	Not used • Connect DI ₆ -DI ₀ to LGND or V _{DD} , avoiding floating.
XCK	Not used • XCK is pulled down in common mode, so connect to LGND or open.
Y ₁ -Y ₂₄₀	LCD drive output pins • Corresponding directly to each bit of the shift register, one level (V ₀ , V ₁₂ , V ₄₃ , or V _{SS}) is selected and output. • Table of truth values is shown in "TRUTH TABLE" in Functional Operations.

6.2 Functional Operations

6.2.1 Truth table

(Segment Mode)

FR	LATCH DATA	/DISPOFF	LCD DRIVE OUTPUT VOLTAGE LEVEL (Y1-Y240)
L	L	H	V ₄₃
L	H	H	V _{SS}
H	L	H	V ₁₂
H	H	H	V ₀
X	X	L	V _{SS}

(Common Mode)

FR	LATCH DATA	/DISPOFF	LCD DRIVE OUTPUT VOLTAGE LEVEL (Y1-Y240)
L	L	H	V ₄₃
L	H	H	V ₀
H	L	H	V ₁₂
H	H	H	V _{SS}
X	X	L	V _{SS}

NOTES:

1. $V_{SS} < V_{43} < V_{12} < V_0$
2. L: LGND (0 V), H: V_{DD} (+2.5 to +5.5 V), X: Don't care
3. "Don't care" should be fixed to "H" or "L", avoiding floating.
There are two kinds of power supply (logic level voltage and LCD drive voltage) for the LCD driver.
Supply regular voltage which is assigned by specification for each power pin.

6.2.2 Relationship between the display data and LCD drive output Pins

(Segment Mode)

(a) 4-bit Parallel Input Mode

MD	L/R	EIO ₁	EIO ₂	DATA INPUT	NUMBER OF CLOCKS						
					60 CLOCK	59 CLOCK	58 CLOCK	...	3 CLOCK	2 CLOCK	1 CLOCK
H	L	Output	Input	DI0	Y1	Y5	Y9	...	Y229	Y233	Y237
				DI1	Y2	Y6	Y10	...	Y230	Y234	Y238
				DI2	Y3	Y7	Y11	...	Y231	Y235	Y239
				DI3	Y4	Y8	Y12	...	Y232	Y236	Y240
H	H	Input	Output	DI0	Y240	Y236	Y232	...	Y12	Y8	Y4
				DI1	Y239	Y235	Y231	...	Y11	Y7	Y3
				DI2	Y238	Y234	Y230	...	Y10	Y6	Y2
				DI3	Y237	Y233	Y229	...	Y9	Y5	Y1

(b) 8-bit Parallel Input Mode

MD	L/R	EIO ₁	EIO ₂	DATA INPUT	NUMBER OF CLOCKS						
					30 CLOCK	29 CLOCK	28 CLOCK	...	3 CLOCK	2 CLOCK	1 CLOCK
L	L	Output	Input	DI0	Y1	Y9	Y17	...	Y217	Y225	Y233
				DI1	Y2	Y10	Y18	...	Y218	Y226	Y234
				DI2	Y3	Y11	Y19	...	Y219	Y227	Y235
				DI3	Y4	Y12	Y20	...	Y220	Y228	Y236
				DI4	Y5	Y13	Y21	...	Y221	Y229	Y237
				DI5	Y6	Y14	Y22	...	Y222	Y230	Y238
				DI6	Y7	Y15	Y23	...	Y223	Y231	Y239
				DI7	Y8	Y16	Y24	...	Y224	Y232	Y240
L	H	Input	Output	DI0	Y240	Y232	Y224	...	Y24	Y16	Y8
				DI1	Y239	Y231	Y223	...	Y23	Y15	Y7
				DI2	Y238	Y230	Y222	...	Y22	Y14	Y6
				DI3	Y237	Y229	Y221	...	Y21	Y13	Y5
				DI4	Y236	Y228	Y220	...	Y20	Y12	Y4
				DI5	Y235	Y227	Y219	...	Y19	Y11	Y3
				DI6	Y234	Y226	Y218	...	Y18	Y10	Y2
				DI7	Y233	Y225	Y217	...	Y17	Y9	Y1

(Common Mode)

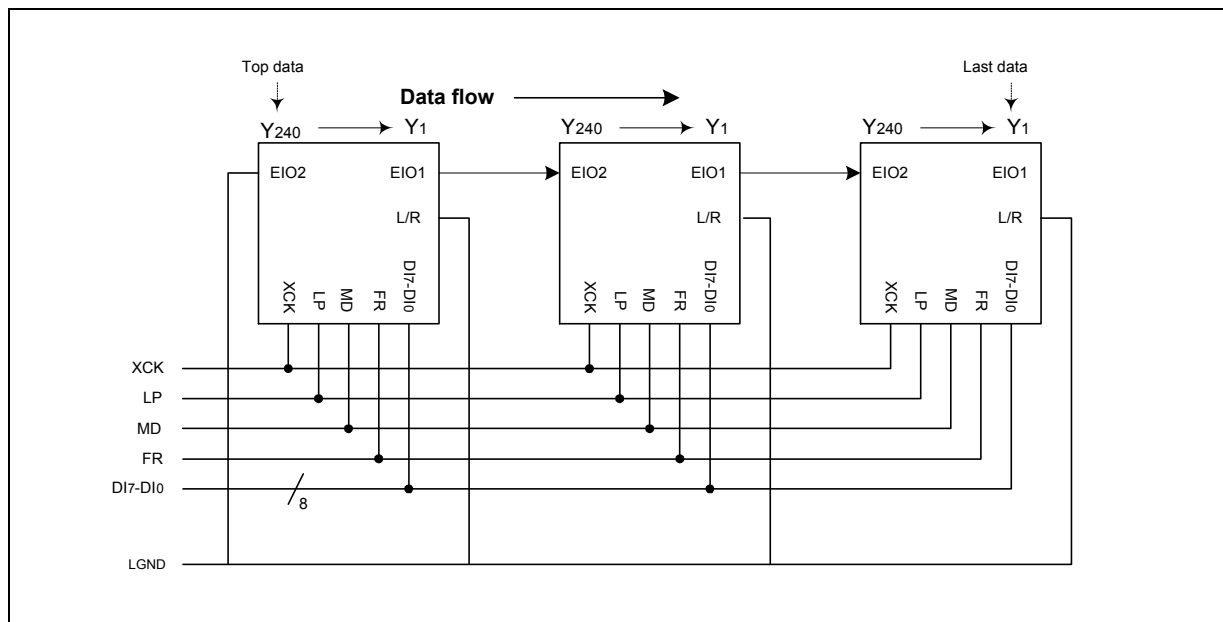
MD	L/R	DATA TRANSFER DIRECTION	EIO ₁	EIO ₂	DI ₇
L (Single)	L	Y240 → Y1	Output	Input	X
	H	Y1 → Y240	Input	Output	X
H (Dual)	L	Y240 → Y121 Y120 → Y1	Output	Input	Input
	H	Y1 → Y120 Y121 → Y240	Input	Output	Input

NOTES:

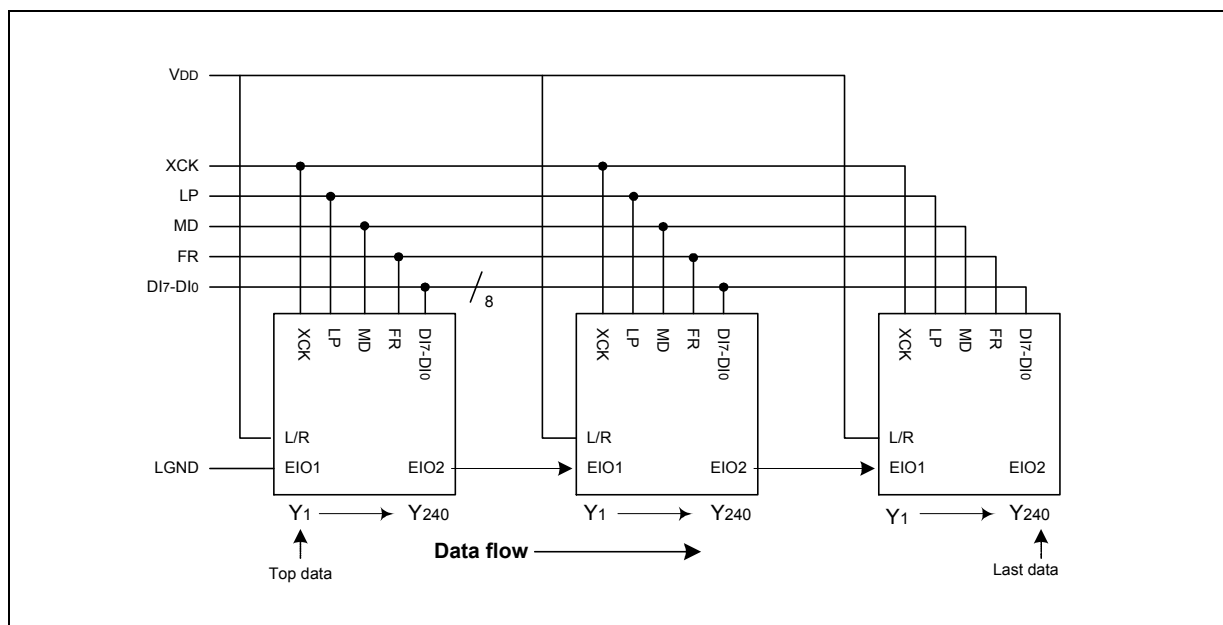
1. L: LGND (0 V), H: V_{DD} (+2.5 to +5.5 V), X: Don't care
2. "Don't care" should be fixed to "H" or "L", avoiding floating.

6.2.3 Connection examples of plural segment drivers

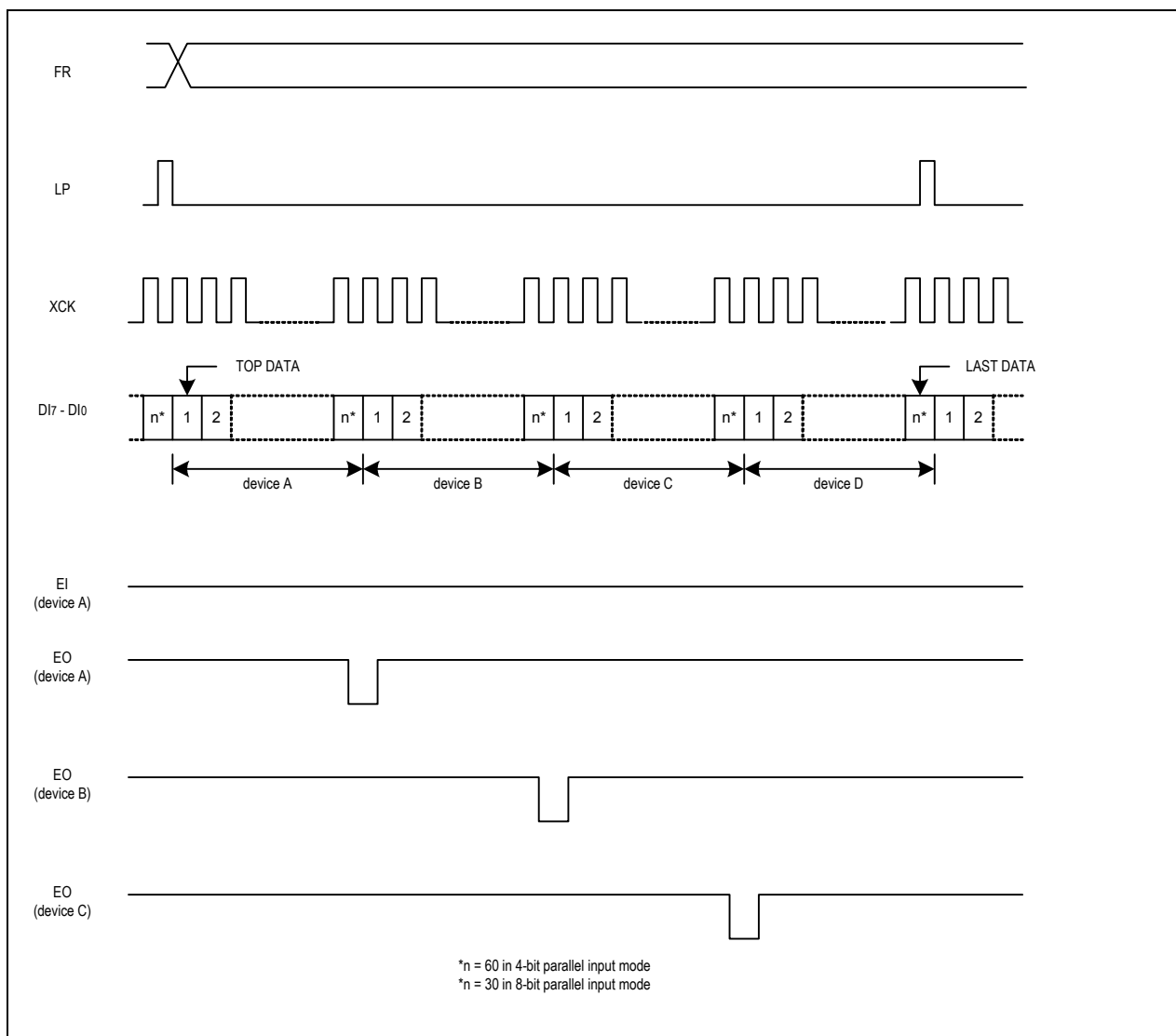
(a) When L/R = "L"



(b) When L/R = "H"

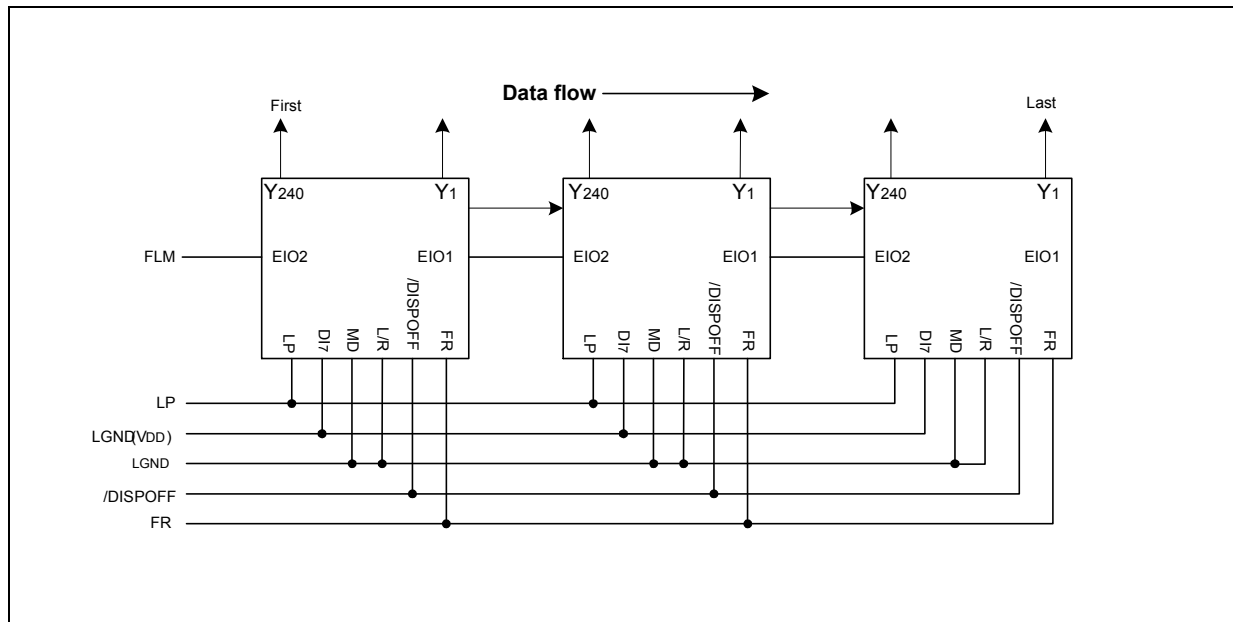


6.2.4 Timing chart of 4-device cascade connection of segment drivers

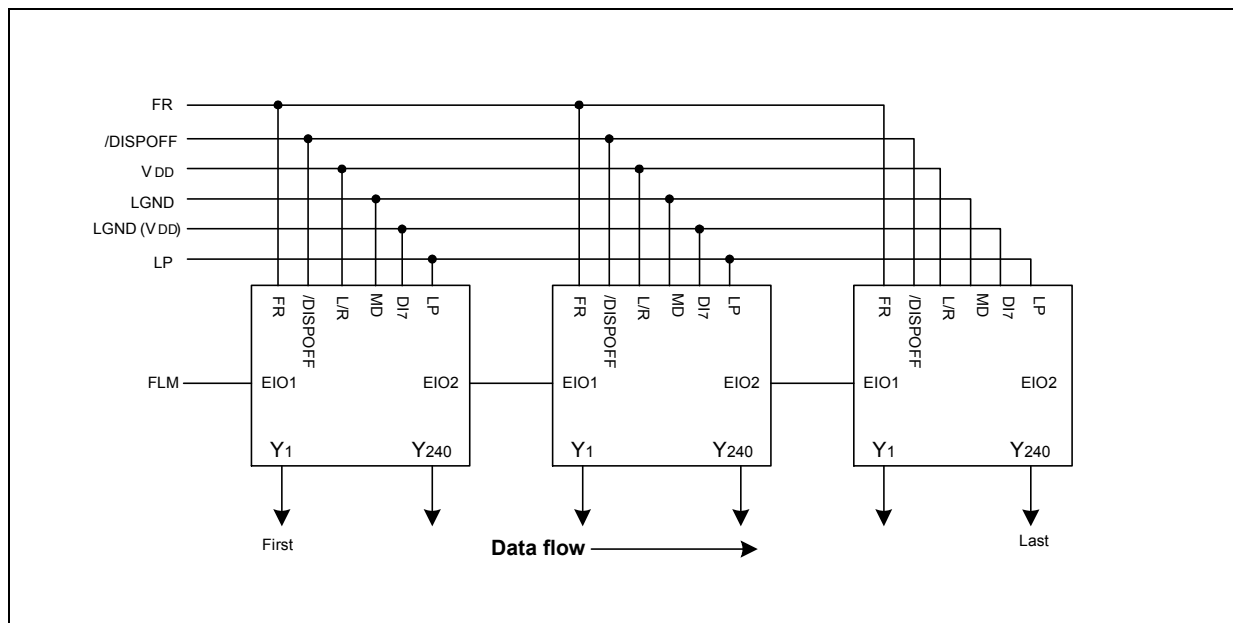


6.2.5 Connection examples for plural common drivers

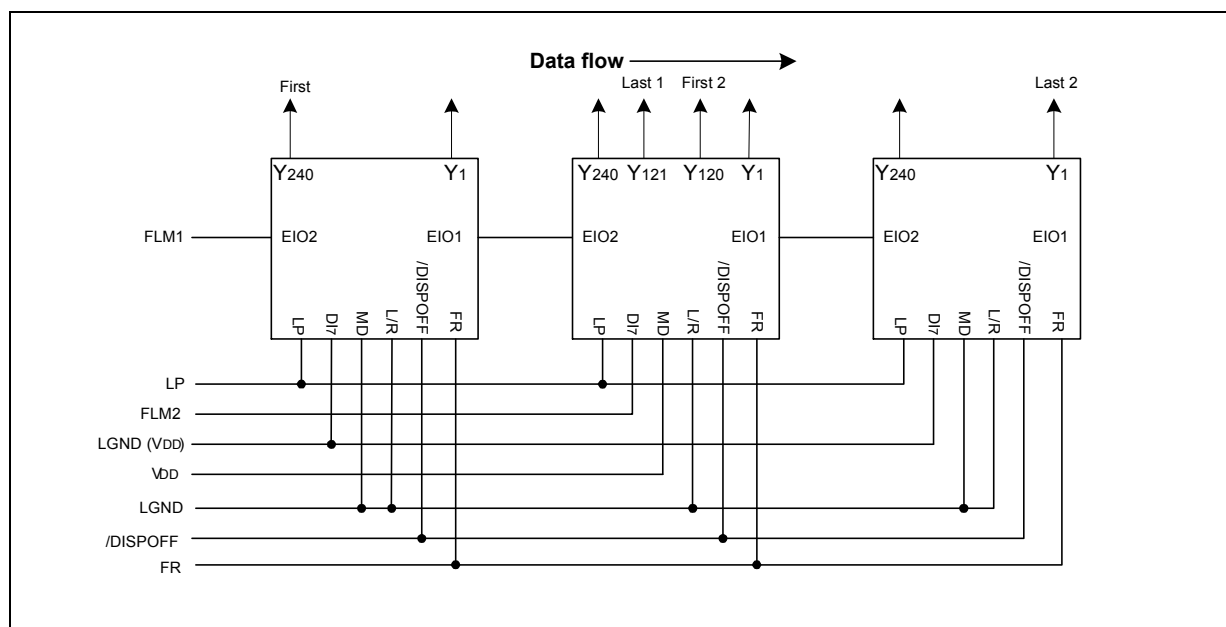
(a) Single Mode (L/R = "L")



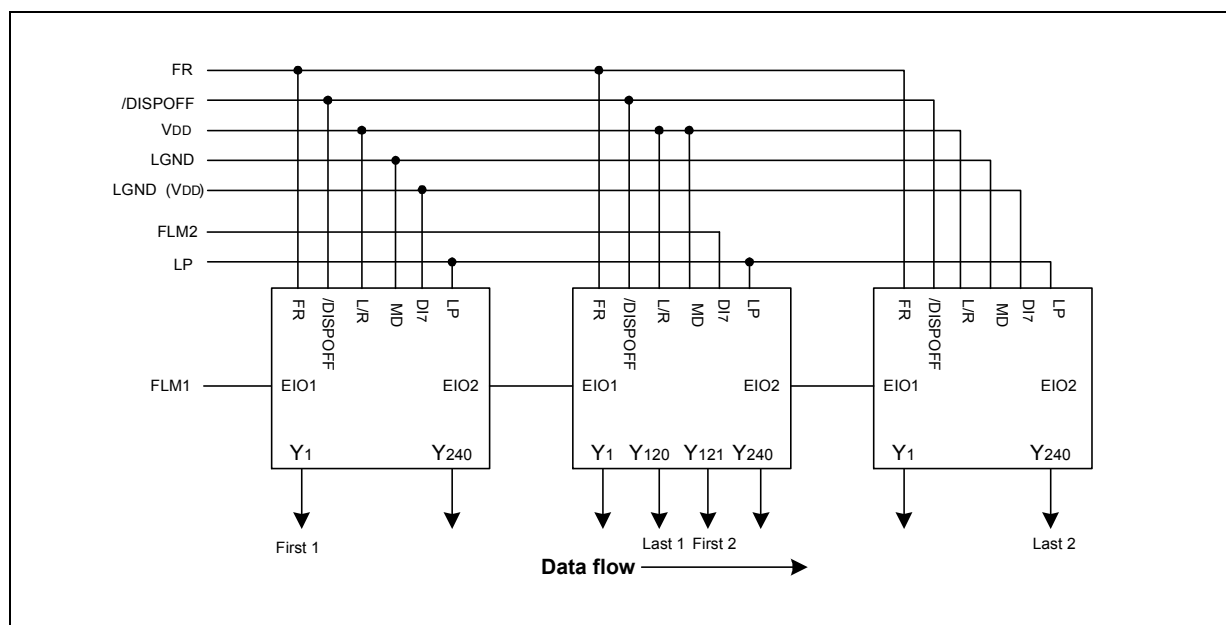
(b) Single Mode (L/R = "H")



(c) Dual Mode (L/R = "L")



(d) Dual mode (L/R = "H")



7. PRECAUTIONS

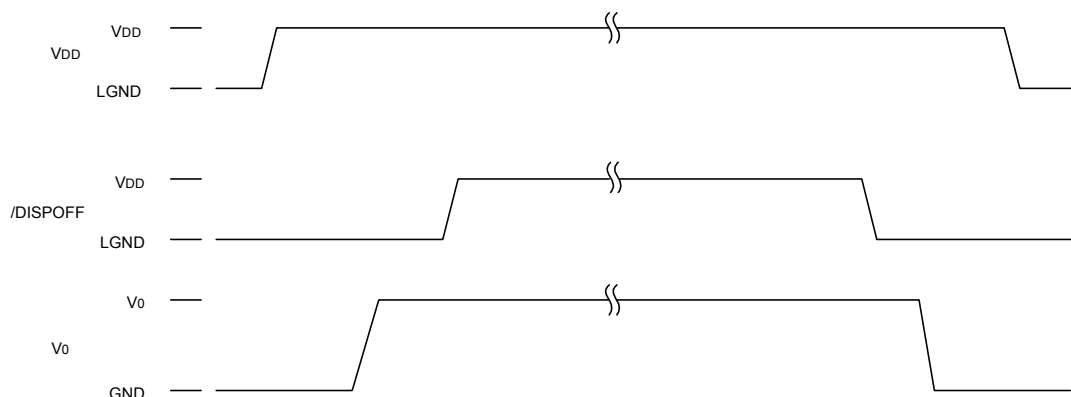
Precautions when connecting or disconnecting the power supply

This IC has a high-voltage LCD driver, so it may be permanently damaged by a high current which may flow if voltage is supplied to the LCD drive power supply while the logic system power supply is floating. The details are as follows,

- When connecting the power supply, connect the LCD drive power after connecting the logic system power. Furthermore, when disconnecting the power, disconnect the logic system power after disconnecting the LCD drive power
- It is advisable to connect the serial resistor (50 to 100 Ω) or fuse to the LCD drive power V_0 of the system as a current limiter. Set up a suitable value of the resistor in consideration of the display grade.

And when connecting the logic power supply, the logic condition of this IC inside is insecure. Therefore connect the LCD drive power supply after resetting logic condition of this IC inside on /DISPOFF function. After that, cancel the /DISPOFF function after the LCD drive power supply has become stable. Furthermore, when disconnecting the power, set the LCD drive output pins to level LGND on /DISPOFF function. Then disconnect the logic system power after disconnecting the LCD drive power.

When connecting the power supply, follow the recommended sequence shown here



8. ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	APPLICABLE PINS	RATING	UNIT	NOTE
Supply voltage (1)	V_{DD}	V_{DD}	-0.3 to +7.0	V	1,2
Supply voltage (2)	V_0	V_{0L}, V_{0R}	-0.3 to +33.0	V	
	V_{12}	V_{12L}, V_{12R}	-0.3 to $V_0 + 0.3$	V	
	V_{43}	V_{43L}, V_{43R}	-0.3 to $V_0 + 0.3$	V	
	V_{SS}	V_{SS}	-0.3 to $V_0 + 0.3$	V	
Input voltage	V_I	DI ₇ -DI ₀ , XCK, LP, L/R, FR, MD, S/C, EIO ₁ , EIO ₂ , /DISPOFF	-0.3 to $V_{DD} + 0.3$	V	
Storage temperature	T_{STG}		-45 to +125	°C	

NOTES:

1. $T_A = +25\text{ °C}$
2. The applicable voltage on logic pins with respect to LGND, high voltage pins with V_{SS} (0 V).
3. Stress over the "Absolute Max. Ratings" conditions will damage the device permanently.

9. RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	APPLICABLE PINS	MIN.	TYP.	MAX.	UNIT	NOTE
Supply voltage (1)	V_{DD}	V_{DD}	+2.5		+5.5	V	1, 2
Supply voltage (2)	V_0	V_{0L}, V_{0R}	+15.0		+30.0	V	
Operating temperature	T_{OPR}		-25		+85	°C	

NOTES:

1. The applicable voltage on logic pins with respect to LGND, high voltage pins with V_{SS} (0 V).
2. Ensure that voltages are set such that $V_{SS} < V_{43} < V_{12} < V_0$.

10. ELECTRICAL CHARACTERISTICS

10.1 DC Characteristics

(Segment Mode) (LGND=V_{SS} = GND = 0V, V_{DD} = +2.5 to +5.5V, V₀ = +15.0 to +30.0V, T_{OPR} = -25 to +85°C)

PARAMETER	SYMBOL	CONDITIONS	APPLICABLE PINS	MIN.	TYP.	MAX.	UNIT	NOTE
Input "Low" voltage	V _{IL}		DI7-DI0, XCK, LP, L/R			0.2V _{DD}	V	
Input "High" voltage	V _{IH}		FR, MD, S/C, EIO ₁ , EIO ₂ , /DISPOFF	0.8V _{DD}		V _{DD} +0.8	V	
Output "Low" voltage	V _{OL}	I _{OL} = +0.4 mA	EIO ₁ , EIO ₂			+0.4	V	
Output "High" voltage	V _{OH}	I _{OH} = -0.4 mA		V _{DD} -0.4			V	
Input leakage current	I _{LIL}	V _i = LGND	DI7-DI0, XCK, LP, L/R FR, MD, S/C, EIO ₁ , EIO ₂ , /DISPOFF			-10.0	μA	
	I _{LIH}	V _i = V _{DD}				+10.0	μA	
Output resistance	R _{ON}	ΔV _{ON} = 0.5V	Y ₁ -Y ₂₄₀		1.5	2.0	kΩ	
		V ₀ =30V V ₀ =20V			2.0	2.5		
Standby current	I _{STB}		LGND			75.0	μA	1
Supply current (1) (Non-selection)	I _{DD1}		V _{DD}			2.0	mA	2
Supply current (2) (Selection)	I _{DD2}		V _{DD}			12.0	mA	3
Supply current (3)	I ₀		V _{0L} , V _{0R}			1.5	mA	4

NOTES:

- V_{DD} = +5.0 V, V₀ = +30.0 V, V_i = LGND.
- V_{DD} = +5.0 V, V₀ = +30.0 V, f_{XCK} = 20 MHz, no-load, EI = V_{DD}. The input data is turned over by data taking clock (4-bit parallel input mode).
- V_{DD} = +5.0 V, V₀ = +30.0 V, f_{XCK} = 20 MHz, no-load, EI = LGND. The input data is turned over by data taking clock (4-bit parallel input mode).
- V_{DD} = +5.0 V, V₀ = +30.0 V, f_{XCK} = 20MHz, f_{LP} = 41.6 kHz, f_{FR} = 80 Hz, no-load. The input data is turned over by data taking clock (4-bit parallel input mode).

(Common Mode) (LGND=V_{SS} = GND = 0V, V_{DD} = +2.5 to +5.5V, V₀ = +15.0 to +30.0V, T_{OPR} = -25 to +85°C)

PARAMETER	SYMBOL	CONDITIONS	APPLICABLE PINS	MIN.	TYP.	MAX.	UNIT	NOTE
Input "Low" voltage	V _{IL}		DI7-DI0, XCK, LP, L/R			0.2V _{DD}	V	
Input "High" voltage	V _{IH}		FR, MD, S/C, EIO ₁ , EIO ₂ , /DISPOFF	0.8V _{DD}		V _{DD} +0.8	V	
Output "Low" voltage	V _{OL}	I _{OL} = +0.4 mA	EIO ₁ , EIO ₂			+0.4	V	
Output "High" voltage	V _{OH}	I _{OH} = -0.4 mA		V _{DD} -0.4			V	
Input leakage current	I _{LIL}	V _i = LGND	DI7-DI0, XCK, LP, L/R FR, MD, S/C, EIO ₁ , EIO ₂ , /DISPOFF			-10.0	μA	
	I _{LIH}	V _i = V _{DD}	DI6-DI0, LP, L/R, FR, MD, S/C, /DISPOFF			+10.0	μA	
Input pull-down current	I _{PD}	V _i = V _{DD}	DI7, XCK, EIO ₁ , EIO ₂			100.0	μA	
Output resistance	R _{ON}	ΔV _{ON} = 0.5V	Y ₁ -Y ₂₄₀		1.5	2.0	kΩ	
		V ₀ =30V V ₀ =20V			2.0	2.5		
Standby current	I _{SPD}		LGND			75.0	μA	1
Supply current (1)	I _{DD}		V _{DD}			120.0	μA	2
Supply current (2)	I ₀		V _{0L} , V _{0R}			240.0	μA	2

NOTES:

- V_{DD} = +5.0 V, V₀ = +30.0 V, V_i = LGND
- V_{DD} = +5.0 V, V₀ = +30.0 V, f_{LP} = 41.6 kHz, f_{FR} = 80 Hz, 1/480 duty operation, no-load.

10.2 AC Characteristics

(Segment Mode 1) (LGND=V_{SS} = GND = 0V, V_{DD} = +5.0±0.5V, V₀ = +15.0 to +30.0V, T_{OPR} = -25 to +85 °C)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP.	MAX.	UNIT	NOTE
Shift clock period	t _{WCK}	t _R , t _F ≤ 10ns	50			ns	1
Shift clock "H" pulse width	t _{WCKH}		15			ns	
Shift clock "L" pulse width	t _{WCKL}		15			ns	
Data setup time	t _{DS}		10			ns	
Data hold time	t _{DH}		12			ns	
Latch pulse "H" pulse width	t _{WLPH}		15			ns	
Shift clock rise to latch pulse rise time	t _{LD}		0			ns	
Shift clock fall to latch pulse fall time	t _{SL}		30			ns	
Latch pulse rise to shift clock rise time	t _{LS}		25			ns	
Latch pulse fall to shift clock fall time	t _{LH}		25			ns	
Enable setup time	t _S		10			ns	
Input signal rise time	t _R				50	ns	2
Input signal fall time	t _F				50	ns	2
/DISPOFF removal time	t _{SD}		100			ns	
/DISPOFF "L" pulse width	t _{WDL}		1.2			μs	
Output delay time (1)	t _D	CL = 15 pF			30	ns	
Output delay time (2)	t _{PD1} , t _{PD2}	CL = 15 pF			1.2	μs	
Output delay time (3)	t _{PD3}	CL = 15 pF			1.2	μs	

NOTES:

1. Takes the cascade connection into consideration.
2. (t_{WCK} - t_{WCKH} - t_{WCKL})/2 is maximum in the case of high speed operation.

(Segment Mode 2) (LGND=V_{SS} = GND = 0V, V_{DD} = +3.0 to +4.5V, V₀ = +15.0 to +30.0V, T_{OPR} = -25 to +85°C)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT	NOTE
Shift clock period	t _{WCK}	t _R , t _F ≤ 10ns	66			ns	1
Shift clock "H" pulse width	t _{WCKH}		23			ns	
Shift clock "L" pulse width	t _{WCKL}		23			ns	
Data setup time	t _{DS}		15			ns	
Data hold time	t _{DH}		23			ns	
Latch pulse "H" pulse width	t _{WLPH}		30			ns	
Shift clock rise to latch pulse rise time	t _{LD}		0			ns	
Shift clock fall to latch pulse fall time	t _{SL}		50			ns	
Latch pulse rise to shift clock rise time	t _{LS}		30			ns	
Latch pulse fall to shift clock fall time	t _{LH}		30			ns	
Enable setup time	t _S		15			ns	
Input signal rise time	t _R				50	ns	2
Input signal fall time	t _F				50	ns	2
/DISPOFF removal time	t _{SD}		100			ns	
/DISPOFF "L" pulse width	t _{WDL}		1.2			μs	
Output delay time (1)	t _D	CL = 15 pF			41	ns	
Output delay time (2)	t _{PD1} , t _{PD2}	CL = 15 pF			1.2	μs	
Output delay time (3)	t _{PD3}	CL = 15 pF			1.2	μs	

NOTES:

1. Takes the cascade connection into consideration.
2. (t_{WCK} - t_{WCKH} - t_{WCKL})/2 is maximum in the case of high speed operation.

(Segment Mode 3) (LGND=V_{SS} = GND = 0V, V_{DD} = +2.5 to +3.0V, V₀ = +15.0 to +30.0V, T_{OPR} = -25 to +85°C)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT	NOTE
Shift clock period	t _{WCK}	t _R , t _F ≤ 10ns	82			ns	1
Shift clock "H" pulse width	t _{WCKH}		28			ns	
Shift clock "L" pulse width	t _{WCKL}		28			ns	
Data setup time	t _{DS}		20			ns	
Data hold time	t _{DH}		23			ns	
Latch pulse "H" pulse width	t _{WLPH}		30			ns	
Shift clock rise to latch pulse rise time	t _{LD}		0			ns	
Shift clock fall to latch pulse fall time	t _{SL}		65			ns	
Latch pulse rise to shift clock rise time	t _{LS}		30			ns	
Latch pulse fall to shift clock fall time	t _{LH}		30			ns	
Enable setup time	t _S		15			ns	
Input signal rise time	t _R				50	ns	2
Input signal fall time	t _F				50	ns	2
/DISPOFF removal time	t _{SD}		100			ns	
/DISPOFF "L" pulse width	t _{WDL}		1.2			μs	
Output delay time (1)	t _D	CL = 15 pF			57	ns	
Output delay time (2)	t _{PD1} , t _{PD2}	CL = 15 pF			1.2	μs	
Output delay time (3)	t _{PD3}	CL = 15 pF			1.2	μs	

NOTES:

1. Takes the cascade connection into consideration.
2. (t_{WCK} - t_{WCKH} - t_{WCKL})/2 is maximum in the case of high speed operation.

(Common Mode) (LGND=V_{SS} = 0V, V_{DD} = +2.5 to +5.5V, V₀ = +15.0 to +30.0V, T_{OPR} = -25 to +85°C)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Shift clock period	t _{WLP}	t _R , t _F ≤ 20ns	250			ns
Shift clock "H" pulse width	t _{WLPH}	V _{DD} = +5.0± 0.5V	15			ns
		V _{DD} = +2.5+ 4.5V	30			ns
Data setup time	t _{SU}		30			ns
Data hold time	t _H		50			ns
Input signal rise time	t _R				50	ns
Input signal fall time	t _F				50	ns
/DISPOFF removal time	t _{SD}		100			ns
/DISPOFF "L" pulse width	t _{WDL}		1.2			μs
Output delay time (1)	t _{DL}	CL = 15 pF			200	ns
Output delay time (2)	t _{PD1} , t _{PD2}	CL = 15 pF			1.2	μs
Output delay time (3)	t _{PD3}	CL = 15 pF			1.2	μs

10.3 Timing Chart of Segment Mode

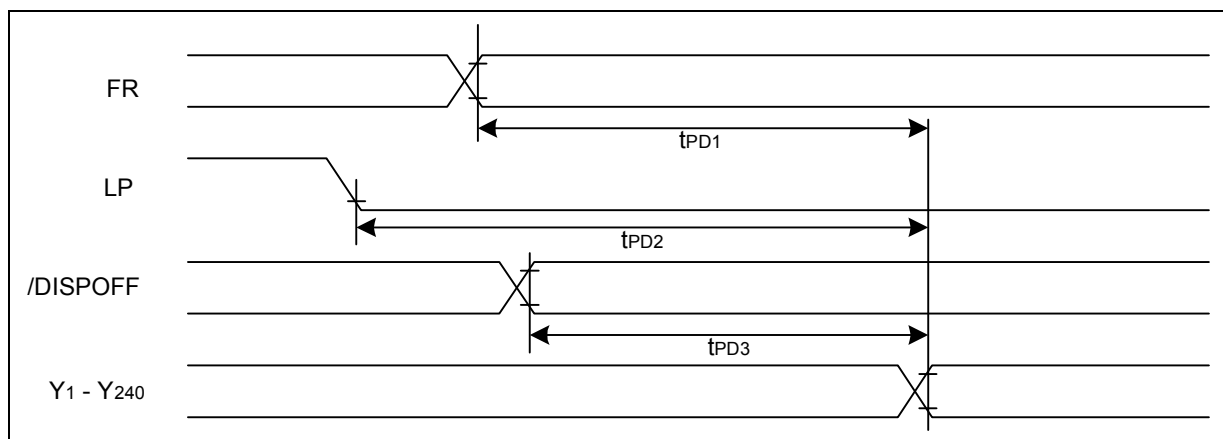
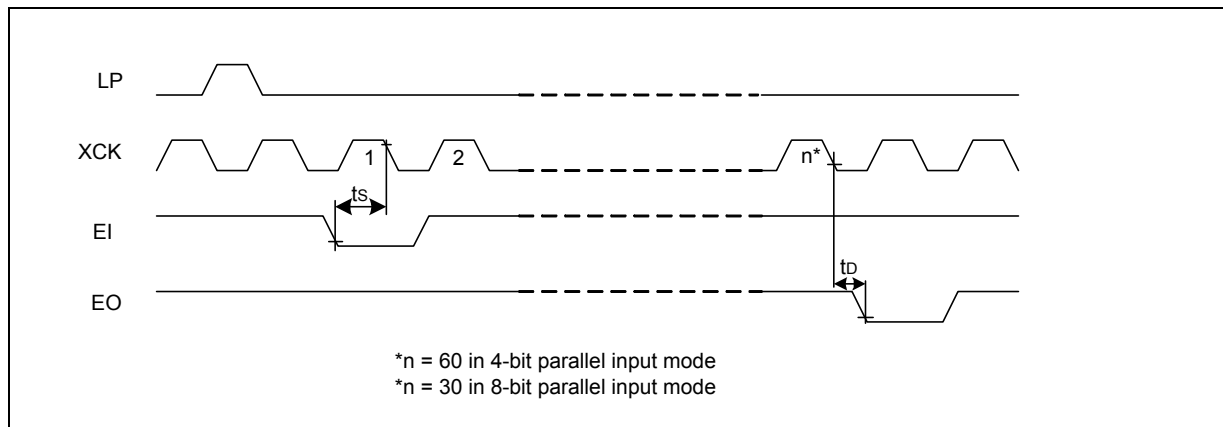
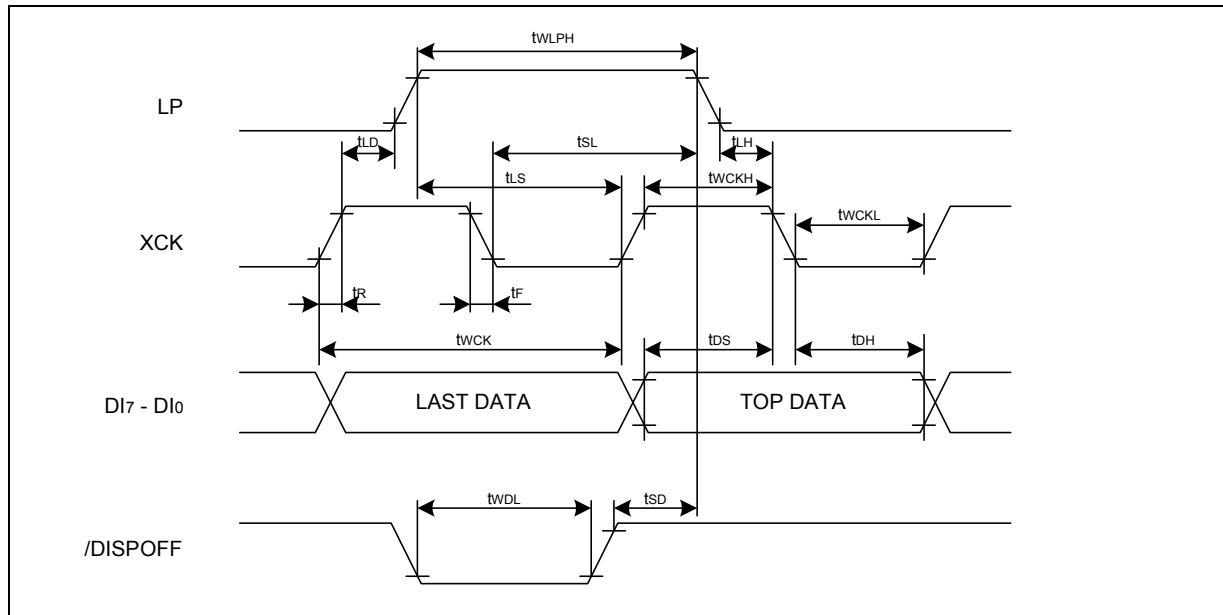
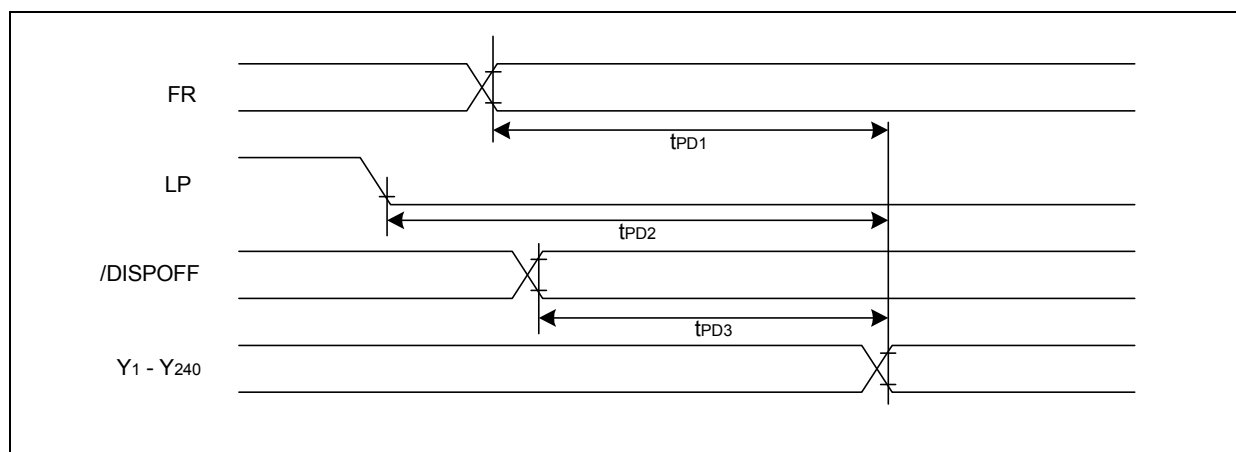
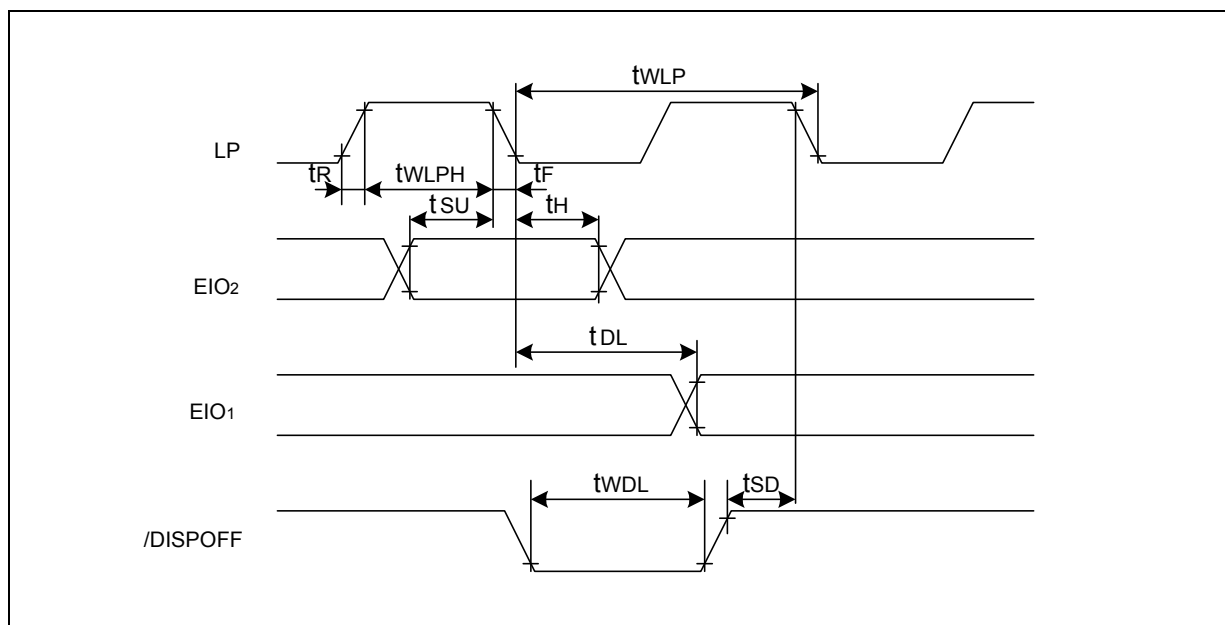


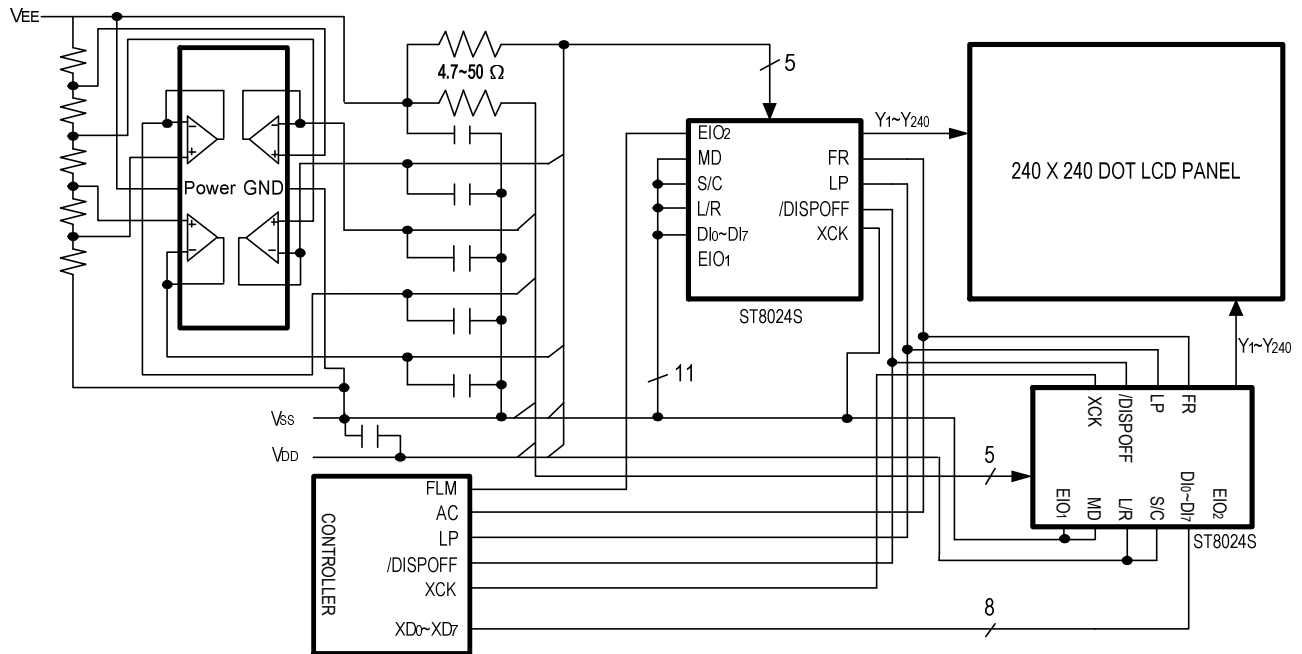
Fig. 8 Timing Characteristics (3)

10.4 Timing Chart of Common Mode

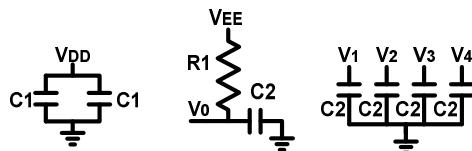
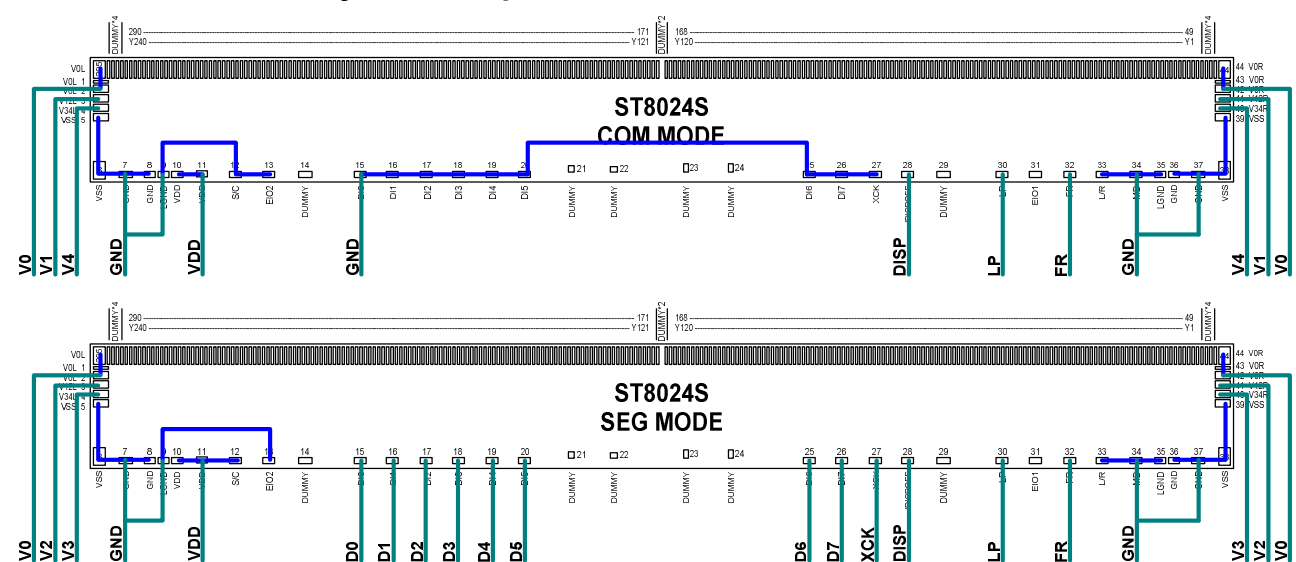


11. APPLICATION CIRCUIT

11.1 Application Circuit for Module



11.2 LCD Panel Layout Example



R1 : 4.7Ω ~ 50Ω
C1 : 0.1uF ~ 4.7uF
C2 : 0.1uF ~ 4.7uF
— Circuit on PCB
— Circuit on LCD

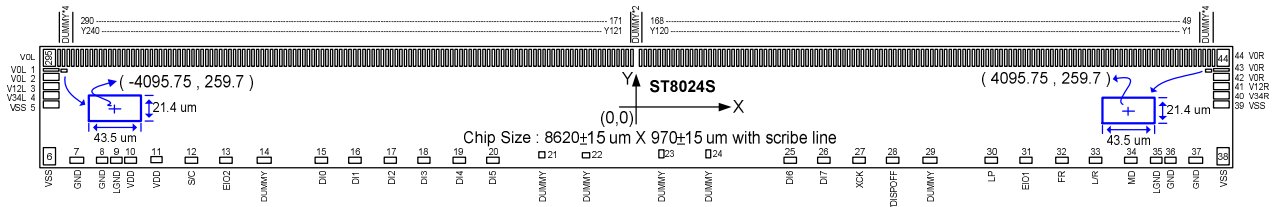
ITO layout Notices (for reference only)

1. We suggest the ITO resistor for LCD panel is under 15Ω/Square, and the resistor value is as smaller as better.
2. Among the interface pins, please to be sure the ITO resistor value of power pins are less than the following values that we suggest.

Pin Name	ITO Resistor Values
LGND, GND, VDD, Vss	Less than 75Ω when VDD ≥ 3.0V, and the smaller the better
V0R, V0L	Less than 150Ω, and the smaller the better
V12R, V12L, V34R, V12L	Less than 250Ω, and the smaller the better

PS : Above resistor value test on 3" LCD panel.

12. PAD DIAGRAM



Notes: Subtract should be connected to GND.

Unit : um

Pad#	Name	X	Y	Pad#	Name	X	Y
1	V0L	-4180.00	264.00	38	VSS	4192.50	-355.00
2	V0L	-4180.00	214.50	39	VSS	4180.00	16.50
3	V12L	-4180.00	148.50	40	V34R	4180.00	82.50
4	V34L	-4180.00	82.50	41	V12R	4180.00	148.50
5	VSS	-4180.00	16.50	42	V0R	4180.00	214.50
6	VSS	-4192.50	-355.00	43	V0R	4180.00	264.00
7	GND	-3995.95	-383.10	44	V0R	4192.50	350.00
8	GND	-3815.75	-383.10	45	DUMMY	4123.70	350.00
9	LGND	-3714.45	-383.10	46	DUMMY	4090.70	350.00
10	VDD	-3611.80	-383.35	47	DUMMY	4057.70	350.00
11	VDD	-3426.65	-379.35	48	DUMMY	4024.70	350.00
12	S/C	-3178.35	-383.10	49	Y1	3991.70	350.00
13	EIO2	-2930.15	-383.10	50	Y2	3958.70	350.00
14	DUMMY	-2657.85	-383.10	51	Y3	3925.70	350.00
15	DI0	-2249.05	-383.10	52	Y4	3892.70	350.00
16	DI1	-2009.05	-383.10	53	Y5	3859.70	350.00
17	DI2	-1756.85	-383.10	54	Y6	3826.70	350.00
18	DI3	-1516.85	-383.10	55	Y7	3793.70	350.00
19	DI4	-1264.65	-383.10	56	Y8	3760.70	350.00
20	DI5	-1024.65	-383.10	57	Y9	3727.70	350.00
21	DUMMY	-674.40	-344.40	58	Y10	3694.70	350.00
22	DUMMY	-358.68	-347.68	59	Y11	3661.70	350.00
23	DUMMY	179.53	-337.73	60	Y12	3628.70	350.00
24	DUMMY	514.13	-337.73	61	Y13	3595.70	350.00
25	DI6	1098.65	-383.10	62	Y14	3562.70	350.00
26	DI7	1338.65	-383.10	63	Y15	3529.70	350.00
27	XCK	1590.85	-383.10	64	Y16	3496.70	350.00
28	/DISPOFF	1830.85	-383.10	65	Y17	3463.70	350.00
29	DUMMY	2098.15	-383.10	66	Y18	3430.70	350.00
30	LP	2534.85	-383.10	67	Y19	3397.70	350.00
31	EIO1	2783.05	-383.10	68	Y20	3364.70	350.00
32	FR	3040.25	-383.10	69	Y21	3331.70	350.00
33	L/R	3280.25	-383.10	70	Y22	3298.70	350.00
34	MD	3532.45	-383.10	71	Y23	3265.70	350.00
35	LGND	3714.45	-383.10	72	Y24	3232.70	350.00
36	GND	3815.75	-383.10	73	Y25	3199.70	350.00
37	GND	3995.95	-383.10	74	Y26	3166.70	350.00

75	Y27	3133.70	350.00	124	Y76	1516.70	350.00
76	Y28	3100.70	350.00	125	Y77	1483.70	350.00
77	Y29	3067.70	350.00	126	Y78	1450.70	350.00
78	Y30	3034.70	350.00	127	Y79	1417.70	350.00
79	Y31	3001.70	350.00	128	Y80	1384.70	350.00
80	Y32	2968.70	350.00	129	Y81	1351.70	350.00
81	Y33	2935.70	350.00	130	Y82	1318.70	350.00
82	Y34	2902.70	350.00	131	Y83	1285.70	350.00
83	Y35	2869.70	350.00	132	Y84	1252.70	350.00
84	Y36	2836.70	350.00	133	Y85	1219.70	350.00
85	Y37	2803.70	350.00	134	Y86	1186.70	350.00
86	Y38	2770.70	350.00	135	Y87	1153.70	350.00
87	Y39	2737.70	350.00	136	Y88	1120.70	350.00
88	Y40	2704.70	350.00	137	Y89	1087.70	350.00
89	Y41	2671.70	350.00	138	Y90	1054.70	350.00
90	Y42	2638.70	350.00	139	Y91	1021.70	350.00
91	Y43	2605.70	350.00	140	Y92	988.70	350.00
92	Y44	2572.70	350.00	141	Y93	955.70	350.00
93	Y45	2539.70	350.00	142	Y94	922.70	350.00
94	Y46	2506.70	350.00	143	Y95	889.70	350.00
95	Y47	2473.70	350.00	144	Y96	856.70	350.00
96	Y48	2440.70	350.00	145	Y97	823.70	350.00
97	Y49	2407.70	350.00	146	Y98	790.70	350.00
98	Y50	2374.70	350.00	147	Y99	757.70	350.00
99	Y51	2341.70	350.00	148	Y100	724.70	350.00
100	Y52	2308.70	350.00	149	Y101	691.70	350.00
101	Y53	2275.70	350.00	150	Y102	658.70	350.00
102	Y54	2242.70	350.00	151	Y103	625.70	350.00
103	Y55	2209.70	350.00	152	Y104	592.70	350.00
104	Y56	2176.70	350.00	153	Y105	559.70	350.00
105	Y57	2143.70	350.00	154	Y106	526.70	350.00
106	Y58	2110.70	350.00	155	Y107	493.70	350.00
107	Y59	2077.70	350.00	156	Y108	460.70	350.00
108	Y60	2044.70	350.00	157	Y109	427.70	350.00
109	Y61	2011.70	350.00	158	Y110	394.70	350.00
110	Y62	1978.70	350.00	159	Y111	361.70	350.00
111	Y63	1945.70	350.00	160	Y112	328.70	350.00
112	Y64	1912.70	350.00	161	Y113	295.70	350.00
113	Y65	1879.70	350.00	162	Y114	262.70	350.00
114	Y66	1846.70	350.00	163	Y115	229.70	350.00
115	Y67	1813.70	350.00	164	Y116	196.70	350.00
116	Y68	1780.70	350.00	165	Y117	163.70	350.00
117	Y69	1747.70	350.00	166	Y118	130.70	350.00
118	Y70	1714.70	350.00	167	Y119	97.70	350.00
119	Y71	1681.70	350.00	168	Y120	64.70	350.00
120	Y72	1648.70	350.00	169	DUMMY	31.70	350.00
121	Y73	1615.70	350.00	170	DUMMY	-31.70	350.00
122	Y74	1582.70	350.00	171	Y121	-64.70	350.00
123	Y75	1549.70	350.00	172	Y122	-97.70	350.00
173	Y123	-130.70	350.00	222	Y172	-1747.70	350.00

174	Y124	-163.70	350.00	223	Y173	-1780.70	350.00
175	Y125	-196.70	350.00	224	Y174	-1813.70	350.00
176	Y126	-229.70	350.00	225	Y175	-1846.70	350.00
177	Y127	-262.70	350.00	226	Y176	-1879.70	350.00
178	Y128	-295.70	350.00	227	Y177	-1912.70	350.00
179	Y129	-328.70	350.00	228	Y178	-1945.70	350.00
180	Y130	-361.70	350.00	229	Y179	-1978.70	350.00
181	Y131	-394.70	350.00	230	Y180	-2011.70	350.00
182	Y132	-427.70	350.00	231	Y181	-2044.70	350.00
183	Y133	-460.70	350.00	232	Y182	-2077.70	350.00
184	Y134	-493.70	350.00	233	Y183	-2110.70	350.00
185	Y135	-526.70	350.00	234	Y184	-2143.70	350.00
186	Y136	-559.70	350.00	235	Y185	-2176.70	350.00
187	Y137	-592.70	350.00	236	Y186	-2209.70	350.00
188	Y138	-625.70	350.00	237	Y187	-2242.70	350.00
189	Y139	-658.70	350.00	238	Y188	-2275.70	350.00
190	Y140	-691.70	350.00	239	Y189	-2308.70	350.00
191	Y141	-724.70	350.00	240	Y190	-2341.70	350.00
192	Y142	-757.70	350.00	241	Y191	-2374.70	350.00
193	Y143	-790.70	350.00	242	Y192	-2407.70	350.00
194	Y144	-823.70	350.00	243	Y193	-2440.70	350.00
195	Y145	-856.70	350.00	244	Y194	-2473.70	350.00
196	Y146	-889.70	350.00	245	Y195	-2506.70	350.00
197	Y147	-922.70	350.00	246	Y196	-2539.70	350.00
198	Y148	-955.70	350.00	247	Y197	-2572.70	350.00
199	Y149	-988.70	350.00	248	Y198	-2605.70	350.00
200	Y150	-1021.70	350.00	249	Y199	-2638.70	350.00
201	Y151	-1054.70	350.00	250	Y200	-2671.70	350.00
202	Y152	-1087.70	350.00	251	Y201	-2704.70	350.00
203	Y153	-1120.70	350.00	252	Y202	-2737.70	350.00
204	Y154	-1153.70	350.00	253	Y203	-2770.70	350.00
205	Y155	-1186.70	350.00	254	Y204	-2803.70	350.00
206	Y156	-1219.70	350.00	255	Y205	-2836.70	350.00
207	Y157	-1252.70	350.00	256	Y206	-2869.70	350.00
208	Y158	-1285.70	350.00	257	Y207	-2902.70	350.00
209	Y159	-1318.70	350.00	258	Y208	-2935.70	350.00
210	Y160	-1351.70	350.00	259	Y209	-2968.70	350.00
211	Y161	-1384.70	350.00	260	Y210	-3001.70	350.00
212	Y162	-1417.70	350.00	261	Y211	-3034.70	350.00
213	Y163	-1450.70	350.00	262	Y212	-3067.70	350.00
214	Y164	-1483.70	350.00	263	Y213	-3100.70	350.00
215	Y165	-1516.70	350.00	264	Y214	-3133.70	350.00
216	Y166	-1549.70	350.00	265	Y215	-3166.70	350.00
217	Y167	-1582.70	350.00	266	Y216	-3199.70	350.00
218	Y168	-1615.70	350.00	267	Y217	-3232.70	350.00
219	Y169	-1648.70	350.00	268	Y218	-3265.70	350.00
220	Y170	-1681.70	350.00	269	Y219	-3298.70	350.00
221	Y171	-1714.70	350.00	270	Y220	-3331.70	350.00
271	Y221	-3364.70	350.00	284	Y234	-3793.70	350.00
272	Y222	-3397.70	350.00	285	Y235	-3826.70	350.00

273	Y223	-3430.70	350.00	286	Y236	-3859.70	350.00
274	Y224	-3463.70	350.00	287	Y237	-3892.70	350.00
275	Y225	-3496.70	350.00	288	Y238	-3925.70	350.00
276	Y226	-3529.70	350.00	289	Y239	-3958.70	350.00
277	Y227	-3562.70	350.00	290	Y240	-3991.70	350.00
278	Y228	-3595.70	350.00	291	DUMMY	-4024.70	350.00
279	Y229	-3628.70	350.00	292	DUMMY	-4057.70	350.00
280	Y230	-3661.70	350.00	293	DUMMY	-4090.70	350.00
281	Y231	-3694.70	350.00	294	DUMMY	-4123.70	350.00
282	Y232	-3727.70	350.00	295	VOL	-4192.50	350.00
283	Y233	-3760.70	350.00				

12.1 Gold Bump Size

Pad No.	X	Y	Area (um ²)
1, 43	112.00	18.00	2016.0000
2, 3, 4, 5, 39, 40, 41, 42	112.00	51.00	5712.0000
44, 295	87.00	122.00	10614.0000
6, 38	87.00	112.00	9744.0000
7, 37	99.00	42.40	4197.6000
8, 9, 35, 36	81.30	42.40	3447.1200
10	84.10	42.90	3620.7600
11	80.70	42.40	3421.6800
12, 13, 15~20, 25~28, 30~34	88.70	42.40	3760.8800
14, 29	100.20	42.40	4248.4800
21	43.30	44.40	1922.5200
22	52.85	37.85	2000.3725
23, 24	34.65	57.75	2001.0375
45~294	18.00	122.00	2196.0000

Wafer thickness = 480±20um, Bump pad height = 15um, strength=30g

13. APPLICATION NOTE(REFERENCE ONLY)

- 13.1 Adjust V1 and V4 voltage to keep the $V0-V1 = V4-VSS$ relation to get better display quality. The $(V0-V1)-(V4-VSS)$ value had better less than 100mV.
- 13.2 Add 0.1uF high frequency by-pass capacitor to filter the noise on V0~V4 to VSS.
- 13.3 When OP follower circuit is used, please be sure the OP power is higher than V0 at least 1.5V.
- 13.4 EIO1 and EIO2 is enable pin for driver, please pay attention to the distance to avoid noise when cascade function is used. Two chip connecting distance is as shorter as better.

14. REVISION

REVISION	DESCRIPTION	PAGE	DATE
0.10	First release	1-25	2005/9/12
0.20	Add LGND definition, and re-define the pin function	1-25	2005/11/22
0.30	Modify suggestion resistor value for V ₀ . Add alignment mark data, Add LCD Panel Layout Example Modify bond pad height to 18um	21	2006/5/22
0.31	Modify bump pad height to 15um and add wafer thickness.	24	2006/6/7
0.32	Modify all Vss for logic setting pins to LGND	1-25	2006/7/21
0.33	Modify description of LGND	6-8	2006/7/21
0.34	Change Sitronix logo and modify description of LGND for COM mode	1-25	2006/7/21
0.35	Modify pad define and size for pad No.6 and No.38.	21-24	2006/7/24
0.36	Modify Chip size and thickness with scribe line Modify "Output resistance" test condition	16,22,24	2006/10/26
0.37	Modify V ₀ Max. voltage in "RECOMMENDED OPERATING CONDITIONS" and "ABSOLUTE MAXIMUM RATINGS" Modify the Max. V ₀ voltage to 40V for test condition Modify V ₀ Max. voltage in feature	2,15-18	2007/1/3
0.38	Modify all the data about absolute max voltage and recommend max voltage	2,16-18	2007/5/25
0.39	Modify the ITO resistor value suggestion Add application note	21,26	2008/5/05