Sitronix

ST7712

262K Color Single-Chip TFT Controller/Driver

1. Introduction

The ST7712 is a single-chip which generates 396 Source lines and 132 gate lines controller/driver for 262K color TFT dot graphic display. ST7712 support 18-bit high-speed bus interface and Serial Peripheral Interface (SPI), thus it can perform bi-operation functions, data transfer, and high-speed RAM write function. Display data can be stored in an on-chip display data RAM of 132x396x6 bits. It can perform display data RAM read/write operation without external operating clock to minimize power consumption. In addition, because it contains power supply circuits necessary to drive liquid crystal, it is possible to make a display system with the fewest components.

2. Features

Driver Output Circuits

–396 source output

–132 gate output

On-chip Display Data RAM

–Capacity: 396 × 132 × 6 =313,632bits

–65K colors (RGB)= (565) mode

–262K colors (RGB)= (666) mode

Applicable Duty Ratios

- Various partial display

- Partial window moving & data scrolling

Microprocessor Interface

–8/9/16/18-bit parallel bi-directional interface with

–6800-series or 8080-series

–4-line serial interface

–3-line serial interface

On-chip Low Power Analog Circuit

–On-chip oscillator circuit

–Voltage converter generating liquid crystal driver up to 6-time scale

–Simultaneous availability of 262K color with γ-correction function

Operating Voltage Range

–Vcc: 2.4~3.3V (logic power supply)

–Vci: 2.5~3.3V (analog power supply)

–IOVcc: 1.8~3.3V (interface power supply)

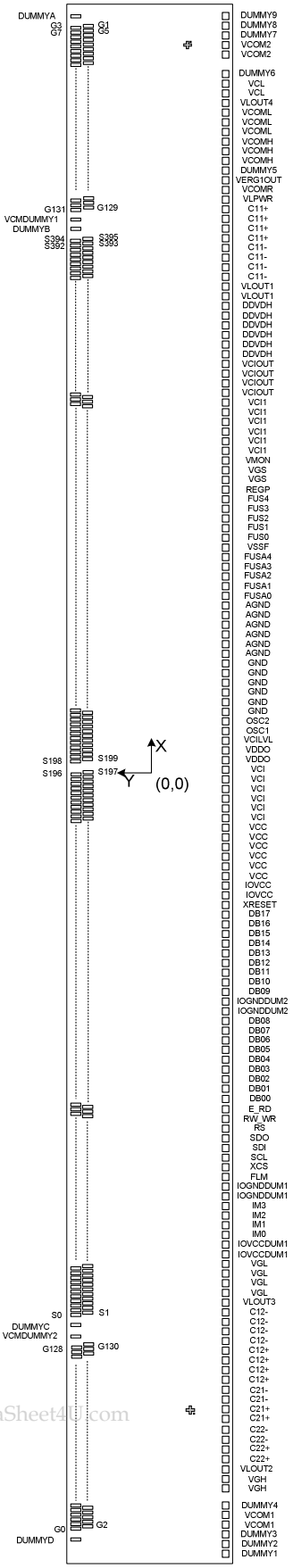
–Source line voltage: DDVDH=4.5~6.0V

Package Type

–Application for COG

ST7712	6800 , 8080 ,4-Line , 3-Line interface	ST

3. Pad Arrangement



Chip size (um): 15,800x1,380

PAD coordinate: PAD center

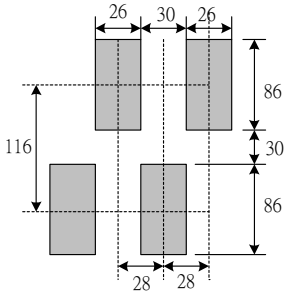
Coordinate origin: Chip center

Chip thickness (um): 400±25

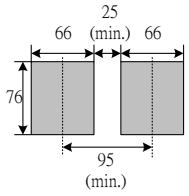
Bump height (um):15±2

Pad Arrangement (Unit: um):

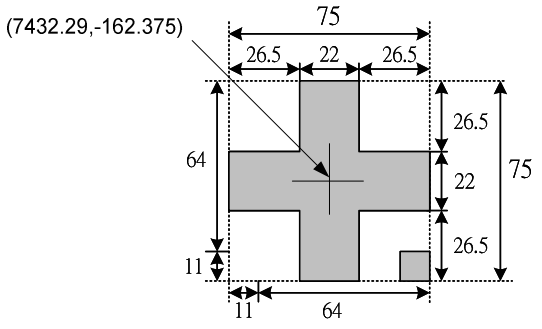
Pad No. 1~ Pad No. 534: 26 x 86

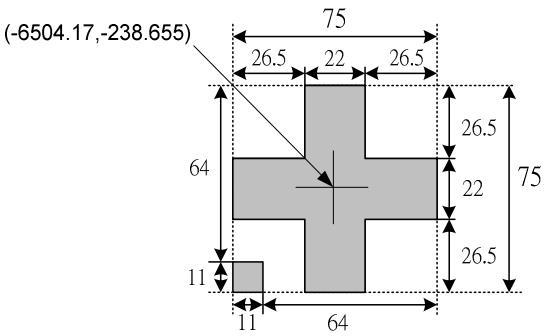


Pad No. 535~ Pad No. 692: 66 x 76



Alignment Mark (Unit: um):





4. Pad Center Coordinates

PAD No.	PIN Name	X	Y
1	DUMMYA	7710	570.715
2	G1	7620.5	454.715
3	G3	7592.5	570.715
4	G5	7564.5	454.715
5	G7	7536.5	570.715
6	G9	7508.5	454.715
7	G11	7480.5	570.715
8	G13	7452.5	454.715
9	G15	7424.5	570.715
10	G17	7396.5	454.715
11	G19	7368.5	570.715
12	G21	7340.5	454.715
13	G23	7312.5	570.715
14	G25	7284.5	454.715
15	G27	7256.5	570.715
16	G29	7228.5	454.715
17	G31	7200.5	570.715
18	G33	7172.5	454.715
19	G35	7144.5	570.715
20	G37	7116.5	454.715
21	G39	7088.5	570.715
22	G41	7060.5	454.715
23	G43	7032.5	570.715
24	G45	7004.5	454.715
25	G47	6976.5	570.715
26	G49	6948.5	454.715
27	G51	6920.5	570.715
28	G53	6892.5	454.715
29	G55	6864.5	570.715
30	G57	6836.5	454.715
31	G59	6808.5	570.715
32	G61	6780.5	454.715
33	G63	6752.5	570.715
34	G65	6724.5	454.715
35	G67	6696.5	570.715

PAD No.	PIN Name	X	Y
36	G69	6668.5	454.715
37	G71	6640.5	570.715
38	G73	6612.5	454.715
39	G75	6584.5	570.715
40	G77	6556.5	454.715
41	G79	6528.5	570.715
42	G81	6500.5	454.715
43	G83	6472.5	570.715
44	G85	6444.5	454.715
45	G87	6416.5	570.715
46	G89	6388.5	454.715
47	G91	6360.5	570.715
48	G93	6332.5	454.715
49	G95	6304.5	570.715
50	G97	6276.5	454.715
51	G99	6248.5	570.715
52	G101	6220.5	454.715
53	G103	6192.5	570.715
54	G105	6164.5	454.715
55	G107	6136.5	570.715
56	G109	6108.5	454.715
57	G111	6080.5	570.715
58	G113	6052.5	454.715
59	G115	6024.5	570.715
60	G117	5996.5	454.715
61	G119	5968.5	570.715
62	G121	5940.5	454.715
63	G123	5912.5	570.715
64	G125	5884.5	454.715
65	G127	5856.5	570.715
66	G129	5828.5	454.715
67	G131	5800.5	570.715
68	VCMDUMMY1	5726.5	570.715
69	DUMMYB	5631.5	570.715
70	S395	5557.5	454.715

PAD No.	PIN Name	X	Y
71	S394	5529.5	570.715
72	S393	5501.5	454.715
73	S392	5473.5	570.715
74	S391	5445.5	454.715
75	S390	5417.5	570.715
76	S389	5389.5	454.715
77	S388	5361.5	570.715
78	S387	5333.5	454.715
79	S386	5305.5	570.715
80	S385	5277.5	454.715
81	S384	5249.5	570.715
82	S383	5221.5	454.715
83	S382	5193.5	570.715
84	S381	5165.5	454.715
85	S380	5137.5	570.715
86	S379	5109.5	454.715
87	S378	5081.5	570.715
88	S377	5053.5	454.715
89	S376	5025.5	570.715
90	S375	4997.5	454.715
91	S374	4969.5	570.715
92	S373	4941.5	454.715
93	S372	4913.5	570.715
94	S371	4885.5	454.715
95	S370	4857.5	570.715
96	S369	4829.5	454.715
97	S368	4801.5	570.715
98	S367	4773.5	454.715
99	S366	4745.5	570.715
100	S365	4717.5	454.715
101	S364	4689.5	570.715
102	S363	4661.5	454.715
103	S362	4633.5	570.715
104	S361	4605.5	454.715
105	S360	4577.5	570.715
106	S359	4549.5	454.715

PAD No.	PIN Name	X	Y
107	S358	4521.5	570.715
108	S357	4493.5	454.715
109	S356	4465.5	570.715
110	S355	4437.5	454.715
111	S354	4409.5	570.715
112	S353	4381.5	454.715
113	S352	4353.5	570.715
114	S351	4325.5	454.715
115	S350	4297.5	570.715
116	S349	4269.5	454.715
117	S348	4241.5	570.715
118	S347	4213.5	454.715
119	S346	4185.5	570.715
120	S345	4157.5	454.715
121	S344	4129.5	570.715
122	S343	4101.5	454.715
123	S342	4073.5	570.715
124	S341	4045.5	454.715
125	S340	4017.5	570.715
126	S339	3989.5	454.715
127	S338	3961.5	570.715
128	S337	3933.5	454.715
129	S336	3905.5	570.715
130	S335	3877.5	454.715
131	S334	3849.5	570.715
132	S333	3821.5	454.715
133	S332	3793.5	570.715
134	S331	3765.5	454.715
135	S330	3737.5	570.715
136	S329	3709.5	454.715
137	S328	3681.5	570.715
138	S327	3653.5	454.715
139	S326	3625.5	570.715
140	S325	3597.5	454.715
141	S324	3569.5	570.715
142	S323	3541.5	454.715

PAD No.	PIN Name	X	Y
143	S322	3513.5	570.715
144	S321	3485.5	454.715
145	S320	3457.5	570.715
146	S319	3429.5	454.715
147	S318	3401.5	570.715
148	S317	3373.5	454.715
149	S316	3345.5	570.715
150	S315	3317.5	454.715
151	S314	3289.5	570.715
152	S313	3261.5	454.715
153	S312	3233.5	570.715
154	S311	3205.5	454.715
155	S310	3177.5	570.715
156	S309	3149.5	454.715
157	S308	3121.5	570.715
158	S307	3093.5	454.715
159	S306	3065.5	570.715
160	S305	3037.5	454.715
161	S304	3009.5	570.715
162	S303	2981.5	454.715
163	S302	2953.5	570.715
164	S301	2925.5	454.715
165	S300	2897.5	570.715
166	S299	2869.5	454.715
167	S298	2841.5	570.715
168	S297	2813.5	454.715
169	S296	2785.5	570.715
170	S295	2757.5	454.715
171	S294	2729.5	570.715
172	S293	2701.5	454.715
173	S292	2673.5	570.715
174	S291	2645.5	454.715
175	S290	2617.5	570.715
176	S289	2589.5	454.715
177	S288	2561.5	570.715
178	S287	2533.5	454.715

PAD No.	PIN Name	X	Y
179	S286	2505.5	570.715
180	S285	2477.5	454.715
181	S284	2449.5	570.715
182	S283	2421.5	454.715
183	S282	2393.5	570.715
184	S281	2365.5	454.715
185	S280	2337.5	570.715
186	S279	2309.5	454.715
187	S278	2281.5	570.715
188	S277	2253.5	454.715
189	S276	2225.5	570.715
190	S275	2197.5	454.715
191	S274	2169.5	570.715
192	S273	2141.5	454.715
193	S272	2113.5	570.715
194	S271	2085.5	454.715
195	S270	2057.5	570.715
196	S269	2029.5	454.715
197	S268	2001.5	570.715
198	S267	1973.5	454.715
199	S266	1945.5	570.715
200	S265	1917.5	454.715
201	S264	1889.5	570.715
202	S263	1861.5	454.715
203	S262	1833.5	570.715
204	S261	1805.5	454.715
205	S260	1777.5	570.715
206	S259	1749.5	454.715
207	S258	1721.5	570.715
208	S257	1693.5	454.715
209	S256	1665.5	570.715
210	S255	1637.5	454.715
211	S254	1609.5	570.715
212	S253	1581.5	454.715
213	S252	1553.5	570.715
214	S251	1525.5	454.715

PAD No.	PIN Name	X	Y
215	S250	1497.5	570.715
216	S249	1469.5	454.715
217	S248	1441.5	570.715
218	S247	1413.5	454.715
219	S246	1385.5	570.715
220	S245	1357.5	454.715
221	S244	1329.5	570.715
222	S243	1301.5	454.715
223	S242	1273.5	570.715
224	S241	1245.5	454.715
225	S240	1217.5	570.715
226	S239	1189.5	454.715
227	S238	1161.5	570.715
228	S237	1133.5	454.715
229	S236	1105.5	570.715
230	S235	1077.5	454.715
231	S234	1049.5	570.715
232	S233	1021.5	454.715
233	S232	993.5	570.715
234	S231	965.5	454.715
235	S230	937.5	570.715
236	S229	909.5	454.715
237	S228	881.5	570.715
238	S227	853.5	454.715
239	S226	825.5	570.715
240	S225	797.5	454.715
241	S224	769.5	570.715
242	S223	741.5	454.715
243	S222	713.5	570.715
244	S221	685.5	454.715
245	S220	657.5	570.715
246	S219	629.5	454.715
247	S218	601.5	570.715
248	S217	573.5	454.715
249	S216	545.5	570.715
250	S215	517.5	454.715

PAD No.	PIN Name	X	Y
251	S214	489.5	570.715
252	S213	461.5	454.715
253	S212	433.5	570.715
254	S211	405.5	454.715
255	S210	377.5	570.715
256	S209	349.5	454.715
257	S208	321.5	570.715
258	S207	293.5	454.715
259	S206	265.5	570.715
260	S205	237.5	454.715
261	S204	209.5	570.715
262	S203	181.5	454.715
263	S202	153.5	570.715
264	S201	125.5	454.715
265	S200	97.5	570.715
266	S199	69.5	454.715
267	S198	41.5	570.715
268	S197	-41.5	454.715
269	S196	-69.5	570.715
270	S195	-97.5	454.715
271	S194	-125.5	570.715
272	S193	-153.5	454.715
273	S192	-181.5	570.715
274	S191	-209.5	454.715
275	S190	-237.5	570.715
276	S189	-265.5	454.715
277	S188	-293.5	570.715
278	S187	-321.5	454.715
279	S186	-349.5	570.715
280	S185	-377.5	454.715
281	S184	-405.5	570.715
282	S183	-433.5	454.715
283	S182	-461.5	570.715
284	S181	-489.5	454.715
285	S180	-517.5	570.715
286	S179	-545.5	454.715

PAD No.	PIN Name	X	Y
287	S178	-573.5	570.715
288	S177	-601.5	454.715
289	S176	-629.5	570.715
290	S175	-657.5	454.715
291	S174	-685.5	570.715
292	S173	-713.5	454.715
293	S172	-741.5	570.715
294	S171	-769.5	454.715
295	S170	-797.5	570.715
296	S169	-825.5	454.715
297	S168	-853.5	570.715
298	S167	-881.5	454.715
299	S166	-909.5	570.715
300	S165	-937.5	454.715
301	S164	-965.5	570.715
302	S163	-993.5	454.715
303	S162	-1021.5	570.715
304	S161	-1049.5	454.715
305	S160	-1077.5	570.715
306	S159	-1105.5	454.715
307	S158	-1133.5	570.715
308	S157	-1161.5	454.715
309	S156	-1189.5	570.715
310	S155	-1217.5	454.715
311	S154	-1245.5	570.715
312	S153	-1273.5	454.715
313	S152	-1301.5	570.715
314	S151	-1329.5	454.715
315	S150	-1357.5	570.715
316	S149	-1385.5	454.715
317	S148	-1413.5	570.715
318	S147	-1441.5	454.715
319	S146	-1469.5	570.715
320	S145	-1497.5	454.715
321	S144	-1525.5	570.715
322	S143	-1553.5	454.715

PAD No.	PIN Name	X	Y
323	S142	-1581.5	570.715
324	S141	-1609.5	454.715
325	S140	-1637.5	570.715
326	S139	-1665.5	454.715
327	S138	-1693.5	570.715
328	S137	-1721.5	454.715
329	S136	-1749.5	570.715
330	S135	-1777.5	454.715
331	S134	-1805.5	570.715
332	S133	-1833.5	454.715
333	S132	-1861.5	570.715
334	S131	-1889.5	454.715
335	S130	-1917.5	570.715
336	S129	-1945.5	454.715
337	S128	-1973.5	570.715
338	S127	-2001.5	454.715
339	S126	-2029.5	570.715
340	S125	-2057.5	454.715
341	S124	-2085.5	570.715
342	S123	-2113.5	454.715
343	S122	-2141.5	570.715
344	S121	-2169.5	454.715
345	S120	-2197.5	570.715
346	S119	-2225.5	454.715
347	S118	-2253.5	570.715
348	S117	-2281.5	454.715
349	S116	-2309.5	570.715
350	S115	-2337.5	454.715
351	S114	-2365.5	570.715
352	S113	-2393.5	454.715
353	S112	-2421.5	570.715
354	S111	-2449.5	454.715
355	S110	-2477.5	570.715
356	S109	-2505.5	454.715
357	S108	-2533.5	570.715
358	S107	-2561.5	454.715

PAD No.	PIN Name	X	Y
359	S106	-2589.5	570.715
360	S105	-2617.5	454.715
361	S104	-2645.5	570.715
362	S103	-2673.5	454.715
363	S102	-2701.5	570.715
364	S101	-2729.5	454.715
365	S100	-2757.5	570.715
366	S99	-2785.5	454.715
367	S98	-2813.5	570.715
368	S97	-2841.5	454.715
369	S96	-2869.5	570.715
370	S95	-2897.5	454.715
371	S94	-2925.5	570.715
372	S93	-2953.5	454.715
373	S92	-2981.5	570.715
374	S91	-3009.5	454.715
375	S90	-3037.5	570.715
376	S89	-3065.5	454.715
377	S88	-3093.5	570.715
378	S87	-3121.5	454.715
379	S86	-3149.5	570.715
380	S85	-3177.5	454.715
381	S84	-3205.5	570.715
382	S83	-3233.5	454.715
383	S82	-3261.5	570.715
384	S81	-3289.5	454.715
385	S80	-3317.5	570.715
386	S79	-3345.5	454.715
387	S78	-3373.5	570.715
388	S77	-3401.5	454.715
389	S76	-3429.5	570.715
390	S75	-3457.5	454.715
391	S74	-3485.5	570.715
392	S73	-3513.5	454.715
393	S72	-3541.5	570.715
394	S71	-3569.5	454.715

PAD No.	PIN Name	X	Y
395	S70	-3597.5	570.715
396	S69	-3625.5	454.715
397	S68	-3653.5	570.715
398	S67	-3681.5	454.715
399	S66	-3709.5	570.715
400	S65	-3737.5	454.715
401	S64	-3765.5	570.715
402	S63	-3793.5	454.715
403	S62	-3821.5	570.715
404	S61	-3849.5	454.715
405	S60	-3877.5	570.715
406	S59	-3905.5	454.715
407	S58	-3933.5	570.715
408	S57	-3961.5	454.715
409	S56	-3989.5	570.715
410	S55	-4017.5	454.715
411	S54	-4045.5	570.715
412	S53	-4073.5	454.715
413	S52	-4101.5	570.715
414	S51	-4129.5	454.715
415	S50	-4157.5	570.715
416	S49	-4185.5	454.715
417	S48	-4213.5	570.715
418	S47	-4241.5	454.715
419	S46	-4269.5	570.715
420	S45	-4297.5	454.715
421	S44	-4325.5	570.715
422	S43	-4353.5	454.715
423	S42	-4381.5	570.715
424	S41	-4409.5	454.715
425	S40	-4437.5	570.715
426	S39	-4465.5	454.715
427	S38	-4493.5	570.715
428	S37	-4521.5	454.715
429	S36	-4549.5	570.715
430	S35	-4577.5	454.715

PAD No.	PIN Name	X	Y
431	S34	-4605.5	570.715
432	S33	-4633.5	454.715
433	S32	-4661.5	570.715
434	S31	-4689.5	454.715
435	S30	-4717.5	570.715
436	S29	-4745.5	454.715
437	S28	-4773.5	570.715
438	S27	-4801.5	454.715
439	S26	-4829.5	570.715
440	S25	-4857.5	454.715
441	S24	-4885.5	570.715
442	S23	-4913.5	454.715
443	S22	-4941.5	570.715
444	S21	-4969.5	454.715
445	S20	-4997.5	570.715
446	S19	-5025.5	454.715
447	S18	-5053.5	570.715
448	S17	-5081.5	454.715
449	S16	-5109.5	570.715
450	S15	-5137.5	454.715
451	S14	-5165.5	570.715
452	S13	-5193.5	454.715
453	S12	-5221.5	570.715
454	S11	-5249.5	454.715
455	S10	-5277.5	570.715
456	S9	-5305.5	454.715
457	S8	-5333.5	570.715
458	S7	-5361.5	454.715
459	S6	-5389.5	570.715
460	S5	-5417.5	454.715
461	S4	-5445.5	570.715
462	S3	-5473.5	454.715
463	S2	-5501.5	570.715
464	S1	-5529.5	454.715
465	S0	-5557.5	570.715
466	DUMMYC	-5631.5	570.715

PAD No.	PIN Name	X	Y
467	VCMDUMMY2	-5726.5	570.715
468	G130	-5800.5	454.715
469	G128	-5828.5	570.715
470	G126	-5856.5	454.715
471	G124	-5884.5	570.715
472	G122	-5912.5	454.715
473	G120	-5940.5	570.715
474	G118	-5968.5	454.715
475	G116	-5996.5	570.715
476	G114	-6024.5	454.715
477	G112	-6052.5	570.715
478	G110	-6080.5	454.715
479	G108	-6108.5	570.715
480	G106	-6136.5	454.715
481	G104	-6164.5	570.715
482	G102	-6192.5	454.715
483	G100	-6220.5	570.715
484	G98	-6248.5	454.715
485	G96	-6276.5	570.715
486	G94	-6304.5	454.715
487	G92	-6332.5	570.715
488	G90	-6360.5	454.715
489	G88	-6388.5	570.715
490	G86	-6416.5	454.715
491	G84	-6444.5	570.715
492	G82	-6472.5	454.715
493	G80	-6500.5	570.715
494	G78	-6528.5	454.715
495	G76	-6556.5	570.715
496	G74	-6584.5	454.715
497	G72	-6612.5	570.715
498	G70	-6640.5	454.715
499	G68	-6668.5	570.715
500	G66	-6696.5	454.715
501	G64	-6724.5	570.715
502	G62	-6752.5	454.715

PAD No.	PIN Name	X	Y
503	G60	-6780.5	570.715
504	G58	-6808.5	454.715
505	G56	-6836.5	570.715
506	G54	-6864.5	454.715
507	G52	-6892.5	570.715
508	G50	-6920.5	454.715
509	G48	-6948.5	570.715
510	G46	-6976.5	454.715
511	G44	-7004.5	570.715
512	G42	-7032.5	454.715
513	G40	-7060.5	570.715
514	G38	-7088.5	454.715
515	G36	-7116.5	570.715
516	G34	-7144.5	454.715
517	G32	-7172.5	570.715
518	G30	-7200.5	454.715
519	G28	-7228.5	570.715
520	G26	-7256.5	454.715
521	G24	-7284.5	570.715
522	G22	-7312.5	454.715
523	G20	-7340.5	570.715
524	G18	-7368.5	454.715
525	G16	-7396.5	570.715
526	G14	-7424.5	454.715
527	G12	-7452.5	570.715
528	G10	-7480.5	454.715
529	G8	-7508.5	570.715
530	G6	-7536.5	454.715
531	G4	-7564.5	570.715
532	G2	-7592.5	454.715
533	G0	-7620.5	570.715
534	DUMMYD	-7710	570.715
535	DUMMY1	-7710	-583.465
536	DUMMY2	-7609.15	-583.465
537	DUMMY3	-7508.3	-583.465
538	VCOM1	-7408.33	-583.465

PAD No.	PIN Name	X	Y
539	VCOM1	-7313.33	-583.465
540	DUMMY4	-7140	-583.465
541	VGH	-7045	-583.465
542	VGH	-6950	-583.465
543	VLOUT2	-6855	-583.465
544	C22+	-6760	-583.465
545	C22+	-6665	-583.465
546	C22-	-6570	-583.465
547	C22-	-6475	-583.465
548	C21+	-6380	-583.465
549	C21+	-6285	-583.465
550	C21-	-6190	-583.465
551	C21-	-6095	-583.465
552	C12+	-6000	-583.465
553	C12+	-5905	-583.465
554	C12+	-5810	-583.465
555	C12+	-5715	-583.465
556	C12-	-5620	-583.465
557	C12-	-5525	-583.465
558	C12-	-5430	-583.465
559	C12-	-5335	-583.465
560	VLOUT3	-5240	-583.465
561	VGL	-5145	-583.465
562	VGL	-5050	-583.465
563	VGL	-4955	-583.465
564	VGL	-4860	-583.465
565	IOVCCDUM1	-4715	-583.465
566	IOVCCDUM1	-4620	-583.465
567	IM0	-4525	-583.465
568	IM1	-4430	-583.465
569	IM2	-4335	-583.465
570	IM3	-4240	-583.465
571	IOGNDDUM1	-4145	-583.465
572	IOGNDDUM1	-4050	-583.465
573	FLM	-3955	-583.465
574	XCS	-3860	-583.465

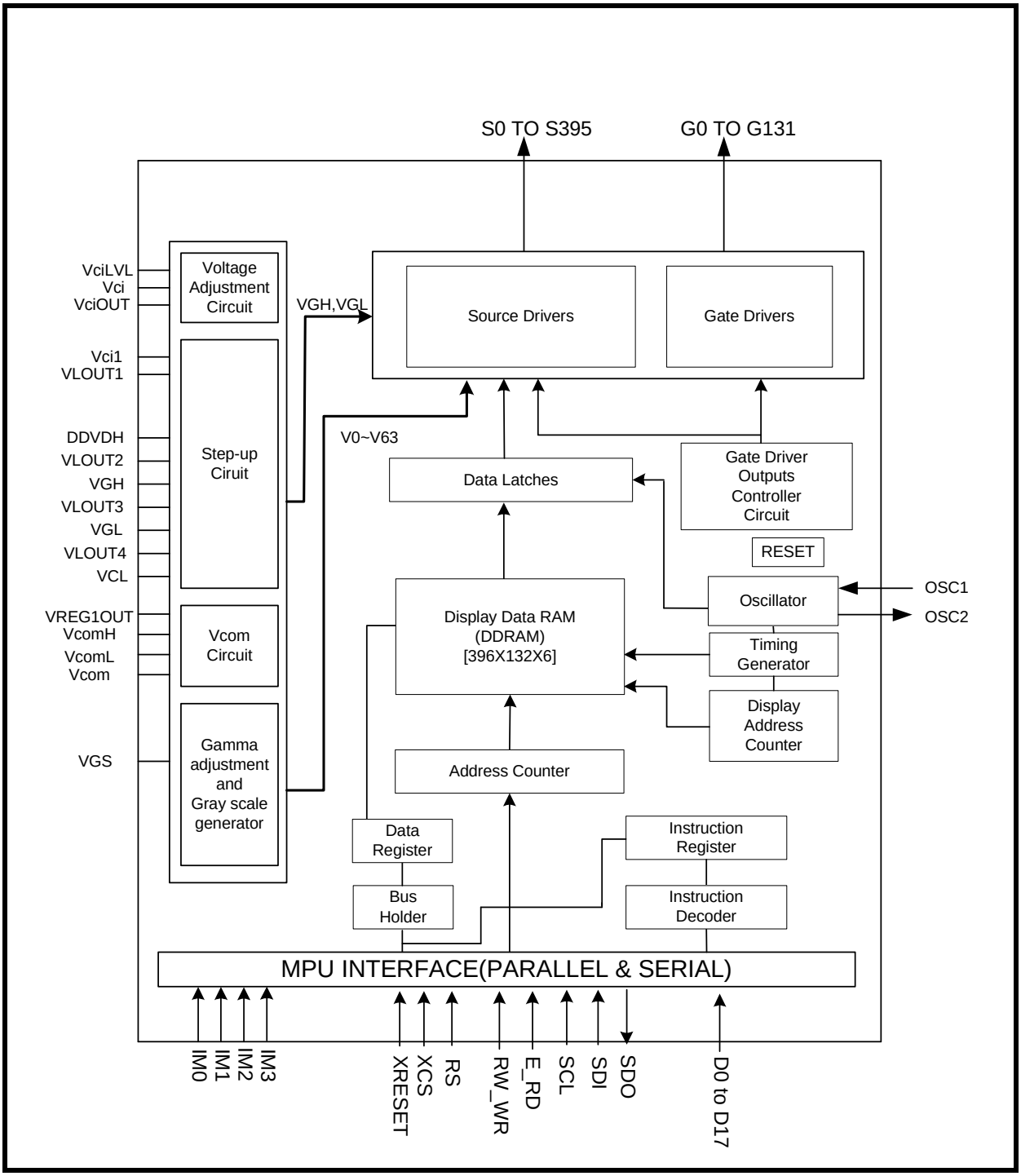
PAD No.	PIN Name	X	Y
575	SCL	-3765	-583.465
576	SDI	-3670	-583.465
577	SDO	-3575	-583.465
578	RS	-3480	-583.465
579	RW_WR	-3385	-583.465
580	E_RD	-3290	-583.465
581	DB0	-3195	-583.465
582	DB1	-3100	-583.465
583	DB2	-3005	-583.465
584	DB3	-2910	-583.465
585	DB4	-2815	-583.465
586	DB5	-2720	-583.465
587	DB6	-2625	-583.465
588	DB7	-2530	-583.465
589	DB8	-2435	-583.465
590	IOGNDDUM2	-2340	-583.465
591	IOGNDDUM2	-2245	-583.465
592	DB9	-2150	-583.465
593	DB10	-2055	-583.465
594	DB11	-1960	-583.465
595	DB12	-1865	-583.465
596	DB13	-1770	-583.465
597	DB14	-1675	-583.465
598	DB15	-1580	-583.465
599	DB16	-1485	-583.465
600	DB17	-1390	-583.465
601	XRESET	-1295	-583.465
602	IOVCC	-1200	-583.465
603	IOVCC	-1105	-583.465
604	VCC	-960	-583.465
605	VCC	-865	-583.465
606	VCC	-770	-583.465
607	VCC	-675	-583.465
608	VCC	-580	-583.465
609	VCC	-485	-583.465
610	VCI	-390	-583.465

PAD No.	PIN Name	X	Y
611	VCI	-295	-583.465
612	VCI	-200	-583.465
613	VCI	-105	-583.465
614	VCI	-10	-583.465
615	VCI	85	-583.465
616	VDDO	180	-583.465
617	VDDO	275	-583.465
618	VCILVL	370	-583.465
619	OSC1	495	-583.465
620	OSC2	590	-583.465
621	GND	715	-583.465
622	GND	810	-583.465
623	GND	905	-583.465
624	GND	1000	-583.465
625	GND	1095	-583.465
626	GND	1190	-583.465
627	AGND	1298.775	-583.465
628	AGND	1393.775	-583.465
629	AGND	1502.415	-583.465
630	AGND	1597.415	-583.465
631	AGND	1692.415	-583.465
632	AGND	1787.415	-583.465
633	FUSA0	1896.055	-583.465
634	FUSA1	1996.055	-583.465
635	FUSA2	2096.055	-583.465
636	FUSA3	2196.055	-583.465
637	FUSA4	2296.055	-583.465
638	VSSF	2396.055	-583.465
639	FUS0	2496.055	-583.465
640	FUS1	2596.055	-583.465
641	FUS2	2696.055	-583.465
642	FUS3	2796.055	-583.465
643	FUS4	2896.055	-583.465
644	REGP	3025	-583.465
645	VGS	3120	-583.465
646	VGS	3215	-583.465

PAD No.	PIN Name	X	Y
647	VMON	3310	-583.465
648	VCI1	3405	-583.465
649	VCI1	3500	-583.465
650	VCI1	3595	-583.465
651	VCI1	3690	-583.465
652	VCI1	3785	-583.465
653	VCI1	3880	-583.465
654	VCIOUT	3975	-583.465
655	VCIOUT	4070	-583.465
656	VCIOUT	4165	-583.465
657	VCIOUT	4260	-583.465
658	DDVDH	4355	-583.465
659	DDVDH	4450	-583.465
660	DDVDH	4545	-583.465
661	DDVDH	4640	-583.465
662	DDVDH	4735	-583.465
663	DDVDH	4830	-583.465
664	VLOUT1	4925	-583.465
665	VLOUT1	5020	-583.465
666	C11-	5115	-583.465
667	C11-	5210	-583.465
668	C11-	5305	-583.465
669	C11-	5400	-583.465
670	C11+	5495	-583.465

PAD No.	PIN Name	X	Y
671	C11+	5590	-583.465
672	C11+	5685	-583.465
673	C11+	5780	-583.465
674	VLPWR	5875	-583.465
675	VCOMR	5970	-583.465
676	VREG1OUT	6065	-583.465
677	DUMMY5	6160	-583.465
678	VCOMH	6255	-583.465
679	VCOMH	6350	-583.465
680	VCOMH	6445	-583.465
681	VCOML	6570	-583.465
682	VCOML	6665	-583.465
683	VCOML	6760	-583.465
684	VLOUT4	6855	-583.465
685	VCL	6950	-583.465
686	VCL	7045	-583.465
687	DUMMY6	7140	-583.465
688	VCOM2	7313.33	-583.465
689	VCOM2	7408.33	-583.465
690	DUMMY7	7508.3	-583.465
691	DUMMY8	7609.15	-583.465
692	DUMMY9	7710	-583.465

5. Block Diagram



6. Pin Function

6.1 Microprocessor Interface

<table>
<tr><th>Name</th><th>I/O</th><th>Description</th><th>No.</th><th>Connect Pin</th></tr>
<tr><td>IM0~IM3</td><td>I</td><td>Pins to select interface mode with MPU.
<table>
<tr><th>IM3</th><th>IM2</th><th>IM1</th><th>IM0</th><th>Interface type</th><th>Acceptable color mode</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>68-system 16 bits parallel</td><td>65K</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>1</td><td>68-system 8 bits parallel</td><td>65K</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>0</td><td>80-system 16 bits parallel</td><td>65K</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>1</td><td>80-system 8 bits parallel</td><td>65K</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>0</td><td>4-line SPI</td><td>65K</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>1</td><td>3-line SPI</td><td>65K</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>0</td><td>68-system 18 bits parallel</td><td>65K, 262K</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>1</td><td>68-system 9 bits parallel</td><td>65K, 262K</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>0</td><td>80-system 18 bits parallel</td><td>65K, 262K</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>1</td><td>80-system 9 bits parallel</td><td>65K, 262K</td></tr>
</table></td><td>4</td><td>GND/ IOVcc</td></tr>
<tr><td>XCS</td><td>I</td><td>Select the ST7712.
When XCS pin is set to “Low”, ST7712 is selected and accessible.
When XCS pin is set to “High”, ST7712 is not selected and not accessible.</td><td>1</td><td>MCU</td></tr>
<tr><td>RS</td><td>I</td><td>Select register.
When RS pins is set to “Low”: Register Index
When RS pin is set to “High”: Register value/Pixel Data</td><td></td><td>MCU</td></tr>
<tr><td>E_RD</td><td>I</td><td>Read/Write execution control pin.
<table>
<tr><th>MPU Type</th><th>E_RD</th><th>Description</th></tr>
<tr><td>6800-series</td><td>E</td><td>Read / Write control input pin
-RW = “H”: When E is “H”, D0 to D17 are in an output state.
-RW = “L”: The data on D0 to D17 are latched at the falling edge of the E signal.</td></tr>
<tr><td>8080-series</td><td>/RD</td><td>Read enable clock input pin
When /RD is “L”, D0 to D17 are in an output state.</td></tr>
</table>
In 3 lines and 4 lines-system bus interface is fixed to “L”</td><td>1</td><td>MCU</td></tr>
<tr><td>RW_WR</td><td>I</td><td>Read/Write execution control pin
<table>
<tr><th>MPU type</th><th>RW_WR</th><th>Description</th></tr>
<tr><td>6800-series</td><td>RW</td><td>Read / Write control input pin
RW = “H” : read
RW = “L” : write</td></tr>
</table></td><td>1</td><td>MCU</td></tr>
</table>

		8080-series: /WR: Write enable clock input pin. The data on D0 to D17 are latched at the rising edge of the /WR signal. In 3 lines and 4 lines-system bus interface write data at the “L” level. In 3 lines and 4 lines-system bus interface read data at the “H” level.		
XRESET	I	Reset pin. When XRESET is "L", initialization is executed.	1	MCU or external RC circuit
OSC1, OSC2	I	Connect to an external resistor for R-C oscillation.	2	-
DB0~DB17	I/O	18-bit parallel bi-directional data bus in 68-systemt/80-system bus interface mode. ■ 8-bit bus: DB17-DB10 are used ,and DB9~DB0 are fixed to “H” or “L” ■ 9-bit bus: DB17-DB9 are used ,and DB8~DB0 are fixed to “H” or “L” ■ 16-bit bus: DB17-DB10 and DB8-DB1 are used; DB9 and DB0 are fixed to “H” or “L” ■ 18-bit bus: DB17-DB0 are all used.	18	MCU
SCL	I	Synchronizing clock signal with amplitude IOVcc-GND in Serial Peripheral Interface (SPI).	1	MCU
SDI	I	Pins for serial data input (SDI). Input at the rising edge of SCL.	1	MCU
SDO	O	Pins for serial data output (SDO). Output at the falling edge of SCL.	1	MCU
S0~S395	O	Source line output signal. Analog output signals to source of TFT. If not used, leave open-circuit.	396	-
G0~G131	O	Gate line output signal. High voltage output signals to gates of TFT. If not used, leave open-circuit.	132	-
FLM	O	Frame head pulse with amplitude IOVcc-GND. Use when writing data to RAM in synchronization with FLM.	1	MCU
Vcc, GND	-	Logic-side Vcc: 2.4~3.3V. Logic-side GND: 0V	12	Power supply
IOVcc		Supply to interface pins, XREST, XCS, RW_WR, E_RD, RS, DB17-0. IOVcc=1.8V~3.3V. IOVcc must be supplied with the voltage in the same condition with the internal logic voltage Vcc. When IOVcc=Vcc and assembled on COG, connect to Vcc on the FPC to avoid noise.	2	Power supply

6.2 Power Supply Pins

Name	I/O	Description	No.	Connect Pin
AGND	I	Ground pin for analog.	6	Power supply
Vci	I	Power pins for analog circuit. Connect an external power supply of 2.5~3.3V.	6	Power supply
VciLVL	I	Generate a reference voltage (VciOUT, REGP) in accordance to the ratio set with VC2~0 registers from VciLVL level. Connect to the same power supply as the Vci, which has separate wiring from the VciLVL on the FPC.	1	Power supply
VciOUT	O	Internal reference voltage with amplitude Vci-GND.	4	Stabilizing capacitor, Vci1
Vci1	I/O	Reference voltage for the step-up circuit 2. Set Vci1 so that VLOUT2 and VLOUT3 do not exceed the pre-determined ranges.	6	VciOUT
VLOUT1	O	Output voltage from step-up circuit 1 . VLOUT1 = 4.0~5.5V	2	Stabilizing capacitor, DDVDH
DDVDH	I/O	Power supply for TFT source driver. DDVDH=4.5V~6.0V	6	VLOUT1
VLOUT2	O	Output voltage from step-up circuit 2. VLOUT2 = max 16.5V	1	Stabilizing capacitor, VGH
VGH	I	Power supply for TFT gate drive. VGH max. = 16.5V.	2	VLOUT2
VLOUT3	O	Output voltage from step-up circuit 2. VLOUT3 = min -15V	1	Stabilizing capacitor, VGL
VGL	I	Power supply for TFT gate drive. VGL = min. – 15V.	4	VLOUT3
VLOUT4	O	Output voltage from step-up circuit 4. VLOUT4 = 0 ~ -3.3V	1	Stabilizing capacitor, VCL
VCL	I	Power supply for VcomL drive. Connect to VLOUT4. VCL=0V~3.3V	2	VLOUT4
C11+,C11-	I/O	Step-up capacitor connection pins for step-up circuit 1.	8	Step-up capacitor
C12+,C12- C21+,C21- C22+,C22-	I/O	Step-up capacitor connection pins for step-up circuit 2 and circuit 4.	16	Step-up capacitor
VREG1OUT	O	Output voltage generated from stepped-up of REGP voltage. VREG1OUT becomes (1) a source driver grayscale reference voltage VDH, (2) a VcomH level reference voltage, or (3) a Vcom amplitude reference voltage. Connect to a stabilizing capacitor. VREG1OUT = 3.0 ~ (DDVDH – 0.5)V.	1	Step-up Capacitor
Vcom1	O	A power supply for the TFT common electrode. Output an alternating	4	TFT

Vcom2		current with amplitude VcomH-VcomL. The alternating cycle is changeable with register setting. The COM register controls the operation start/halt.		command electrode
VcomH	O	This pin indicates a high level of Vcom generated in driving the Vcom alternation.	3	Stabilizing Capacitor
VcomL	O	When the Vcom alternation is driven, this pin indicates a low level of Vcom. An internal register can be used to adjust the voltage.	3	Stabilizing Capacitor
VcomR	I	Use to adjust VcomH with an external variable resistor. To adjust VcomH, place a variable resistor between VREG1OUT and GND.	1	Variable resistor or open
VGS	I	A reference level for the grayscale voltage generating circuit.	2	GND
VMON	--	Test pin. Leave open.	1	Open
VLPWR	--	Test pin. Connect to capacitors externally or leave open.	1	Capacitor or open
REGP	--	Test pin. Leave open.	1	Open
VSSF	--	For Vcom voltage fine tune by trim fuse	1	Open
FUS0~4	--	Test pin. Leave open.	5	Open
FUSA0~A4	--	For Vcom voltage fine tune by trim fuse	4	Open
VDDO	--	Test pin. Connect to capacitors externally	2	Capacitor or open
IOVccDUM1	O	Internal IOVcc level. Use to fix the electric potential for unused interface or fixed pins . When not used, leave open.	2	Open
IOGNDDUM1,2	O	Internal GND level. Use to fix the electric potential for unused interface or fixed pins. When not used, leave open.	4	Open
VCMDUMMY1,2	--	A power supply for the TFT common electrode. Output an alternating current with amplitude VcomH-VcomL. The alternating cycle is changeable with register setting. The COM register controls the operation start/halt.	2	Open
DUMMYA,B,C,D	--	DUMMY pad, When no used, leave open	4	open
DUMMY1,2,3,4,5,6,7,8,9	--	DUMMY pad, When no used, leave open	9	open

7. Functional Description

7.1 Microprocessor Interface

Chip Select Input

There is XCS pin for chip selection. The ST7712 can connect with MPU when XCS is "L". If XCS is “H”, these pins are set to any other combination, RS, E_RD, and RW_WR inputs are disabled and DB0 to DB17 are to be high impedance. And, in case of 4-line/3-line serial interface, the internal shift register and the counter are reset.

7.1.1 Selecting Parallel / Serial Interface

ST7712 has 10 types of interface with MPU, including two serial and eight parallel interfaces. This parallel or serial interface is determined by IM3~IM0 pins as shown in table 7.1.1**.**

Table 7.1.1 Parallel / Serial Interface Mode

IM3	IM2	IM1	IM0	Interface type	Data Bus	Acceptable Color mode
0	0	0	0	68-series 16 bits parallel	DB17~DB10, DB8~DB1	65K
0	0	0	1	68-series 8 bits parallel	DB17~DB10	65K
0	0	1	0	80-series 16 bits parallel	DB17~DB10, DB8~DB1	65K
0	0	1	1	80-series 8 bits parallel	DB17~DB10	65K
0	1	0	0	4-line SPI	SDI, SDO	65K
0	1	0	1	3-line SPI	SDI, SDO	65K
1	0	0	0	68-series 18 bits parallel	DB17~DB0	65K, 262K
1	0	0	1	68-series 9 bits parallel	DB17~DB9	65K, 262K
1	0	1	0	80-series 18 bits parallel	DB17~DB0	65K, 262K
1	0	1	1	80-series 9 bits parallel	DB17~DB9	65K, 262K

7.1.2 8-bit/9-bit/16-bit/18-bit Parallel Interface

The ST7712 identifies various types of the data bus signals according to combinations of RS, E_RD and WR_RW. The signal types are shown as table 7.1.2.

Table 7.1.2 Parallel Data Transfer

Common	68-system		80-system		Description
RS	E	RW	RD	WR	
H	H	H	L	H	Display data read out
H	H	L	H	L	Display data write
L	H	H	L	H	Register status read
L	H	L	H	L	Writes to internal register (instruction)

7.1.2.1 Relation between Data Bus and Gradation Data

ST7712 offers the 65K color display, 262K color display.

When using either 65K or 262K, you can specify color for each of R, G, B by using the palette function.

Use the command ("Entry Mode (03H)" ID[1:0]) for switching between these modes.

(1) 65K color display

1. 8-bit mode

	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
1st write	R4	R3	R2	R1	R0	G5	G4	G3	--	--	--	--	--	--	--	--	--	--
2nd write	G2	G1	G0	B4	B3	B2	B1	B0	--	--	--	--	--	--	--	--	--	--

A single pixel of data is read after the second write operation as shown, and it is written in the display RAM.

"--": Don't care

2 16-bit mode

	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
write	R4	R3	R2	R1	R0	G5	G4	G3	--	G2	G1	G0	B4	B3	B2	B1	B0	--

Data is acquired through signal write operation and then written to the display RAM. "--": Don't care

(2) 262K color display

1. 9-bit mode

	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
1st write	R5	R4	R3	R2	R1	R0	G5	G4	G3	--	--	--	--	--	--	--	--	--
2nd write	G2	G1	G0	B5	B4	B3	B2	B1	B0	--	--	--	--	--	--	--	--	--

A single pixel of data is read after the second write operation as shown, and it is written in the display RAM.

"--": Don't care

2. 18 bit mode

	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Write	R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0

Data is acquired through signal write operation and then written to the display RAM.

7.1.3 Serial Interface

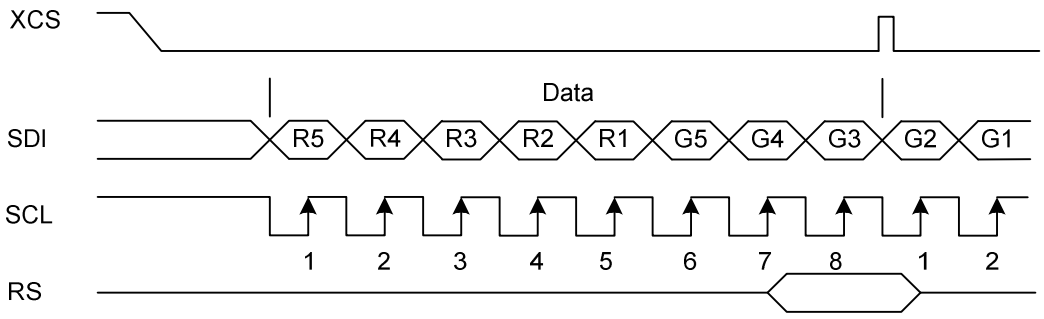
The 4-line serial interface uses four pins XCS, SDI/SDO, SCL, and RS to enter commands and data. Meanwhile, the 3-line serial interface uses three pins XCS, SDI/SDO and SCL for the same purpose.

Data read is not available in the serial interface. Data entered must be 8 bits in 4-line serial interface and 9 bits in 3-line serial interface. Refer to the following chart for entering commands, parameters or gray-scale data.

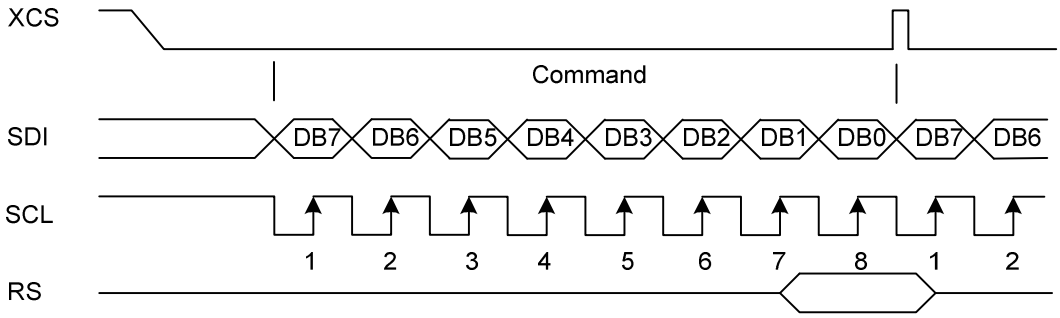
The relation between gray-scale data and data bus in the serial input is the same as that in the parallel interface mode at every gradation.

- 4-line SPI

When entering data (parameters): RS= HIGH at the rising edge of the 8th SCL.

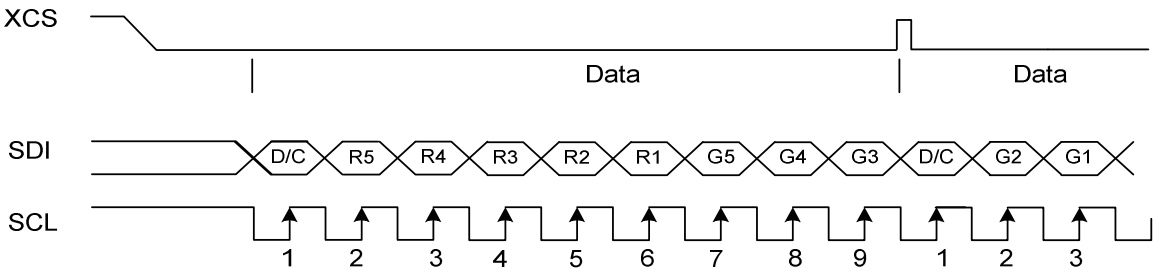


When entering instruction register: RS= LOW at the rising edge of the 8th SCL

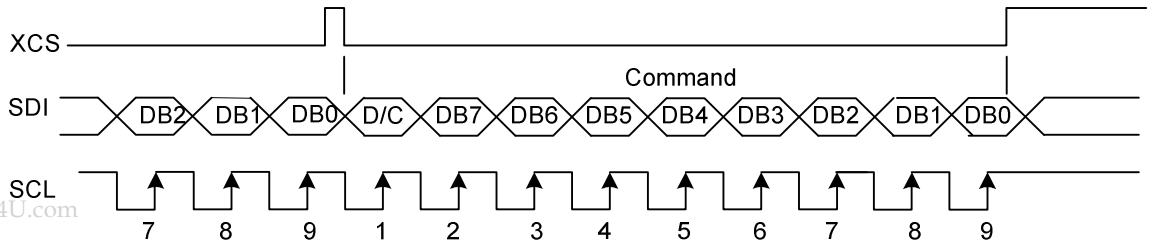


- 3-line SPI

When entering data (parameters): SDI= HIGH at the rising edge of the 1st SCL.



When entering instruction register: SDI= LOW at the rising edge of the 1st SCL.



- If XCS is caused to HIGH before 8 bits from D7 to D0 are entered, the data concerned is invalidated. Before entering succeeding sets of data, you must correctly input the data concerned again.

- In order to avoid data transfer error due to incoming noise, it is recommended to set XCS at HIGH on byte basis to initialize the serial-to-parallel conversion counter and the register.
- When executing the command RAMWR, set XCS to HIGH after writing the last address (after starting the 9th pulse in case of 9-bit serial input or after starting the 8th pulse in case of 8-bit serial input).

7-2 Access to DDRAM and Internal Registers

ST7712 realizes high-speed data transfer because the access from MPU is a sort of pipeline processing done via the bus holder attached to the internal, requiring the cycle time alone without needing the wait time.

For example, when MPU writes data to the DDRAM, the data is once held by the bus holder and then written to the DDRAM before the succeeding write cycle is started. When MPU reads data from the DDRAM, the first read cycle is dummy and the bus holder holds the data read in the dummy cycle, and then it read from the bus holder to the system bus in the succeeding read cycle. Fig. 7.2.1 and Fig 7.2.2 illustrates these relations.

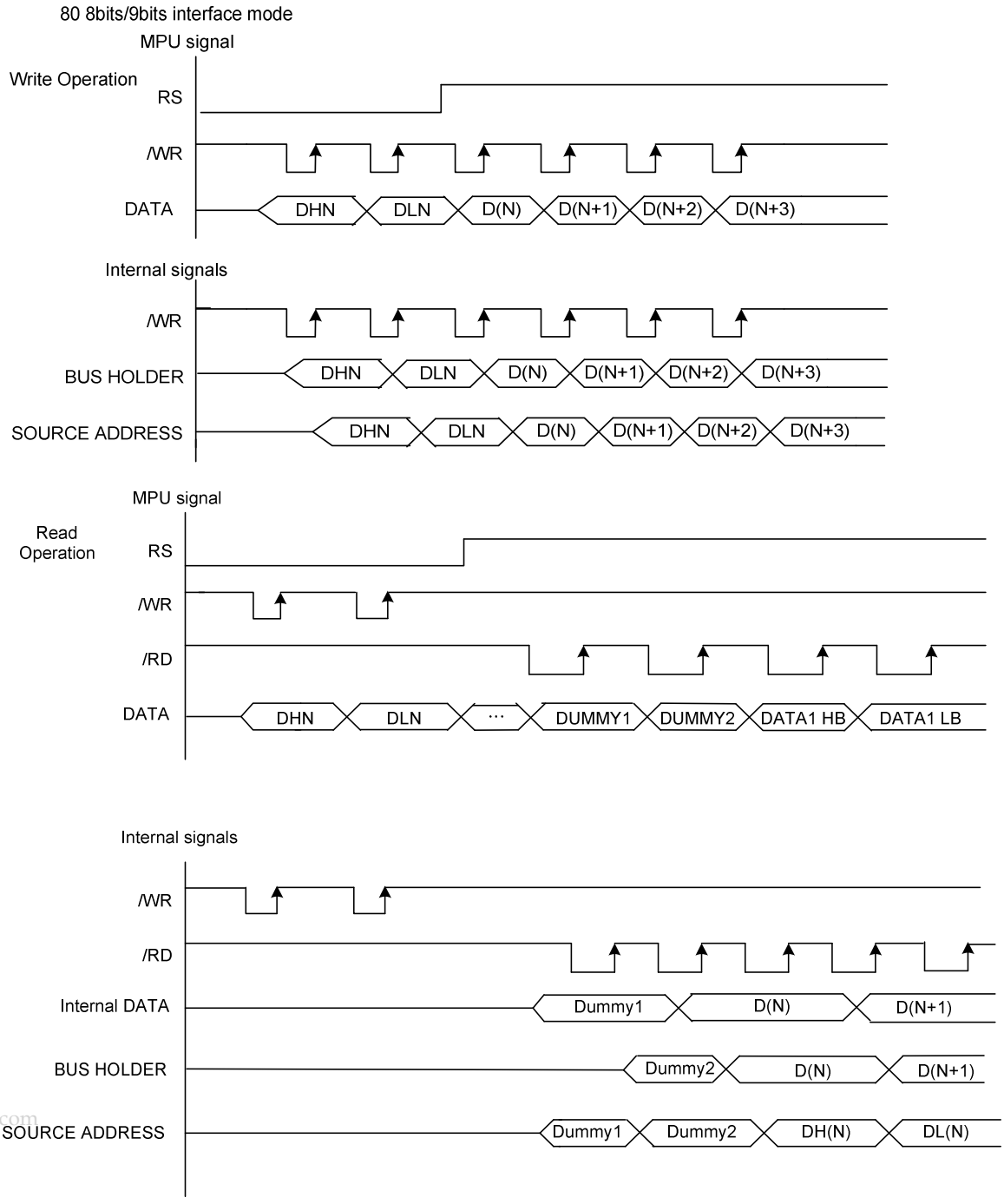


Fig 7.2.1

8080 series 16 bits/18 bits interface mode

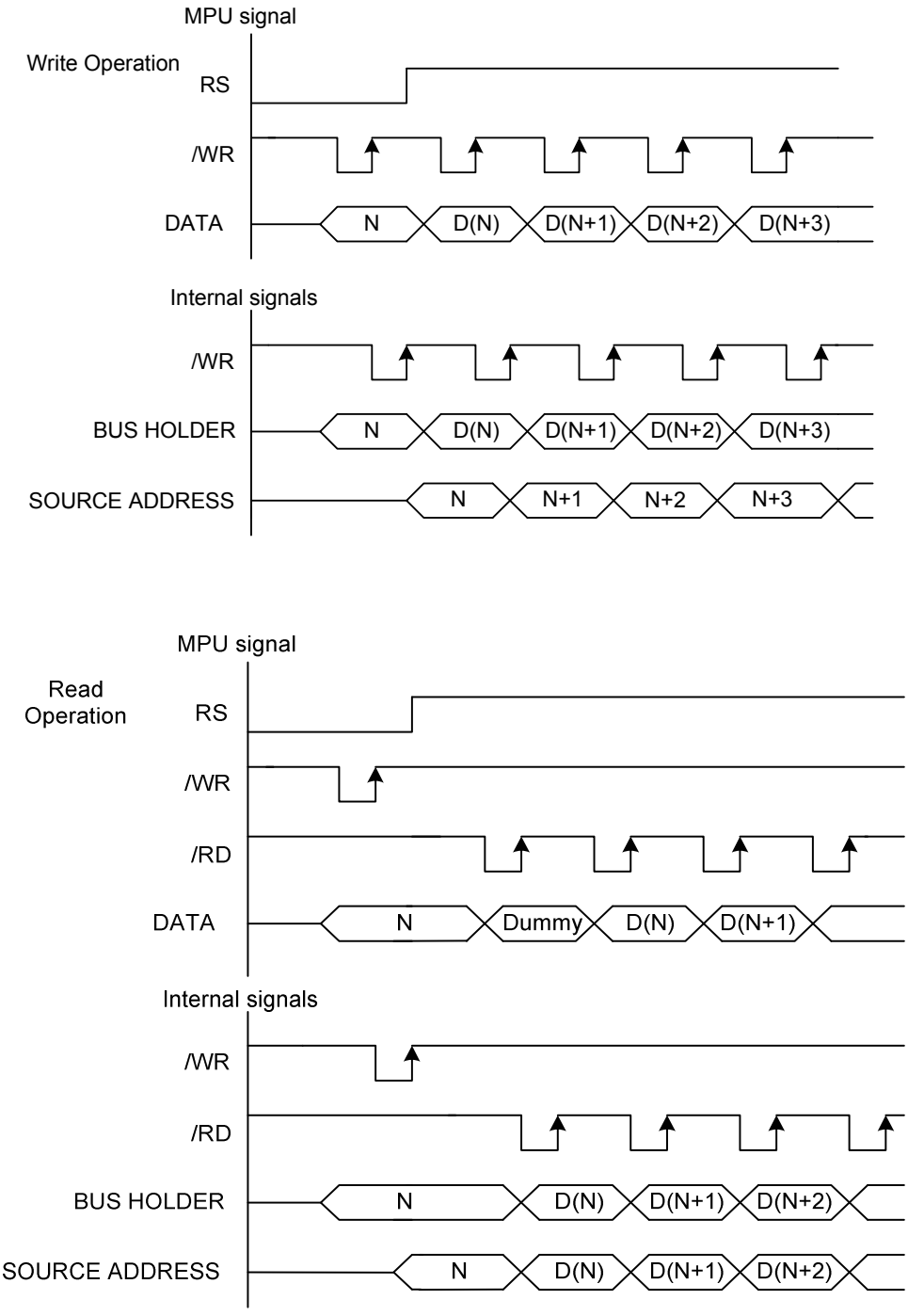
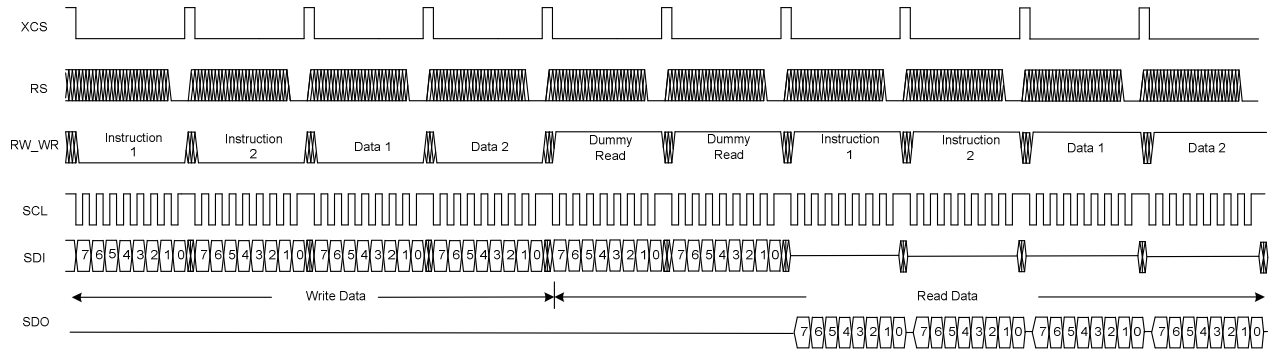
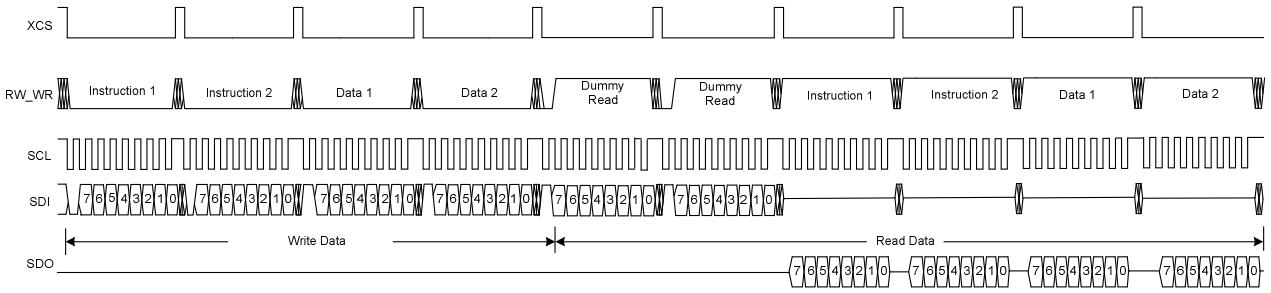


Fig 7.2.2

SPI 4-Line interface mode



SPI 3–Line interface mode



7.3 Display Data RAM (DDRAM)

7.3.1 DDRAM

It is 396 X 132 X 6 bits capacity RAM prepared for storing dot data. You can access a desired bit by specifying the gate address and source address. Since display data from MCU D8 to D0 and D17 to D9 correspond to one or two pixels of RGB, data transfer related restrictions are reduced, realizing the display flexing.

MCU's read and write operations to and from the RAM are performed via the I/O buffer circuit; Reading of the RAM for the liquid crystal drive is controlled from another separate circuit. Refer to the following memory map for the RAM configuration.

- Memory Map (When using the 65Kcolor. 8-bit mode)

RGB alignment												
		Column										
Pixels		0			1					131		
SS=0		**S0**	**S1**	**S2**	**S3**	**S4**	**S5**			**S393**	**S394**	**S395**
Color		R	G	B	R	G	B			R	G	B
Data		D17 D16 D15 D14 D13	D12 D11 D10 D17 D16 D15	D14 D13 D12 D11 D10	D17 D16 D15 D14 D13	D12 D11 D10 D17 D16 D15	D14 D13 D12 D11 D10			D17 D16 D15 D14 D13	D12 D11 D10 D17 D16 D15	D14 D13 D12 D11 D10
Pixels		131			130					0		
SS=1		**S395**	**S394**	**S393**	**S392**	**S391**	**S390**			**S2**	**S1**	**S0**
Color		R	G	B	R	G	B			R	G	B
Data		D17 D16 D15 D14 D13	D12 D11 D10 D17 D16 D15	D14 D13 D12 D11 D10	D17 D16 D15 D14 D13	D12 D11 D10 D17 D16 D15	D14 D13 D12 D11 D10			D17 D16 D15 D14 D13	D12 D11 D10 D17 D16 D15	D14 D13 D12 D11 D10
GS=0	**GS=1**											
0	131											
1	130											
2	129											
3	128											
4	127											
5	126											
6	125											
7	124											
124	7											
125	6											
126	5											
127	4											
128	3											
129	2											
130	1											
131	0											

- Memory Map (When using the 65Kcolor. 16-bit mode)

RGB alignment												
		Column										
Pixels		0			1					131		
SS=0		**S0**	**S1**	**S2**	**S3**	**S4**	**S5**			**S393**	**S394**	**S395**
Color		R	G	B	R	G	B			R	G	B
Data		D17 D16 D15 D14 D13	D12 D11 D10 D8 D7 D6	D5 D4 D3 D2 D1	D17 D16 D15 D14 D13	D12 D11 D10 D8 D7 D6	D5 D4 D3 D2 D1			D17 D16 D15 D14 D13	D12 D11 D10 D8 D7 D6	D5 D4 D3 D2 D1
Pixels		131			130					0		
SS=1		**S395**	**S394**	**S393**	**S392**	**S391**	**S390**			**S2**	**S1**	**S0**
Color		R	G	B	R	G	B			R	G	B
Data		D17 D16 D15 D14 D13	D12 D11 D10 D8 D7 D6	D5 D4 D3 D2 D1	D17 D16 D15 D14 D13	D12 D11 D10 D8 D7 D6	D5 D4 D3 D2 D1			D17 D16 D15 D14 D13	D12 D11 D10 D8 D7 D6	D5 D4 D3 D2 D1
GS=0	**GS=1**											
0	131											
1	130											
2	129											
3	128											
4	127											
5	126											
6	125											
7	124											
124	7											
125	6											
126	5											
127	4											
128	3											
129	2											
130	1											
131	0											

- Memory Map (When using the 262K color. 9-bit mode)

RGB alignment												
		Column										
Pixels		0			1					131		
SS=0		**S0**	**S1**	**S2**	**S3**	**S4**	**S5**			**S393**	**S394**	**S395**
Color		R	G	B	R	G	B			R	G	B
Data		D17	D11	D14	D17	D11	D14			D17	D11	D14
		D16	D10	D13	D16	D10	D13			D16	D10	D13
		D15	D9	D12	D15	D9	D12			D15	D9	D12
		D14	D17	D11	D14	D17	D11			D14	D17	D11
		D13	D16	D10	D13	D16	D10			D13	D16	D10
		D12	D15	D9	D12	D15	D9			D12	D15	D9
Pixels		131			130					0		
SS=1		**S395**	**S394**	**S393**	**S392**	**S391**	**S390**			**S2**	**S1**	**S0**
Color		R	G	B	R	G	B			R	G	B
Data		D17	D11	D14	D17	D11	D14			D17	D11	D14
		D16	D10	D13	D16	D10	D13			D16	D10	D13
		D15	D9	D12	D15	D9	D12			D15	D9	D12
		D14	D17	D11	D14	D17	D11			D14	D17	D11
		D13	D16	D10	D13	D16	D10			D13	D16	D10
GS=0	**GS=1**	D12	D15	D9	D12	D15	D9			D12	D15	D9
0	131											
1	130											
2	129											
3	128											
4	127											
5	126											
6	125											
7	124											
124	7											
125	6											
126	5											
127	4											
128	3											
129	2											
130	1											
131	0											

- Memory Map (When using the 262K color. 18-bit mode)

RGB alignment												
		Column										
Pixels		0			1					131		
SS=0		**S0**	**S1**	**S2**	**S3**	**S4**	**S5**			**S393**	**S394**	**S395**
Color		R	G	B	R	G	B			R	G	B
Data		D17	D11	D5	D17	D11	D5			D17	D11	D5
		D16	D10	D4	D16	D10	D4			D16	D10	D4
		D15	D9	D3	D15	D9	D3			D15	D9	D3
		D14	D8	D2	D14	D8	D2			D14	D8	D2
		D13	D7	D1	D13	D7	D1			D13	D7	D1
		D12	D6	D0	D12	D6	D0			D12	D6	D0
Pixels		131			130					0		
SS=1		**S395**	**S394**	**S393**	**S392**	**S391**	**S390**			**S2**	**S1**	**S0**
Color		R	G	B	R	G	B			R	G	B
Data		D17	D11	D5	D17	D11	D5			D17	D11	D5
		D16	D10	D4	D16	D10	D4			D16	D10	D4
		D15	D9	D3	D15	D9	D3			D15	D9	D3
		D14	D8	D2	D14	D8	D2			D14	D8	D2
		D13	D7	D1	D13	D7	D1			D13	D7	D1
GS=0	**GS=1**	D12	D6	D0	D12	D6	D0			D12	D6	D0
0	131											
1	130											
2	129											
3	128											
4	127											
5	126											
6	125											
7	124											
124	7											
125	6											
126	5											
127	4											
128	3											
129	2											
130	1											
131	0											

7.3.2 Gate Address Control Circuit

This circuit is used to control the address in the gate direction when MPU accesses the DDRAM or when reading the DDRAM to display image on the LCD.

When the gate -direction scan is specified with RAM address command (21H) and the address are incremented from the start up to the end gate, the source address is incremented by 1 and the gate address returns to start page.

The DDRAM supports up to 132 lines, and thus the total gate becomes 132.

In the read operation, as the end gate is reached, the source address is automatically incremented by 1 and the gate address is returned to start gate.

Using the address normal/inverse parameter of Driver output set(01H) command allows you to inverse the correspondence between the DDRAM address and command output.

7.3.3 Source Address Control Circuit

This circuit is used to control the address in the source direction when MPU accesses the DDRAM. You can specify a scope of the source address using source address set command. When the source -direction scan is specified with RAM address command (21H) and the address are incremented from the start up to the end gate, the gate address is incremented by 1 and the column address returns to start source.

In the read operation, too, the gate address is automatically incremented by 1 and returned to start gate as the end source is reached.

Just like the gate address control circuit, using the source address normal/inverse parameter of Driver output set(01H) command enables to inverse the correspondence between the DDRAM source address and segment output. This arrangement relaxes restrictions in the chip layout on the LCD module.

7.3.4 I/O Buffer Circuit

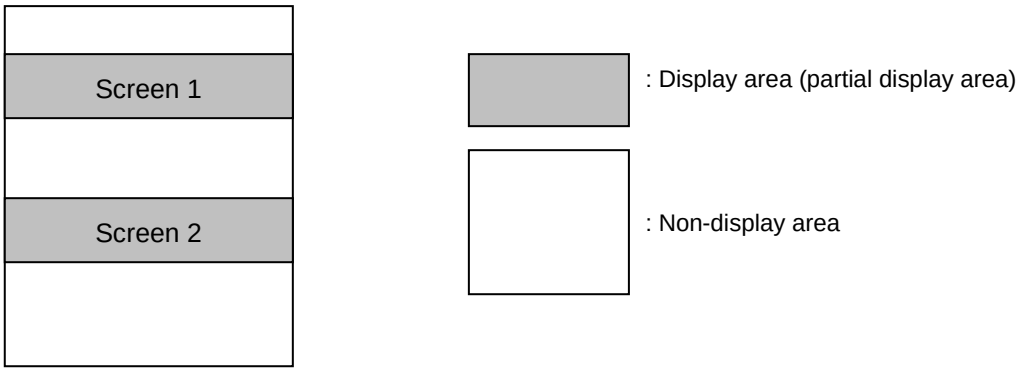
It is the bi-directional buffer used when MCU reads or writes the DDRAM. Since MCU's read or write of DDRAM is performed independently from data output to the display data latch circuit, asynchronous access to the DDRAM white the LCD is turned on does not cause troubles such as flicking of the display images.

7.3.5 Display data Latch Circuit

This circuit is used to temporarily hold display data to be output from the DDRAM to the source line decoder circuit. Since display normal/inverse and display on/off commands are used to control data in the latch circuit alone, they do not modify data in the DDRAM.

7.4 Partial Display

Using partial in command allows you turn on two separated partial display (division by line) of the screen. This mode requires less current consumption than the whole screen display, making it suitable for the equipment in the standby state.

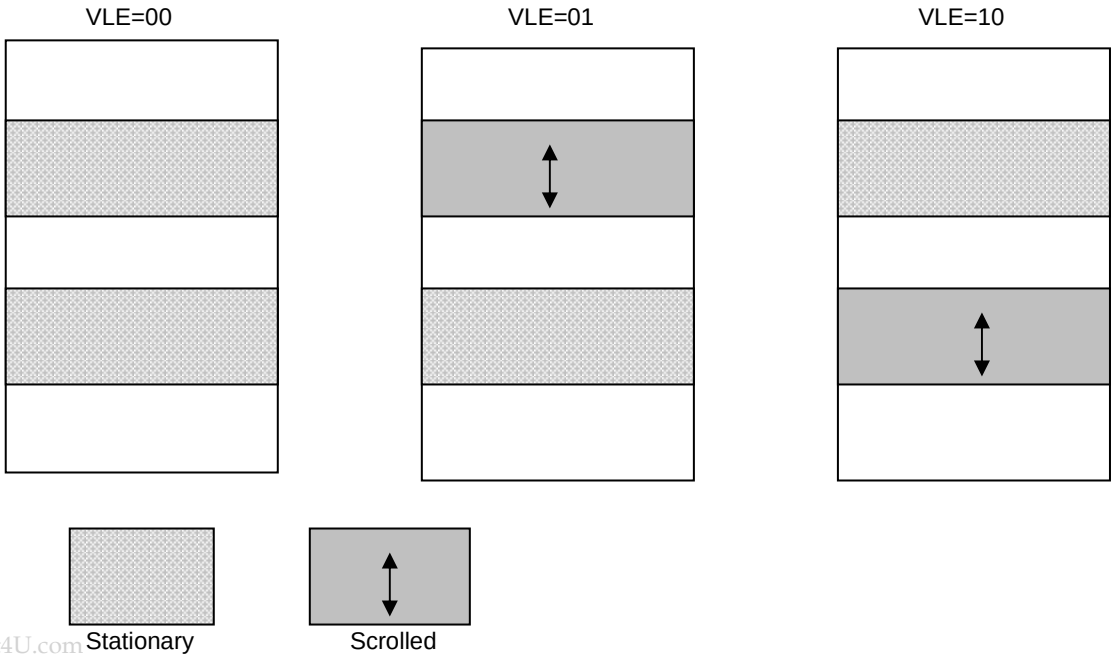


If the partial display region is out of the Max. Display range, it would be no operation.

7.5 Area Scroll Display

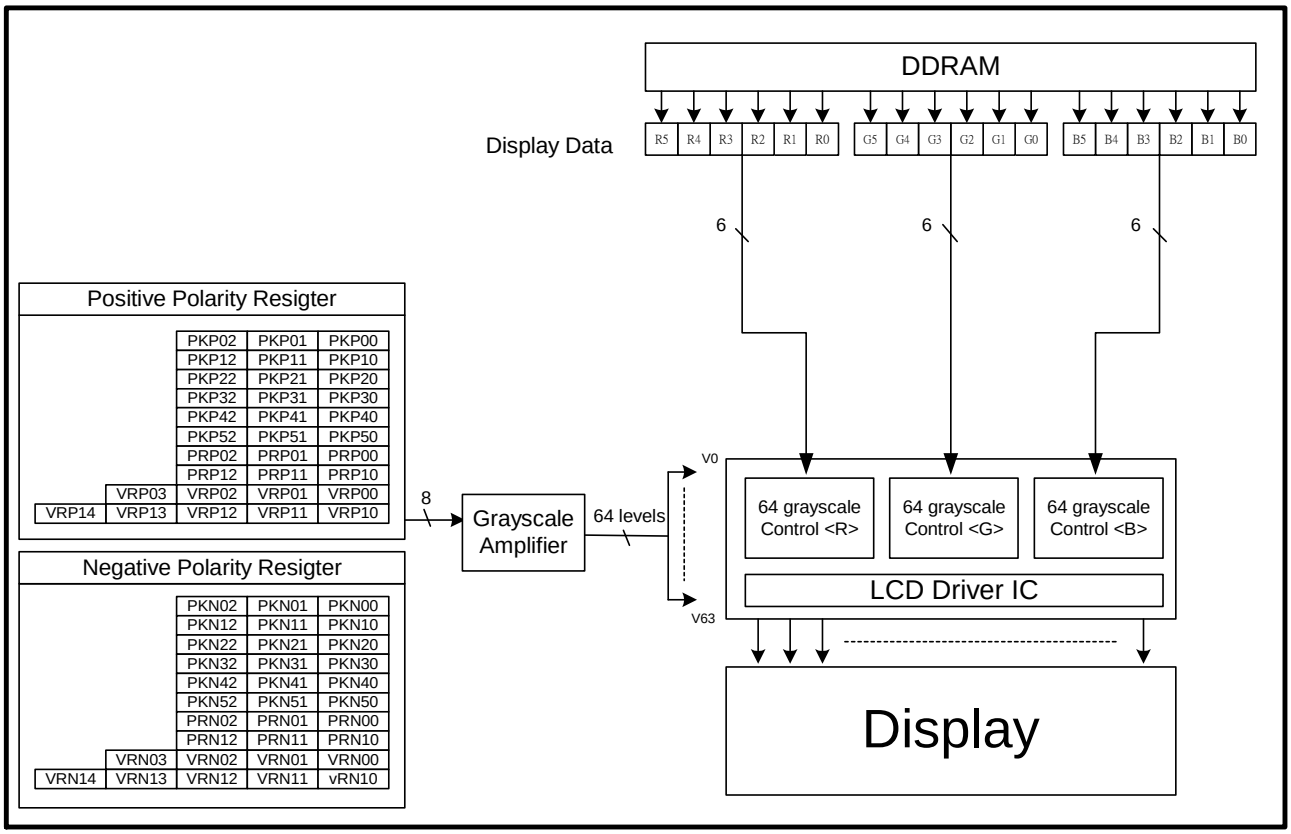
Using the scroll volume set commands (VLE) allows you to scroll the display screen.

You can select screen1 or screen2 to be scrolled with screen scroll enable set commands (VLE). Notice that you can not scroll two screens (screen1 and screen 2) at the same time. Please referred to command “Display control 1 (07H)” and Vertical Scroll Set (41H) for further description.



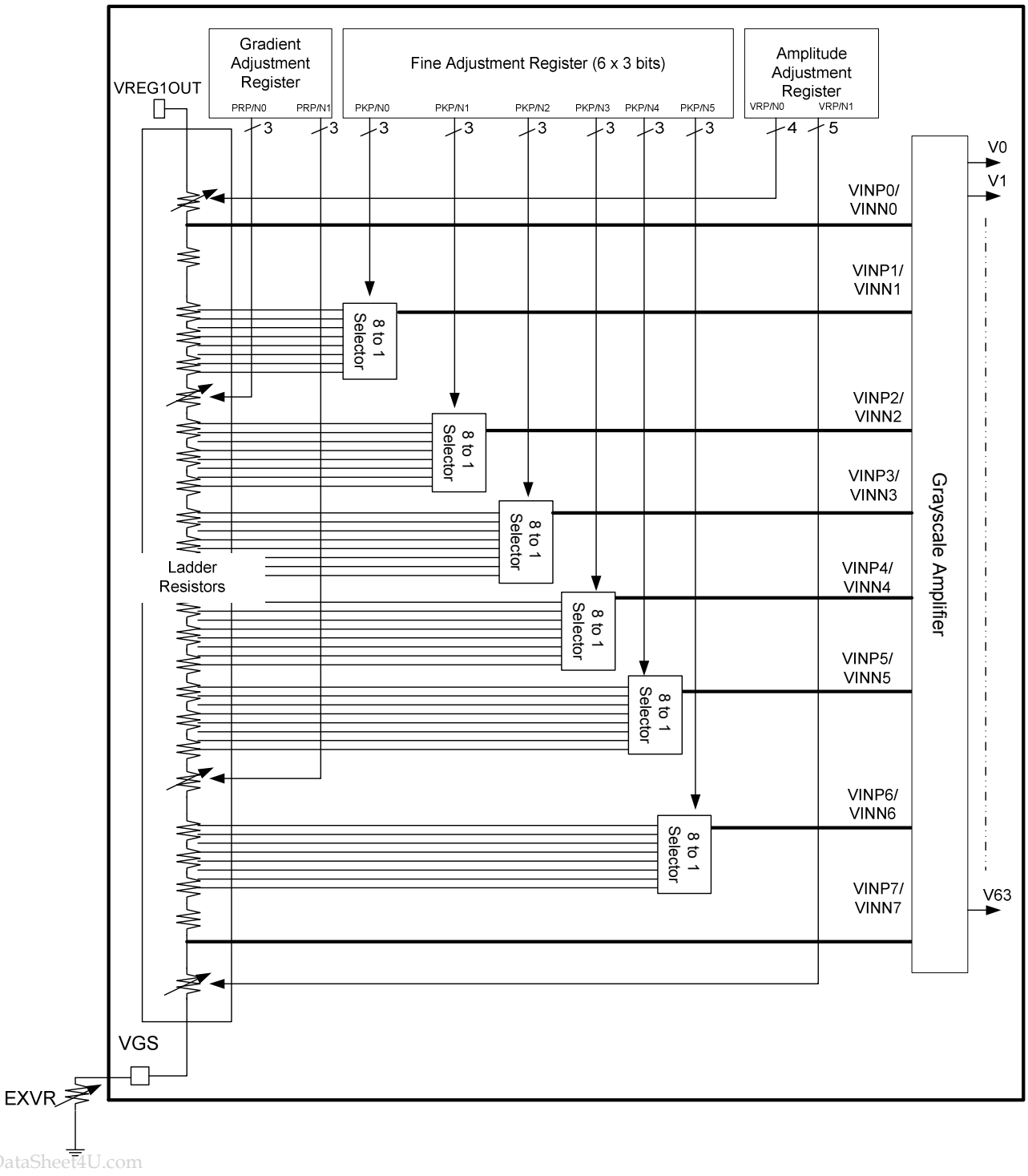
7-6 γ-Correction Function

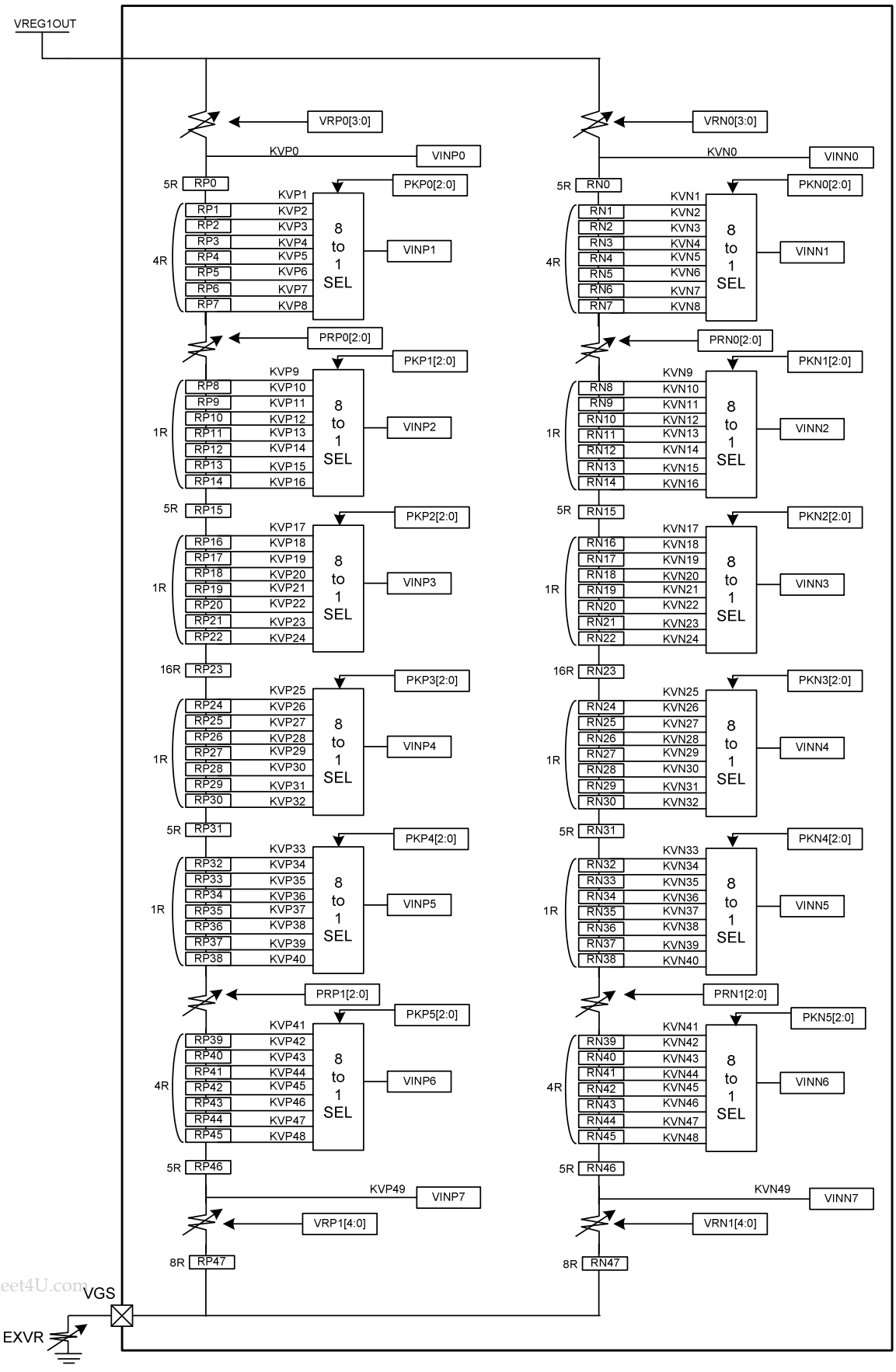
The ST7712 incorporates γ-correction function to display 262K colors simultaneously by 8-level grayscale. The 8-level grayscale is determined by the by the gradient adjustment register and the micro-adjustment register. Select either positive or negative polarity of the registers according to the characteristics of a liquid crystal panel.



7.6.1 Grayscale Amplifier

The eight levels (VIN0 t0 VIN7) of grayscale are determined by gradient adjustment register and the micro-adjustment register. The 8 levels are then divided into 64 levels (V0-63) by the ladder resistors placed between each level. (The structure of the grayscale amplifier is shown as below).

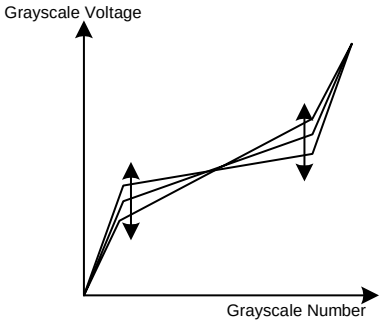




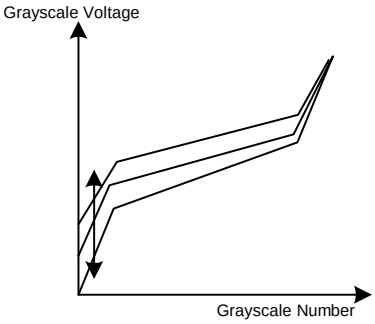
Structure of Ladder / 8 to 1 selector

7.6.2 γ -Adjustment Register

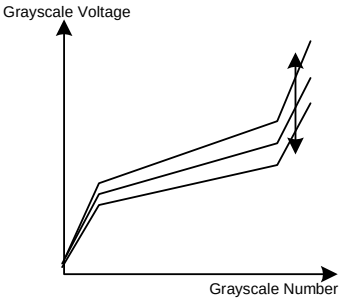
The γ -adjustment registers set an appropriate grayscale voltage for the γ -characteristics of a liquid crystal display. The register group is categorized into the 4-types of register groups to adjust gradient and amplitude on the number of grayscale, the characteristics of the grayscale voltage. Each register can make an independent setting for the positive/negative polarity (the reference value and RGB are common for all registers). The figure below shows the operation of each adjusting register.



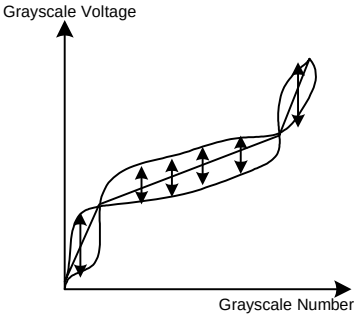
a. Gradient adjustment



b. Amplitude adjustment



c. Reference adjustment



d. Micro adjustment

The Operation of adjusting register

a) Gradient adjustment resistor

The gradient adjustment resistors are used to adjust the gradient in the middle of the grayscale characteristics for the voltage without changing the dynamic range. It controls the variable resistor (VRHP (N) / VRLP (N)) of the ladder resistor for the grayscale voltage generator to achieve the adjustment. Also, there is a separate resistor on the positive and negative polarities in order for corresponding to asymmetry drive.

b) Amplitude adjustment resistor

The Amplitude-adjusting resistor is to adjust amplitude of the grayscale voltage. To accomplish the adjustment, it controls the variable resistor (VRP(N)1) of the ladder resistor for the grayscale voltage generator located at lower side of the ladder resistor.

c) Reference adjustment resistor

The Reference-adjusting resistor is to adjust reference of the grayscale voltage. To accomplish the adjustment, it controls the variable resistor (VRP(N)0) of the ladder resistor for the grayscale voltage generator located at upper side of the ladder resistor.

d) Micro adjustment resistor

The micro adjustment resistor is to make subtle adjustment of the grayscale voltage level. To accomplish the adjustment, it controls the each reference voltage level by the 8 to 1 selector towards the 8-leveled reference voltage generated from the ladder resistor. Also, there is an independent resistor on the positive/negative polarities as well as other adjusting resistors.

γ-correction registers

Register	Positive Polarity	Negative Polarity	Set-up contents
Gradient Adjustment	PRP0[2:0]	PRN0[2:0]	Variable resistor VRHP(N)
	PRP1[2:0]	PRN1[2:0]	Variable resistor VRLP(N)
Amplitude Adjustment	VRP0[3:0]	VRN0[3:0]	Variable resistor VRP(N)0
	VRP1[4:0]	VRN1[4:0]	Variable resistor VRP(N)1
Micro Adjustment	PKP0[2:0]	PKN0[2:0]	The voltage of grayscale number 1 is selected by the 8 to 1 selector
	PKP1[2:0]	PKN1[2:0]	The voltage of grayscale number 8 is selected by the 8 to 1 selector
	PKP3[2:0]	PKN3[2:0]	The voltage of grayscale number 20 is selected by the 8 to 1 selector
	PKP4[2:0]	PKN4[2:0]	The voltage of grayscale number 43 is selected by the 8 to 1 selector
	PKP5[2:0]	PKN5[2:0]	The voltage of grayscale number 55 is selected by the 8 to 1 selector
	PKP6[2:0]	PKN6[2:0]	The voltage of grayscale number 62 is selected by the 8 to 1 selector

7.6.3 Ladder resistors and 8 to 1 Selector

This block outputs the reference voltage of the grayscale voltage. There are two ladder resistors including the variable resistor and the 8 to 1 selector selecting voltage generated by the ladder resistance voltage. The variable and 8 to 1 resistors are controlled by the gamma resistor. Also, there are pins that connect to the external volume resistor and can compensate the variation among the panels.

Variable Resistors

There are 2 types of the variable resistors that is for the gradient adjustment (VRHP (N) / VRLP (N)) and for the oscillation adjustment (VRP (N)0/VRP (N)1). The resistance value is set by the gradient adjusting resistor and the oscillation adjustment resistor as below.

Gradient Adjustment (1)

Register Value PRP(N)0 [2:0]	Resistance Value VRHP(N)
000	0R
001	4R
010	8R
011	12R
100	16R
101	20R
110	24R
111	28R

Gradient Adjustment (2)

Register value PRP(N)1[2:0]	Resistance value VRLP(N)
000	0R
001	4R
010	8R
011	12R
100	16R
101	20R
110	24R
111	28R

Amplitude Adjustment (1)

Register value VRP(N)[3:0]	Resistance value VRP(N)0
0000	0R
0001	2R
0010	4R
: :	: :
1101	26R
1110	28R
1111	30R

Oscillation Adjustment (2)

Register value VRP(N)1[4:0]	Resistance value VRP(N)1
00000	0R
00001	1R
00010	2R
: :	: :
11101	29R
11110	30R
11111	31R

8-to-1 Selector

In the 8-to-1 selector, the voltage level must be selected given by the ladder resistance and the micro-adjusting register and output the voltage the six types of the reference voltage, the VIN1 to VIN6. Following figure explains the relationship between the micro-adjusting register and the selecting voltage.

Relationship between Micro-adjustment Register and Selected Voltage

Register value PKP(N) [2:0]	**Selected voltage**					
	VINP(N)1	**VINP(N)2**	**VINP(N)3**	**VINP(N)4**	**VINP(N)5**	**VINP(N)6**
000	KVP(N)1	KVP(N)9	KVP(N)17	KVP(N)25	KVP(N)33	KVP(N)41
001	KVP(N)2	KVP(N)10	KVP(N)18	KVP(N)26	KVP(N)34	KVP(N)42
010	KVP(N)3	KVP(N)11	KVP(N)19	KVP(N)27	KVP(N)35	KVP(N)43
011	KVP(N)4	KVP(N)12	KVP(N)20	KVP(N)28	KVP(N)36	KVP(N)44
100	KVP(N)5	KVP(N)13	KVP(N)21	KVP(N)29	KVP(N)37	KVP(N)45
101	KVP(N)6	KVP(N)14	KVP(N)22	KVP(N)30	KVP(N)38	KVP(N)46
110	KVP(N)7	KVP(N)15	KVP(N)23	KVP(N)31	KVP(N)39	KVP(N)47
111	KVP(N)8	KVP(N)16	KVP(N)24	KVP(N)32	KVP(N)40	KVP(N)48

γ-Correction Voltage Formula (Positive polarity) --1

Pins	Formula	Micro-adjusting register value	Reference voltage
KVP0	VREG1OUT-ΔV*VRP0/SUMRP	--	VINP0
KVP1	VREG1OUT-ΔV*(VRP0+5R)/SUMRP	PKP02-00 =“000”	VINP1
KVP2	VREG1OUT-ΔV*(VRP0+9R)/SUMRP	PKP02-00=“001”	
KVP3	VREG1OUT-ΔV*(VRP0+13R)/SUMRP	PKP02-00=“010”	
KVP4	VREG1OUT-ΔV*(VRP0+17R)/SUMRP	PKP02-00=“011”	
KVP5	VREG1OUT-ΔV*(VRP0+21R)/SUMRP	PKP02-00=“100”	
KVP6	VREG1OUT-ΔV*(VRP0+25R)/SUMRP	PKP02-00=“101”	
KVP7	VREG1OUT-ΔV*(VRP0+29R)/SUMRP	PKP02-00=“110”	
KVP8	VREG1OUT-ΔV*(VRP0+33R)/SUMRP	PKP02-00=“111”	
KVP9	VREG1OUT-ΔV*(VRP0+33R+VRHP)/SUMRP	PKP12-10 =“000”	VINP2
KVP10	VREG1OUT-ΔV*(VRP0+34R+VRHP)/SUMRP	PKP12-10 =“001”	
KVP11	VREG1OUT-ΔV*(VRP0+35R+VRHP)/SUMRP	PKP12-10 =“010”	
KVP12	VREG1OUT-ΔV*(VRP0+36R+VRHP)/SUMRP	PKP12-10 =“011”	
KVP13	VREG1OUT-ΔV*(VRP0+37R+VRHP)/SUMRP	PKP12-10 =“100”	
KVP14	VREG1OUT-ΔV*(VRP0+38R+VRHP)/SUMRP	PKP12-10 =“101”	
KVP15	VREG1OUT-ΔV*(VRP0+39R+VRHP)/SUMRP	PKP12-10 =“110”	
KVP16	VREG1OUT-ΔV*(VRP0+40R+VRHP)/SUMRP	PKP12-10 =“111”	
KVP17	VREG1OUT-ΔV*(VRP0+45R+VRHP)/SUMRP	PKP22-10 =“000”	VINP3
KVP18	VREG1OUT-ΔV*(VRP0+46R+VRHP)/SUMRP	PKP22-10 =“001”	
KVP19	VREG1OUT-ΔV*(VRP0+47R+VRHP)/SUMRP	PKP22-20 =“010”	
KVP20	VREG1OUT-ΔV*(VRP0+48R+VRHP)/SUMRP	PKP22-20 =“011”	
KVP21	VREG1OUT-ΔV*(VRP0+49R+VRHP)/SUMRP	PKP22-20 =“100”	
KVP22	VREG1OUT-ΔV*(VRP0+50R+VRHP)/SUMRP	PKP22-20 =“101”	
KVP23	VREG1OUT-ΔV*(VRP0+51R+VRHP)/SUMRP	PKP22-20 =“110”	
KVP24	VREG1OUT-ΔV*(VRP0+52R+VRHP)/SUMRP	PKP22-20 =“111”	
KVP25	VREG1OUT-ΔV*(VRP0+68R+VRHP)/SUMRP	PKP32-30 =“000”	VINP4
KVP26	VREG1OUT-ΔV*(VRP0+69R+VRHP)/SUMRP	PKP32-30 =“001”	
KVP27	VREG1OUT-ΔV*(VRP0+70R+VRHP)/SUMRP	PKP32-30 =“010”	
KVP28	VREG1OUT-ΔV*(VRP0+71R+VRHP)/SUMRP	PKP32-30 =“011”	
KVP29	VREG1OUT-ΔV*(VRP0+72R+VRHP)/SUMRP	PKP32-30 =“100”	
KVP30	VREG1OUT-ΔV*(VRP0+73R+VRHP)/SUMRP	PKP32-30 =“101”	
KVP31	VREG1OUT-ΔV*(VRP0+74R+VRHP)/SUMRP	PKP32-30 =“110”	
KVP32	VREG1OUT-ΔV*(VRP0+75R+VRHP)/SUMRP	PKP32-30 =“111”	
KVP33	VREG1OUT-ΔV*(VRP0+80R+VRHP)/SUMRP	PKP42-40 =“000”	VINP5
KVP34	VREG1OUT-ΔV*(VRP0+81R+VRHP)/SUMRP	PKP42-40 =“001”	
KVP35	VREG1OUT-ΔV*(VRP0+82R+VRHP)/SUMRP	PKP42-40 =“010”	
KVP36	VREG1OUT-ΔV*(VRP0+83R+VRHP)/SUMRP	PKP42-40 =“011”	
KVP37	VREG1OUT-ΔV*(VRP0+84R+VRHP)/SUMRP	PKP42-40 =“100”	
KVP38	VREG1OUT-ΔV*(VRP0+85R+VRHP)/SUMRP	PKP42-40 =“101”	
KVP39	VREG1OUT-ΔV*(VRP0+86R+VRHP)/SUMRP	PKP42-40 =“110”	
KVP40	VREG1OUT-ΔV*(VRP0+87R+VRHP)/SUMRP	PKP42-40 =“111”	
KVP41	VREG1OUT-ΔV*(VRP0+87R+VRHP+VRLP)/SUMRP	PKP52-50 =“000”	VINP6
KVP42	VREG1OUT-ΔV*(VRP0+91R+VRHP+VRLP)/SUMRP	PKP52-50 =“001”	
KVP43	VREG1OUT-ΔV*(VRP0+95R+VRHP+VRLP)/SUMRP	PKP52-50 =“010”	
KVP44	VREG1OUT-ΔV*(VRP0+99R+VRHP+VRLP)/SUMRP	PKP52-50 =“011”	
KVP45	VREG1OUT-ΔV*(VRP0+103R+VRHP+VRLP)/SUMRP	PKP52-50 =“100”	
KVP46	VREG1OUT-ΔV*(VRP0+107R+VRHP+VRLP)/SUMRP	PKP52-50 =“101”	
KVP47	VREG1OUT-ΔV*(VRP0+111R+VRHP+VRLP)/SUMRP	PKP52-50 =“110”	
KVP48	VREG1OUT-ΔV*(VRP0+115R+VRHP+VRLP)/SUMRP	PKP52-50 =“111”	
KVP49	VREG1OUT-ΔV*(VRP0+120R+VRHP+VRLP)/SUMRP	--	VINP7

SUMRP: Total of the positive polarity ladder resistance = 128R + VRHP + VRLP + VRP

SUMRN: Total of the negative polarity ladder resistance = 128R + VRHN + VRLN + VRN

ΔV: Potential difference between KV0 and KV49 = VREG1OUT*SUMRP*SUMRN / [SUMRP*SUMRN+EXVR*(SUMRP+SUMRN)]

γ-Correction Voltage Formula (Positive polarity) --2

Voltage of grayscale	Formula	Voltage of grayscale	Formula
V0	VINP0	V32	V43+(V20-V43)*(11/23)
V1	VINP1	V33	V43+(V20-V43)*(10/23)
V2	V3+(V1-V3)*(8/24)	V34	V43+(V20-V43)*(9/23)
V3	V8+(V1-V8)*(450/800)	V35	V43+(V20-V43)*(8/23)
V4	V8+(V3-V8)*(16/24)	V36	V43+(V20-V43)*(7/23)
V5	V8+(V3-V8)*(12/24)	V37	V43+(V20-V43)*(6/23)
V6	V8+(V3-V8)*(8/24)	V38	V43+(V20-V43)*(5/23)
V7	V8+(V3-V8)*(4/24)	V39	V43+(V20-V43)*(4/23)
V8	VINP2	V40	V43+(V20-V43)*(3/23)
V9	V20+(V8-V20)*(22/24)	V41	V43+(V20-V43)*(2/23)
V10	V20+(V8-V20)*(20/24)	V42	V43+(V20-V43)*(1/23)
V11	V20+(V8-V20)*(18/24)	V43	VINP4
V12	V20+(V8-V20)*(16/24)	V44	V55+(V43-V55)*(22/24)
V13	V20+(V8-V20)*(14/24)	V45	V55+(V43-V55)*(20/24)
V14	V20+(V8-V20)*(12/24)	V46	V55+(V43-V55)*(18/24)
V15	V20+(V8-V20)*(10/24)	V47	V55+(V43-V55)*(16/24)
V16	V20+(V8-V20)*(8/24)	V48	V55+(V43-V55)*(14/24)
V17	V20+(V8-V20)*(6/24)	V49	V55+(V43-V55)*(12/24)
V18	V20+(V8-V20)*(4/24)	V50	V55+(V43-V55)*(10/24)
V19	V20+(V8-V20)*(2/24)	V51	V55+(V43-V55)*(8/24)
V20	VINP3	V52	V55+(V43-V55)*(6/24)
V21	V43+(V20-V43)*(22/23)	V53	V55+(V43-V55)*(4/24)
V22	V43+(V20-V43)*(21/23)	V54	V55+(V43-V55)*(2/24)
V23	V43+(V20-V43)*(20/23)	V55	VINP5
V24	V43+(V20-V43)*(19/23)	V56	V60+(V55-V60)*(20/24)
V25	V43+(V20-V43)*(18/23)	V57	V60+(V55-V60)*(16/24)
V26	V43+(V20-V43)*(17/23)	V58	V60+(V55-V60)*(12/24)
V27	V43+(V20-V43)*(16/23)	V59	V60+(V55-V60)*(8/24)
V28	V43+(V20-V43)*(15/23)	V60	V62+(V55-V62)*(350/800)
V29	V43+(V20-V43)*(14/23)	V61	V62+(V60-V62)*(16/24)
V30	V43+(V20-V43)*(13/23)	V62	VINP6
V31	V43+(V20-V43)*(12/23)	V63	VINP7

γ-Correction Voltage Formula (Negative Polarity)--1

Pins	Formula	Micro-adjusting register value	Reference voltage
KVP0	VREG1OUT-ΔV*VRN0/SUMRN	--	VINN0
KVP1	VREG1OUT-ΔV*(VRN0+5R)/SUMRN	PKN02-00 =“000”	VINN1
KVP2	VREG1OUT-ΔV*(VRN0+9R)/SUMRN	PKN02-00=“001”	
KVP3	VREG1OUT-ΔV*(VRN0+13R)/SUMRN	PKN02-00=“010”	
KVP4	VREG1OUT-ΔV*(VRN0+17R)/SUMRN	PKN02-00=“011”	
KVP5	VREG1OUT-ΔV*(VRN0+21R)/SUMRN	PKN02-00=“100”	
KVP6	VREG1OUT-ΔV*(VRN0+25R)/SUMRN	PKN02-00=“101”	
KVP7	VREG1OUT-ΔV*(VRN0+29R)/SUMRN	PKN02-00=“110”	
KVP8	VREG1OUT-ΔV*(VRN0+33R)/SUMRN	PKN02-00=“111”	
KVP9	VREG1OUT-ΔV*(VRN0+33R+VRHP)/SUMRN	PKN12-10 =“000”	VINN2
KVP10	VREG1OUT-ΔV*(VRN0+34R+VRHP)/SUMRN	PKN12-10 =“001”	
KVP11	VREG1OUT-ΔV*(VRN0+35R+VRHP)/SUMRN	PKN12-10 =“010”	
KVP12	VREG1OUT-ΔV*(VRN0+36R+VRHP)/SUMRN	PKN12-10 =“011”	
KVP13	VREG1OUT-ΔV*(VRN0+37R+VRHP)/SUMRN	PKN12-10 =“100”	
KVP14	VREG1OUT-ΔV*(VRN0+38R+VRHP)/SUMRN	PKN12-10 =“101”	
KVP15	VREG1OUT-ΔV*(VRN0+39R+VRHP)/SUMRN	PKN12-10 =“110”	
KVP16	VREG1OUT-ΔV*(VRN0+40R+VRHP)/SUMRN	PKN12-10 =“111”	
KVP17	VREG1OUT-ΔV*(VRN0+45R+VRHP)/SUMRN	PKN22-10 =“000”	VINN3
KVP18	VREG1OUT-ΔV*(VRN0+46R+VRHP)/SUMRN	PKN22-10 =“001”	
KVP19	VREG1OUT-ΔV*(VRN0+47R+VRHP)/SUMRN	PKN22-20 =“010”	
KVP20	VREG1OUT-ΔV*(VRN0+48R+VRHP)/SUMRN	PKN22-20 =“011”	
KVP21	VREG1OUT-ΔV*(VRN0+49R+VRHP)/SUMRN	PKN22-20 =“100”	
KVP22	VREG1OUT-ΔV*(VRN0+50R+VRHP)/SUMRN	PKN22-20 =“101”	
KVP23	VREG1OUT-ΔV*(VRN0+51R+VRHP)/SUMRN	PKN22-20 =“110”	
KVP24	VREG1OUT-ΔV*(VRN0+52R+VRHP)/SUMRN	PKN22-20 =“111”	
KVP25	VREG1OUT-ΔV*(VRN0+68R+VRHP)/SUMRN	PKN32-30 =“000”	VINN4
KVP26	VREG1OUT-ΔV*(VRN0+69R+VRHP)/SUMRN	PKN32-30 =“001”	
KVP27	VREG1OUT-ΔV*(VRN0+70R+VRHP)/SUMRN	PKN32-30 =“010”	
KVP28	VREG1OUT-ΔV*(VRN0+71R+VRHP)/SUMRN	PKN32-30 =“011”	
KVP29	VREG1OUT-ΔV*(VRN0+72R+VRHP)/SUMRN	PKN32-30 =“100”	
KVP30	VREG1OUT-ΔV*(VRN0+73R+VRHP)/SUMRN	PKN32-30 =“101”	
KVP31	VREG1OUT-ΔV*(VRN0+74R+VRHP)/SUMRN	PKN32-30 =“110”	
KVP32	VREG1OUT-ΔV*(VRN0+75R+VRHP)/SUMRN	PKN32-30 =“111”	
KVP33	VREG1OUT-ΔV*(VRN0+80R+VRHP)/SUMRN	PKN42-40 =“000”	VINN5
KVP34	VREG1OUT-ΔV*(VRN0+81R+VRHP)/SUMRN	PKN42-40 =“001”	
KVP35	VREG1OUT-ΔV*(VRN0+82R+VRHP)/SUMRN	PKN42-40 =“010”	
KVP36	VREG1OUT-ΔV*(VRN0+83R+VRHP)/SUMRN	PKN42-40 =“011”	
KVP37	VREG1OUT-ΔV*(VRN0+84R+VRHP)/SUMRN	PKN42-40 =“100”	
KVP38	VREG1OUT-ΔV*(VRN0+85R+VRHP)/SUMRN	PKN42-40 =“101”	
KVP39	VREG1OUT-ΔV*(VRN0+86R+VRHP)/SUMRN	PKN42-40 =“110”	
KVP40	VREG1OUT-ΔV*(VRN0+87R+VRHP)/SUMRN	PKN42-40 =“111”	
KVP41	VREG1OUT-ΔV*(VRN0+87R+VRHP+VRLP)/SUMRN	PKN52-50 =“000”	VINN6
KVP42	VREG1OUT-ΔV*(VRN0+91R+VRHP+VRLP)/SUMRN	PKN52-50 =“001”	
KVP43	VREG1OUT-ΔV*(VRN0+95R+VRHP+VRLP)/SUMRN	PKN52-50 =“010”	
KVP44	VREG1OUT-ΔV*(VRN0+99R+VRHP+VRLP)/SUMRN	PKN52-50 =“011”	
KVP45	VREG1OUT-ΔV*(VRN0+103R+VRHP+VRLP)/SUMRN	PKN52-50 =“100”	
KVP46	VREG1OUT-ΔV*(VRN0+107R+VRHP+VRLP)/SUMRN	PKN52-50 =“101”	
KVP47	VREG1OUT-ΔV*(VRN0+111R+VRHP+VRLP)/SUMRN	PKN52-50 =“110”	
KVP48	VREG1OUT-ΔV*(VRN0+115R+VRHP+VRLP)/SUMRN	PKN52-50 =“111”	
KVP49	VREG1OUT-ΔV*(VRN0+120R+VRHP+VRLP)/SUMRN	--	VINN7

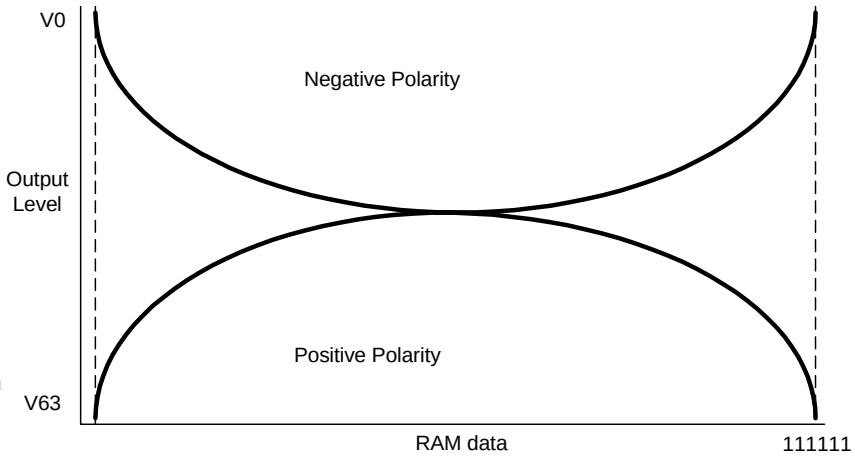
SUMRN: Total of the positive polarity ladder resistance = 128R + VRHP + VRLP + VRN

SUMRN: Total of the negative polarity ladder resistance = 128R + VRHN + VRLN + VRN

ΔV: Potential difference between KV0 and KV49 = VREG1OUT*SUMRP*SUMRN / SUMRP*SUMRN+EXVR*(SUMRP+SUMRN)]

Gamma Voltage Formula (Negative Polarity) --2

Voltage of grayscale	Formula	Voltage of grayscale	Formula
V0	VINN0	V32	V43+(V20-V43)*(11/23)
V1	VINN1	V33	V43+(V20-V43)*(10/23)
V2	V3+(V1-V3)*(8/24)	V34	V43+(V20-V43)*(9/23)
V3	V8+(V1-V8)*(450/800)	V35	V43+(V20-V43)*(8/23)
V4	V8+(V3-V8)*(16/24)	V36	V43+(V20-V43)*(7/23)
V5	V8+(V3-V8)*(12/24)	V37	V43+(V20-V43)*(6/23)
V6	V8+(V3-V8)*(8/24)	V38	V43+(V20-V43)*(5/23)
V7	V8+(V3-V8)*(4/24)	V39	V43+(V20-V43)*(4/23)
V8	VINN2	V40	V43+(V20-V43)*(3/23)
V9	V20+(V8-V20)*(22/24)	V41	V43+(V20-V43)*(2/23)
V10	V20+(V8-V20)*(20/24)	V42	V43+(V20-V43)*(1/23)
V11	V20+(V8-V20)*(18/24)	V43	VINN4
V12	V20+(V8-V20)*(16/24)	V44	V55+(V43-V55)*(22/24)
V13	V20+(V8-V20)*(14/24)	V45	V55+(V43-V55)*(20/24)
V14	V20+(V8-V20)*(12/24)	V46	V55+(V43-V55)*(18/24)
V15	V20+(V8-V20)*(10/24)	V47	V55+(V43-V55)*(16/24)
V16	V20+(V8-V20)*(8/24)	V48	V55+(V43-V55)*(14/24)
V17	V20+(V8-V20)*(6/24)	V49	V55+(V43-V55)*(12/24)
V18	V20+(V8-V20)*(4/24)	V50	V55+(V43-V55)*(10/24)
V19	V20+(V8-V20)*(2/24)	V51	V55+(V43-V55)*(8/24)
V20	VINN3	V52	V55+(V43-V55)*(6/24)
V21	V43+(V20-V43)*(22/23)	V53	V55+(V43-V55)*(4/24)
V22	V43+(V20-V43)*(21/23)	V54	V55+(V43-V55)*(2/24)
V23	V43+(V20-V43)*(20/23)	V55	VINN5
V24	V43+(V20-V43)*(19/23)	V56	V60+(V55-V60)*(20/24)
V25	V43+(V20-V43)*(18/23)	V57	V60+(V55-V60)*(16/24)
V26	V43+(V20-V43)*(17/23)	V58	V60+(V55-V60)*(12/24)
V27	V43+(V20-V43)*(16/23)	V59	V60+(V55-V60)*(8/24)
V28	V43+(V20-V43)*(15/23)	V60	V62+(V55-V62)*(350/800)
V29	V43+(V20-V43)*(14/23)	V61	V62+(V60-V62)*(16/24)
V30	V43+(V20-V43)*(13/23)	V62	VINN6
V31	V43+(V20-V43)*(12/23)	V63	VINN7



Relationship between RAM data and output voltage

7.7 Oscillation circuit

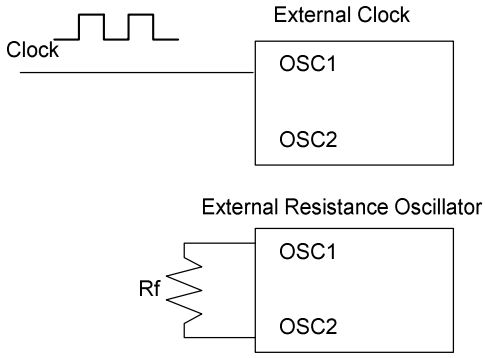
The ST7712 can either use the internal resistor or external resistors to generate the oscillation.

7.7.1 Internal Resistor

The ST7712 can use the on-chip Oscillator without external resistor. When the internal oscillator is used, OSC1 and OSC2 must left open. This oscillator signal is used in the voltage converter and display timing generation circuit.

7.7.2 External Resistor

The ST7712 can oscillate between the OSC1 and OSC2 pins using an internal R-C oscillator with an external oscillation resistor. Note that in R-C oscillation, the oscillation frequency is changed according to the external resistance value, wiring length, or operating power-supply voltage. If Rf is increased or power supply voltage is decrease, the oscillation frequency decreases. For the relationship between Rf resistor value and oscillation frequency, see the Electric Characteristics Notes section.



Notes:

The Rf resistor value should be based on the RC loading of panel and FPC to fine tune Rf value to apparoach the osc frequency that customer need.

7.8 Frame-Frequency Adjustment Function

The ST7712 includes frame frequency adjustment function. While the oscillation frequency is fixed, the frame frequency during the LC drive can be adjusted by the Frame cycle set instruction (0BH) setting (DIV, RTN). Setting the oscillation frequency high in advance allows switching the frame frequency in accordance to the kind of picture to display (i.e. moving/still picture). When displaying a still picture, set the frame frequency low to save power consumption, while setting the frame frequency high for displaying a moving picture which requires high-speed switching of screens.

7.8.1 Relationship between Liquid Crystal Drive Duty and Frame Frequency

The relationship between the liquid crystal drive duty and the frame frequency is calculated by the following formula. The frame frequency is adjusted through the Frame cycle set instruction (0BH) setting with the 1-H period adjustment bit (RTN bit) and the operation clock division bit (DIV bit).

$$\text{Frame frequency} = \frac{fOSC}{\text{Clock cycles per raster-row x division ratio x (Line+BP+FP)}} \text{ [Hz]}$$

fOSC: R-C oscillation frequency
Line: Number of raster-rows (NL bit)
Clock cycles per raster-row: RTN bit
Division ratio: DIV bit
The No. of raster-rows for the front porch: FP
The No. of raster-row for hte back porch: BP

Example calculation

Number of drive raster-rows: 132

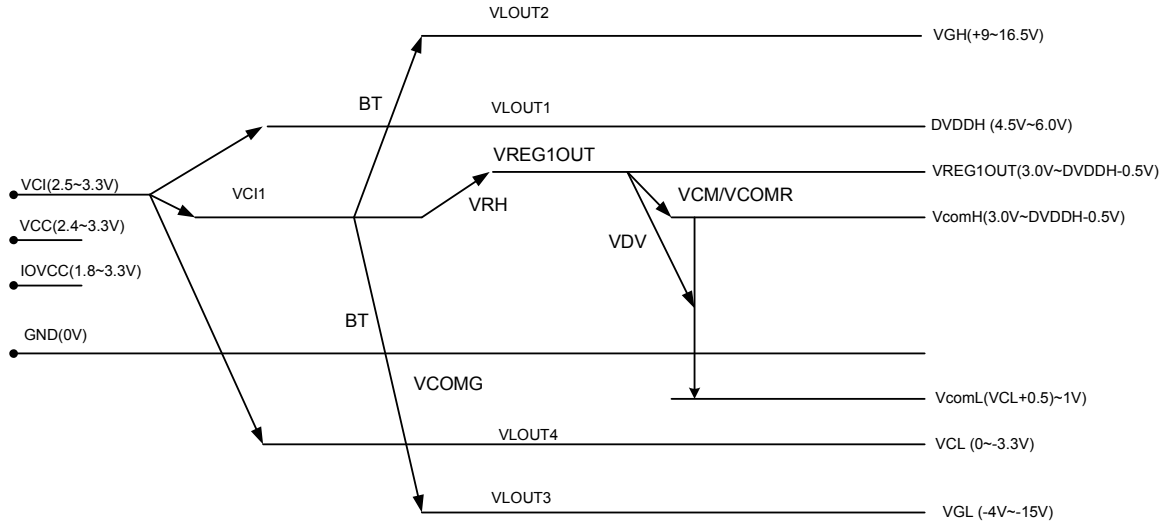
1-H period: 16 clock cycles (RTN3-0 = 0000)

Operation clock division ratio: 1/1

fosc = 60 Hz × (0 + 16) clock × 1/1 × (132 + 16) lines = 142 (kHz)

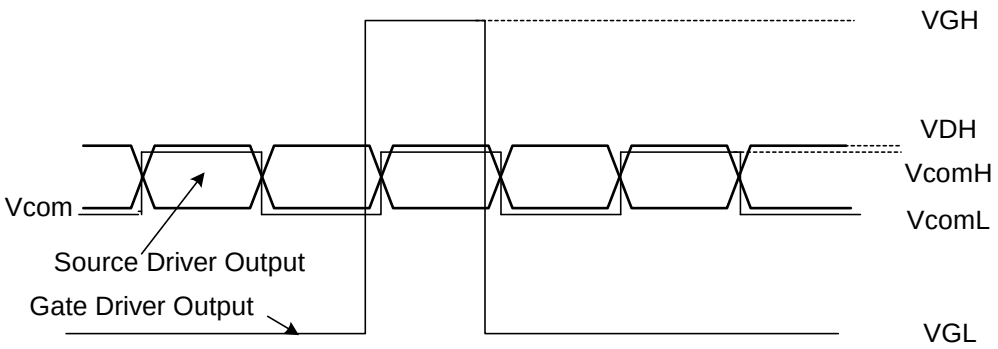
In this case, the R-C oscillation frequency becomes 142 kHz. Adjust the external resistor to the R-C oscillator to 142 kHz.

7.9 Voltage Setting



Note

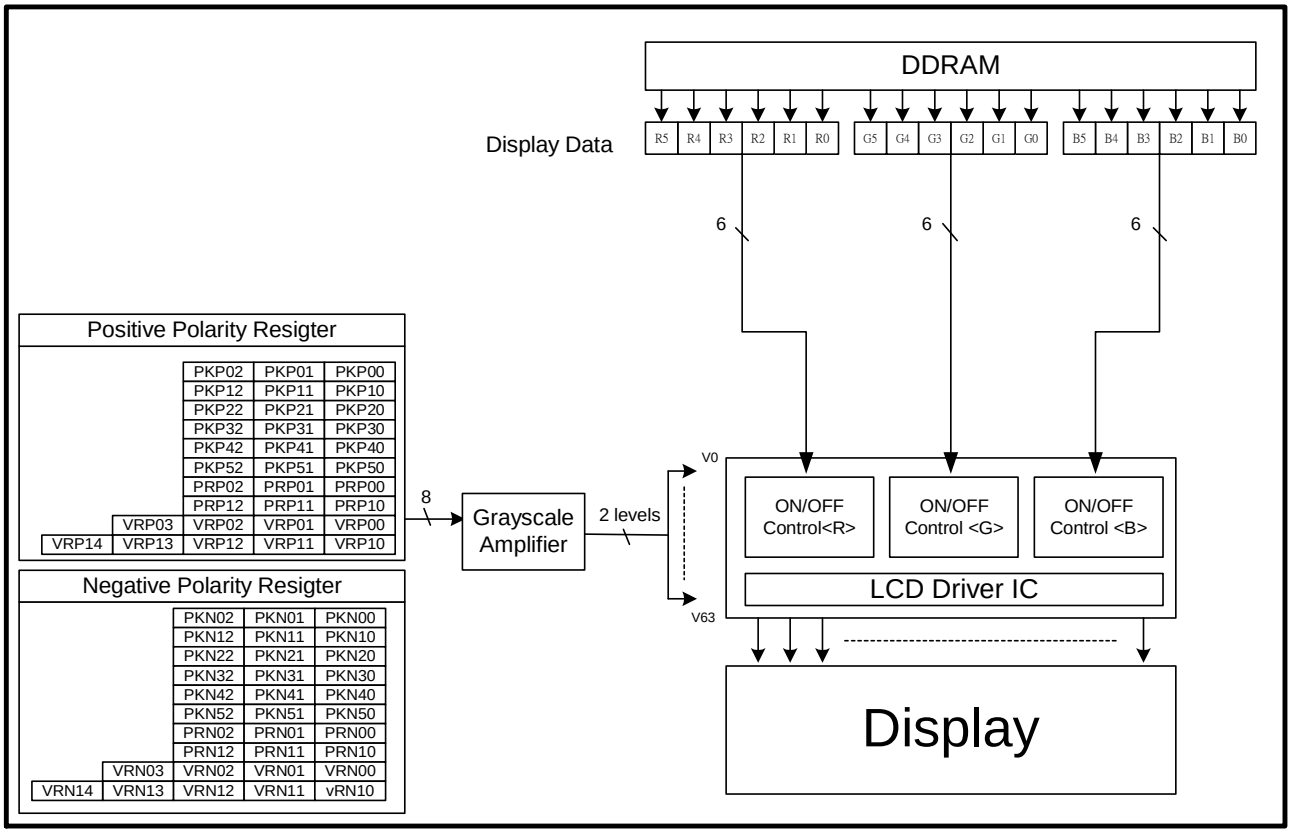
1) the voltage will drop from the set voltage (an ideal voltage) with regard to each DDVDH, VGH, VGL, VCL output due to current consumption. (DDVDH - VREG1OUT) > 0.5V and (VcomL – VCL) > 0.5V show the relationship in relation to the actual voltage. When Vcom alternating frequency is high (e.g. alternation occurs by line), current consumption is also large. In this case, check voltage before use.



Voltage output to TFT LCD

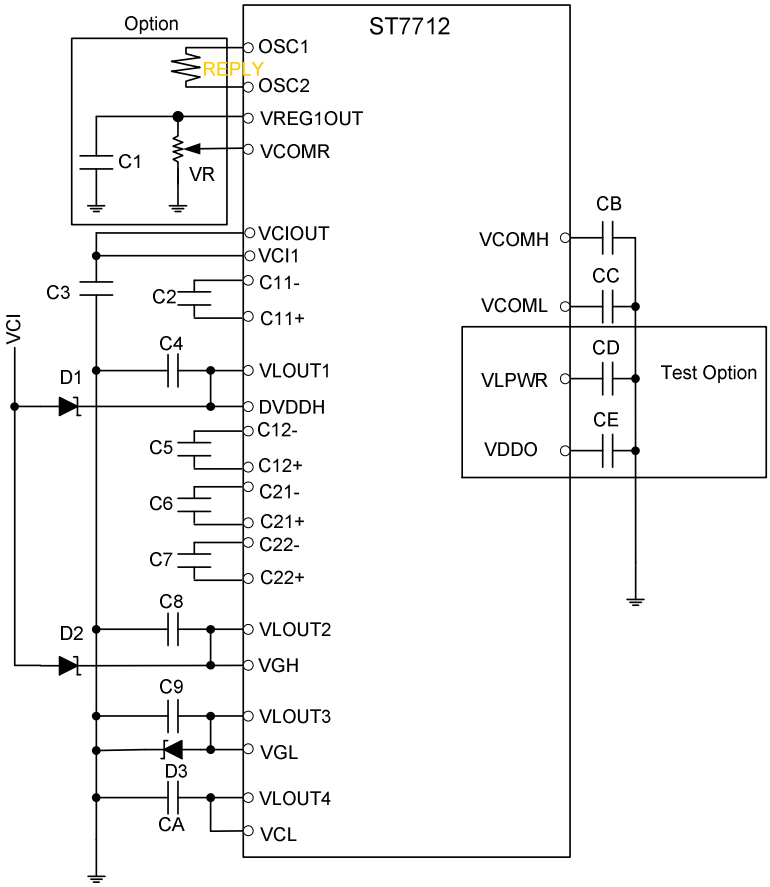
7.10 8-Color Display Mode

The ST7712 incorporates 8-color display mode. Using grayscale levels are V0 and V63 and all other level power supplies are halt. So that it's power consumption will be fewer. Also, during the 8-color mode, the Gamma micro adjustment register, PKP00-PKP52 and PKN00-PKN52 are invalid. Rewrite the data of DDRAM R/G/B to 000000 or 111111 before set the mode. The level power supply (V1-V62) is in OFF condition during the 8-color mode in order to select V0/V63.



7.11 Power Supply Circuit

7.11.1 External Configuration of Power Supply Circuit



Capacitor

Capacity	Recommended voltage	Capacitor No.
1uF	6V	C1, C2, C3, C4, C7, CA, CB, CC, CD, CE
0.1μF~1.0uF	25V	C5, C6, C8, C9

Shot-Key Diode

Feature	Connect Pin.
VF<0.4V/20mA at 25 ℃, VR>=30V	GND-VGL VCI-VGH VCI-DVDDH

Variable resistor

Feature	Connect Pin.
>200KΩ	VcomR

8. Internal Instruction (Command) Data Bus and Register

			MSB								LSB								
	R/W	R/S	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Code
Command	W	0	-	-	-	-	-	-	-	-	-	I[6:0]							
read/write	R	0	*	*	*	*	*	*	*	*	0	*	*	*	*	*	*	*	
Internal OSC	W	1	-	-	-	-	-	-	-	-	-	-	-	RAJ[2:0]			OSCPWR	OSCON	
Resistor selection	R	1	0	1	1	1	0	0	0	1	0	0	1	0	0	0	*	*	00h
Driver Output Set	W	1	-	-	-	-	-	SM	GS	SS	-	-	-	NL[4:0]					01h
LCD Driving Wave Form Set	W	1	-	-	-	-	FLD[1:0]		B/C	EOR	-	-	NW[5:0]						02h
Entry Mode	W	1	-	DFM[1:0]		BGR	-	-	-	-	-	-	ID[1]	ID[0]	AM	ACGO	-	-	03h
Display Control 1	W	1	-	-	-	PT[1:0]		VLE[1:0]		SPT	-	-	GON	DTE	CL	REV	D[1]	D[0]	07h
Display Control 2	W	1	-	-	-	-	FP[3:0]				-	-	-	-	BP[3:0]				08h
Display Control 3	W	1	-	-	-	-	-	-	-	-	-	-	PTG[1:0]		ISC[3:0]				09h
Frame Cycle Set	W	1	NO[1:0]		SDT[1:0]		EQ[1:0]		-	-	-	DIV[2:0]			RTN[3:0]				0Bh
Power Control 1	W	1	-	SAP[2:0]			-	BT[2:0]			-	AP[2:0]			-	DK	SLP	STB	10h
Power Control 2	W	1	-	DC2[2:0]			-	DC1[2:0]			-	DC0[2:0]			-	VC[2:0]			11h
Power Control 3	W	1	-	-	-	-	-	-	-	-	-	-	-	PON	VRH[3:0]				12h
Power Control 4	W	1	-	-	VCOMG	VDV[4:0]					-	VCM[4:0]					VCMF[1:0]		13h
Fuse Set	W	1	-	-	-	-	-	-	-	-	-	-	FSAEN	FSA[4:0]					15h
	R	1	0	0	0	0	0	0	0	0	0	0	*	*	*	*	*	*	
RAM Address Set	W	1	AD[15:0]																21h
Write Data to DDRAM	W	1	Write Data to DDRAM WD[17:0], depend on the selected interface																22h
	R	1	Read Data from DDRAM RD[17:0], depend on the selected interface																
Gamma Control Set	W	1	-	-	-	-	-	PKP1[2:0]			-	-	-	-	-	PKP0[2:0]			30h
	W	1	-	-	-	-	-	PKP3[2:0]			-	-	-	-	-	PKP2[2:0]			31h
	W	1	-	-	-	-	-	PKP5[2:0]			-	-	-	-	-	PKP4[2:0]			32h
	W	1	-	-	-	-	-	PRP1[2:0]			-	-	-	-	-	PRP0[2:0]			33h
	W	1	-	-	-	-	-	PKN1[2:0]			-	-	-	-	-	PKN0[2:0]			34h
	W	1	-	-	-	-	-	PKN3[2:0]			-	-	-	-	-	PKN2[2:0]			35h
	W	1	-	-	-	-	-	PKN5[2:0]			-	-	-	-	-	PKN4[2:0]			36h
	W	1	-	-	-	-	-	PRN1[2:0]			-	-	-	-	-	PRN0[2:0]			37h
	W	1	-	-	-	VRP1[4:0]					-	-	-	-	VRP0[3:0]				38h
	W	1	0	0	0	VRN1[4:0]					-	-	-	-	VRN0[3:0]				39h
Gate Scan Set	W	1	-	-	-	-	-	-	-	-	-	-	-	SCN[4:0]					40h
Vertical Scroll Set	W	1	-	-	-	-	-	-	-	-	VL[7:0]								41h
1st Screen Drive Set	W	1	SE1[7:0]								SS1[7:0]								42h
2nd Screen Drive Set	W	1	SE2[7:0]								SS2[7:0]								43h
Horizontal RAM Address Position	W	1	0	HEA[7:0]							HSA[7:0]								44h
Vertical RAM Address Position	W	1	0	VEA[7:0]							VSA[7:0]								45h

Note

- **Instruction Data Bus and External Data Bus mapping**

  EXT: External Data Bus

  CMD: Internal Instruction Data Bus

- **18,16 Bits Interface**

EXT	D17	16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
CMD	D15	D14	D13	D12	D11	D10	D9	D8	--	D7	D6	D5	D4	D3	D2	D1	D0	--

"--": don't care

- **9,8 Bits Interface**

First Transfer

EXT	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
CMD	D15	D14	D13	D12	D11	D10	D9	D8	--	--	--	--	--	--	--	--	--	--

"--": don't care

Second Transfer

EXT	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
CMD	D7	D6	D5	D4	D3	D2	D1	D0	--	--	--	--	--	--	--	--	--	--

"--": don't care

■ Command read/write (IR)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	0	-	-	-	-	-	-	-	-	-	I[6:0]						
INI		-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0

Write: The index instruction specifies the RAM control indexes (R00h to R45h). It sets the register number from 0000000 to 1111111 in binary form. Don't use the register or instruction bits to which the index is not assigned.

Read: Read instruction reads the internal status of the ST7712.
(**LADDER[7:0]:** Indicate the position of raster-row driving liquid crystal; **I[6:0]:** Read value of the Instruction Register.)

INI: The internal state after resetting of ST7712

■ Internal Register selection (00h)

W/R	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	-	-	-	-	-	-	-	-	-	-	-	RAJ[2:0]			OSCPWR	OSCON
R	1	0	1	1	1	0	0	0	1	0	0	1	0	0	0	*	*
INI		-	-	-	-	-	-	-	-	-	-	-	1	0	0	0	0

Write

RAJ[2:0]: When OSCON=1 and OSCPWR=0, the internal resistor for OSC can be adjusted by setting RAJ[2:0].

RAJ1	RAJ2	RAJ3	internal resistor for OSC
0	0	0	350K
0	0	1	280K
0	1	0	250K
0	1	1	220K
1	0	0	190K (Default value)
1	0	1	170K
1	1	0	160K
1	1	1	120K

Unit(KHz)

OSCPWR: Select Internal or external OSC power and OSC.
When OSCPWR=0, use the internal OSC power and resistor
When OSCPWR=1, use the external OSC power and resistor
OSCON: Turn on or turn off the OSC.
When OSCON=0, OSC OFF
When OSCON=1, OSC ON

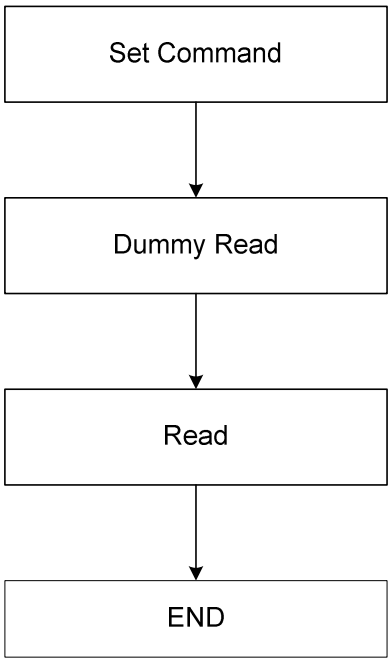
Read

D15-D4: Identify the ST7712. The data read from D15-D4 can tell ST7712 from the other ICs.
D15-D12 fixed to "0111" (07h)
D11-D8 fixed to "0001" (01h)
D7-D4 fixed to "0010" (02h)

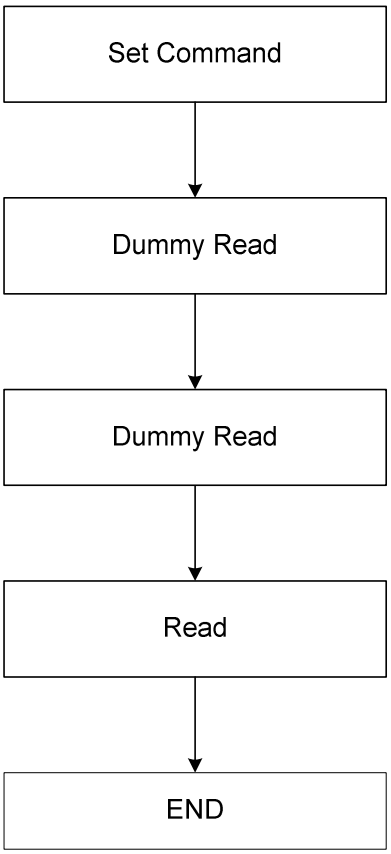
D1 and D0 are read as the status of OSCPWR and OSCON.

Command Read flow chart

18bits and 16 bits interface mode read flow chart



9bit, 8bit and SPI interface mode read flow chart

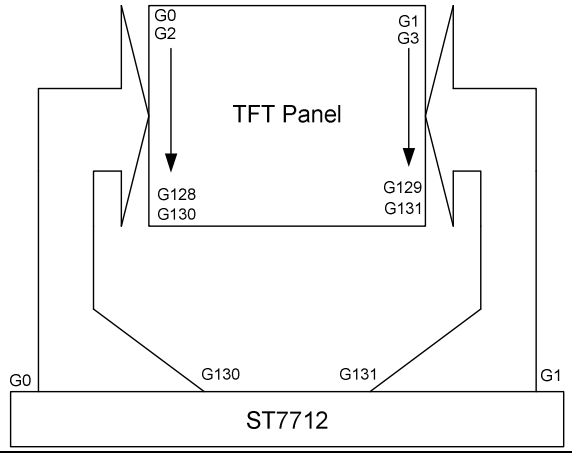
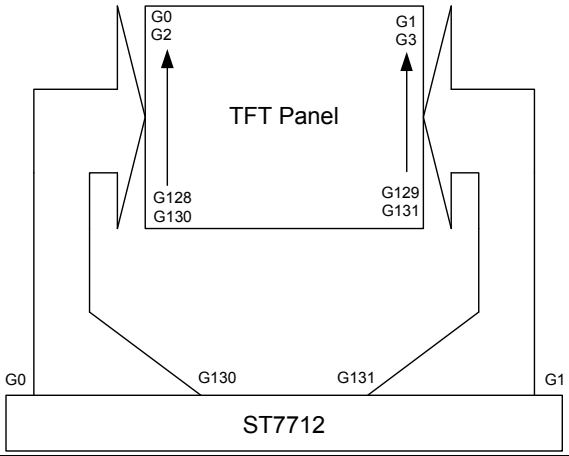


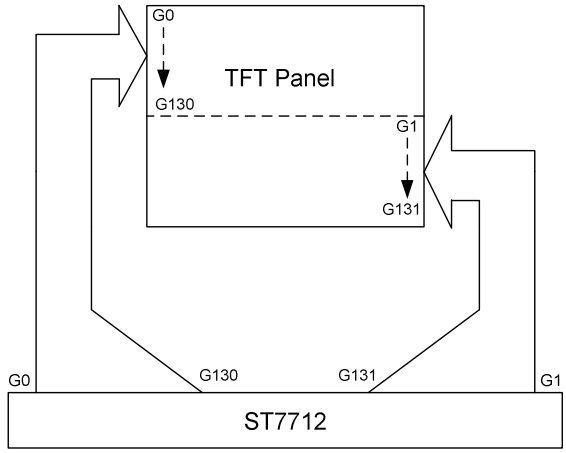
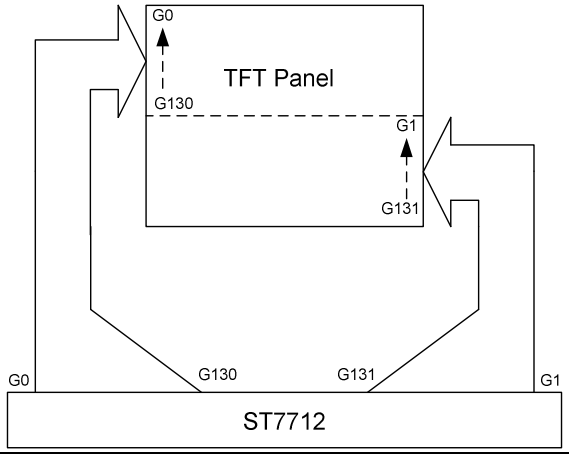
- **Driver Output Set (01h)**

W/R	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	-	-	-	-	-	SM	GS	SS	-	-	-	NL[4:0]				
INI		-	-	-	-	-	0	0	0	-	-	-	1	1	1	0	1

SM: Set the scan order by the gate driver.

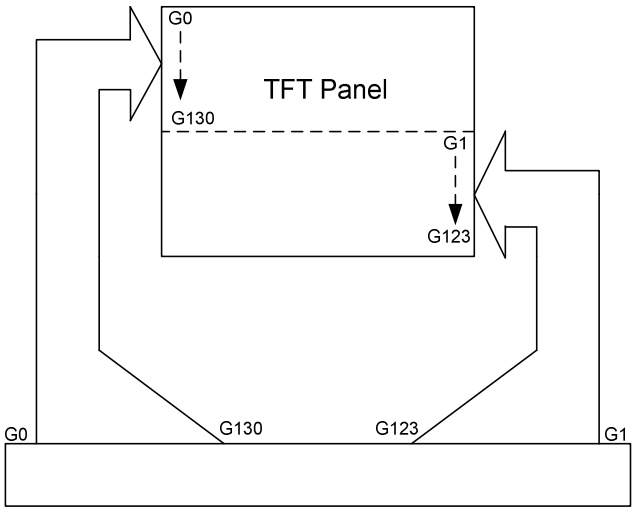
SM	Scan order
0	interlaced gate order
1	cascaded gate order

SM	GS	Scan direction	
0	0		G0,G1,G2,G3….. G129,G130,G131
0	1		G131,G130,G129…. G4,G3,G2,G1

1	0		G0,G2,G4,G6…. G128,G130 G1,G3,G5,G7…. G129,G131
1	1		G0,G2,G4,G6…. G128,G130 G1,G3,G5,G7…. G129,G131

Note: When the cascade function is used (SM=1) with 128X128 resolution, the even side layout of gate line must be starting from G0,G2,…,G130 and the odd side layout of gate line must be starting from G1,G3,..G123.

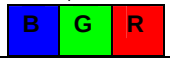
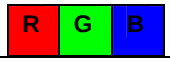
Example: TFT-Panel layout with 128X128 resolution.



GS: Set the shift direction of outputs from the gate driver. When GS=0, G0 shift to G131; when GS=1, G131 shift to G0.

GS	Shift direction
0	Low to High Gate order (G0 to G131)
1	High to Low Gate order (G131 to G0)

SS: Set the shift direction of outputs from the source driver.
When SS=0, S0 shift t0 S395; when SS=1, S395 shift to S0.

SS	Shift direction	Note	
0	Source shift from S0 to S395	SS=0, BGR=0 	SS=0, BGR=1 
1	Source shift from S395 to S0	SS=1, BGR=0 	SS=1. BGR=1 

Note1: When source output channels and Gate output channels of IC are not total occupied, some lines will no display when GS or SS register is changed.

NL[4:0]: Set the number of LCD raster-rows. The DDRAM address mapping is not affected by this setting. Raster-rows number= NL*4+16.
Note: The setting value should be larger than the panel size.

NL4	NL3	NL2	NL1	NL0	LCD raster-rows	Display size	Gate line in use
0	0	0	0	0	16	396x16 dots	G0~G15
0	0	0	0	1	20	396x20 dots	G0~G19
0	0	0	1	0	24	396x24 dots	G0~G23
0	0	0	1	1	28	396x28 dots	G0~G27
0	0	1	0	0	32	396x32 dots	G0~G31
0	0	1	0	1	36	396x36 dots	G0~G35
:	:	:	:	:	:	:	:
1	1	0	1	1	124	396x124 dots	G0~G123
1	1	1	0	0	128	396x128 dots	G0~G127
1	1	1	0	1	132	396x132 dots	G0~G131
1	1	1	1	0	Setting Disable		
1	1	1	1	1			

Note: A front porch (FP) and a back porch period (BP) will be inserted as a blank period area before/after driving all gate lines.

■ LCD Driving Wave Form Set (02h)

W/R	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	-	-	-	-	FLD[1:0]		B/C	EOR	-	-	NW[5:0]					
INI		-	-	-	-	0	1	0	0	-	-	0	0	0	0	0	0

FLD [1:0]: Set the number of fields during n-field interlaced drive.

FLD[1:0]		Number of Fields
0	0	1 field VS when B/C=0 VCOMAC fix at VCOMH B/C=1 VCOMAC fix at VCOML
0	1	1 field
1	0	2 field
1	1	3 field

B/C: When B/C =0, enter the VCOMAC frame inversion mode, means where alternations occur every frame while driving liquid crystal. When B/C=1, enter the VCOMAC n-raster-rows inversion mode.

EOR: When BC=1 and EOR = 1, the odd/even frame-select signals and the n-raster-row reversed signals are EOR (Exclusive-OR) for alternating drive. EOR is used when the LCD is not alternated by combining the set values of the number of the LCD drive raster-row and the n raster-row. When BP and FP setting value is even, set EOR=1 to gain better display quality.

NW[5:0]: Set the number “n” of n-raster-rows VCOMAC inversion (when B/C=”1”)
The number of “n”= NW[5:0]+1 (NW[5:0] sets from 0 to 63)

■ Entry Mode (03h)

W/R	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	-	DFM[1:0]		BGR	-	-	-	-	-	-	ID[1]	ID[0]	AM	ACGO	-	-
INI		-	1	0	0	-	-	-	-	-	-	1	1	0	0	-	-

DFM[1:0]: Decide the data format for the RAM write data transmission.

DFM1	DFM0	Number of Colors
0	0	Setting disable
0	1	Setting disable
1	0	262K color
1	1	65K color

BGR: When BGR=0, the data order write to DDRAM is R, G, B.
When BGR=1, the data write to DDRAM order reverse from R, G, B to B, G, R.

RGB	SEG0	SEG1	SEG2	SEG3	SEG4	SEG5	SEG6	SEG7	…	SEG395
0	R	G	B	R	G	B	R	G	…	B
1	B	G	R	B	G	R	B	G	…	R

Note:
When BGR is used (BGR=1), the read out data of red-pixel and blue-pixel should be exchanged to gain the correct data or the data of red-pixel and blue-pixel are not correct.

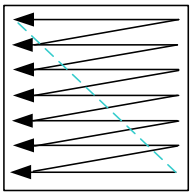
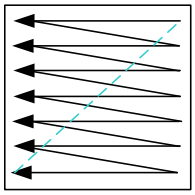
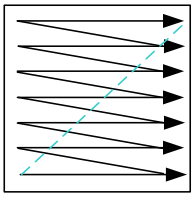
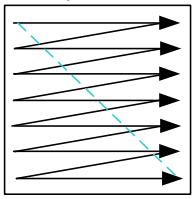
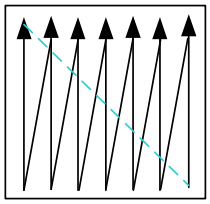
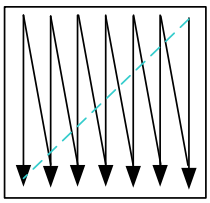
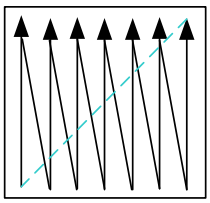
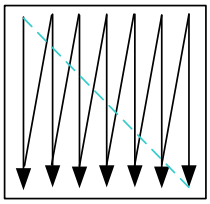
ID[1]: When ID[1]=1, the Address Counter incremented by 1 horizontally.
When ID[1]=0, Address Counter horizontal decremented by 1 horizontally.

ID[0]: When ID[0]=1, the Address Counter incremented by 1 vertically.
When ID[0]=0, Address Counter horizontal decremented by 1 vertically.

Note: The increment/decrement setting of the address counter by ID[1] and ID[0] is performed independently for the upper (AD15-8) and lower (AD7-0) addresses. The AM bit sets the direction of moving through the addresses when the DDRAM is written.

AM: When AM = “0”, the address counter is updated in the horizontal direction after data are written to DDRAM.
When AM = “1”, the address counter is updated in the vertical direction after data are written to DDRAM.

When the window address is specified, data are written to the DDRAM area specified by the window address in the manner specified with ID[1] ,ID[0] ,and AM settings.

	ID[1]=0; ID[0]=0 H: decrement V: decrement	ID[1]=0; ID[0]=1 H: increment V: increment	ID[1]=1; ID[0]=0 H: decrement V: increment	ID[1]=1; ID[0]=1 H: increment V: increment
AM=0 Horizontal	(00h,00h)  (83h,83h)	(00h,00h)  (83h,83h)	(00h,00h)  (83h,83h)	(00h,00h)  (83h,83h)
AM=1 Vertical	(00h,00h)  (83h,83h)	(00h,00h)  (83h,83h)	(00h,00h)  (83h,83h)	(00h,00h)  (83h,83h)

Note: When changing the setting of ID[1-0] value, please set the RAM address set command(21h) again.
Example:
Panel resolution is 132X132 AM=0, ID[1-0]=00, RAM address set command (21h) is 83h,83h

WR	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	1	0	0	0	0	0	1	1	1	0	0	0	0	0	1	1

ACGO: Decide the Address Counter will update after data are written to the DDRAM automatically or not.
When ACGO=0, AC updates after data are written to the DDRAM area.
When ACGO=1, AC doesn't change (keep on the AD value which be set) after data are written to or read from DDRAM area.

ACGO	AC status
0	AC update
1	AC keep AD value

■ Power up (04h)

W/R	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	-	-	-	-	-	-	-	-	0	0	0	0	0	0	UP	0
INI		-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0

UP： Help analog circuit stability of IC when IC turn on moment to avoid abnormal display. After analog voltage stable, must turn off this function.

UP	UP status
0	Turn OFF
1	Turn ON

■ Display Control 1 (07h)

W/R	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	-	-	-	PT[1:0]		VLE[1:0]		SPT	-	-	GON	DTE	CL	REV	D[1]	D[0]
INI		-	-	-	0	0	0	0	0	-	-	0	0	0	1	0	0

PT[1:0]: Decide the source output voltage in the non-display area when entry the partial display mode.

PT[1:0]		Positive Polarity	Negative Polarity
0	0	V63	V0
0	1	V63	V0
1	0	GND	GND
1	1	Hi-Z	Hi-Z

VLE[1:0]: When VLE[0] = 1, the first screen is scrolled in the vertical direction; when VLE[1] = 1, the second screen is scrolled in the vertical direction. Note: The first and second screens can't be scrolled at the same time.

VLE[1]	VLE[0]	Scree2	Screen1
0	0	Stationary	Stationary
0	1	Stationary	Scrolled
1	0	Scrolled	Stationary
1	1	Setting disabled	

SPT: When SPT=0, liquid crystal is one screen.
When SPT = 1, liquid crystal is driven with 2 split screens.

GON: When GON = 0, the gate-on level is VGH, and the gate-off level is GND.
When GOC=1, the gate-on level is VGH, and the gate-off level is VGL.

DTE: When DTE=0, the DISPTMG is fixed to GND, and when DTE=1, the DISPTMG is output operation.

CL: When CL = 1, entry the 8-color display mode. RAM data format have to redefine before writing into IC RAM to avoid abnormal display. CL=0: 262K color; CL=1: 8 color

8 color mode data format:

Pattern	REV=1	REV=0
Black	000000,000000,000000	111111,111111,111111
White	111111,111111,111111	000000,000000,000000
Red	111111,000000,000000	000000,111111,111111
Green	000000,111111,000000	111111,000000,111111
Blue	000000,000000,111111	111111,111111,000000
Yellow	111111,111111,000000	000000,000000,111111
Magenta	111111,000000,111111	000000,1111111,000000
Cyan	000000,111111,111111	111111,000000,000000

REV: When REV=0, the display is normal in display area; when REV = 1, the display entries reverse mode in display area. Normally white or normally black panels can be controlled by the grayscale level inversion without changing the data.

REV	DDRAM Data	Positive Polarity	Negative Polarity
0	000000 : 111111	V63 : V0	V0 : V63
1	000000 : 111111	V0 : V63	V63 : V0

D[1]/ D[0]: Display is on when D[1] = 1 and off when D[1] = 0. When off, the display data remains in the DDRAM, and can be displayed instantly by setting D[1] = 1. When D[1]= 0, the display is off with the entire source outputs set to the GND level. By this function, ST7712 can control the charging current for the LCD with AC driving. Control the display on/off while control GON and DTE. When D[1]=0 and D[0]=1, the internal display of ST7712 performed although the display is off. When D[1]=0 and D[0]=0, the internal display operation halts and the display is off.

D[1]	D[0]	Source Output	Internal operation	Gate-Driver Control Signals
0	0	GND	Halt	Halt
0	1	GND	Operate	Operate
1	0	Non-lit display	Operate	Operate
1	1	Display	Operate	Operate

Note: 1. Write from the microcomputer to the DDRAM is independent from D[1] and D[0].
2. In sleep and standby mode, D[1]=0 D[0]=0. However, the register contents of D[1] and D[0] are not modified.

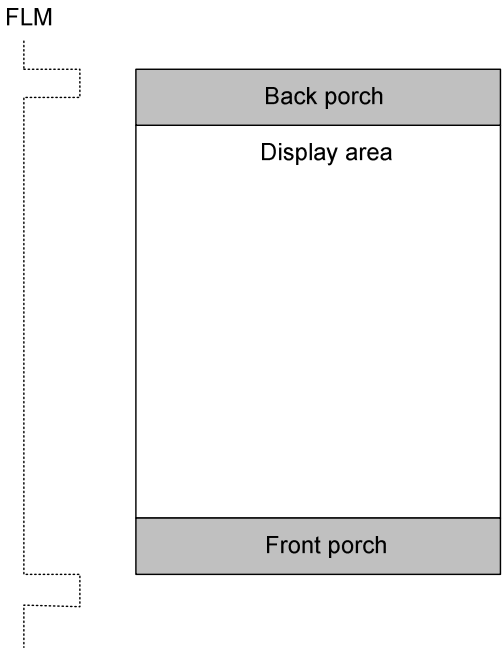
■ Display Control 2 (08h)

W/R	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	-	-	-	-	FP[3:0]				-	-	-	-	BP[3:0]			
INI		-	-	-	-	1	0	1	0	-	-	-	-	0	0	1	0

FP[3:0]/ BP[3:0]: Setting the blank display area (the front porch and the back porch). The front porch is placed at the beginning of the display and the back porch is placed at the end of the display.
FP[3:0] and BP[3:0] bits specify the number of raster-rows for the front and back porches respectively.
When making this setting, make sure that BP + FP ≤ 16 raster-rows, FP ≥ 1 raster-rows, and BP ≥ 0 raster-rows.

FP3	FP2	FP1	FP0	Number of lines for the Front Porch
0	0	0	0	Setting disable
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8
1	0	0	1	9
1	0	1	0	10
1	0	1	1	11
1	1	0	0	12
1	1	0	1	13
1	1	1	0	14
1	1	1	1	Setting disable
BP3	BP2	BP1	BP0	Number of lines for the Back Porch
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8
1	0	0	1	9
1	0	1	0	10

1	0	1	1	11
1	1	0	0	12
1	1	0	1	13
1	1	1	0	14
1	1	1	1	Setting disable



■ **Display Control 3 (09h)**

W/R	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	-	-	-	-	-	-	-	-	-	-	PTG[1:0]		ISC[3:0]			
INI		-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0

PTG[1:0]: Set the mode of scanning gate lines when non-display area is driven.

PTG[1]	PTG[0]	Gate output in non display area
0	0	Normal scan
0	1	Fixed VGL
1	0	Interval scan
1	1	Setting disable

ISC[3:0]: Set the cycle to scan gate lines. When PTG bits set the scan mode in the non-display area to the interval scan mode, the scan cycle is always odd number of frames, and polarity inversion is applied each timing when gate lines are scanned.

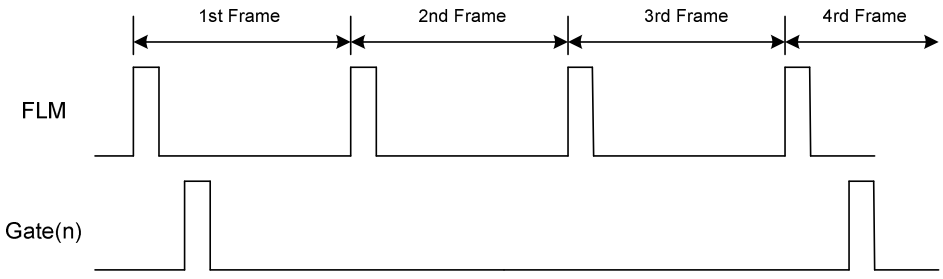
Note:

1. When PTG is set to "Normal Scan", the source output in non-display area should be set to "V63-V0" (PT=0 or 1) to avoid flicker effect.
2. When PTG is set to "Fixed VGL" and "Interval Scan", the source output in non-display area should be set to "GND" (PT=2) to avoid data leakage.

ISC3	ISC2	ISC1	ISC0	Scan cycle (Scan cycle=ISC*2+1)
0	0	0	0	0
0	0	0	1	3
0	0	1	0	5
0	0	1	1	7
0	1	0	0	9
0	1	0	1	11
0	1	1	0	13
0	1	1	1	15
1	0	0	0	17
1	0	0	1	19
1	0	1	0	21
1	0	1	1	23
1	1	0	0	25
1	1	0	1	27
1	1	1	0	29
1	1	1	1	31

Example:

Interval scan: Scan cycle=3.



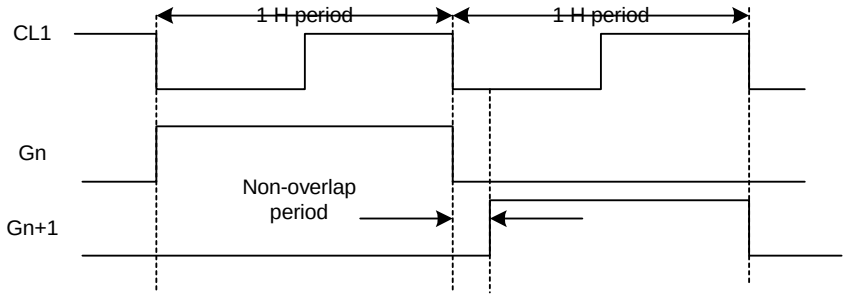
■ Frame Cycle Set (0Bh)

W/R	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	NO[1:0]		SDT[1:0]		EQ[1:0]		EQPW[1:0]		-	DIV[2:0]			RTN[3:0]			
INI		0	0	0	0	0	0	0	0	-	0	0	0	0	0	0	0

NO[1:0]: Set the non-overlap width of gate output

NO1	NO0	Non-overlap width
0	0	0 clocks
0	1	4 clocks
1	0	6 clocks
1	1	8 clocks

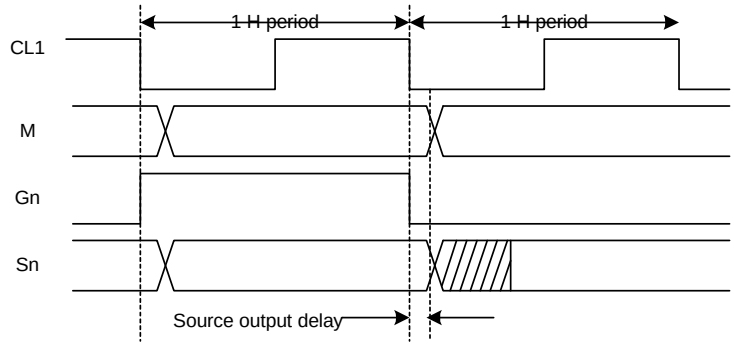
Note: The amount of non-overlap width is defined from the falling edge of the CL1.



SDT[1:0]: Specify the delay time for the source output from the falling edge of the gate output.

SDT1	SDT0	Delay time for source output
0	0	disable
0	1	2 clocks
1	0	3 clocks
1	1	4 clocks

Note: The delay time for the source output is measured from the falling edge of the CL1.



EQ[1:0]: EQ period is sustained for the number of clock cycle which is set on EQ[1:0].

EQ1	EQ0	
0	0	No EQ
0	1	1 clocks
1	0	2 clocks
1	1	3 clocks

EQPW[1:0]: Decide the source output voltage in the equalized area.

EQPW[1:0]		Positive Polarity	Negative Polarity
0	0	V0	V63
0	1	V63	V0
1	0	GND	GND
1	1	Hi-Z	Hi-Z

DIV[2:0]: Set the division ratio of clocks for internal operations. Internal operations are in synchronization with the clock, the frequency of which is divided according to the DIV[2:0] setting. Frame frequency can be adjusted in combination with the adjustment of 1H period (RTN [3:0]). When changing the number of drive raster-rows, adjust the frame frequency too. For details, see “Frame Frequency Adjustment Function”.

DIV2	DIV1	DIV0	Division Ratio	Internal Operating Clock Frequency
0	0	0	1	fosc/1
0	0	1	2	fosc/2
0	1	0	4	fosc/4
0	1	1	8	fosc/8
1	0	0	3	fosc/3
1	0	1	5	fosc/5
1	1	0	6	fosc/6
1	1	1	7	fosc/7

RTN[3:0]: Set the clock cycles per raster-row

RTN3	RTN2	RTN1	RTN0	clock cycles per raster-row
0	0	0	0	16 clocks
0	0	0	1	17 clocks
0	0	1	0	18 clocks
0	0	1	1	19 clocks
0	1	0	0	20 clocks
0	1	0	1	21 clocks
0	1	1	0	22 clocks
0	1	1	1	23 clocks
1	0	0	0	24 clocks
1	0	0	1	25 clocks
1	0	1	0	26 clocks
1	0	1	1	27 clocks
1	1	0	0:	28 clocks
1	1	0	1	29 clocks
1	1	1	0	30 clocks
1	1	1	1	31 clocks

■ Power Control 1 (10h)

W/R	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	-	SAP[2:0]			-	BT[2:0]			-	AP[2:0]			-	DK	SLP	STB
INI		-	1	0	0	-	0	0	0	-	1	0	0	-	1	0	0

SAP[2:0]: The amount of fixed current from the fixed current source in the operational amplifier for the source driver is adjusted. When the amount of fixed current is large, LCD driving ability and the display quality become high, but the current consumption is increased. Adjust the fixed current considering the display quality and the current consumption. During non-display operation, set SAP[2:0]="000" to halt the operational amplifier to reduce the current consumption.

SAP2	SAP1	SAP0	OP current
0	0	0	Halt
0	0	1	Setting Disabled
0	1	0	0.63
0	1	1	0.73
1	0	0	1
1	0	1	1.25
1	1	0	1.42
1	1	1	Setting Disabled

BT[2:0]: Change the step-up scale of the step-up circuit by VCI1. Adjust the scale according to the voltage in use. Smaller scale consumes lesser current. Adjust the frequency considering the display quality and the current consumption.

BT2	BT1	BT0	VLOUT1 output (DDVDH)	VLOUT4 output (VCL)	VLOUT2 output (VGH)	VLOUT3 output (VGL)	Capacitor connection pins
0	0	0	Vci x 2	Vci x -1	Vci1 x 6	Vci1x-5	DDVDH, VGH, VGL, VCL, C11±, C12±, C21±, C22±,
0	0	1	↑	↑	Vci1 x 6	Vci1x –4	DDVDH, VGH, VGL, VCL, C11±, C12±, C21±, C22±,
0	1	0	↑	↑	Vci1 x 6	Vci1x-3	DDVDH, VGH, VGL, VCL, C11±, C12±, C21±, C22±,
0	1	1	↑	↑	Vci1x5	Vci1x–5	DDVDH, VGH, VGL, VCL, C11±, C12±, C21±, C22±,
1	0	0	↑	↑	Vci1x5	Vci1x-4	DDVDH, VGH, VGL, VCL, C11±, C12±, C21±, C22±,
1	0	1	↑	↑	Vci1x5	Vci1x –3	DDVDH, VGH, VGL, VCL, C11±, C12±, C21±, C22±,
1	1	0	↑	↑	Vci1x4	Vci1x –4	DDVDH, VGH, VGL, VCL, C11±, C12±, C21±, C22±,
1	1	1	↑	↑	Vci1x4	Vci1x-3	DDVDH, VGH, VGL, VCL, C11±, C12±, C21±, C22±,

Note 1) The capacitor connection pins are step-up capacitors which are necessary for DDVDH, VCL, VGH, VGL voltages.
Note 2) Each of following voltages should be within the following range: DDVDH = 6.0 V (Max.), VCL = - 3.3V (Min.), VGH = 16.5 V (Max.), VGL = -15V (Min.)

AP[2:0]: Adjust the amount of constant current from the constant current source of operational amplifier for the liquid crystal drive power supply. When the amount of constant current is set large, the liquid crystal drive capacity will be enhanced and the display quality will improve, while the current consumption will increase. Select an optimum amount of current taking both the display quality and the current consumption into account. During non-display operation, set AP[2:0]= “000” to halt the operational amplifier and step-up circuits to reduce current consumption.

AP2	AP1	AP0	Output OP Driver current adjustment
0	0	0	Setting Disabled
0	0	1	Setting Disabled
0	1	0	0.54
0	1	1	0.75
1	0	0	1
1	0	1	1.26
1	1	0	1.53
1	1	1	1.74

DK: Control the operation of the step-up circuit 1. When turning on the power supply, stop the startup of VLOUT1 for a moment, and wait for an enough time until VLOUT2 is stabilized before starting up VLOUT1.

DK	Operation of step-up circuit 1
0	Operation
1	Halt

SLP: When SLP = 1, the sleep mode is entered.

SLP	Status
0	Operation
1	Sleep only OSC is working

In the sleep mode, internal display operation is halted except the R-C oscillator to reduce current consumption. Only power control instructions (BT[2:0], DC[2:0], AP[2:0], SLP, STB, VC[2:0], VRH[4:0], VCOMG, VDV[4:0], and VCM[4:0] bits) are executed during the sleep mode. No change is made to the DDRAM data or instructions during the sleep mode, and the DDRAM data and the instructions are retained.

STB: When STB = 1, the standby mode is entered.

STB	Status
0	Operation
1	Stand-by OSC is halted

In the standby mode, display operation is completely halted, and all internal operations including the internal R-C oscillator and reception of external clock pulse, are halted. For details, see the “Standby Mode” section. Only instructions to release from the standby mode (STB = 0) and to start oscillation are accepted during the standby mode. DDRAM data and instructions are susceptible to destruction during the standby mode and require resetting after release from the standby mode.

■ Power Control 2 (11h)

W/R	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	-	DC2[2:0]			-	DC1[2:0]			-	DC0[2:0]			-	VC[2:0]		
INI		-	1	0	0	-	1	0	0	-	1	0	0	-	1	0	0

DC2[2:0]: Set the frequency of the step-up circuit 4.
Note: The higher frequency causes the better drive capacity of step-up circuit as well as the display quality, but it causes the higher current consumption, too.

DC22	DC21	DC20	frequency of the step-up circuit 4
0	0	0	fosc/4
0	0	1	fosc/8
0	1	0	fosc/16
0	1	1	fosc/32
1	0	0	fosc/64
1	0	1	fosc/128
1	1	0	Setting disable
1	1	1	Setting disable

DC1[2:0]: Set the frequency of the step-up circuit 2.
Note: The higher frequency causes the better drive capacity of step-up circuit as well as the display quality, but it causes the higher current consumption, too.

DC12	DC11	DC10	frequency of the step-up circuit 2
0	0	0	fosc/4
0	0	1	fosc/8
0	1	0	fosc/16
0	1	1	fosc/32
1	0	0	fosc/64
1	0	1	fosc/128
1	1	0	Setting disable
1	1	1	Setting disable

DC0[2:0]: Set the frequency of the step-up circuit 1.
Note: The higher frequency causes the better drive capacity of step-up circuit as well as the display quality, but it causes the higher current consumption, too.

DC02	DC01	DC00	frequency of the step-up circuit 1
0	0	0	fosc/2
0	0	1	fosc/4
0	1	0	fosc/8
0	1	1	fosc/16
1	0	0	fosc/32
1	0	1	fosc/64
1	1	0	Setting disable
1	1	1	Setting disable

VC[2:0]: Adjust the reference voltage for VREG1OUT, VciOUT voltages to the optimum ratio of VCI.

VC2	VC1	VC0	REGP reference voltage
0	0	0	VCI
0	0	1	0.92xVCI
0	1	0	0.87xVCI
0	1	1	0.83xVCI
1	0	0	0.76xVCI
1	0	1	0.73xVCI
1	1	0	Hi-Z
1	1	1	VCIRIN (2.4V regulated)

■ Power Control 3 (12h)

W/R	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	-	-	-	-	-	-	-	-	-	-	-	PON	VRH[3:0]			
INI		-	-	-	-	-	-	-	-	-	-		0	0	0	0	0

PON: Start operation of Step 2 and Step 4 circuit.
PON = “0”: stop operation of Step 2 and Step 4 circuit; PON =”1”: start operation the operation of Step 2 and Step 4circuit.

VRH[3:0]: Set the ratio of VREG1OUT voltage (the reference voltage for VCOM and grayscale voltage). REGP voltage is amplified by 1.33 ~ 2.79 times.

VRH3	VRH2	VRH1	VRH0	VREG1OUT ratio by REGP
0	0	0	0	1.33
0	0	0	1	1.45
0	0	1	0	1.55
0	0	1	1	1.66
0	1	0	0	1.76
0	1	0	1	1.81
0	1	1	0	1.86
0	1	1	1	Halt
1	0	0	0	1.91
1	0	0	1	1.96
1	0	1	0	2.01
1	0	1	1	2.07
1	1	0	0	2.13
1	1	0	1	2.17
1	1	1	0	2.22
1	1	1	1	Halt

Power Control 4 (13h)

W/R	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	-	-	VCOMG	VDV[4:0]					-	VCM[4:0]					VCMF[1:0]	
INI		-	-	0	0	0	0	0	0	-	0	0	0	0	0	0	0

VCOMG: When VCOMG = 1, VCOML can output the negative voltage. VCOMG = 1 is valid when PON = 1.
When VCOMG = 0, VCOML will fixed to GND.

VDV[4:0]: Set the Vcom alternating amplitude during Vcom alternating drive. The amplitude can be selected among VREG1OUT x discrete times from 0.6 to 1.2. When VCOMG = 0, this setting is invalid.

VDV4	VDV3	VDV2	VDV1	VDV0	Vcom amplitude
0	0	0	0	0	VREG1OUTx0.6
0	0	0	0	1	VREG1OUTx0.61
0	0	0	1	0	VREG1OUTx0.62
0	0	0	1	1	VREG1OUTx0.63
0	0	1	0	0	VREG1OUTx0.64
0	0	1	0	1	VREG1OUTx0.65
0	0	1	1	0	VREG1OUTx0.66
0	0	1	1	1	VREG1OUTx0.67
0	1	0	0	0	VREG1OUTx0.68
0	1	0	0	1	VREG1OUTx0.70
0	1	0	1	0	VREG1OUTx0.71
0	1	0	1	1	VREG1OUTx0.72
0	1	1	0	0	VREG1OUTx0.74
0	1	1	0	1	VREG1OUTx0.75
0	1	1	1	0	VREG1OUTx0.77
1	0	0	0	0	VREG1OUT x0.78
1	0	0	0	1	VREG1OUT x0.8
1	0	0	1	0	VREG1OUT x0.81
1	0	0	1	1	VREG1OUT x0.83
1	0	1	0	0	VREG1OUT x0.85
1	0	1	0	1	VREG1OUT x0.87
1	0	1	1	0	VREG1OUT x0.89
1	0	1	1	1	VREG1OUT x0.91
1	1	0	0	0	VREG1OUT x0.93
1	1	0	0	1	VREG1OUT x0.96
1	1	0	1	0	VREG1OUT x0.98
1	1	0	1	1	VREG1OUT x1.04
1	1	1	0	0	VREG1OUT x1.07

1	1	1	0	1	VREG1OUT x1.10
1	1	1	1	0	VREG1OUT x 1.13
1	1	1	1	1	VREG1OUTx1.16

VCM[4:0]: Set the VcomH voltage (a high-level voltage at the Vcom alternating drive). These bits amplify the VcomH voltage 0.4 to 0.98 times the VREG1 voltage. When VCM[4:0] = “11111” and VCMF[1:0] = “11”, the adjustment of the internal volume stops, and VcomH can be adjusted from VcomR by an external resistor.

VCM4	VCM3	VCM2	VCM1	VCM0	VcomH
0	0	0	0	0	VREG1OUTx0.98
0	0	0	0	1	VREG1OUTx0.96
0	0	0	1	0	VREG1OUTx0.94
0	0	0	1	1	VREG1OUTx0.92
0	0	1	0	0	VREG1OUTx0.90
0	0	1	0	1	VREG1OUTx0.88
0	0	1	1	0	VREG1OUTx0.86
0	0	1	1	1	VREG1OUTx0.84
0	1	0	0	0	VREG1OUTx0.82
0	1	0	0	1	VREG1OUTx0.80
0	1	0	1	0	VREG1OUTx0.78
0	1	0	1	1	VREG1OUTx0.76
0	1	1	0	0	VREG1OUTx0.74
0	1	1	0	1	VREG1OUTx0.72
0	1	1	1	0	VREG1OUTx0.70
0	1	1	1	1	VREG1OUTx0.68
1	0	0	0	0	VREG1OUT x0.66
1	0	0	0	1	VREG1OUT x0.64
1	0	0	1	0	VREG1OUT x0.62
1	0	0	1	1	VREG1OUT x0.60
1	0	1	0	0	VREG1OUT x0.58
1	0	1	0	1	VREG1OUT x0.56
1	0	1	1	0	VREG1OUT x0.54
1	0	1	1	1	VREG1OUT x0.52
1	1	0	0	0	VREG1OUT x0.50
1	1	0	0	1	VREG1OUT x0.48
1	1	0	1	0	VREG1OUT x0.46
1	1	0	1	1	VREG1OUT x0.44
1	1	1	0	0	VREG1OUT x0.42
1	1	1	0	1	VREG1OUT x0.40

1	1	1	1	0	VREG1OUT x 0.38
1	1	1	1	1	Halt internal volume. Adjust with a variable external resistor from VcomR. (Note: VCMF[1:0]="11")

VCMF[1:0]: To fine tune the VCOM value. After adjust the VCOM by setting VCM[4:0], the fine tuning of each scale of VCM[4:0] can be achieved by setting VCMF[1:0]. Each scale of VCM[4:0] can be divided into 4 . When use VcomR as VcomH reference voltage VCMF[1:0], should be "11"

■ Fuse Set (15h)

W/R	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	-	-	-	-	-	-	-	-	-	-	FSAEN	FSA[4:0]				
R	1	0	0	0	0	0	0	0	0	0	0	*	*	*	*	*	*
INI		-	-	-	-	-	-	-	-	-	-	0	1	0	0	0	0

Write

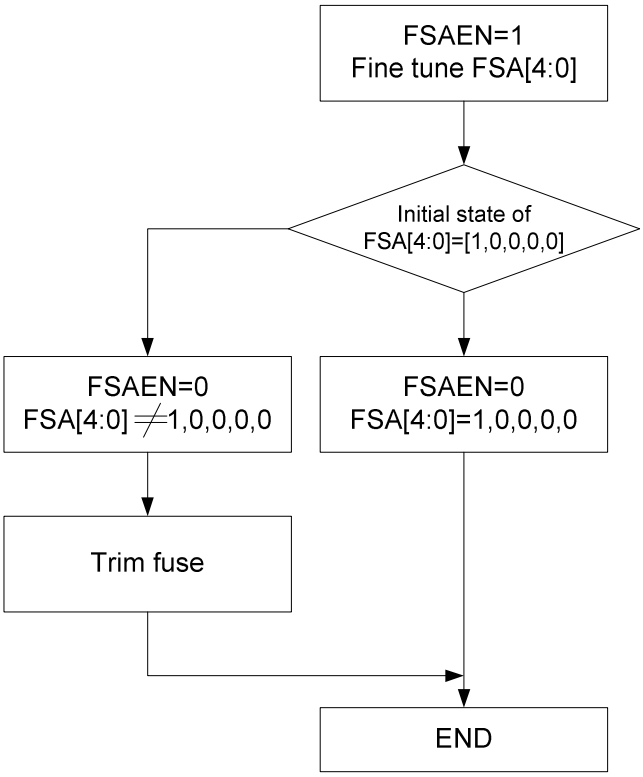
FSAEN: When FSAEN=0, the VcomH Reference voltage is shifted by setting up the fuse pins of FUSA[4:0].
When FSAEN=1, the VcomH Reference voltage is shifted by setting up the registers of FSA[4:0].

FSA[4:0]: FSA[4:0] are the fuse registers for VcomH reference voltage offset. The more accurate VcomH voltage can be adjusted by setting FSA[4:0].

Read

D[5]: Read the stats of FSAEN

D[4:0]: Read the status of FUSA[4:0] or FSA[4:0].
When FSAEN=0, the read-out value of D[4:0] is the setting value of FUSA[4:0]
When FSAEN=1, the read-out value of D[4:0] is the setting value of FSA[4:0]



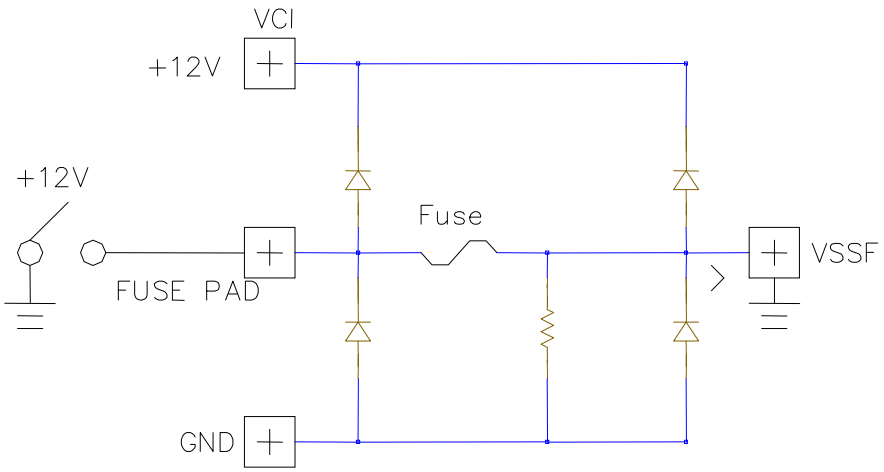
Fuse set flow chart

Trim Fuse:

1. Connect ground to pin VSSF of ST7712,
2. Vci pad should be connected with FUSA4 to FUSA0 sequentially with a voltage pulse. The width of pulse should be longer than 100ms, the voltage level should be higher than 10V (Current limitation of power supply should be smaller 200mA to avoid damaging fuse circuit) and current level should be higher than 50mA.
3. Each fuse pins within FUSA0 to FUSA3 corresponding to the registers FSA0 to FSA3 won't be trimmed when each register value is 0. THe fuse pin FUSA4 won't be trimmed as the logic value of corresponding register FSA4 is 1.
4. Set register FSAN to 0 in command 15H to enable the VCOM adjustment controlled by fuse pins FUSA[4:0].

Example:

	FSA4	FSA3	FSA2	FSA1	FSA0
Initial	1	0	0	0	0
Adjusted by Register	0	0	1	1	0
Need to Trim	Yes	No	Yes	Yes	No



Connect diagram

■ RAM Address Set (21h)

W/R	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	AD[15:0]															
INI		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

AD[15:0]: Set DDRAM addresses to the address counter (AC). The AC is automatically updated according to the AM and ID bit settings after the DDRAM data is written. This allows consecutive accesses without resetting address. Once the DDRAM data is read, the AC is not automatically updated. DDRAM address setting is not allowed in the standby mode. Make sure that the address is set within the specified window address.

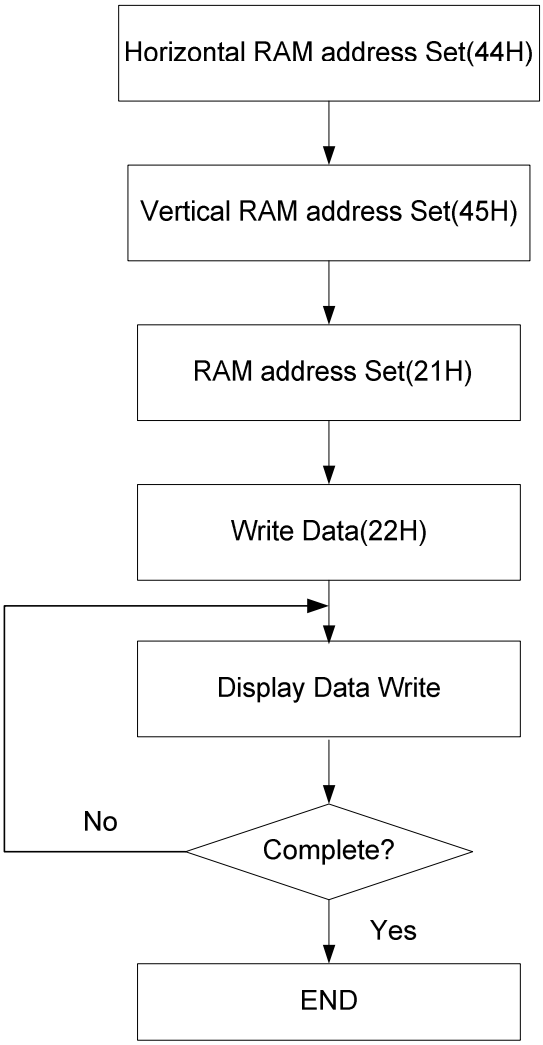
DDRAM Setting		Bitmap data for Source				
		S0	S1	..	S130	S131
Bitmap data for Gate	G0	“0000”H	“0001”H	..	“0082”H	“0083”H
	G1	“0100”H	“0101”H	..	“0182”H	“0183”H
	G2	“0200”H	“0201”H	..	“0282”H	“0283”H
	:	:	:	..	:	:
	G128	“8000”H	“8001”H	..	“8082”H	“8083”H
	G129	“8100”H	“8101”H	..	“8182”H	“8183”H
	G130	“8200”H	“8201”H	..	“8282”H	“8283”H
	G131	“8300”H	“8301”H	..	“8382”H	“8383”H

■ Write Data to DDRAM (22h)

W/R	RS	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	WD[17:0]																	
R	1	RD[17:0]																	

Write

WD[17:0]: Write 18-bit data to the DDRAM (depend on the selected interface). This data selects the grayscale level. After a write, the address is automatically updated according to AM and ID bit settings. During the standby mode, the DDRAM cannot be accessed.

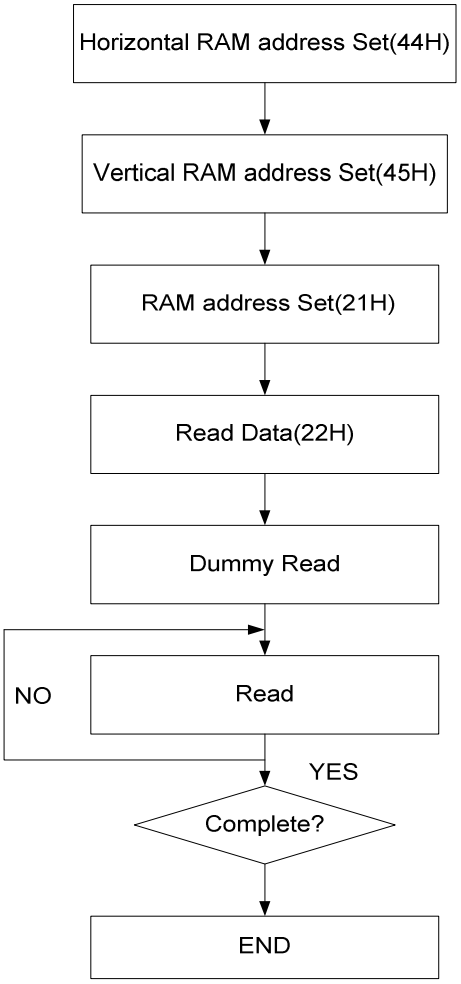


Write Data Flow chart

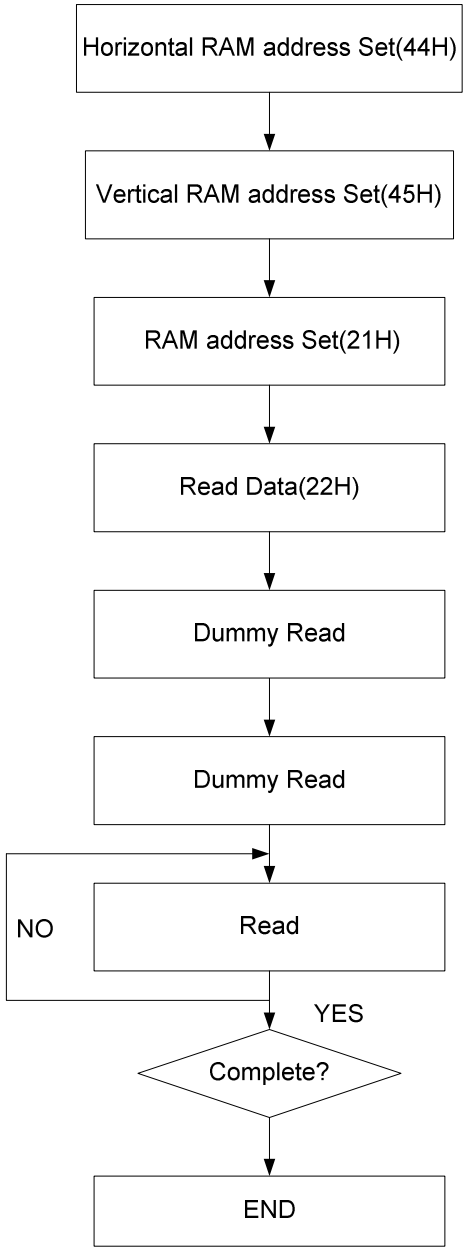
Read

RD[17:0]: Read 18-bit data from the DDRAM (depend on the selected interface). When the data is read to the MCU, the first-word read immediately after the DDRAM address setting is latched from the DDRAM to the internal read-data latch. The data on the data bus (DB17–DB0) becomes invalid and the second-word read is normal.

18bit and 16bit interface mode Read flow chart



9bit, 8bit and SPI interface mode Read flow chart



■ Gamma Control Set (30h~39h)

W/R	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	-	-	-	-	-	PKP1[2:0]			-	-	-	-	-	PKP0[2:0]		
INI		-	-	-	-	-	0	0	0	-	-	-	-	-	0	0	0
W	1	-	-	-	-	-	PKP3[2:0]			-	-	-	-	-	PKP2[2:0]		
INI		-	-	-	-	-	0	0	0	-	-	-	-	-	0	0	0
W	1	-	-	-	-	-	PKP5[2:0]			-	-	-	-	-	PKP4[2:0]		
INI		-	-	-	-	-	0	0	0	-	-	-	-	-	0	0	0
W	1	-	-	-	-	-	PRP1[2:0]			-	-	-	-	-	PRP0[2:0]		
INI		-	-	-	-	-	0	0	0	-	-	-	-	-	0	0	0
W	1	-	-	-	-	-	PKN1[2:0]			-	-	-	-	-	PKN0[2:0]		
INI		-	-	-	-	-	0	0	0	-	-	-	-	-	0	0	0
W	1	-	-	-	-	-	PKN3[2:0]			-	-	-	-	-	PKN2[2:0]		
INI		-	-	-	-	-	0	0	0	-	-	-	-	-	0	0	0
W	1	-	-	-	-	-	PKN5[2:0]			-	-	-	-	-	PKN4[2:0]		
INI		-	-	-	-	-	0	0	0	-	-	-	-	-	0	0	0
W	1	-	-	-	-	-	PRN1[2:0]			-	-	-	-	-	PRN0[2:0]		
INI		-	-	-	-	-	0	0	0	-	-	-	-	-	0	0	0
W	1	-	-	-	VRP1[4:0]					-	-	-	-	VRP0[3:0]			
INI		-	-	-	0	0	0	0	0	-	-	-	-	0	0	0	0
W	1	-	-	-	VRN1[4:0]					-	-	-	-	VRN0[3:0]			
INI		-	-	-	0	0	0	0	0	-	-	-	-	0	0	0	0

PKP5[2:0]~ PKP0[2:0]: The γ fine adjustment registers for positive polarity.
PRP1[2:0]~ PRP0[2:0]: The γ gradient adjustment registers for positive polarity.
PKN5[2:0]~ PKN0[2:0]: The γ fine adjustment registers for negative polarity.
PRN1[2:0] ~PRN0[2:0]: The γ gradient adjustment registers for negative polarity.
VRP1[4:0]~ VRP0[3:0]: The amplitude adjustment registers for positive polarity.
VRN1[4:0]~ VRN0[3:0]: The amplitude adjustment registers for negative polarity.

For details, see the “Gamma Control” section.

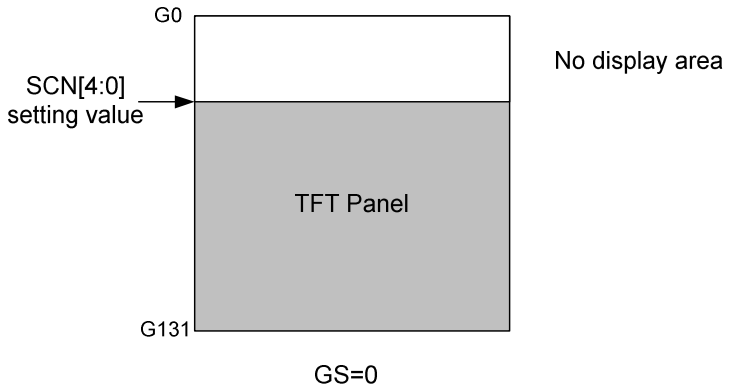
■ Gate Scan Set (40h)

W/R	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	-	-	-	-	-	-	-	-	-	-	-	SCN[4:0]				
INI		-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0

SCN[4:0]: Set the scanning starting position of the gate driver.

SCN4	SCN3	SCN2	SCN1	SCN0	Scan start line (Start line=SCN*8)
0	0	0	0	0	0
0	0	0	0	1	G7
0	0	0	1	0	G15
0	0	0	1	1	G23
:	:	:	:	:	:
1	0	0	0	0	127
1	0	0	0	1	Setting disable
:	:	:	:	:	
1	1	1	1	1	

Note: When setting the Gate scan set instruction SCN[4:0] value, it will not output data .



■ Vertical Scroll Set (41h)

W/R	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	-	-	-	-	-	-	-	-	VL[7:0]							
INI		-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0

VL[7:0]: Specify scroll length at the scroll display for vertical smooth scrolling. The number of raster-rows is specified from 0 to 131. The raster-rows of the specified number are scrolled during display. When the 132nd raster-row is displayed, the scrolling display starts to fresh from the 1st raster-row. The display-start raster-row VL[7:0] is valid when VLE[0] = 1 or VLE[1] = 1.

VL7	VL6	VL5	VL4	VL3	VL2	VL1	VL0	Display-start Raster-row
0	0	0	0	0	0	0	0	0 raster-row
0	0	0	0	0	0	0	1	1 raster-row
0	0	0	0	0	0	1	0	2 raster-row
0	0	0	0	0	0	1	1	3 raster-row
:	:	:	:	:	:	:	:	:
1	0	0	0	0	0	1	0	130 raster-row
1	0	0	0	0	0	1	1	131 raster-row
1	0	0	0	0	1	0	0	Setting disable
:	:	:	:	:	:	:	:	
1	1	1	1	1	1	1	1	

Note: The scroll range of screen can't not over partial display screen size or it will happen abnormal display.

■ 1st Screen Drive Set (42h)

W/R	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	SE1[7:0]								SS1[7:0]							
INI		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

SE1[7:0]: Setting the end line of 1st screen. The liquid crystal is driven by to the gate driver of the set value. For instance, when SS1[7:0]= “03”H and SE1[7:0] = “09”H, the liquid crystal is driven from G3 to G9, and G0 to G2, and G10 thereafter are non-display drive. Ensure that 00h≦SS1[7:0]≦SE1[7:0]≦83h.

SS1[7:0]: Setting the start line of 1st screen. The liquid crystal is driven by from the gate driver of the set value .

■ 2nd Screen Drive Set (43h)

W/R	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	SE2[7:0]								SS2[7:0]							
INI		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

SE2[7:0]: Setting the end line of 2nd screen. The liquid crystal is driven by from the gate driver of the set value .
SS2[7:0]: Setting the start line of 2nd screen. The liquid crystal is driven by from the gate driver of the set value .

Note1: The second screen is driven when SPT = 1.
Note2: Ensure that 00h≦SS1[7:0]≦ SE1[7:0]≦SS2[7:0]≦SE2[7:0]≦83h.

■ Horizontal RAM Address Position (44h)

W/R	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	HEA[7:0]								HSA[7:0]							
INI		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

HEA[7:0]: Setting the end line of the window-address range in the horizontal direction by address.

HSA[7:0]: Setting the Start line of the window-address range in the horizontal direction by address.

These addresses must be set before RAM write and data are written to DDRAM within the area limited by the addresses set by HSA[7:0] and HEA[7:0].
Note: Ensure that “00h”≦ HSA[7:0]≦HEA[7:0]≦“83h

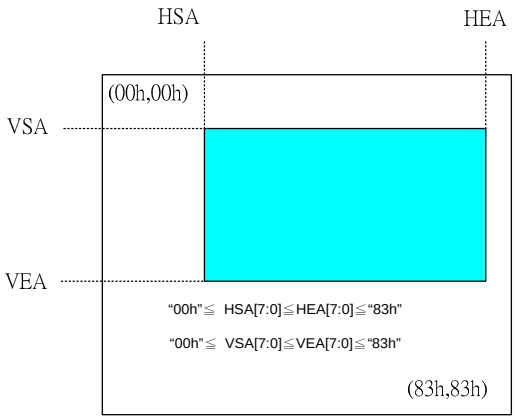
■ Vertical RAM Address Position (45h)

W/R	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	VEA[7:0]								VSA[7:0]							
INI		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

VEA[7:0]: Setting the end line of the window-address range in the vertical direction by address.

VSA[7:0]: Setting the start line of the window-address range in the vertical direction by address.

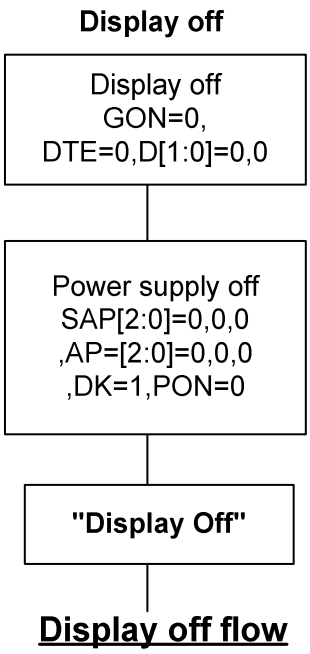
These addresses must be set before RAM write and data are written to DDRAM within the area limited by the addresses set by VSA[7:0] and VEA[7:0].
Note: Ensure that “00h”≦ VEA[7:0]≦VSA[7:0]≦“83h”

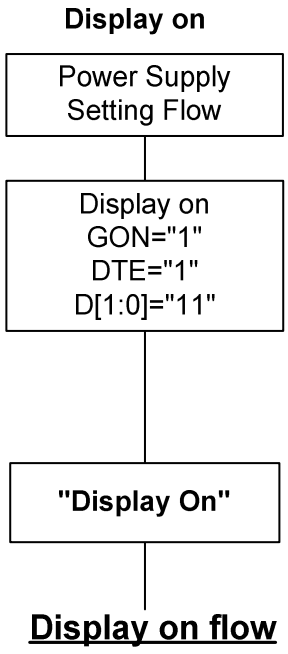


9 Instruction Setting Flow

Make the setting for each instruction according to the following sequence.

9.1 Display OFF & Display ON

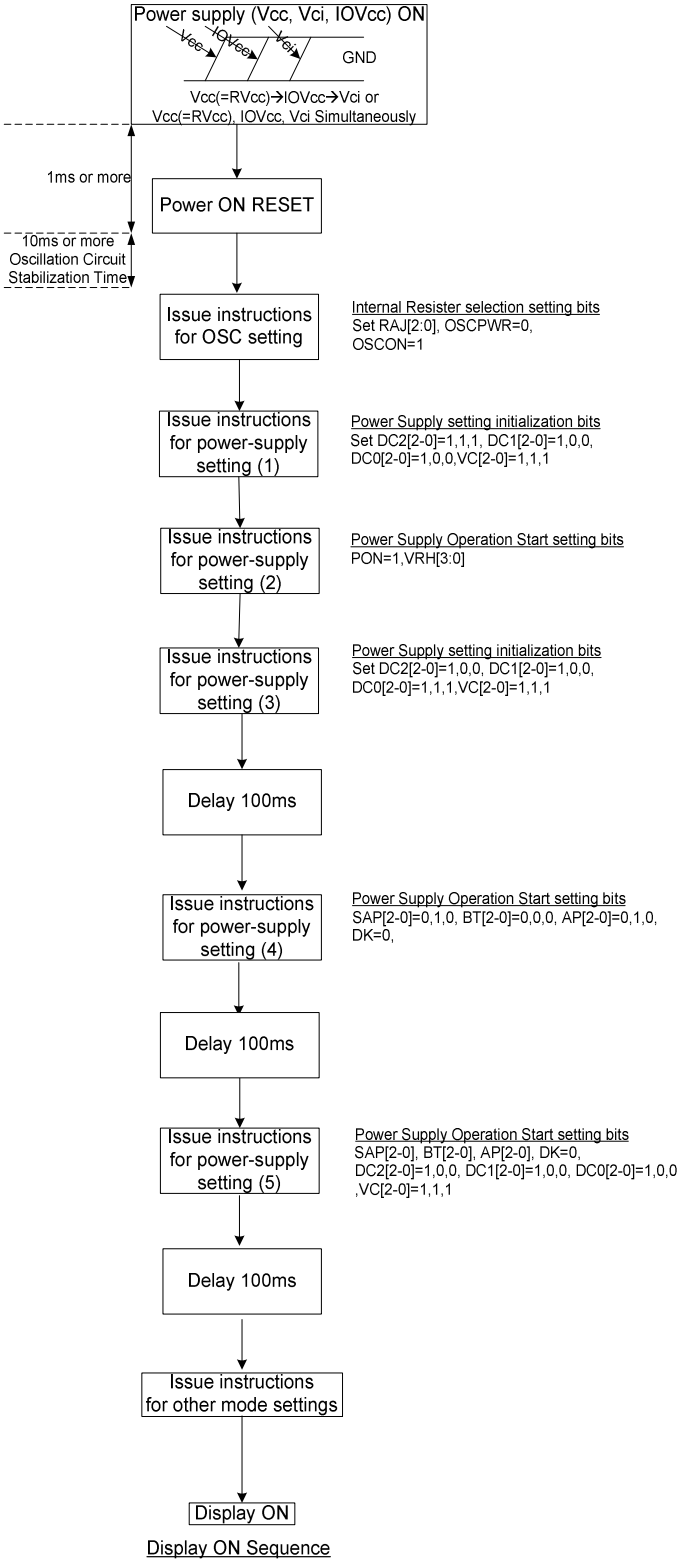




9.2 Initial Code Setting Flow chart

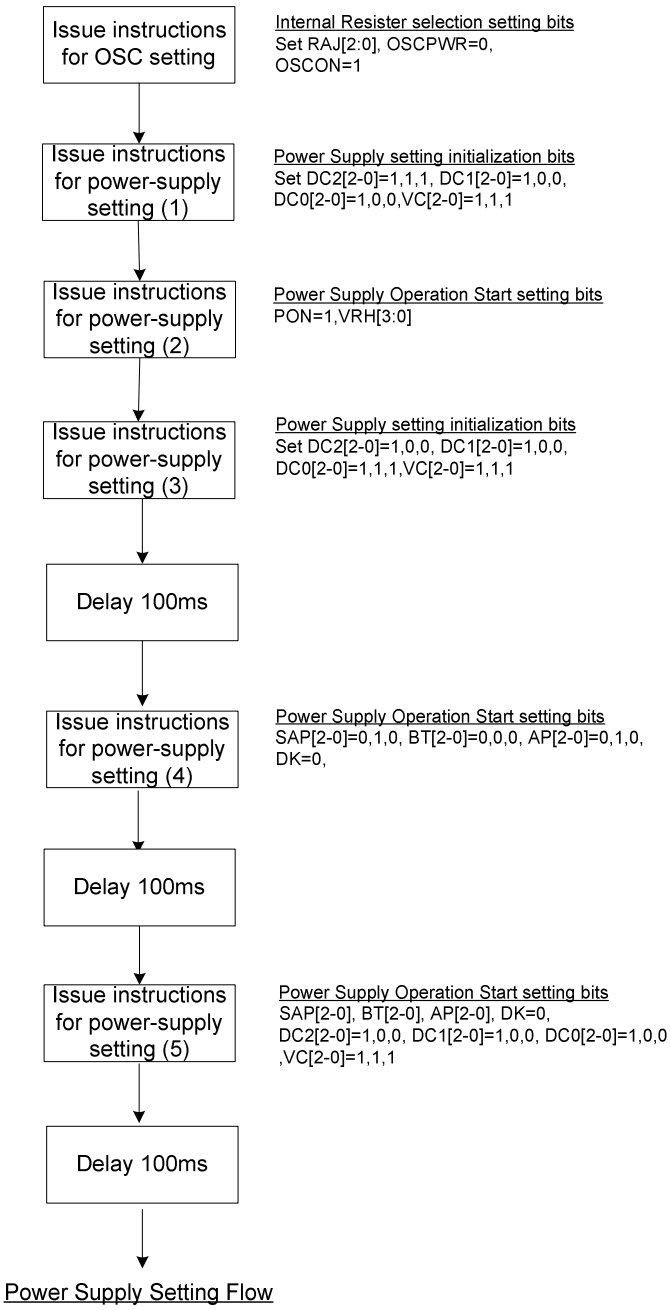
When turning on the power supply, follow the sequence below.

The stabilization time for the oscillation circuits, step-up circuits, and operation amplifiers may vary depending on the external resistors and capacitors.



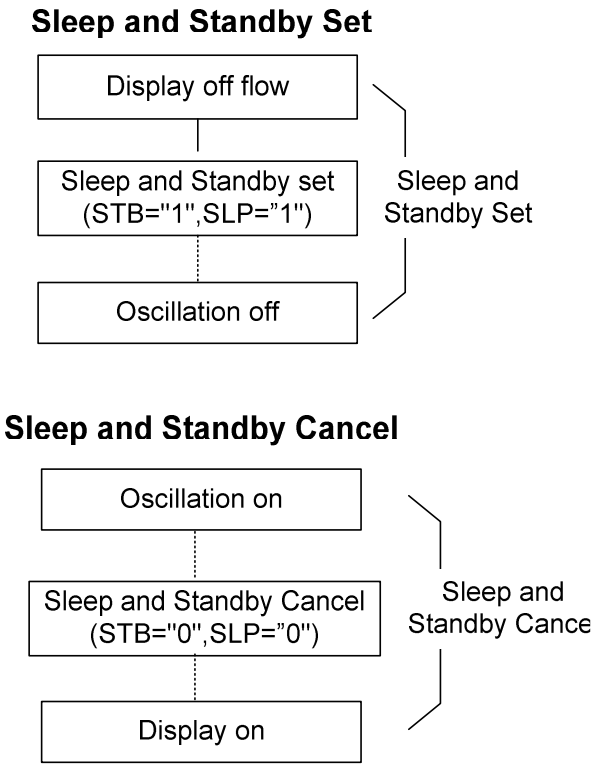
Display ON Sequence

9.3 Power Supply Setting Flow

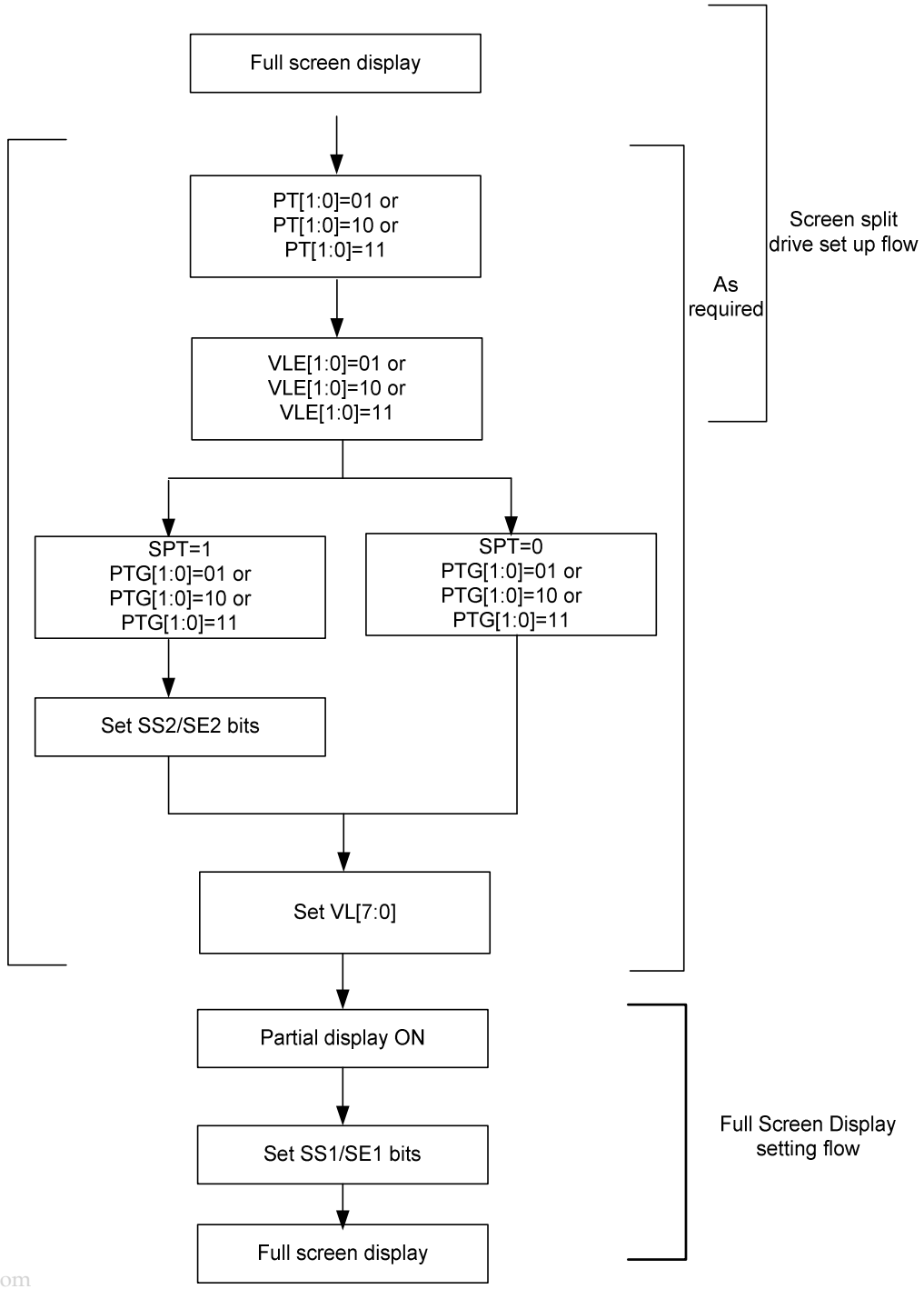


Power Supply Setting Flow

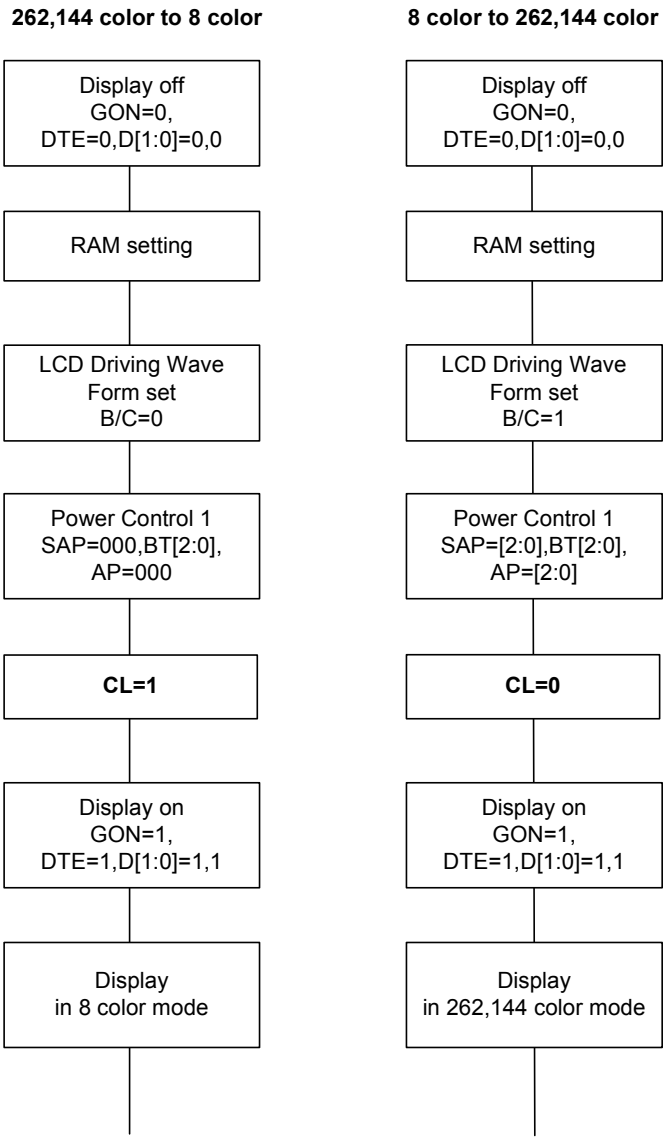
9.4 Sleep and Standby Sequence



9.5 Partial Display Setting Flow



9.6 Switch Between 262,144-color mode and 8-color mode setting flow chart



10. Absolute Maximum Values

Item	Symbol	Unit	Value	Notes
Power supply voltage (1)	Vcc	V	-0.3 ~ + 4.6	1, 2
Power supply voltage (2)	Vci - GND	V	-0.3 ~ + 4.6	1, 2
Power supply voltage (3)	DDVDH - GND	V	-0.3 ~ + 7.0	1, 2
Power supply voltage (4)	GND -VCL	V	-0.3 ~ -4.0	1, 2
Power supply voltage (5)	DDVDH- VCL	V	-0.3 ~ + 8.0	1
Power supply voltage (6)	VGH - GND	V	-0.3 ~ + 16.5	1, 2
Power supply voltage (7)	GND - VGL	V	-0.3 ~ - 15	1, 2
Input voltage	Vt	V	-0.3 ~ Vcc + 0.3	1
Operating temperature	Topr	°C	-40 ~ + 85	1, 3
Storage temperature	Tstg	°C	-55 ~ + 110	1

Note 1) The LSI may be permanently damaged if it is used under the condition exceeding the above absolute maximum values. It is also recommended to use the LSI within the electric characteristic conditions during normal operation. Exceeding the conditions may lead to malfunction of LSI and affect its credibility.

Note 2) The voltage from GND.

Note 3) The DC and AC characteristics of chip and wafer products are guaranteed at 85 °C.

10. Electric Characteristics

DC Characteristics

(V_{DD} = 1.8 to 3.3 V, Ta = –40 to +85℃ Note 1)

Item	Symbol	Unit	Test Condition	Min	Typ	Max	Notes
Input high value	V_{IH}	V	V_{CC} = 1.8 to 3.3 V	0.8 V_{CC}	--	V_{CC}	1
Input low voltage (1) (OSC1 pin)	$V_{IL}1$	V	V_{CC} = 1.8 to 3.3 V	0	--	0.2 V_{CC}	1
Input low voltage (2) (Except OSC1 pin)	$V_{IL}2$	V	Vcc=1.8V to 2.4V	0	--	0.2 V_{CC}	1
			Vcc=2.4V to 3.3V	0	--	0.2 V_{CC}	1
Output high voltage (1) (DB0~17 pins)	V_{OH}	V	V_{CC} = 1.8 to 3.3 V, I_{OH} = 0.1 mA	0.8V_{CC}	--	V_{cc}	1
Output low voltage (1) (DB0~17 pins)	V_{OL}	V	V_{CC} = 1.8 to 3.3 V, I_{OL} = 0.1 mA	0	--	0.2 V_{CC}	1
I/O leakage current (I_{IOVCC}+I_{VCC}+I_{VCI})	I_{Li}	µA	Vin = 0 to V_{CC}	0	--	1	1
Current consumption during normal operation 262K mode ($I_{IOVCC-GND}$+$I_{VCC-GND}$+$I_{VCI-GND}$)	I_{OP1}	mA	R-C oscillation=190KHZ; V_{CC} = 2.8 V, DVDDH=5.4V, REV=1, Ta = 25℃, SAP="010",AP="010",FLD="01", BC=1, NW="00000" RAM data 0000h		1.3		1
Current consumption 8-color mode, 30-line partial ($I_{IOVCC-GND}$+$I_{VCC-GND}$+$I_{VCI-GND}$)	I_{op2}	µA	R-C oscillation=190KHZ; V_{CC} = 2.8 V, DVDDH=5.4V, REV=1, Ta = 25℃, SAP="010",AP="010",FLD="01", BC=1, NW="00000" RAM data 0000h		350		1
Current consumption during normal operation (Vcc-GND)	I_{VCC}	µA	R-C oscillation=190KHZ; V_{CC} = 2.8 V, DVDDH=5.4V, REV=0, Ta = 25℃, SAP="010",AP="010",FLD="01", BC=1, NW="00000" RAM data 0000h	--	60	80	1
LCD power supply current (Vci-GND) 262,144 color display mode	I_{Vci1}	mA	R-C oscillation=190KHZ; V_{CC} = 2.8 V, DVDDH=5.4V, REV=1, Ta = 25℃, SAP="010",AP="010",FLD="01", BC=1, NW="00000" RAM data 0000h		1.2		1
LCD power supply current (Vci-GND) 8-color mode,	I_{Vci2}	µA	R-C oscillation=190KHZ; V_{CC} = 2.8 V, DVDDH=5.4V, REV=1, Ta = 25℃,		250		1

30-line partial			SAP="010",AP="010",FLD="01", BC=1, NW="00000" RAM data 0000h				
Current consumption during standby & sleep operation (V_{DD}-GND)	I_{ST}	μA	Vcc = 2.8V, Ta<=50℃	--	40	100	1
Liquid Crystal Power Current (DDVDH-GND)	I_{LCD}	μA	Vcc=2.8V, VDH=5.243V, CR Oscillation=190KHz; Ta=25℃, RAMdata:0000h, REV="0", SAP="010",AP="010", VRN[4:0]="0", PKP[52:00]="0", PRP[52:00]="0", VRN[4:0]=VRP[4:0]="0" PKP[52:00]="0", PRP[52:00]="0"	--	450	550	1
Liquid Crystal Drive Voltage (DDVDH-GND)	V_{LCD}	V	--	4.5	--	6.0	1
Output Voltage deviation	∠Vo	mV	Source>4.2V, Source<0.8V	--	20	--	1
			0.8V<Source<4.2		12		
Variation of average output voltage		mV	--	--	--	35	1
Gate Ron resistor	Ron	Ω			360		1

Notes to Electrical Characteristics

1. The TEST1 and TEST2 pins must be grounded (GND). The IM3/2/1/0 must be fixed at either GND or Iovcc level
2. The output voltage difference is the difference in voltage levels output from adjacent source pins for a same grayscale. This value is for reference.
3. The average output voltage variance is the difference in the average source output voltages of the same product. The average voltage source output voltage is measured when all output pins output the voltage for a same grayscale.

AC Characteristics

(V_{DD} = 1.8 to 3.3 V, Ta = –40 to +85℃)

Clock Characteristics (V_{DD} = 1.8 to 3.3 V)

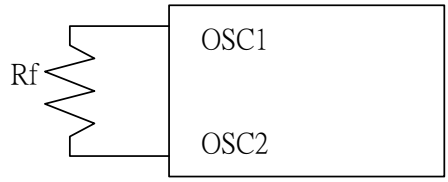
Item	Symbol	Unit	Test Condition	Min	Typ	Max	Notes
External clock Frequency	Fcp	kHz	V_{DD} = 1.8 t0 3.3V	100	270	600	
External clock duty ratio	Duty	%	V_{DD} = 1.8 t0 3.3V	45	50	55	
External clock rise time	Trcp	μs	V_{DD} = 1.8 t0 3.3V	--	--	0.2	
External clock fall time	Tfcp	μs	V_{DD} = 1.8 t0 3.3V	--	--	0.2	
R-C oscillation clock	FOSC	kHz	Rf=240KΩ VCC=3V	192	240	288	

Liquid crystal driver output characteristics

Item	Symbol	Unit	Test Condition	Min	Typ	Max
Driver output delay time	tdd	μs	V_{DD} =2.8V, VDH=5.4V, CR oscillation ;fosc=190kHz(132 lines), Ta=25℃、REV="0", SAP="010", AP="010", VRN[4:0]="0",VRP[4:0]="0" PKP[52:00]="0",PRP[12:00]="0" PKP[52:00]="0",PRP[12:00]="0" All pins changes at the same time from same grayscale. The time till output level reaches —35mV when VCOM polarity changes. Load resistance R=10kΩ、Load capacity C=20pF	--	30	--

Electrical Characteristics

1. Applies to the internal oscillator operations using external oscillation resistor Rf



The oscillation frequency may vary
depending on the capacitors for OSC1, OSC2 pins.
Place OSC1 and OSC2 close to each other.

Notes:

The Rf resistor value should be based on the RC loading of panel and FPC to fine tune Rf value to apparoach the osc frequency that customer need.

11. TIMING CHARACTERISISTICS

condition：Bare Die

System Bus Read/Write Characteristics 1(For the 8080 Series MPU)

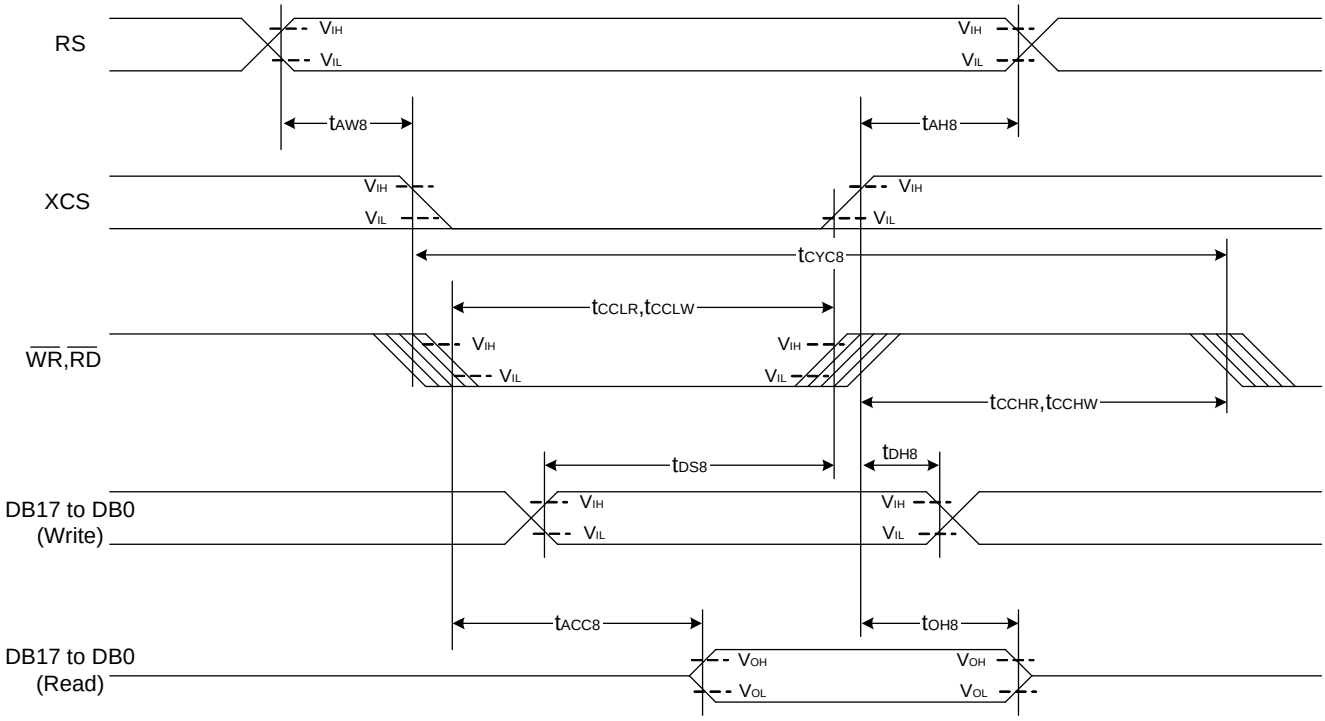


Figure 11-1

(V_{DD} =3.3V, Ta=-40℃~85℃)

Item	Signal	Symbol	Rating		Units
			Min	Max	
Address hold time	RS	t_{AH8}	10		ns
Address setup time		t_{AW8}	30		ns
System cycle time	WR	t_{CYC8}	120		ns
Enable L pulse width (WRITE)		t_{CCLW}	50		ns
Enable H pulse width (WRITE)		t_{CCHW}	70		ns
WRITE Data setup time	DB0~DB17	t_{DS8}	50		ns
WRITE Data hold time		t_{DH8}	10		ns
Enable L pulse width (READ)	RD	t_{CCLR}	80		ns
Enable H pulse width (READ)		t_{CCHR}	80		ns

(V_{DD} =2.8V, Ta=-40℃~85℃)

Item	Signal	Symbol	Rating		Units
			Min	Max	
Address hold time	RS	t_{AH8}	10		ns
Address setup time		t_{AW8}	30		ns
System cycle time	WR	t_{CYC8}	120		ns
Enable L pulse width (WRITE)		t_{CCLW}	50		ns
Enable H pulse width (WRITE)		t_{CCHW}	70		ns
WRITE Data setup time	DB0~DB17	t_{DS8}	50		ns
WRITE Data hold time		t_{DH8}	10		ns
Enable L pulse width (READ)	RD	t_{CCLR}	80		ns
Enable H pulse width (READ)		t_{CCHR}	80		ns

(V_{DD} =1.8V, Ta=-40℃~85℃)

Item	Signal	Symbol	Rating		Units
			Min	Max	
Address hold time	RS	t_{AH8}	10		ns
Address setup time		t_{AW8}	30		ns
System cycle time	WR	t_{CYC8}	120		ns
Enable L pulse width (WRITE)		t_{CCLW}	50		ns
Enable H pulse width (WRITE)		t_{CCHW}	70		ns
WRITE Data setup time	DB0~DB17	t_{DS8}	50		ns
WRITE Data hold time		t_{DH8}	10		ns
Enable L pulse width (READ)	RD	t_{CCLR}	80		ns
Enable H pulse width (READ)		t_{CCHR}	80		ns

System Bus Read/Write Characteristics 1(For the 6800 Series MPU)

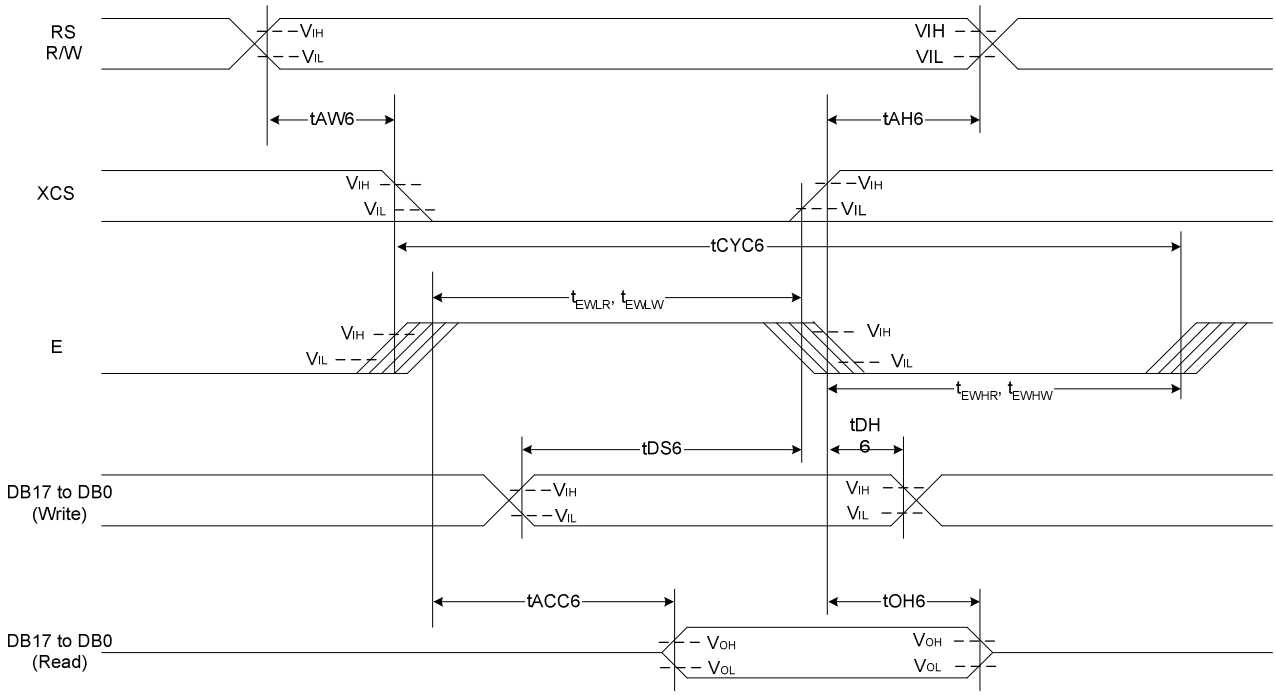


Figure 11-2

(VDD =3.3V, Ta=-40℃~85℃)

Item	Signal	Symbol	Rating		Units
			Min	Max	
Address hold time	RS	t_{AH8}	10		ns
Address setup time		t_{AW8}	20		ns
System cycle time	E	t_{CYC8}	80		ns
Enable H pulse width (WRITE)		t_{EWLW}	40		ns
Enable L pulse width (WRITE)		t_{EWHW}	40		ns
WRITE Data setup time	DB0~DB17	t_{DS8}	40		ns
WRITE Data hold time		t_{DH8}	10		ns
Enable L pulse width (READ)	RW	t_{ACC6}	70		ns
Enable H pulse width (READ)		t_{OH6}	70		ns

(V_{DD} =2.8V, Ta=-40℃~85℃)

Item	Signal	Symbol	Rating		Units
			Min	Max	
Address hold time	RS	t_{AH8}	10		ns
Address setup time		t_{AW8}	20		ns
System cycle time	E	t_{CYC8}	80		ns
Enable L pulse width (WRITE)		t_{CCLW}	40		ns
Enable H pulse width (WRITE)		t_{CCHW}	40		ns
WRITE Data setup time	DB0~DB17	t_{DS8}	40		ns
WRITE Data hold time		t_{DH8}	10		ns
Enable L pulse width (READ)	RW	t_{CCLR}	70		ns
Enable H pulse width (READ)		t_{CCHR}	70		ns

(V_{DD} =1.8V, Ta=-40℃~85℃)

Item	Signal	Symbol	Rating		Units
			Min	Max	
Address hold time	RS	t_{AH8}	10		ns
Address setup time		t_{AW8}	20		ns
System cycle time	E	t_{CYC8}	80		ns
Enable L pulse width (WRITE)		t_{CCLW}	40		ns
Enable H pulse width (WRITE)		t_{CCHW}	40		ns
WRITE Data setup time	DB0~DB17	t_{DS8}	40		ns
WRITE Data hold time		t_{DH8}	10		ns
Enable L pulse width (READ)	RW	t_{CCLR}	70		ns
Enable H pulse width (READ)		t_{CCHR}	70		ns

Serial Interface (4-Line Interface)

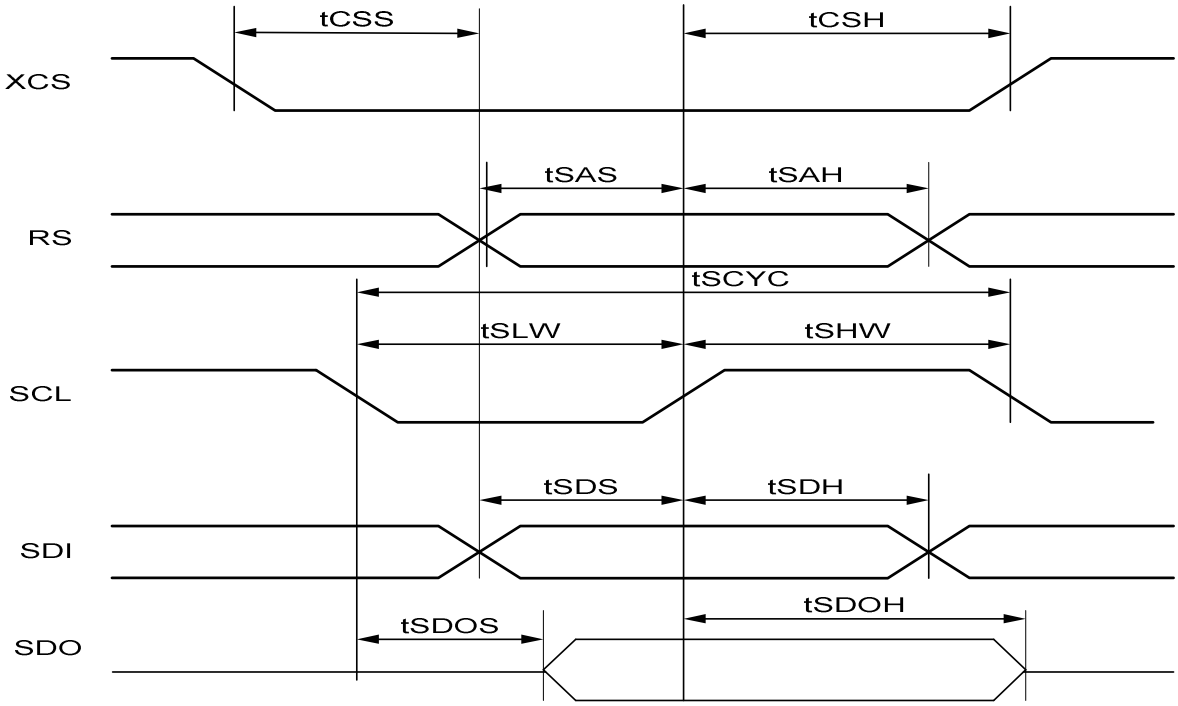


Figure 11-3

(V_{DD} =3.3V, Ta=-40℃~85℃)

Item	Signal	Symbol	Rating		Units
			Min	Max	
Serial Clock Period	SCL	tSCYC	50		ns
SCL “H” pulse width		tSHW	20		
SCL “L” pulse width		tSLW	30		
Address setup time	RS	tSAS	20		ns
Address hold time		tSAH	10		
Data setup time	SDI	tSDS	10		ns
Data hold time		tSDH	20		
XCS-SCL time	XCS	tCSS	20		ns
		tCSH	30		
SCL L pulse width (READ)		tSDOS	110		ns
SCL H pulse width (READ)		tSDOH	110		ns

(V_{DD} =2.8V, Ta=-40℃~85℃)

Item	Signal	Symbol	Rating		Units
			Min	Max	
Serial Clock Period	SCL	tSCYC	50		ns
SCL “H” pulse width		tSHW	20		
SCL “L” pulse width		tSLW	30		
Address setup time	RS	tSAS	20		ns
Address hold time		tSAH	10		
Data setup time	SI	tSDS	10		ns
Data hold time		tSDH	20		
CS-SCL time	XCS	tCSS	20		ns
		tCSH	30		
SCL L pulse width (READ)		tSDOS	110		ns
SCL H pulse width (READ)		tSDOH	110		ns

(V_{DD} =1.8V, Ta=-40℃~85℃)

Item	Signal	Symbol	Rating		Units
			Min	Max	
Serial Clock Period	SCL	tSCYC	50		ns
SCL “H” pulse width		tSHW	20		
SCL “L” pulse width		tSLW	30		
Address setup time	RS	tSAS	20		ns
Address hold time		tSAH	10		
Data setup time	SDI	tSDS	10		ns
Data hold time		tSDH	20		
XCS-SCL time	XCS	tCSS	20		ns
		tCSH	30		
SCL L pulse width (READ)		tSDOS	110		ns
SCL H pulse width (READ)		tSDOH	110		ns

Serial Interface(3-Line Interface)

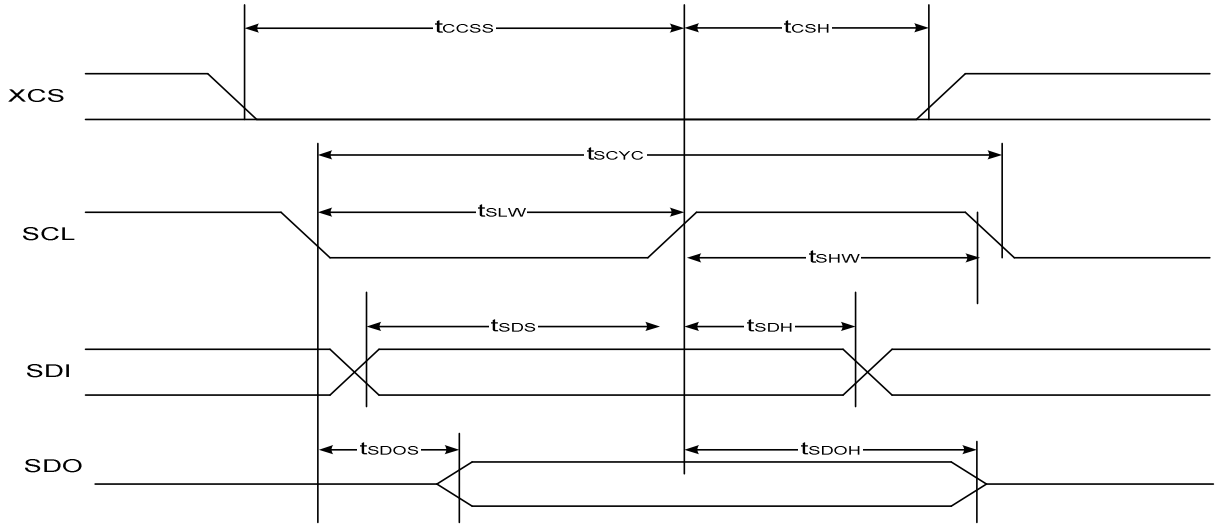


Figure 11-4

(V_{DD} =3.3V, Ta=-40℃~85℃)

Item	Signal	Symbol	Rating		Units
			Min	Max	
Serial Clock Period	SCL	tSCYC	50		ns
SCL “H” pulse width		tSHW	20		
SCL “L” pulse width		tSLW	30		
Data setup time	SDI	tSDS	10		ns
Data hold time		tSDH	20		
XCS-SCL time	XCS	tCSS	20		ns
		tCSH	30		
SCL L pulse width (READ)		tSDOS	110		ns
SCL H pulse width (READ)		tSDOH	110		ns

(V_{DD} =2.8V, Ta=-40℃~85℃)

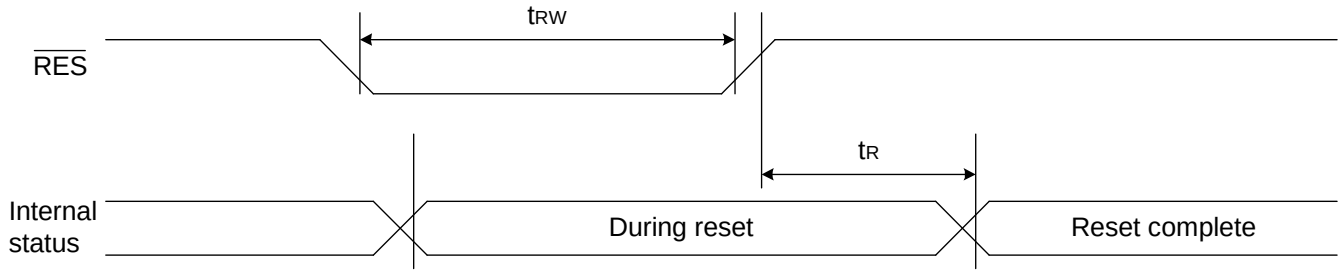
Item	Signal	Symbol	Rating		Units
			Min	Max	
Serial Clock Period	SCL	tSCYC	50		ns
SCL “H” pulse width		tSHW	20		
SCL “L” pulse width		tSLW	30		
Data setup time	SDI	tSDS	10		ns
Data hold time		tSDH	20		
XCS-SCL time	XCS	tCSS	20		ns
		tCSH	30		
SCL L pulse width (READ)		tSDOS	110		ns

SCL H pulse width (READ)		tSDOH	110		ns

(VDD =1.8V, Ta=-40℃~85℃)

Item	Signal	Symbol	Rating		Units
			Min	Max	
Serial Clock Period	SCL	tSCYC	50		ns
SCL “H” pulse width		tSHW	20		
SCL “L” pulse width		tSLW	30		
Data setup time	SDI	tSDS	10		ns
Data hold time		tSDH	20		
XCS-SCL time	XCS	tCSS	20		ns
		tCSH	30		
SCL L pulse width (READ)		tSDOS	110		ns
SCL H pulse width (READ)		tSDOH	110		ns

Reset Timing Characteristics (Vdd = 1.8 to 3.3V)



(VDD =3.3V, Ta=-40℃~85℃)

Item	Symbol	Rating			Units
		Min	Typ	Max	
Reset low-level width	tRW	1	--	--	us
Reset high-level width	tR			1	

(VDD =2.7V, Ta=-40℃~85℃)

Item	Symbol	Rating			Units
		Min	Typ	Max	
Reset low-level width	tRW	1	--	--	us
Reset high-level width	tR			1	

(VDD =1.8V, Ta=-40℃~85℃)

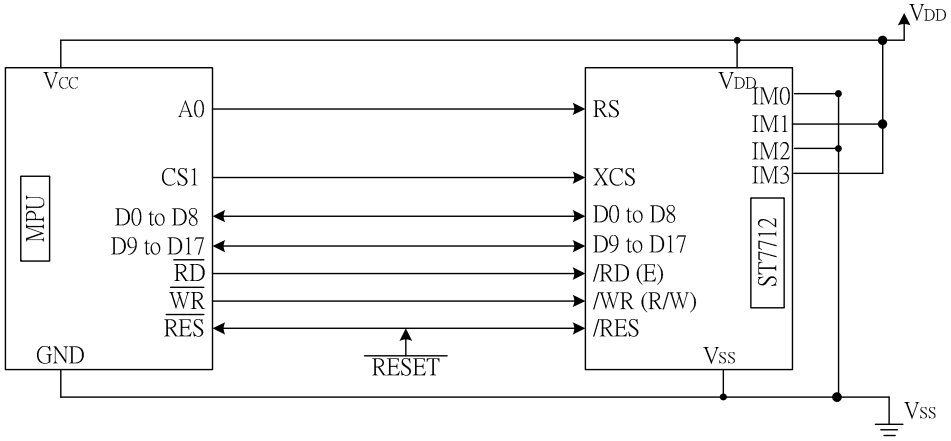
Item	Symbol	Rating			Units
		Min	Typ	Max	
Reset low-level width	tRW	1	--	--	us
Reset high-level width	tR			1	

12. THE MPU INTERFACE (REFERENCE EXAMPLES)

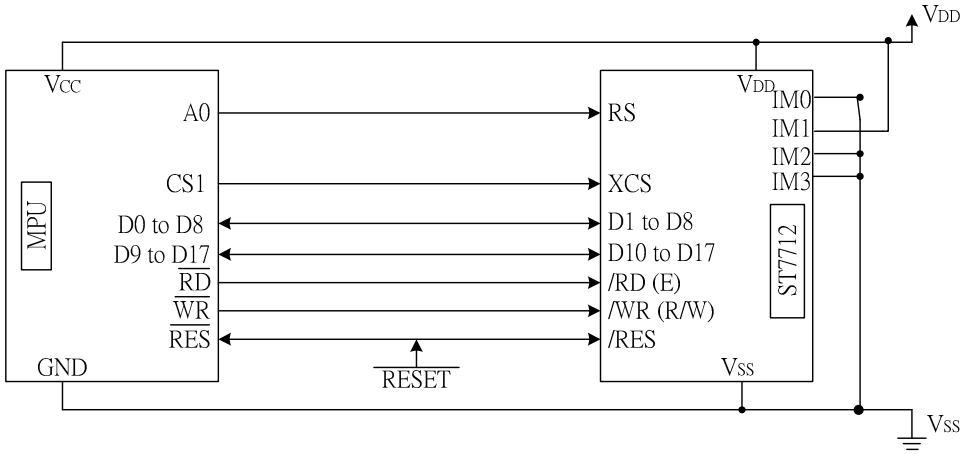
The ST7712 Series can be connected to either 8080 Series MPUs or to 6800 Series MPUs. Moreover, using the serial interface it is possible to operate the ST7712 series chips with fewer signal lines.

The display area can be enlarged by using multiple ST7712 Series chips. When this is done, the chip select signal can be used to select the individual Ics to access.

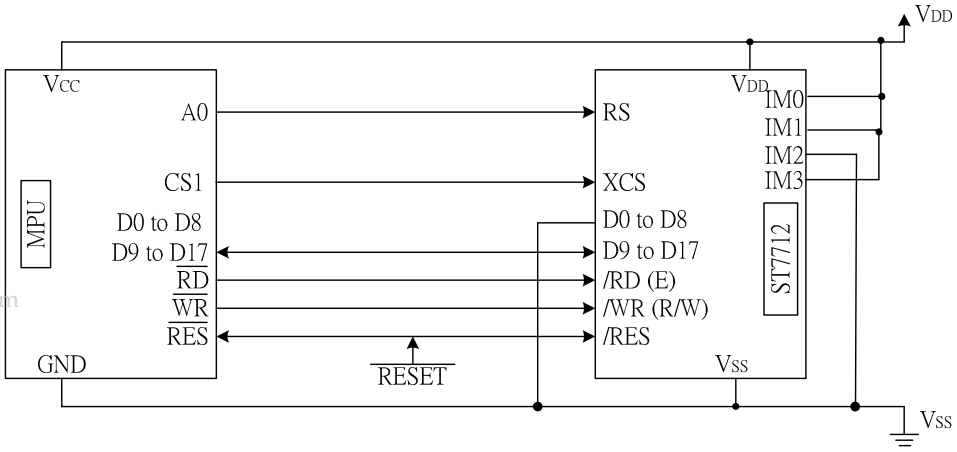
(1) 8080 Series 18bits MPUs



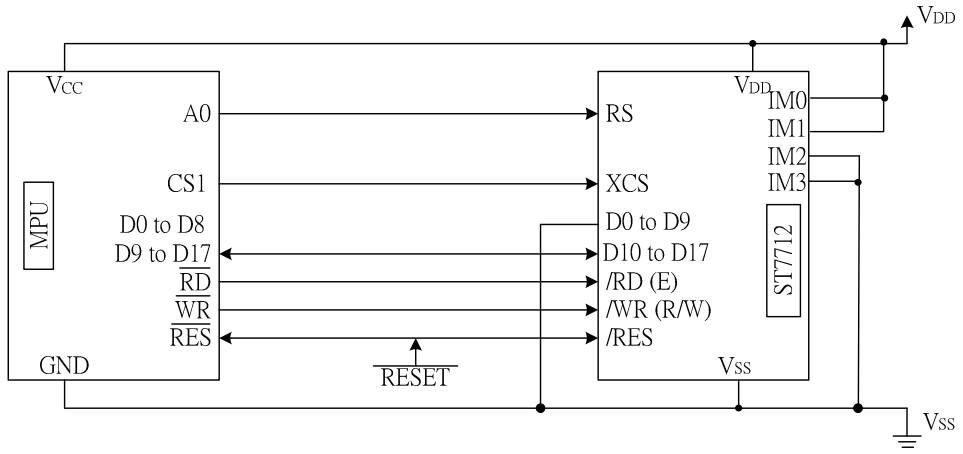
(2) 8080 Series 16bits MPUs



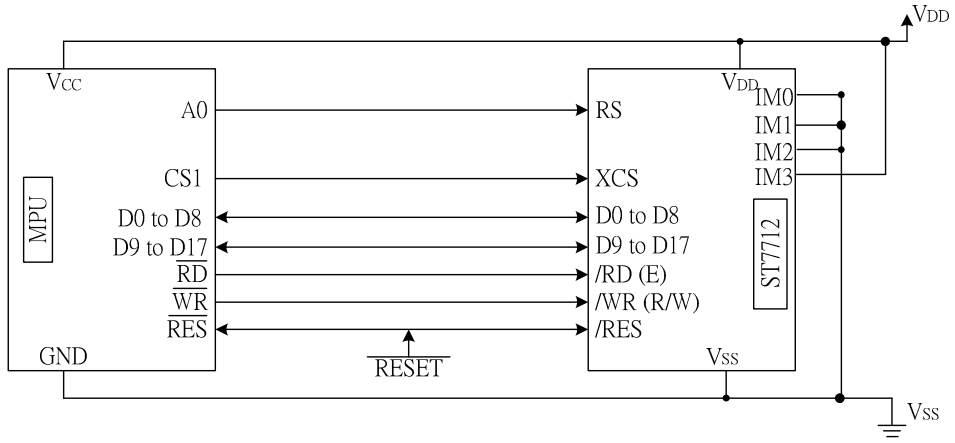
(3) 8080 Series 9 bits MPUs



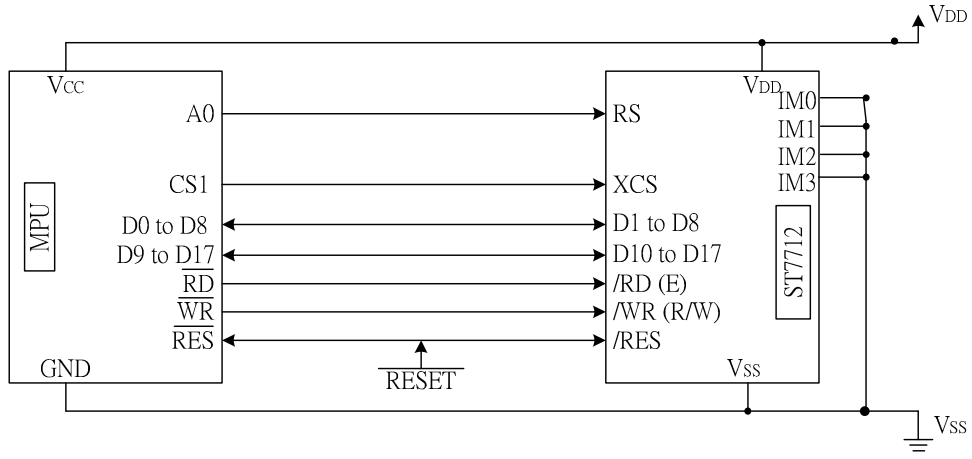
(4) 8080 Series 8 bits MPUs



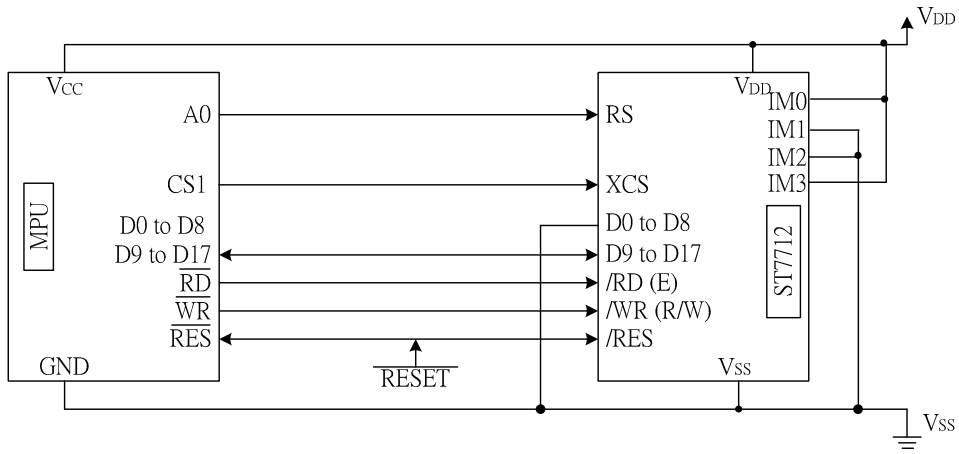
(5) 6800 Series 18 bits MPUs



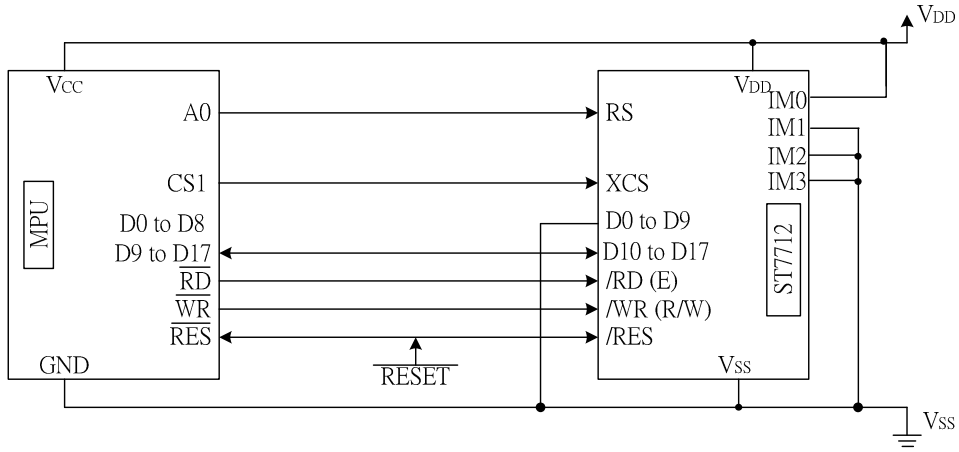
(6) 6800 Series 16 bits MPUs



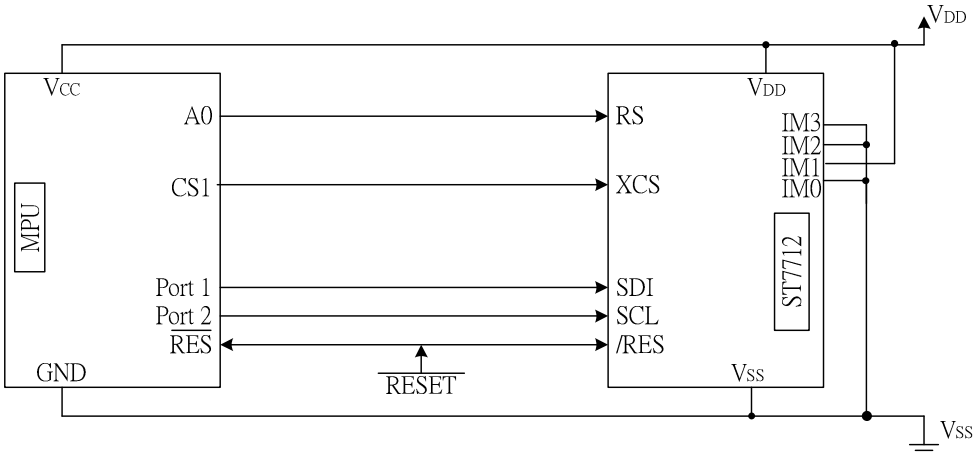
(7) 6800 Series 9 bits MPUs



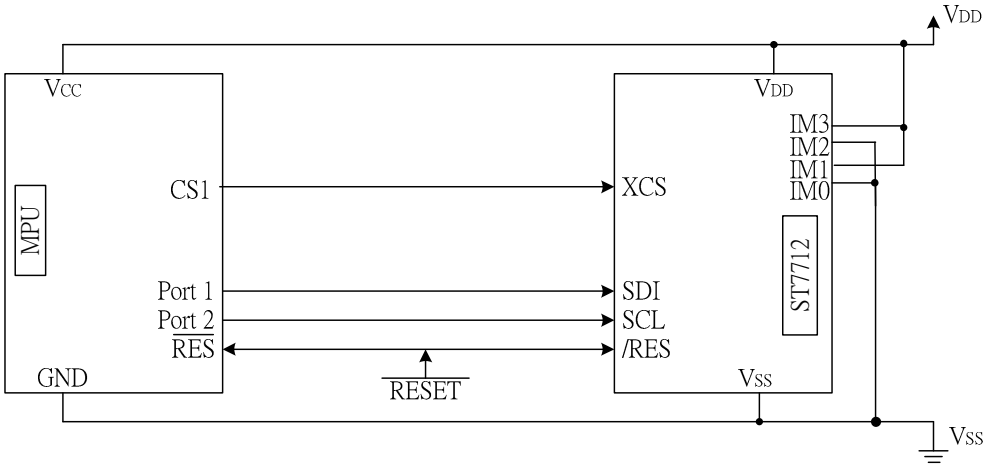
(8) 6800 Series 8 bits MPUs



(9) Using the Serial Interface (4-line interface)



(9) Using the Serial Interface (3-line interface)



13. Application circuit

Interface: 8080 series-18bits

Vcc=2.4V~3.3V

Vci=2.5V~3.3V

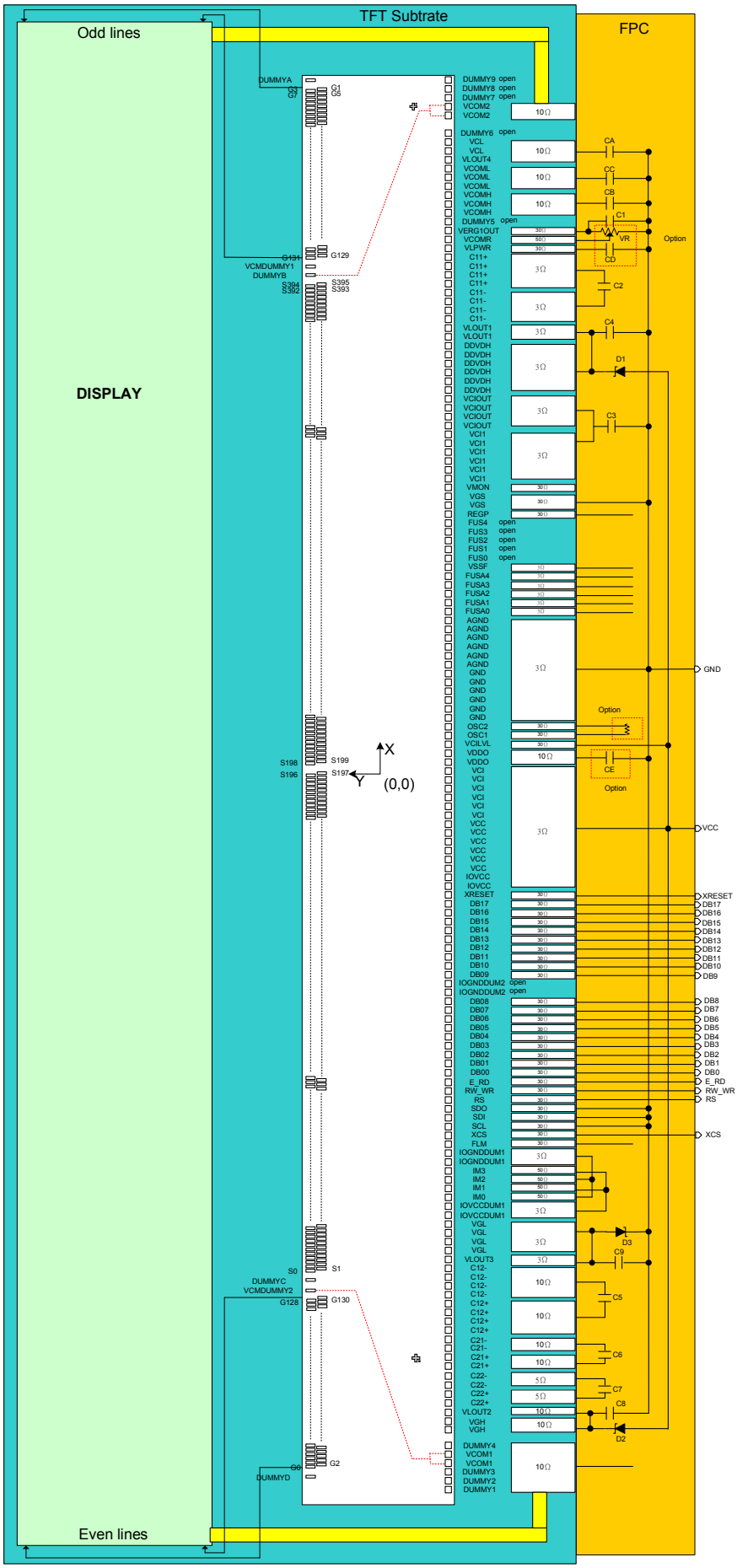
IOVCC=1.8V~3.3V

1uF(6V):C2,C3,C4,C7,CA,CB,CC,CD,CE

0.1uF(20V):C5,C6,C8,C9

Shot key diode (VF<0.4V/20mA at 25 ℃ VR>=30V)

VR>200KΩ



Interface: 8080 series-16bits

Vcc=2.4V~3.3V

Vci=2.5V~3.3V

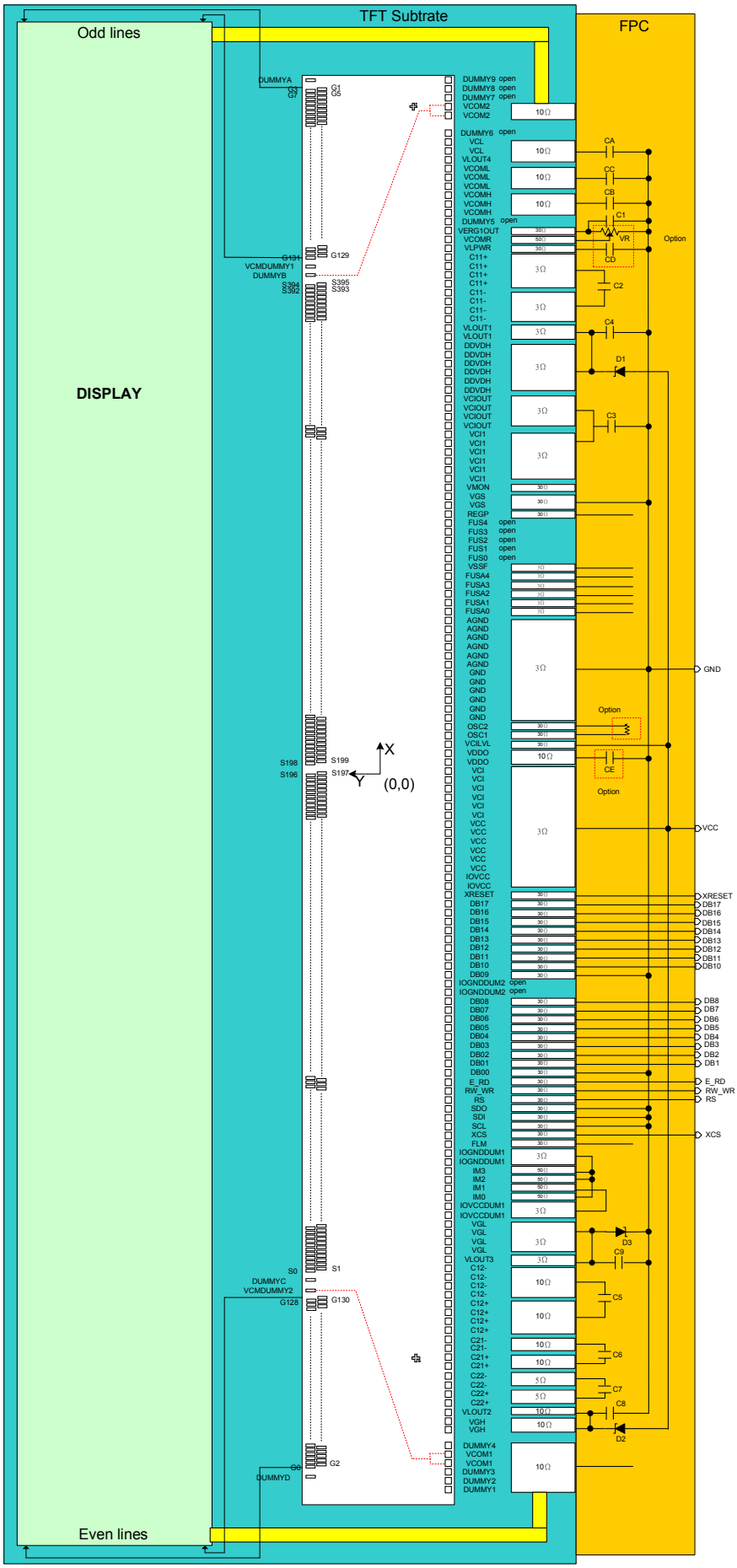
IOVCC=1.8V~3.3V

1uF(6V):C2,C3,C4,C7,CA,CB,CC,CD,CE

0.1uF(20V):C5,C6,C8,C9

Shot key diode (VF<0.4V/20mA at 25 ℃ VR>=30V)

VR>200KΩ



Interface: 8080 series-9bits

Vcc=2.4V~3.3V

Vci=2.5V~3.3V

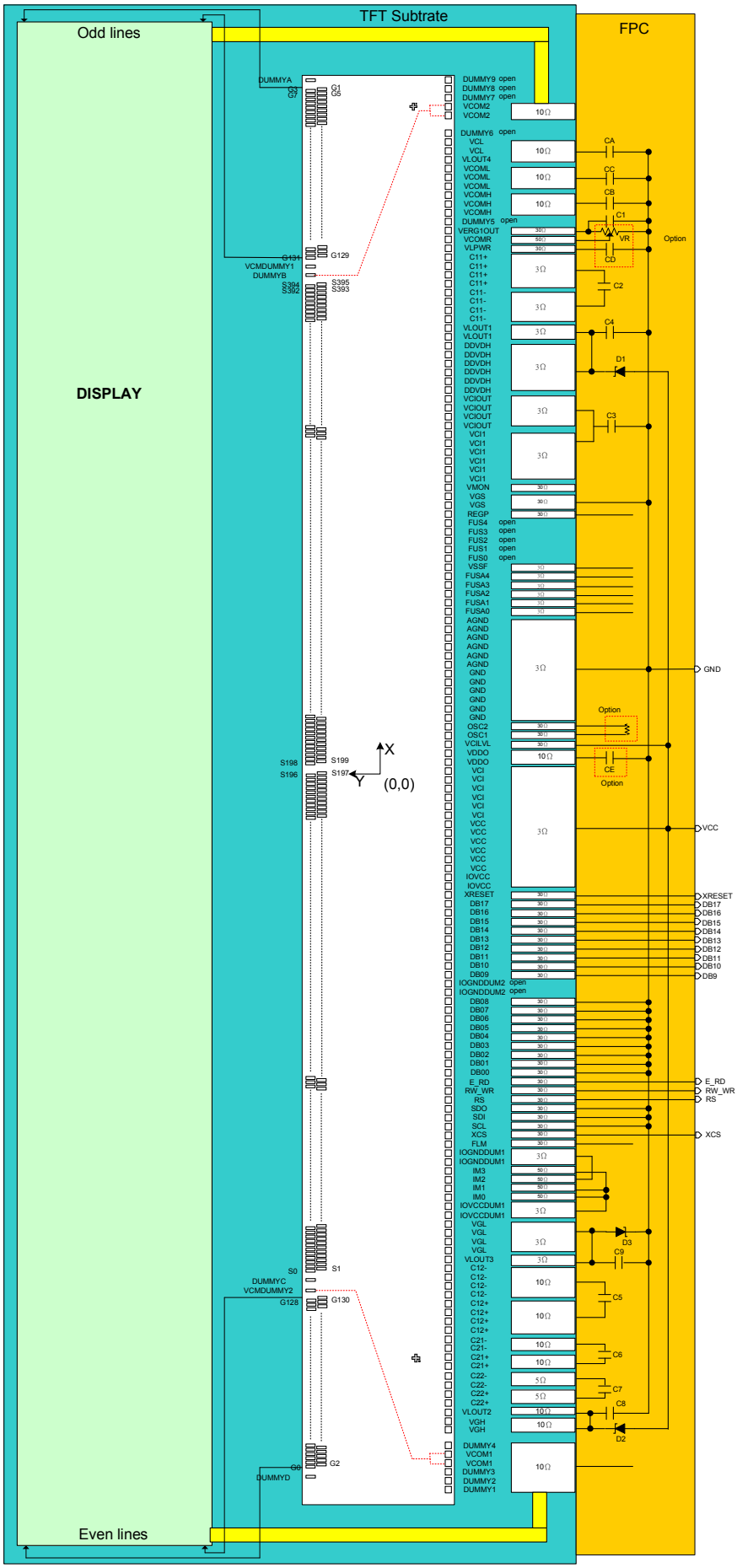
IOVCC=1.8V~3.3V

1uF(6V):C2,C3,C4,C7,CA,CB,CC,CD,CE

0.1uF(20V):C5,C6,C8,C9

Shot key diode (VF<0.4V/20mA at 25 ℃ VR>=30V)

VR>200KΩ



Interface: 8080 series-8bits

Vcc=2.4V~3.3V

Vci=2.5V~3.3V

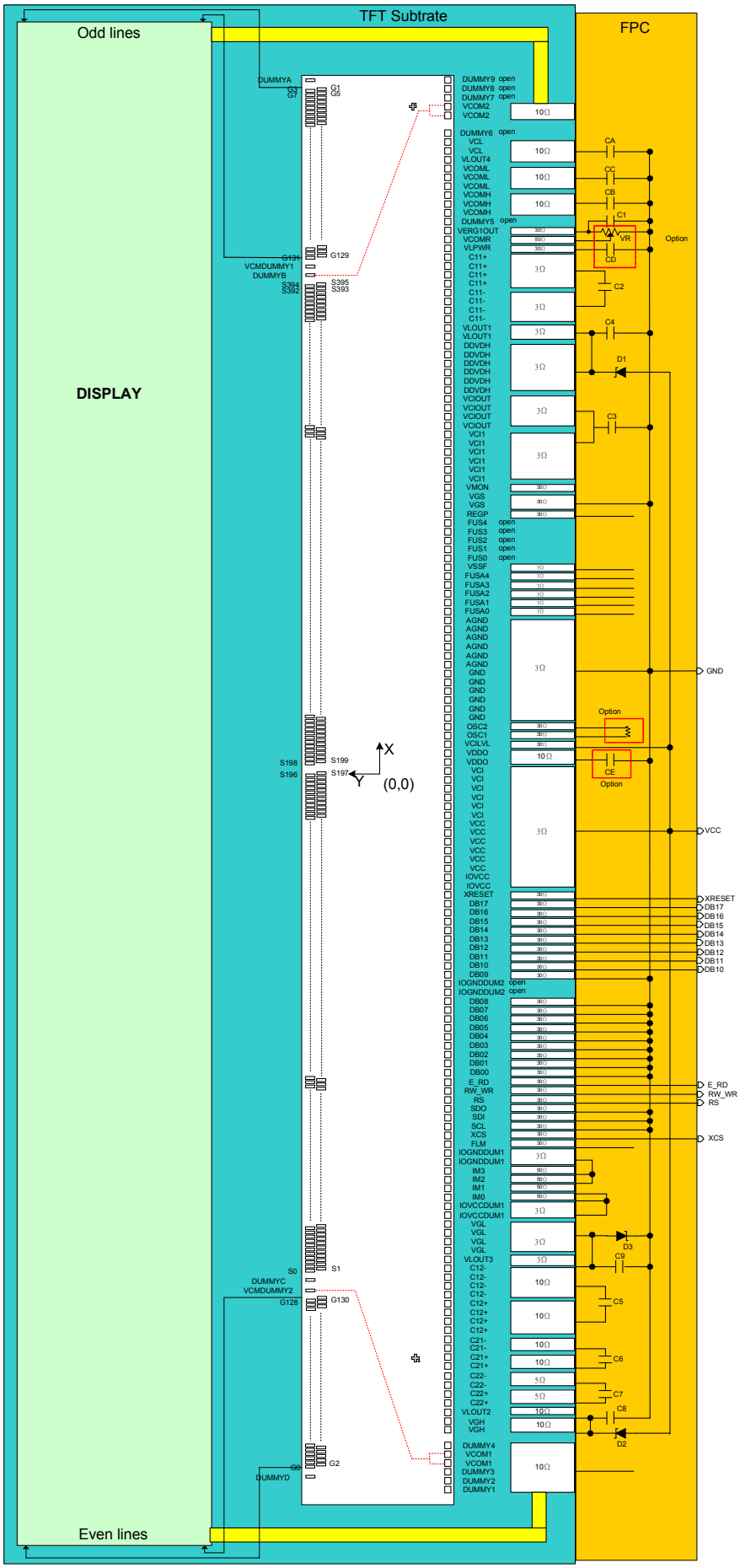
IOVCC=1.8V~3.3V

1uF(6V):C2,C3,C4,C7,CA,CB,CC,CD,CE

0.1uF(20V):C5,C6,C8,C9

Shot key diode (VF<0.4V/20mA at 25 ℃ VR>=30V)

VR>200KΩ



Interface: 6800 series-18bits

Vcc=2.4V~3.3V

Vci=2.5V~3.3V

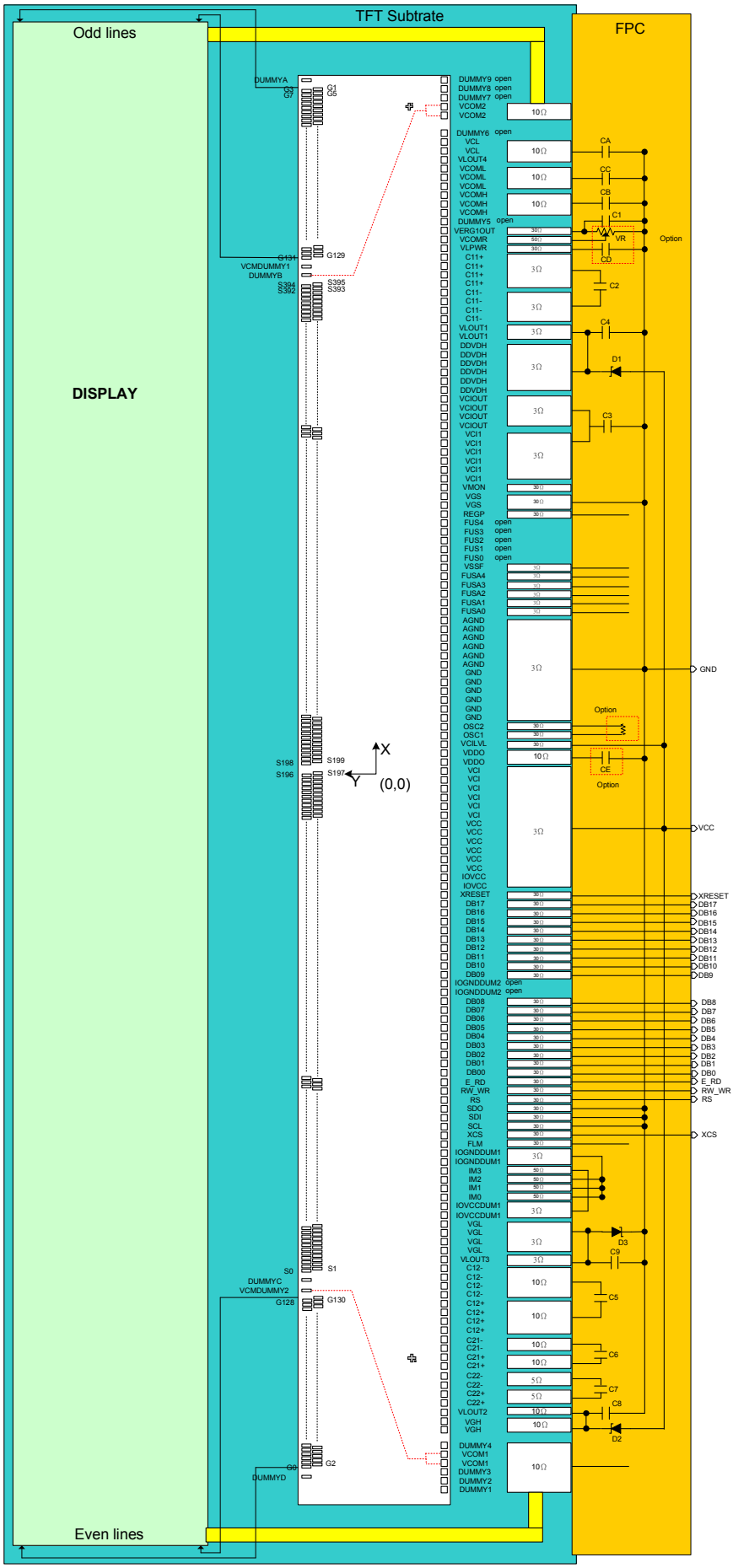
IOVCC=1.8V~3.3V

1uF(6V):C2,C3,C4,C7,CA,CB,CC,CD,CE

0.1uF(20V):C5,C6,C8,C9

Shot key diode (VF<0.4V/20mA at 25 ℃ VR>=30V)

VR>200KΩ



Interface: 6800 series-16bits

Vcc=2.4V~3.3V

Vci=2.5V~3.3V

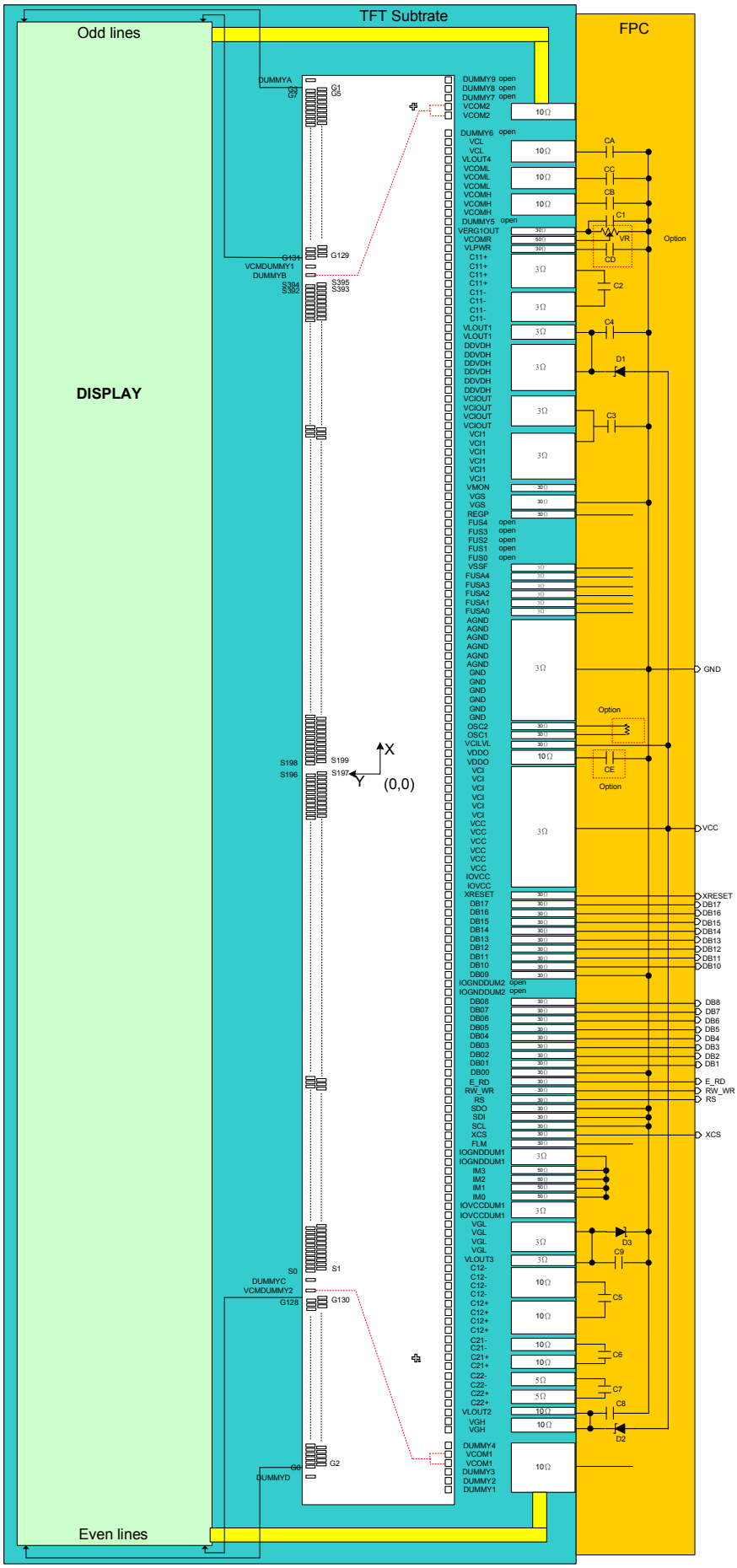
IOVCC=1.8V~3.3V

1uF(6V):C2,C3,C4,C7,CA,CB,CC,CD,CE

0.1uF(20V):C5,C6,C8,C9

Shot key diode (VF<0.4V/20mA at 25 ℃ VR>=30V)

VR>200KΩ



Interface: 6800 series-9bits

Vcc=2.4V~3.3V

Vci=2.5V~3.3V

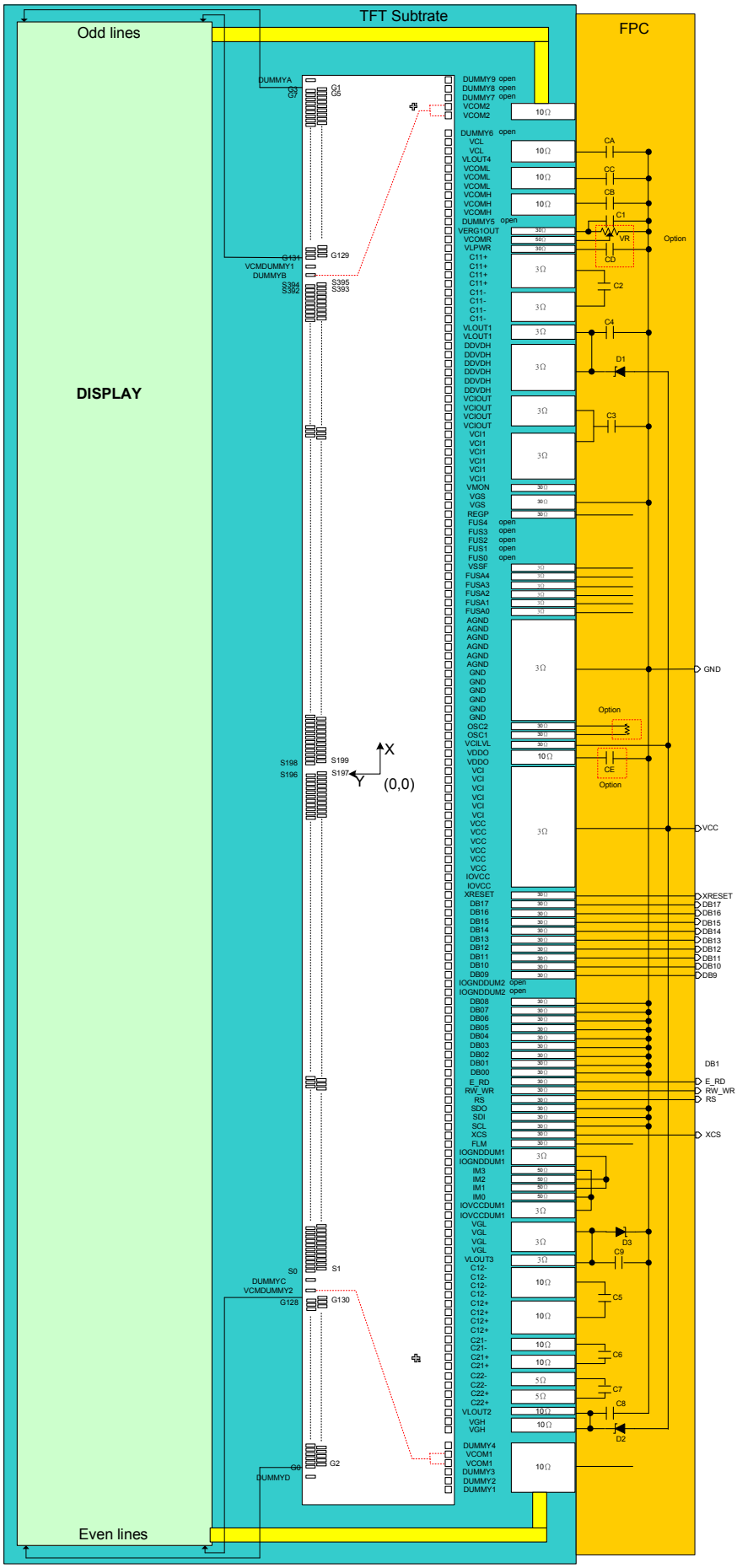
IOVCC=1.8V~3.3V

1uF(6V):C2,C3,C4,C7,CA,CB,CC,CD,CE

0.1uF(20V):C5,C6,C8,C9

Shot key diode (VF<0.4V/20mA at 25 ℃ VR>=30V)

VR>200KΩ



Interface: 6800 series-8bits

Vcc=2.4V~3.3V

Vci=2.5V~3.3V

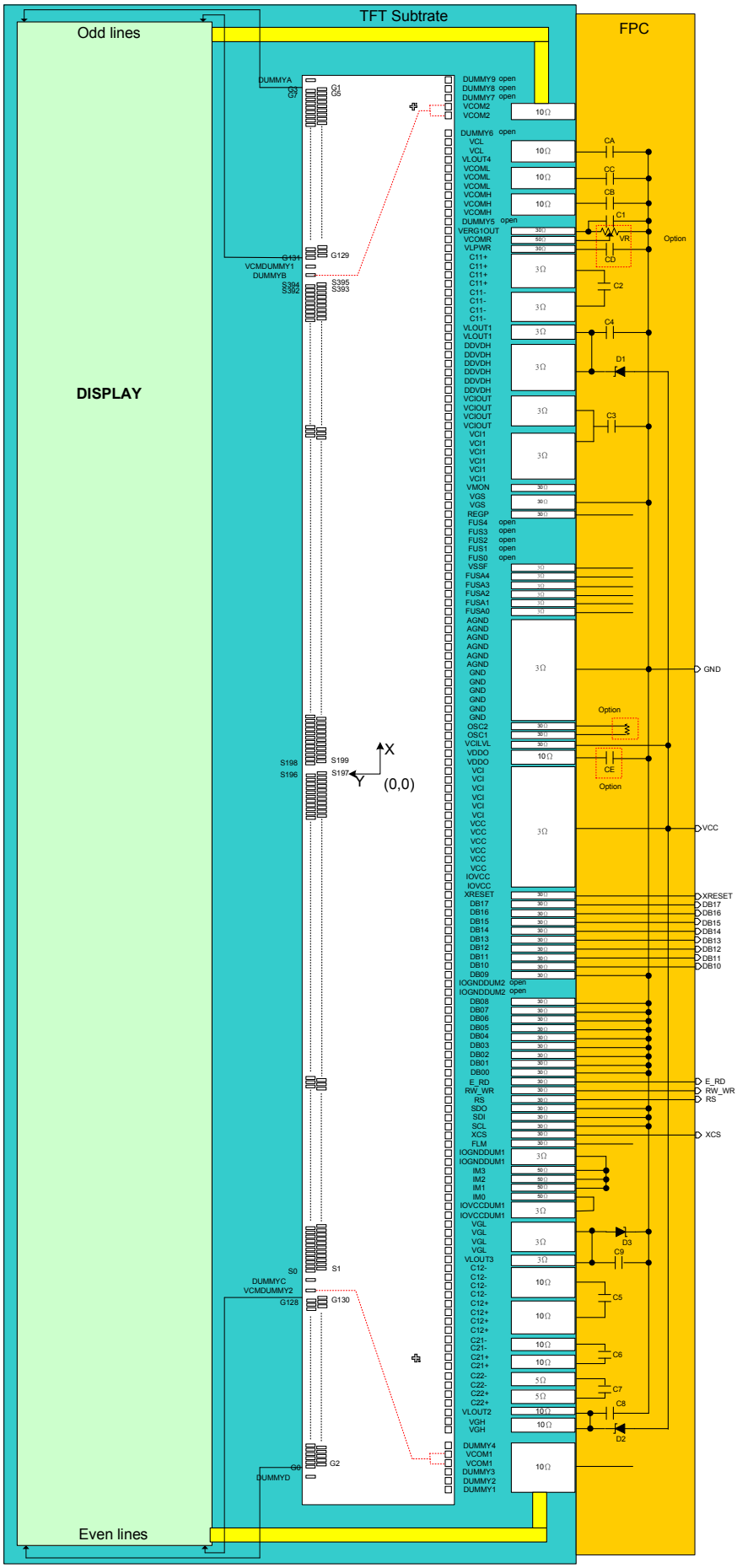
IOVCC=1.8V~3.3V

1uF(6V):C2,C3,C4,C7,CA,CB,CC,CD,CE

0.1uF(20V):C5,C6,C8,C9

Shot key diode (VF<0.4V/20mA at 25 ℃ VR>=30V)

VR>200KΩ



Interface: SPI 4-Lines

Vcc=2.4V~3.3V

Vci=2.5V~3.3V

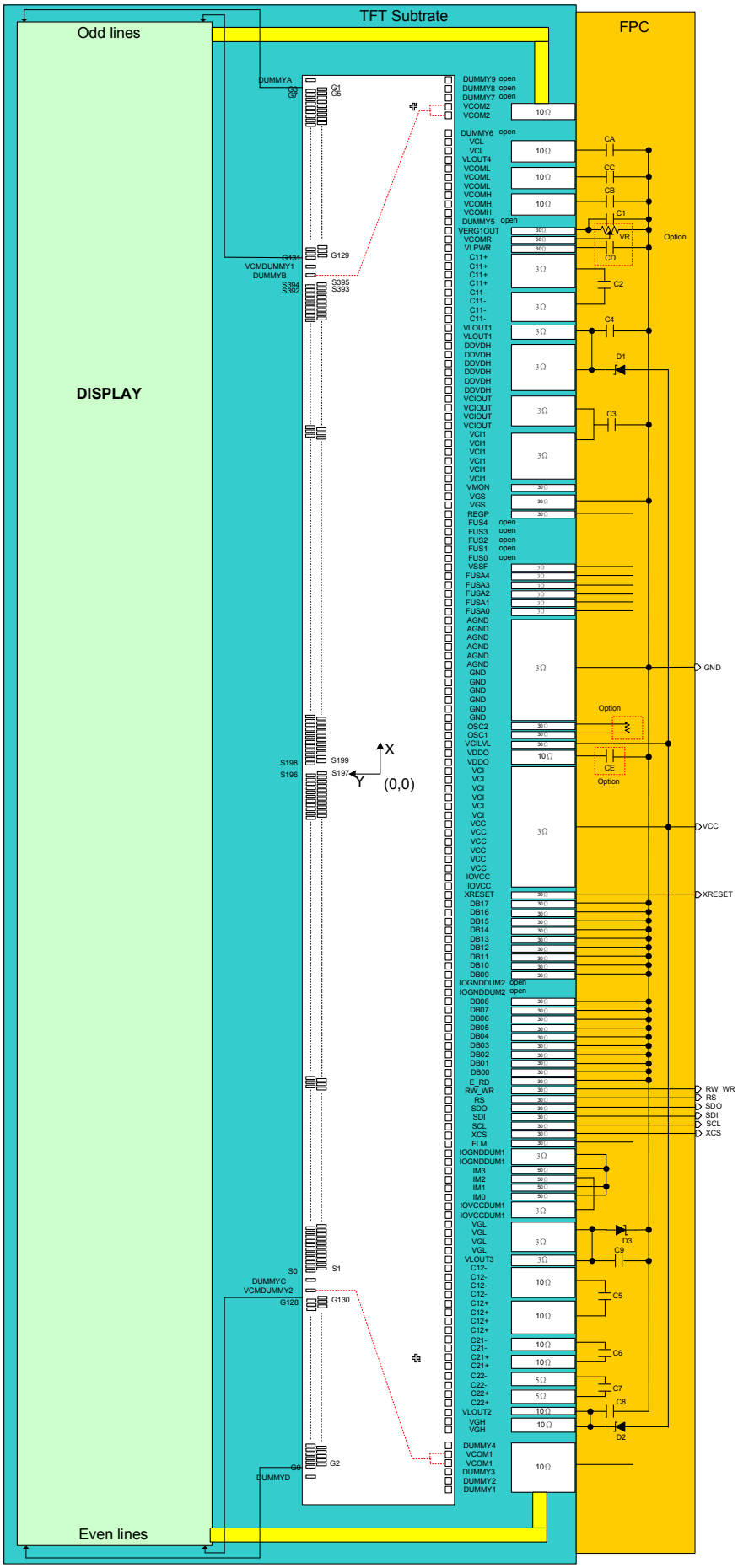
IOVCC=1.8V~3.3V

1uF(6V):C2,C3,C4,C7,CA,CB,CC,CD,CE

0.1uF(20V):C5,C6,C8,C9

Shot key diode (VF<0.4V/20mA at 25 ℃ VR>=30V)

VR>200KΩ



Interface: SPI 3-Lines

Vcc=2.4V~3.3V

Vci=2.5V~3.3V

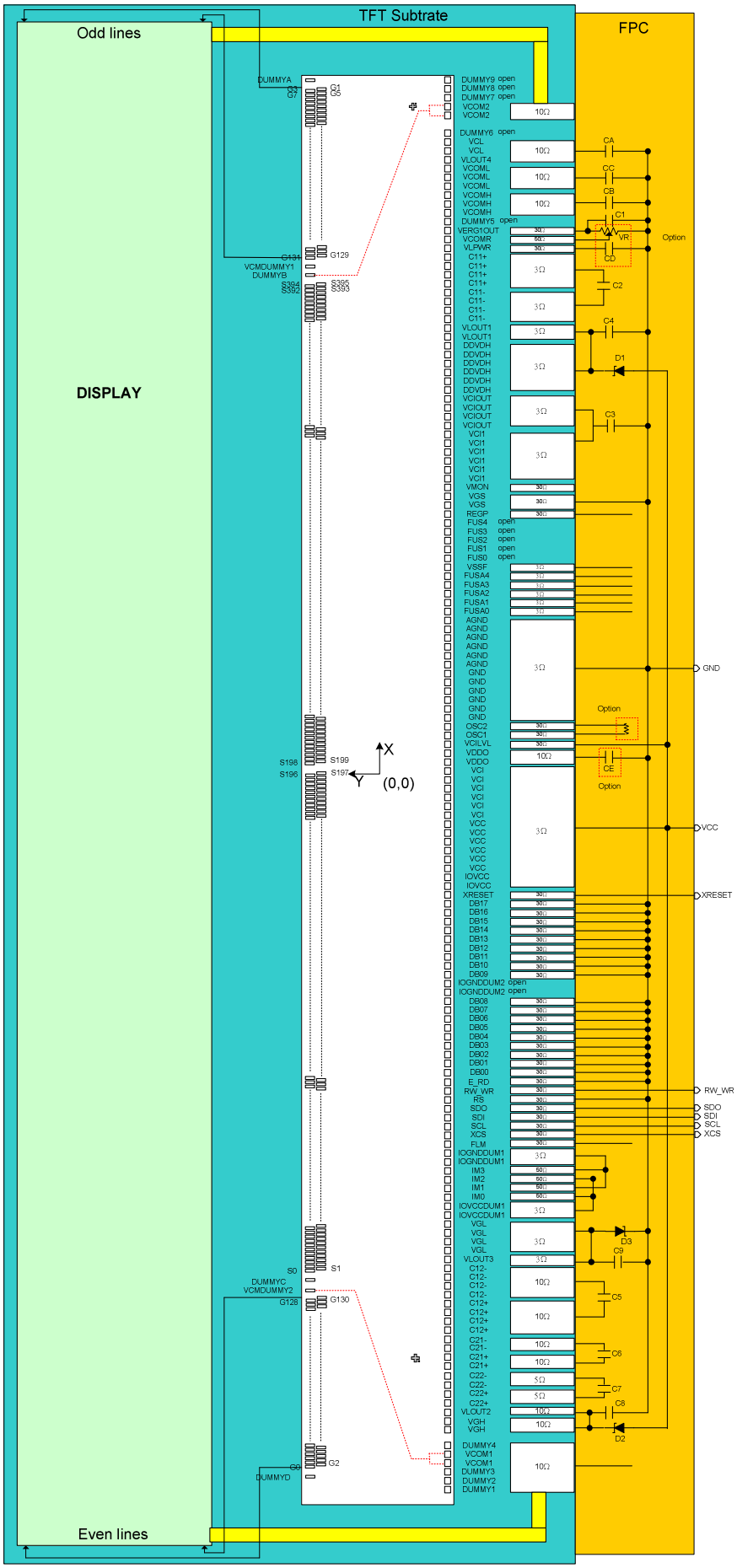
IOVCC=1.8V~3.3V

1uF(6V):C2,C3,C4,C7,CA,CB,CC,CD,CE

0.1uF(20V):C5,C6,C8,C9

Shot key diode (VF<0.4V/20mA at 25 ℃ VR>=30V)

VR>200KΩ



ST7712 Serial Specification Revision History		
Version	**Date**	**Description**
0.0	2004/7/26	Preliminary spec.
0.2f	2005/6/8	Add application notes and timing
0.2f	2005/6/8	Add Alignment mark coordinate
0.2f	2005/6/8	Add instruction flow chart and demo code
0.3a	2005/7/7	Change GVDD to VREG1OUT
0.3a	2005/7/7	Modify partial_display flow chart code
0.3a	2005/7/7	Modify STB and SLP operation code form 0x0010 to 0x0001
0.3a	2005/7/7	Modify VCM and VDV register ratio table
0.3a	2005/7/7	Delete EQ description when Vcom<0 abnormal display
0.3a	2005/7/7	Modify application circuit and add recommend OBL resistor
0.3a	2005/7/7	Add VCMDUMMY1,VCMDUMMY2/DUMMY1~DUMMY9 /DUMMYA~DUMMYD description
0.4a	2005/9/5	Add switch 8-color mode to 262,144-color mode flow chart and code
0.4a	2005/9/5	Add partial-display note
0.4a	2005/9/5	Modify partial-display flow chart
0.4a	2005/9/5	Modify DC1[2:0] and DC0[2:0] frequency
0.4a	2005/9/5	Modify Trim fuse note
0.4b	2005/9/26	Add 8 color mode data format table
0.4b	2005/9/26	Add power up command (04H)
0.4b	2005/9/26	Modify command 42H,43H set value of gate driver
0.4b	2005/9/26	Modify external capacitor(C5,C6.C8,C9) of power supply circuit range 0.1uF~1.0uF
0.4b	2005/9/26	Correct Partial_display flow chart
0.5	2005/10/3	Specification modify
0.6	2005/11/24	Modify VCM table
0.6	2005/11/24	Modify timing table and add SPI read timing
0.6	2005/11/24	Add cascade application note
0.6	2005/11/24	Modify power up command table(04H)
0.6	2005/11/24	Add BGR=1 application note
0.6	2005/11/24	Modify VOH/VOL specification table
0.6	2005/11/24	Add option test capacitance notes in Application circuit
0.6	2005/11/24	Modify internal signals of read mode

1.0	2006/01/04	VRH table modify
1.0	2006/01/04	Modify Trim fuse current limitation specification
1.0	2006/01/04	Modify 8 color display flow chart
1.0	2006/01/04	Modify 8 color mode and partial display current specification
1.0	2006/01/04	Modify SLP and STB example code setting value
1.1	2006/1/19	Modify SLP and STB flow chart
1.1	2006/1/19	Modify Initial Code Setting Flow Chart remark
1.1	2006/1/19	Add Power Supply Setting Flow
1.1	2006/1/19	Modify SLP and STB current maximum value
1.2	2006/5/10	Delete external resistor table and add application notes
1.2	2006/5/10	Disable SDT=1 colocks register value
1.2	2006/5/10	Add trim fuse connect diagram
2.0	2006/6/16	Delet example initial code setting. Please refer to application notes
2.0	2006/6/16	Modify Chip thickness 381±25um→400±25um and Bump heigh 17±3um→15±3um
2.1	2006/7/4	Modify Figure 7.2.1 timing chart
2.1	2006/7/4	Modify 12.The MCU interface(reference sample) Data pin defind of IC side
2.1	2006/7/4	Modify 13. Application circuit the node of C1
2.2	2006/7/7	Modify SDO direction of Block diagram
2.3	2007/7/19	Correct I/O pad size