1. INTRODUCTION

ST7579 is a driver & controller LSI for graphic dot-matrix liquid crystal display systems. It contains 102-segment and 67-common with 1-icon-common driver circuits. This chip is connected directly to a microprocessor which accepts 3-line or 4-line serial peripheral interface (SPI) or 8-bit parallel interface. Display data stores in an on-chip display data RAM (DDRAM) of 68 x 102 bits. It performs display data RAM read/write operation with no external operating clock to minimize power consumption. In addition, because it contains power supply circuits to drive liquid crystal, it is possible to make a display system with the fewest components.

2. FEATURES

Single-chip LCD Controller & Driver

Driver Output Circuits

102-segment / 67-common+1-icon-common (1/68 duty)

102-segment / 32-common+1-icon-common (1/33 duty)

102-segment / 16-common+1-icon-common (1/17 duty)

(1/33 duty and 1/17 duty are under partial screen mode)

On-chip Display Data Ram

- Capacity: 68X102=6,936 bits

Microprocessor Interface

- 8-bit parallel bi-directional interface supports 6800-series or 8080-series MPU
- 3-line & 4-line SPI (serial peripheral interface) are available (write only)

External RESB (reset) pin

Built-in oscillation circuit

- Oscillator requires no external component

Low Power Consumption Analog Circuit

- Voltage booster (X3, X4, X5)
- Voltage regulator generates LCD operating voltage (Temperature Gradient: -0.11%/°C)
- Electronic contrast control (255 steps)
- Voltage follower generates LCD bias voltages (1/4 ~ 1/11 bias)

Wide supply voltage range

- VDD1 – VSS1 : 1.8 ~ 3.3V
- VDD2 – VSS2 : 2.4 ~ 3.3V

Display supply voltage range

- Application Vop range : 4V ~ 9.5V
- Programmable voltage (Vop) : 10.56V (max)

Temperature range: -30 to +85 °C

Support LCD Module Size up to 1.8”

3-1. ST7579 Pad Arrangement

Chip Size: 5570 um ×770 um

Bump Height: 15 um

Chip Thickness: 480 um

Bump Pitch: (minimum) **Unit: um**

PAD Number	Pitch	PAD Number	Pitch
1~27, 130~156, 157~163, 243~250	37.20	212~213	48.59
28~129	33.00	213~216,218~221	33.30
27~28	62.91	216~217,217~218	38.80
129~130	60.70	221~222	46.31
163~164	329.58	228~229	66.44
164~207, 208~211,222~228,229~235,236~242	59.30	235~236	62.45
207~208	131.84	242~243	79.90
211~212	69.36		

*** Refer to “Pad Center Coordinates” section for ITO layout.**

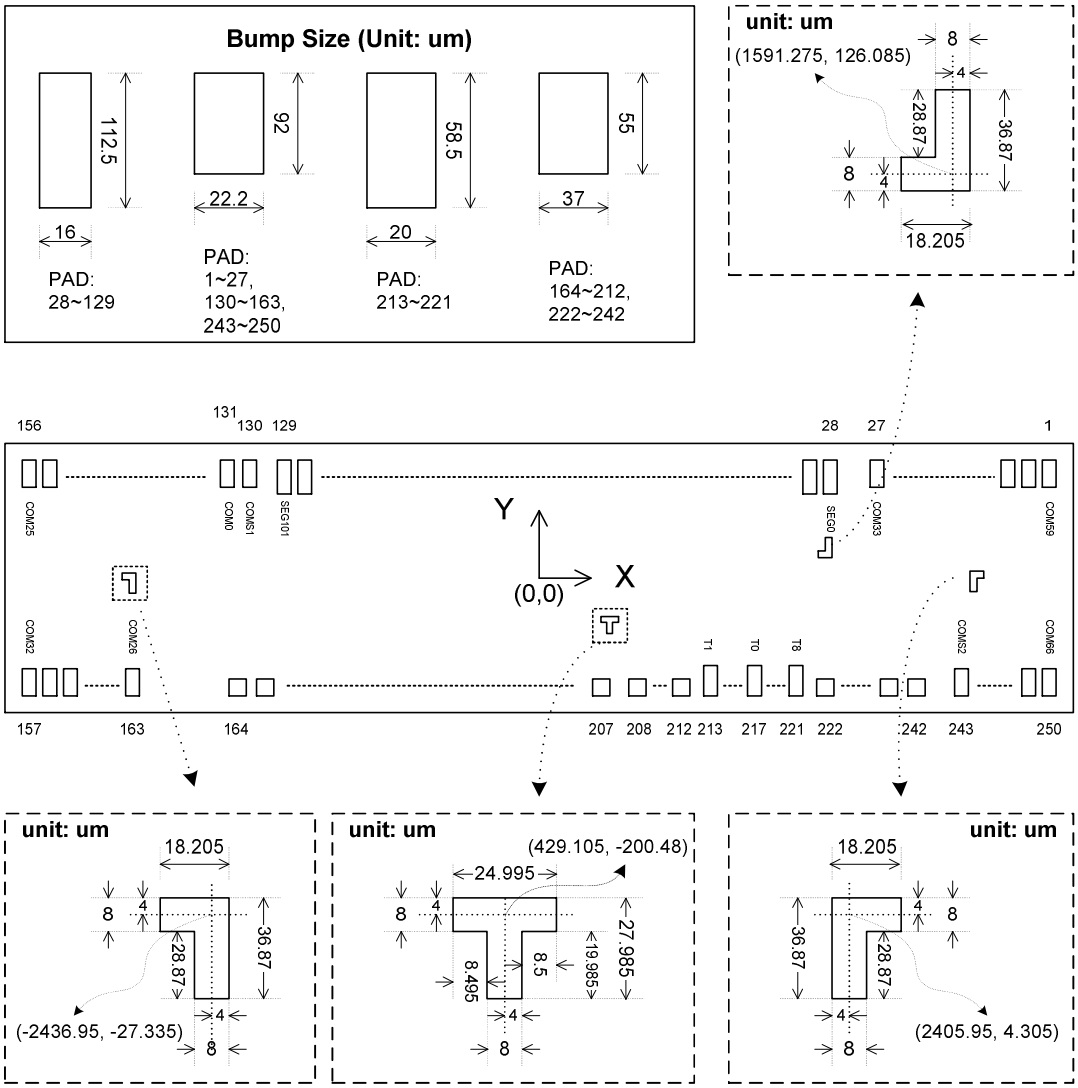


Fig 1.

3-2. Pad Center Coordinates

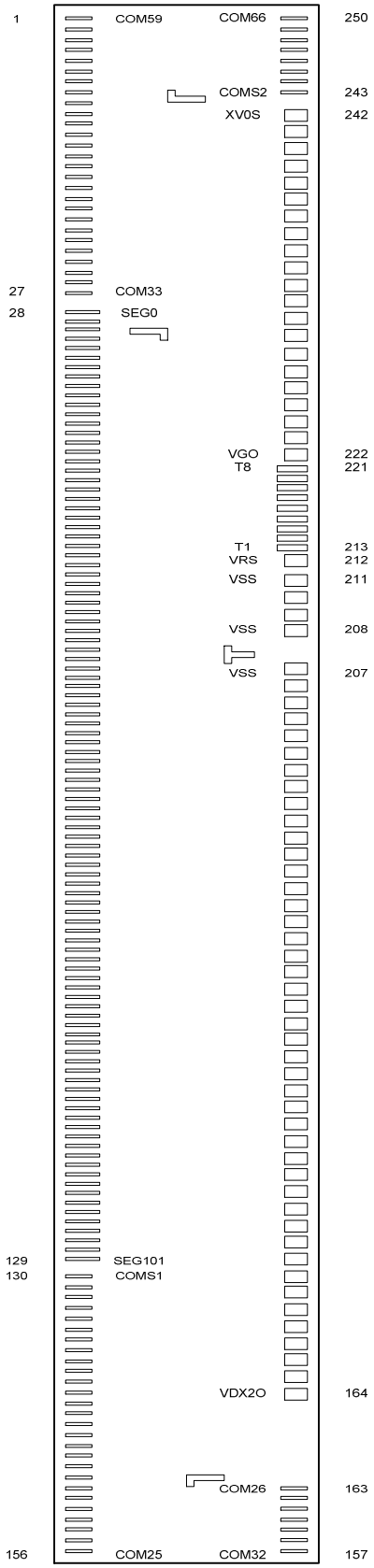


Fig 2. MX=0, MY=0

68 Duty (MY=0)

PAD NO.	PIN Name	X	Y
1	COM[59]	2695.50	293.00
2	COM[58]	2658.30	293.00
3	COM[57]	2621.10	293.00
4	COM[56]	2583.90	293.00
5	COM[55]	2546.70	293.00
6	COM[54]	2509.50	293.00
7	COM[53]	2472.30	293.00
8	COM[52]	2435.10	293.00
9	COM[51]	2397.90	293.00
10	COM[50]	2360.70	293.00
11	COM[49]	2323.50	293.00
12	COM[48]	2286.30	293.00
13	COM[47]	2249.10	293.00
14	COM[46]	2211.90	293.00
15	COM[45]	2174.70	293.00
16	COM[44]	2137.50	293.00
17	COM[43]	2100.30	293.00
18	COM[42]	2063.10	293.00
19	COM[41]	2025.90	293.00
20	COM[40]	1988.70	293.00
21	COM[39]	1951.50	293.00
22	COM[38]	1914.30	293.00
23	COM[37]	1877.10	293.00
24	COM[36]	1839.90	293.00
25	COM[35]	1802.70	293.00
26	COM[34]	1765.50	293.00
27	COM[33]	1728.30	293.00
28	SEG[0]	1665.39	282.75
29	SEG[1]	1632.39	282.75
30	SEG[2]	1599.39	282.75

PAD NO.	PIN Name	X	Y
31	SEG[3]	1566.39	282.75
32	SEG[4]	1533.39	282.75
33	SEG[5]	1500.39	282.75
34	SEG[6]	1467.39	282.75
35	SEG[7]	1434.39	282.75
36	SEG[8]	1401.39	282.75
37	SEG[9]	1368.39	282.75
38	SEG[10]	1335.39	282.75
39	SEG[11]	1302.39	282.75
40	SEG[12]	1269.39	282.75
41	SEG[13]	1236.39	282.75
42	SEG[14]	1203.39	282.75
43	SEG[15]	1170.39	282.75
44	SEG[16]	1137.39	282.75
45	SEG[17]	1104.39	282.75
46	SEG[18]	1071.39	282.75
47	SEG[19]	1038.39	282.75
48	SEG[20]	1005.39	282.75
49	SEG[21]	972.39	282.75
50	SEG[22]	939.39	282.75
51	SEG[23]	906.39	282.75
52	SEG[24]	873.39	282.75
53	SEG[25]	840.39	282.75
54	SEG[26]	807.39	282.75
55	SEG[27]	774.39	282.75
56	SEG[28]	741.39	282.75
57	SEG[29]	708.39	282.75
58	SEG[30]	675.39	282.75
59	SEG[31]	642.39	282.75
60	SEG[32]	609.39	282.75

PAD NO.	PIN Name	X	Y
61	SEG[33]	576.39	282.75
62	SEG[34]	543.39	282.75
63	SEG[35]	510.39	282.75
64	SEG[36]	477.39	282.75
65	SEG[37]	444.39	282.75
66	SEG[38]	411.39	282.75
67	SEG[39]	378.39	282.75
68	SEG[40]	345.39	282.75
69	SEG[41]	312.39	282.75
70	SEG[42]	279.39	282.75
71	SEG[43]	246.39	282.75
72	SEG[44]	213.39	282.75
73	SEG[45]	180.39	282.75
74	SEG[46]	147.39	282.75
75	SEG[47]	114.39	282.75
76	SEG[48]	81.39	282.75
77	SEG[49]	48.39	282.75
78	SEG[50]	15.39	282.75
79	SEG[51]	-17.60	282.75
80	SEG[52]	-50.60	282.75
81	SEG[53]	-83.60	282.75
82	SEG[54]	-116.60	282.75
83	SEG[55]	-149.60	282.75
84	SEG[56]	-182.60	282.75
85	SEG[57]	-215.60	282.75
86	SEG[58]	-248.60	282.75
87	SEG[59]	-281.60	282.75
88	SEG[60]	-314.60	282.75
89	SEG[61]	-347.60	282.75
90	SEG[62]	-380.60	282.75

PAD NO.	PIN Name	X	Y
91	SEG[63]	-413.60	282.75
92	SEG[64]	-446.60	282.75
93	SEG[65]	-479.60	282.75
94	SEG[66]	-512.60	282.75
95	SEG[67]	-545.60	282.75
96	SEG[68]	-578.60	282.75
97	SEG[69]	-611.60	282.75
98	SEG[70]	-644.60	282.75
99	SEG[71]	-677.60	282.75
100	SEG[72]	-710.60	282.75
101	SEG[73]	-743.60	282.75
102	SEG[74]	-776.60	282.75
103	SEG[75]	-809.60	282.75
104	SEG[76]	-842.60	282.75
105	SEG[77]	-875.60	282.75
106	SEG[78]	-908.60	282.75
107	SEG[79]	-941.60	282.75
108	SEG[80]	-974.60	282.75
109	SEG[81]	-1007.60	282.75
110	SEG[82]	-1040.60	282.75
111	SEG[83]	-1073.60	282.75
112	SEG[84]	-1106.60	282.75
113	SEG[85]	-1139.60	282.75
114	SEG[86]	-1172.60	282.75
115	SEG[87]	-1205.60	282.75
116	SEG[88]	-1238.60	282.75
117	SEG[89]	-1271.60	282.75
118	SEG[90]	-1304.60	282.75
119	SEG[91]	-1337.60	282.75
120	SEG[92]	-1370.60	282.75

PAD NO.	PIN Name	X	Y
121	SEG[93]	-1403.60	282.75
122	SEG[94]	-1436.60	282.75
123	SEG[95]	-1469.60	282.75
124	SEG[96]	-1502.60	282.75
125	SEG[97]	-1535.60	282.75
126	SEG[98]	-1568.60	282.75
127	SEG[99]	-1601.60	282.75
128	SEG[100]	-1634.60	282.75
129	SEG[101]	-1667.60	282.75
130	COMS1	-1728.30	293.00
131	COM[0]	-1765.50	293.00
132	COM[1]	-1802.70	293.00
133	COM[2]	-1839.90	293.00
134	COM[3]	-1877.10	293.00
135	COM[4]	-1914.30	293.00
136	COM[5]	-1951.50	293.00
137	COM[6]	-1988.70	293.00
138	COM[7]	-2025.90	293.00
139	COM[8]	-2063.10	293.00
140	COM[9]	-2100.30	293.00
141	COM[10]	-2137.50	293.00
142	COM[11]	-2174.70	293.00
143	COM[12]	-2211.90	293.00
144	COM[13]	-2249.10	293.00
145	COM[14]	-2286.30	293.00
146	COM[15]	-2323.50	293.00
147	COM[16]	-2360.70	293.00
148	COM[17]	-2397.90	293.00
149	COM[18]	-2435.10	293.00
150	COM[19]	-2472.30	293.00

PAD NO.	PIN Name	X	Y
151	COM[20]	-2509.50	293.00
152	COM[21]	-2546.70	293.00
153	COM[22]	-2583.90	293.00
154	COM[23]	-2621.10	293.00
155	COM[24]	-2658.30	293.00
156	COM[25]	-2695.50	293.00
157	COM[32]	-2695.50	-293.00
158	COM[31]	-2658.30	-293.00
159	COM[30]	-2621.10	-293.00
160	COM[29]	-2583.90	-293.00
161	COM[28]	-2546.70	-293.00
162	COM[27]	-2509.50	-293.00
163	COM[26]	-2472.30	-293.00
164	VDX2O	-2142.72	-311.50
165	VDX2O	-2083.42	-311.50
166	VDX2O	-2024.11	-311.50
167	VSS1	-1964.81	-311.50
168	T11	-1905.50	-311.50
169	T12	-1846.19	-311.50
170	BR	-1786.89	-311.50
171	CP	-1727.58	-311.50
172	T9	-1668.28	-311.50
173	T10	-1608.97	-311.50
174	PS2	-1549.67	-311.50
175	PS1	-1490.36	-311.50
176	PS0	-1431.06	-311.50
177	VMO	-1371.75	-311.50
178	VMO	-1312.45	-311.50
179	VMO	-1253.14	-311.50
180	VSS1	-1193.84	-311.50

PAD NO.	PIN Name	X	Y
181	VDD1	-1134.54	-311.50
182	VDD1	-1075.23	-311.50
183	VDD1	-1015.92	-311.50
184	VDD1	-956.62	-311.50
185	VDD2	-897.32	-311.50
186	VDD2	-838.01	-311.50
187	VDD2	-778.70	-311.50
188	VDD2	-719.40	-311.50
189	RESB	-660.09	-311.50
190	CSB	-600.79	-311.50
191	RWR	-541.48	-311.50
192	ERD	-482.18	-311.50
193	A0	-422.88	-311.50
194	VDD1	-363.57	-311.50
195	D7	-304.27	-311.50
196	D6	-244.96	-311.50
197	D5	-185.66	-311.50
198	D4	-126.35	-311.50
199	D3	-67.05	-311.50
200	D2	-7.74	-311.50
201	D1	51.56	-311.50
202	D0	110.87	-311.50
203	OSC	170.17	-311.50
204	VSS2	229.47	-311.50
205	VSS2	288.78	-311.50
206	VSS2	348.09	-311.50
207	VSS2	407.39	-311.50
208	VSS1	539.23	-311.50
209	VSS1	598.53	-311.50
210	VSS1	657.84	-311.50

PAD NO.	PIN Name	X	Y
211	VSS1	717.15	-311.50
212	VRS	786.51	-311.50
213	T1	835.10	-307.75
214	T2	868.40	-307.75
215	T3	901.70	-307.75
216	T4	935.00	-307.75
217	T0	973.80	-307.75
218	T5	1012.60	-307.75
219	T6	1045.90	-307.75
220	T7	1079.20	-307.75
221	T8	1112.50	-307.75
222	VGO	1158.81	-311.50
223	VGO	1218.11	-311.50
224	VGI	1277.42	-311.50
225	VGI	1336.72	-311.50
226	VGI	1396.03	-311.50
227	VGI	1455.33	-311.50
228	VGS	1514.64	-311.50
229	V0O	1581.08	-309.75
230	V0O	1640.38	-309.75
231	V0I	1699.69	-309.75
232	V0I	1759.00	-309.75
233	V0I	1818.30	-309.75
234	V0I	1877.60	-311.50
235	V0S	1936.91	-311.50
236	XV0O	1999.36	-311.50
237	XV0O	2058.67	-311.50
238	XV0I	2117.98	-311.50
239	XV0I	2177.28	-311.50
240	XV0I	2236.58	-311.50

PAD NO.	PIN Name	X	Y
241	XV0I	2295.89	-311.50
242	XV0S	2355.20	-311.50
243	COMS2	2435.10	-293.00
244	COM[60]	2472.30	-293.00
245	COM[61]	2509.50	-293.00
246	COM[62]	2546.70	-293.00
247	COM[63]	2583.90	-293.00
248	COM[64]	2621.10	-293.00
249	COM[65]	2658.30	-293.00
250	COM[66]	2695.50	-293.00

68 Duty (MY=1)

PAD NO.	PIN Name	X	Y
1	COM[7]	2695.50	293.00
2	COM[8]	2658.30	293.00
3	COM[9]	2621.10	293.00
4	COM[10]	2583.90	293.00
5	COM[11]	2546.70	293.00
6	COM[12]	2509.50	293.00
7	COM[13]	2472.30	293.00
8	COM[14]	2435.10	293.00
9	COM[15]	2397.90	293.00
10	COM[16]	2360.70	293.00
11	COM[17]	2323.50	293.00
12	COM[18]	2286.30	293.00
13	COM[19]	2249.10	293.00
14	COM[20]	2211.90	293.00
15	COM[21]	2174.70	293.00
16	COM[22]	2137.50	293.00
17	COM[23]	2100.30	293.00
18	COM[24]	2063.10	293.00
19	COM[25]	2025.90	293.00
20	COM[26]	1988.70	293.00
21	COM[27]	1951.50	293.00
22	COM[28]	1914.30	293.00
23	COM[29]	1877.10	293.00
24	COM[30]	1839.90	293.00
25	COM[31]	1802.70	293.00
26	COM[32]	1765.50	293.00
27	COM[33]	1728.30	293.00
28	SEG[0]	1665.39	282.75
29	SEG[1]	1632.39	282.75
30	SEG[2]	1599.39	282.75

PAD NO.	PIN Name	X	Y
31	SEG[3]	1566.39	282.75
32	SEG[4]	1533.39	282.75
33	SEG[5]	1500.39	282.75
34	SEG[6]	1467.39	282.75
35	SEG[7]	1434.39	282.75
36	SEG[8]	1401.39	282.75
37	SEG[9]	1368.39	282.75
38	SEG[10]	1335.39	282.75
39	SEG[11]	1302.39	282.75
40	SEG[12]	1269.39	282.75
41	SEG[13]	1236.39	282.75
42	SEG[14]	1203.39	282.75
43	SEG[15]	1170.39	282.75
44	SEG[16]	1137.39	282.75
45	SEG[17]	1104.39	282.75
46	SEG[18]	1071.39	282.75
47	SEG[19]	1038.39	282.75
48	SEG[20]	1005.39	282.75
49	SEG[21]	972.39	282.75
50	SEG[22]	939.39	282.75
51	SEG[23]	906.39	282.75
52	SEG[24]	873.39	282.75
53	SEG[25]	840.39	282.75
54	SEG[26]	807.39	282.75
55	SEG[27]	774.39	282.75
56	SEG[28]	741.39	282.75
57	SEG[29]	708.39	282.75
58	SEG[30]	675.39	282.75
59	SEG[31]	642.39	282.75
60	SEG[32]	609.39	282.75

PAD NO.	PIN Name	X	Y
61	SEG[33]	576.39	282.75
62	SEG[34]	543.39	282.75
63	SEG[35]	510.39	282.75
64	SEG[36]	477.39	282.75
65	SEG[37]	444.39	282.75
66	SEG[38]	411.39	282.75
67	SEG[39]	378.39	282.75
68	SEG[40]	345.39	282.75
69	SEG[41]	312.39	282.75
70	SEG[42]	279.39	282.75
71	SEG[43]	246.39	282.75
72	SEG[44]	213.39	282.75
73	SEG[45]	180.39	282.75
74	SEG[46]	147.39	282.75
75	SEG[47]	114.39	282.75
76	SEG[48]	81.39	282.75
77	SEG[49]	48.39	282.75
78	SEG[50]	15.39	282.75
79	SEG[51]	-17.60	282.75
80	SEG[52]	-50.60	282.75
81	SEG[53]	-83.60	282.75
82	SEG[54]	-116.60	282.75
83	SEG[55]	-149.60	282.75
84	SEG[56]	-182.60	282.75
85	SEG[57]	-215.60	282.75
86	SEG[58]	-248.60	282.75
87	SEG[59]	-281.60	282.75
88	SEG[60]	-314.60	282.75
89	SEG[61]	-347.60	282.75
90	SEG[62]	-380.60	282.75

PAD NO.	PIN Name	X	Y
91	SEG[63]	-413.60	282.75
92	SEG[64]	-446.60	282.75
93	SEG[65]	-479.60	282.75
94	SEG[66]	-512.60	282.75
95	SEG[67]	-545.60	282.75
96	SEG[68]	-578.60	282.75
97	SEG[69]	-611.60	282.75
98	SEG[70]	-644.60	282.75
99	SEG[71]	-677.60	282.75
100	SEG[72]	-710.60	282.75
101	SEG[73]	-743.60	282.75
102	SEG[74]	-776.60	282.75
103	SEG[75]	-809.60	282.75
104	SEG[76]	-842.60	282.75
105	SEG[77]	-875.60	282.75
106	SEG[78]	-908.60	282.75
107	SEG[79]	-941.60	282.75
108	SEG[80]	-974.60	282.75
109	SEG[81]	-1007.60	282.75
110	SEG[82]	-1040.60	282.75
111	SEG[83]	-1073.60	282.75
112	SEG[84]	-1106.60	282.75
113	SEG[85]	-1139.60	282.75
114	SEG[86]	-1172.60	282.75
115	SEG[87]	-1205.60	282.75
116	SEG[88]	-1238.60	282.75
117	SEG[89]	-1271.60	282.75
118	SEG[90]	-1304.60	282.75
119	SEG[91]	-1337.60	282.75
120	SEG[92]	-1370.60	282.75

PAD NO.	PIN Name	X	Y
121	SEG[93]	-1403.60	282.75
122	SEG[94]	-1436.60	282.75
123	SEG[95]	-1469.60	282.75
124	SEG[96]	-1502.60	282.75
125	SEG[97]	-1535.60	282.75
126	SEG[98]	-1568.60	282.75
127	SEG[99]	-1601.60	282.75
128	SEG[100]	-1634.60	282.75
129	SEG[101]	-1667.60	282.75
130	COMS1	-1728.30	293.00
131	COM[66]	-1765.50	293.00
132	COM[65]	-1802.70	293.00
133	COM[64]	-1839.90	293.00
134	COM[63]	-1877.10	293.00
135	COM[62]	-1914.30	293.00
136	COM[61]	-1951.50	293.00
137	COM[660	-1988.70	293.00
138	COM[59]	-2025.90	293.00
139	COM[58]	-2063.10	293.00
140	COM[57]	-2100.30	293.00
141	COM[56]	-2137.50	293.00
142	COM[55]	-2174.70	293.00
143	COM[54]	-2211.90	293.00
144	COM[53]	-2249.10	293.00
145	COM[52]	-2286.30	293.00
146	COM[51]	-2323.50	293.00
147	COM[50]	-2360.70	293.00
148	COM[49]	-2397.90	293.00
149	COM[48]	-2435.10	293.00
150	COM[47]	-2472.30	293.00

PAD NO.	PIN Name	X	Y
151	COM[46]	-2509.50	293.00
152	COM[45]	-2546.70	293.00
153	COM[44]	-2583.90	293.00
154	COM[43]	-2621.10	293.00
155	COM[42]	-2658.30	293.00
156	COM[41]	-2695.50	293.00
157	COM[34]	-2695.50	-293.00
158	COM[35]	-2658.30	-293.00
159	COM[36]	-2621.10	-293.00
160	COM[37]	-2583.90	-293.00
161	COM[38]	-2546.70	-293.00
162	COM[39]	-2509.50	-293.00
163	COM[40]	-2472.30	-293.00
164	VDX2O	-2142.72	-311.50
165	VDX2O	-2083.42	-311.50
166	VDX2O	-2024.11	-311.50
167	VSS1	-1964.81	-311.50
168	T11	-1905.50	-311.50
169	T12	-1846.19	-311.50
170	BR	-1786.89	-311.50
171	CP	-1727.58	-311.50
172	T9	-1668.28	-311.50
173	T10	-1608.97	-311.50
174	PS2	-1549.67	-311.50
175	PS1	-1490.36	-311.50
176	PS0	-1431.06	-311.50
177	VMO	-1371.75	-311.50
178	VMO	-1312.45	-311.50
179	VMO	-1253.14	-311.50
180	VSS1	-1193.84	-311.50

PAD NO.	PIN Name	X	Y
181	VDD1	-1134.54	-311.50
182	VDD1	-1075.23	-311.50
183	VDD1	-1015.92	-311.50
184	VDD1	-956.62	-311.50
185	VDD2	-897.32	-311.50
186	VDD2	-838.01	-311.50
187	VDD2	-778.70	-311.50
188	VDD2	-719.40	-311.50
189	RESB	-660.09	-311.50
190	CSB	-600.79	-311.50
191	RWR	-541.48	-311.50
192	ERD	-482.18	-311.50
193	A0	-422.88	-311.50
194	VDD1	-363.57	-311.50
195	D7	-304.27	-311.50
196	D6	-244.96	-311.50
197	D5	-185.66	-311.50
198	D4	-126.35	-311.50
199	D3	-67.05	-311.50
200	D2	-7.74	-311.50
201	D1	51.56	-311.50
202	D0	110.87	-311.50
203	OSC	170.17	-311.50
204	VSS2	229.47	-311.50
205	VSS2	288.78	-311.50
206	VSS2	348.09	-311.50
207	VSS2	407.39	-311.50
208	VSS1	539.23	-311.50
209	VSS1	598.53	-311.50
210	VSS1	657.84	-311.50

PAD NO.	PIN Name	X	Y
211	VSS1	717.15	-311.50
212	VRS	786.51	-311.50
213	T1	835.10	-307.75
214	T2	868.40	-307.75
215	T3	901.70	-307.75
216	T4	935.00	-307.75
217	T0	973.80	-307.75
218	T5	1012.60	-307.75
219	T6	1045.90	-307.75
220	T7	1079.20	-307.75
221	T8	1112.50	-307.75
222	VGO	1158.81	-311.50
223	VGO	1218.11	-311.50
224	VGI	1277.42	-311.50
225	VGI	1336.72	-311.50
226	VGI	1396.03	-311.50
227	VGI	1455.33	-311.50
228	VGS	1514.64	-311.50
229	V0O	1581.08	-309.75
230	V0O	1640.38	-309.75
231	V0I	1699.69	-309.75
232	V0I	1759.00	-309.75
233	V0I	1818.30	-309.75
234	V0I	1877.60	-311.50
235	V0S	1936.91	-311.50
236	XV0O	1999.36	-311.50
237	XV0O	2058.67	-311.50
238	XV0I	2117.98	-311.50
239	XV0I	2177.28	-311.50
240	XV0I	2236.58	-311.50

PAD NO.	PIN Name	X	Y
241	XV0I	2295.89	-311.50
242	XV0S	2355.20	-311.50
243	COMS2	2435.10	-293.00
244	COM[6]	2472.30	-293.00
245	COM[5]	2509.50	-293.00
246	COM[4]	2546.70	-293.00
247	COM[3]	2583.90	-293.00
248	COM[2]	2621.10	-293.00
249	COM[1]	2658.30	-293.00
250	COM[0]	2695.50	-293.00

4. BLOCK DIAGRAM

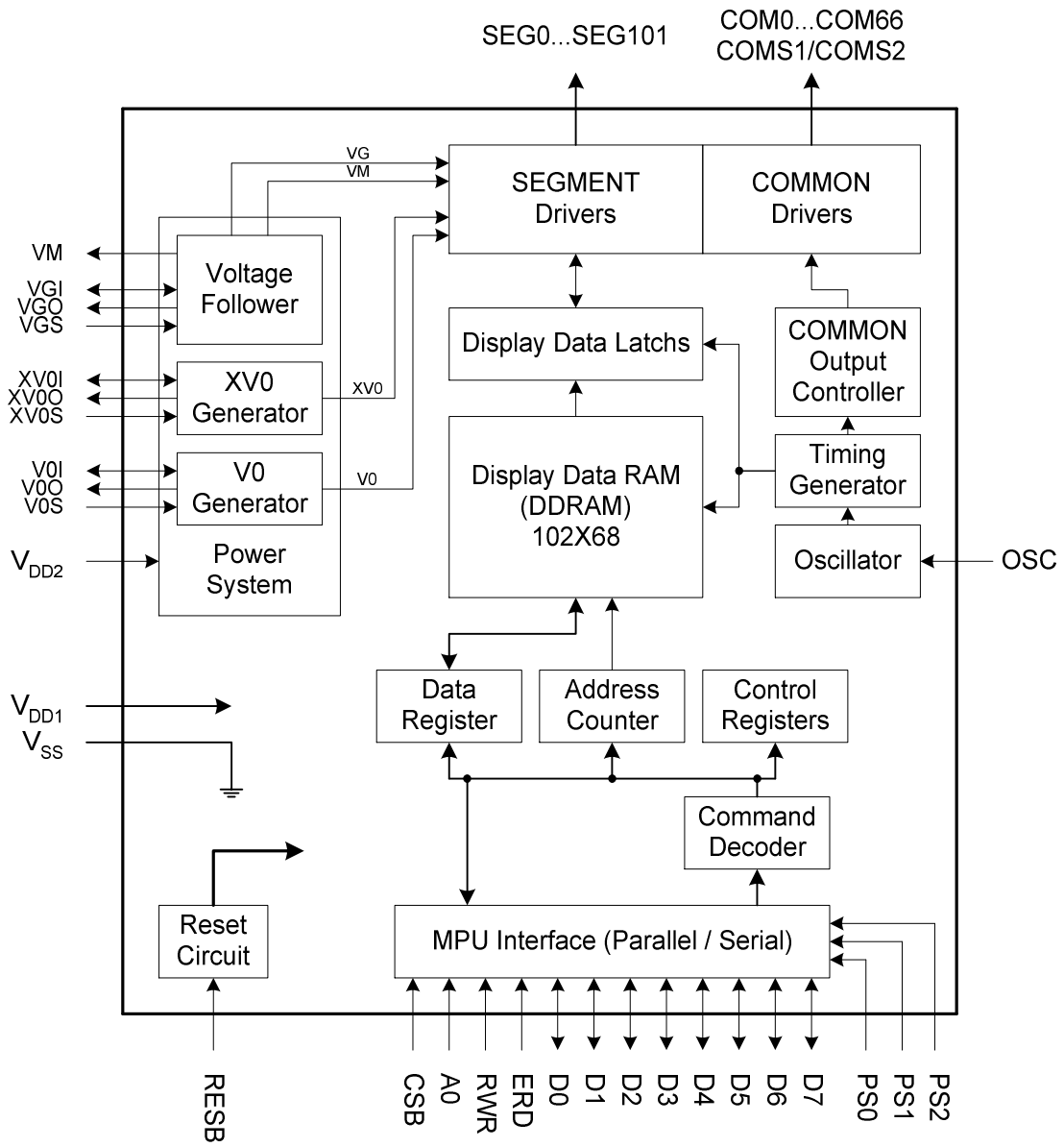


Fig 3. Block Diagram

5. PINNING DESCRIPTIONS

LCD Driver Output Pins

<table>
<tr><th>Pin Name</th><th>Type</th><th>Description</th><th>No. of Pins</th></tr>
<tr><td>SEG0 to SEG101</td><td>O</td><td>LCD segment driver outputs.
The display data and the frame control the output voltage.
<table>
<tr><th rowspan="2">Display data</th><th rowspan="2">Frame</th><th colspan="2">Segment driver output voltage</th></tr>
<tr><th>Normal display</th><th>Reverse display</th></tr>
<tr><td>H</td><td>+</td><td>VG</td><td>VSS</td></tr>
<tr><td>H</td><td>-</td><td>VSS</td><td>VG</td></tr>
<tr><td>L</td><td>+</td><td>VSS</td><td>VG</td></tr>
<tr><td>L</td><td>-</td><td>VG</td><td>VSS</td></tr>
<tr><td colspan="2">Display OFF, Power Save</td><td>VSS</td><td>VSS</td></tr>
</table></td><td>102</td></tr>
<tr><td>COM0 to COM66</td><td>O</td><td>LCD common driver outputs.
The internal scanning signal and the frame control the output voltage.
<table>
<tr><th rowspan="2">Scan signal</th><th rowspan="2">Frame</th><th colspan="2">Common driver output voltage</th></tr>
<tr><th>Normal display</th><th>Reverse display</th></tr>
<tr><td>H</td><td>+</td><td colspan="2">XV0</td></tr>
<tr><td>H</td><td>-</td><td colspan="2">V0</td></tr>
<tr><td>L</td><td>+</td><td colspan="2">VM</td></tr>
<tr><td>L</td><td>-</td><td colspan="2">VM</td></tr>
<tr><td colspan="2">Display OFF, Power Save</td><td colspan="2">VSS</td></tr>
</table></td><td>67</td></tr>
<tr><td>COMS1,COMS2
(COMS)</td><td>O</td><td>LCD common driver outputs for icons.
The output signals of these two pins are the same.
When icon feature is not used, these pins should be left open.</td><td>2</td></tr>
</table>

Microprocessor Interface Pins

<table>
<tr><th>Pin Name</th><th>Type</th><th>Description</th><th>No. of Pins</th></tr>
<tr><td>PS[2:0]</td><td>I</td><td>Microprocessor interface select pins.
<table>
<tr><th>PS2</th><th>PS1</th><th>PS0</th><th>Selected Interface</th></tr>
<tr><td>“L”</td><td>“L”</td><td>“L”</td><td>4 Pin-SPI MPU interface</td></tr>
<tr><td>“H”</td><td>“L”</td><td>“L”</td><td>3 Pin-SPI MPU interface</td></tr>
<tr><td>“L”</td><td>“H”</td><td>“L”</td><td>8080-series parallel MPU interface</td></tr>
<tr><td>“H”</td><td>“H”</td><td>“L”</td><td>6800-series parallel MPU interface</td></tr>
</table></td><td>3</td></tr>
<tr><td>CSB</td><td>I</td><td>Chip select input pin.
Interface access is enabled when CSB is “L”.
When CSB is non-active (CSB=“H”), D[7:0] pins are high impedance.</td><td>1</td></tr>
<tr><td>RESB</td><td>I</td><td>Reset input pin.
When RESB is “L”, internal initialization is executed.</td><td>1</td></tr>
<tr><td>A0</td><td>I</td><td>It determines whether the access is related to data or command.
A0=“H” : Indicates that D[7:0] are display data.
A0=“L” : Indicates that D[7:0] are control data.
A0 is not used in 3-Line SPI interface and should fix to “H” by VDD1.</td><td>1</td></tr>
</table>

<table>
<tr><th>Pin Name</th><th>Type</th><th>Description</th><th>No. of Pins</th></tr>
<tr><td>RWR</td><td>I</td><td>Read/Write execution control pin. When PS[1:0]=(H,L),
<table>
<tr><th>PS2</th><th>MPU Type</th><th>RWR</th><th>Description</th></tr>
<tr><td>H</td><td>6800 series</td><td>R/W</td><td>Read/Write control input pin.
R/W=“H”: read.
R/W=“L”: write.</td></tr>
<tr><td>L</td><td>8080 series</td><td>/WR</td><td>Write enable input pin.
Signals on D[7:0] will be latched at the rising edge of /WR signal.</td></tr>
</table>
RWR is not used in serial interfaces and should fix to “H” by VDD1.</td><td>1</td></tr>
<tr><td>ERD</td><td>I</td><td>Read/Write execution control pin. When PS[1:0]=(H,L),
<table>
<tr><th>PS2</th><th>MPU Type</th><th>ERD</th><th>Description</th></tr>
<tr><td>H</td><td>6800 series</td><td>E</td><td>Read/Write control input pin.
R/W=”H“: When E is “H”, D[7:0] are in an output status.
R/W=”L“: Signals on D[7:0] are latched at the falling edge of E signal.</td></tr>
<tr><td>L</td><td>8080 series</td><td>/RD</td><td>Read enable input pin.
When /RD is “L”, D[7:0] are in output status.</td></tr>
</table>
ERD is not used in serial interfaces and should fix to “H” by VDD1.</td><td>1</td></tr>
<tr><td rowspan="2">D[7:0]</td><td>I/O</td><td>When using 8-bit parallel interface: 6800 or 8080 mode
8-bit bi-directional data bus. Connect to the data bus of 8-bit microprocessor.
When CSB is non-active (CSB=“H”), D[7:0] pins are high impedance.</td><td rowspan="2">8</td></tr>
<tr><td>I</td><td>When using serial interface: 4-LINE or 3-LINE
D[7:4] : Not used and should fix to “H” by VDD1.
D[3:1]=SDA : Serial data input, must be connected together.
D0=SCLK : Serial clock input.
When CSB is non-active (CSB=“H”), D[7:0] pins are high impedance.</td></tr>
</table>

Note:

1. After VDD1 is turned ON, any MPU interface pins cannot be left floating.

Clock System Input

Pin Name	Type	Description	No. of Pins
OSC	**I**	OSC=“H” : On-chip oscillator is used. Connect to VDD1 to set OSC=“H”. OSC=External clock : Use external clock. Connect external clock to this pin. OSC=“L” : Stop system clock. The whole circuit is stopped except the logical and DDRAM circuits. It is not recommended to stop the system clock. When system clock is stopped, the driver outputs (SEGx & COMx) will be hold at the last state (like DC output) and the liquid crystal maybe polarized. To avoid this, never stop system clock before entering Power Down Mode.	**1**

Power System Pins

Pin Name	Type	Description	No. of Pins
VSS1	**Power**	Digital ground. Connect to VSS2 externally. For pins that are set to be “L”, connect them to this power (use VSS1 for “L”).	**4**
VSS2	**Power**	Analog ground. Connect to VSS1 externally.	**6**
VDX2O	**Power**	Power for test mode. Left this pin floating.	**3**
VDD1	**Power**	Digital power. If VDD1=VDD2, connect to VDD2 externally. For pins that are set to be “H”, connect them to this power (use VDD1 for “H”).	**5**
VDD2	**Power**	Analog power. If VDD1=VDD2, connect to VDD1 externally.	**4**
V0 (V0O, V0I, V0S)	**Power**	LCD driving voltage for commons at negative frame. V0 ≥ VG > VM > VSS ≥ XV0 V0O, V0I & V0S should be separated in ITO layout. V0O, V0I & V0S should be connected together in FPC layout.	**7**
XV0 (XV0O, XV0I, XV0S)	**Power**	LCD driving voltage for commons at positive frame. XV0O, XV0I & XV0S should be separated in ITO layout. XV0O, XV0I & XV0S should be connected together in FPC layout.	**7**
VG (VGO, VGI, VGS)	**Power**	LCD driving voltage for segments. VGO, VGI & VGS should be separated in ITO layout. VGO, VGI & VGS should be connected together in FPC layout. 1.24 ≤ VG < VDD2.	**7**
VMO	**Power**	VM output. LCD driving voltage for commons. 0.62V ≤ VM < VDD2.	**4**
VRS	**Power**	Test pin for monitoring voltage reference level. This pin must be left open (without any kinds of connection).	**1**
CP	**I**	Booster configuration pin for default setting : “L”=4X; “H”=5X. This pin set the default booster stage after reset. The booster stage can be changed by software instruction.	**1**
BR	**I**	Bias circuit configuration pin for default setting : “L”=1/7; “H”=1/9. This pin set the default value of bias ratio after reset. The bias ratio can be changed by software instruction.	**1**

Test Pins

Pin Name	Type	Description	No. of Pins
T0~T10	**T**	Do NOT use. Reserved for testing. Must be floating.	**11**
T11	**T**	Do NOT use. Reserved for testing. Must be “H”. Connect to VDD1 for pull-high.	**1**
T12	**T**	Do NOT use. Reserved for testing. Must be “H”. Connect to VDD1 for pull-high.	**1**

Recommend ITO Resistance

Pin Name	ITO Resistance
T[0:10], VRS, VDX2O	Floating
VDD1, VDD2, VSS1, VSS2	< 100Ω
V0(V0I, V0O, V0S), VG(VGI, VGO, VGS), XV0(XV0I, XV0O, XV0S), VMO	< 300Ω
A0, RWR, ERD, CSB, D[7:0] *1	< 1KΩ
PS[2:0], OSC *2, CP, BR, T11, T12	< 5KΩ
RESB *3	< 10KΩ

Note:

1. If using 3-Line or 4-Line SPI interface with VDD1 less than 2.4V, the SDA signal resistance should be less than 500Ω.
2. If using internal clock, OSC is connect to VDD1 and the limitation of ITO resistance will be “No Limitation”.
   If using external clock, the ITO resistance of OSC should be kept lower than 300Ω to keep the clock signal quality.
3. To prevent the ESD pulse resetting the internal register, applications should increase the resistance of RESB signal (add a series resistor or increase ITO resistance). The value is different from modules.
4. The option setting to be “H” should connect to VDD1.
5. The option setting to be “L” should connect to VSS1.

6. FUNCTIONS DESCRIPTION

Microprocessor Interface

Chip Select Input

CSB pin is used for chip selection. ST7579 can interface with an MPU when CSB is "L". When CSB is “H”, the inputs of A0, ERD and RWR with any combination will be ignored and D[7:0] are high impedance. In 3-Line and 4-Line serial interface, the internal shift register and serial counter are reset when CSB is “H”.

Parallel / Serial Interface

ST7579 has types of interface for kinds of MPU. The MPU interface is selected by PS[2:0] pins as shown in table 1.

Table 1. Parallel/Serial Interface Mode

PS2	PS1	PS0	CSB	A0	ERD	RWR	D[7:0]	MPU Interface
“L”	“L”	“L”	CSB	A0	---	---	Refer to serial interface.	4-Line SPI interface
“H”	“L”	“L”		---				3-Line SPI interface
“L”	“H”	“L”	CSB	A0	/RD	/WR	D[7:0]	8080-series parallel interface
“H”	“H”	“L”			E	R/W		6800-series parallel interface

* The un-used pins are marked as “---” and should be fixed to “H” by VDD1.

Parallel Interface

The 8-bit bi-directional data bus is used in parallel interface and the type of MPU is selected by PS2 (fix PS1=H, PS0=L) as shown in table 2. The data transfer type is determined by signals of A0, ERD and RWR as shown in table 3.

Table 2. Microprocessor Selection for Parallel Interface

PS2	PS1	PS0	CSB	A0	ERD	RWR	D[7:0]	MPU Interface
“L”	“H”	“L”	CSB	A0	/RD	/WR	D[7:0]	8080-series
“H”	“H”	“L”			E	R/W		6800-series

Table 3. Parallel Data Transfer

Common	6800-series		8080-series		Description
A0	E (ERD)	R/W (RWR)	/RD (ERD)	/WR (RWR)	
“H”	“H”	“H”	“L”	“H”	Display data read out
“H”	“H”	“L”	“H”	“L”	Display data write
“L”	“H”	“H”	“L”	“H”	Internal status read
“L”	“H”	“L”	“H”	“L”	Writes to internal register (instruction)

NOTE: In 6800-series interface mode, fixing E (ERD) pin at high can use CSB as enable signal instead. In this case, interface data is latched at the rising edge of CSB and the type of data transfer is determined by signals at A0 and R/W (RWR) pins as defined in 6800-series mode.

Setting Serial Interface

Serial Mode	PS[2:0]	CSB	A0	ERD	RWR	D[7:0]
4-Line SPI interface	“L, L, L”	CSB	A0	---	---	---, ---, ---, ---, SDA, SDA, SDA, SCLK
3-Line SPI interface	“H, L, L”		---			

* The un-used pins are marked as “---” and should be fixed to “H” by VDD1.

Note:

1. The option setting to be “H” should connect to VDD1.
2. The option setting to be “L” should connect to VSS1.

PS2= "L", PS1= "L", PS0= "L" : 4-line SPI interface

When ST7579 is active (CSB="L"), serial data (SDA) and serial clock (SCLK) inputs are enabled. When ST7579 is not active (CSB="H"), the internal 8-bit shift register and 3-bit counter are reset. The display data/command indication is controlled by the register selection pin (A0). The signals transferred on data bus will be display data when A0 is high and will be instruction when A0 is low. The read feature is not supported in this mode. Serial data on SDA is latched at the rising edge of serial clock on SCLK. After the 8th serial clock, the serial data will be processed as 8-bit parallel data. The DDRAM column address pointer will be increased by one automatically after each byte of DDRAM access.

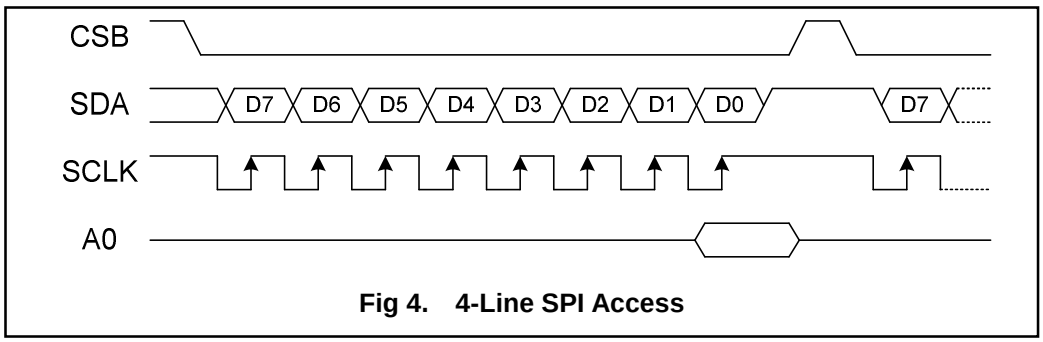


Fig 4. 4-Line SPI Access

PS2= "L", PS1= "L", PS0= "H": 3-line SPI interface

When ST7579 is active (CSB="L"), serial data (SDA) and serial clock (SCLK) inputs are enabled. When ST7579 is not active (CSB="H"), the internal 8-bit shift register and 3-bit counter are reset. The A0 pin is not available in this mode. Before issuing serial data, an A0 bit is required to indicate the following 8-bit signals are data or instruction. The read feature is not supported in this mode. Serial data on SDA is latched at the rising edge of serial clock on SCLK. After the 9th serial clock, the serial data will be processed as 8-bit parallel data. The DDRAM column address pointer will be increased by one automatically after each byte of DDRAM access.

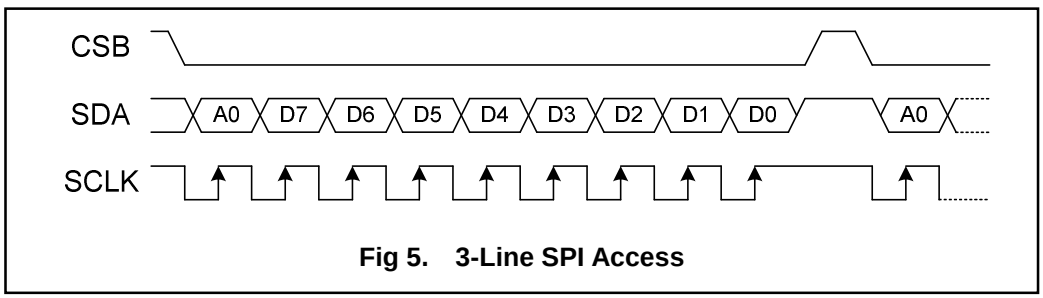


Fig 5. 3-Line SPI Access

Data Transfer

ST7579 uses bus holder and internal data bus for data transfer with MPU. When writing data from the MPU to on-chip RAM, data is automatically transferred from the bus holder to the RAM as shown in Fig 6. And when reading data from on-chip RAM to the MPU, the data for the initial read cycle is stored in the bus holder (dummy read) and the MPU reads this stored data from bus holder for the next data read cycle as shown in Fig 7. This means that a dummy read cycle must be inserted between each pair of address sets when a sequence of address sets is executed. Therefore, the data of the specified address cannot be output with the read display data instruction right after the address sets, but can be output at the second read of data.

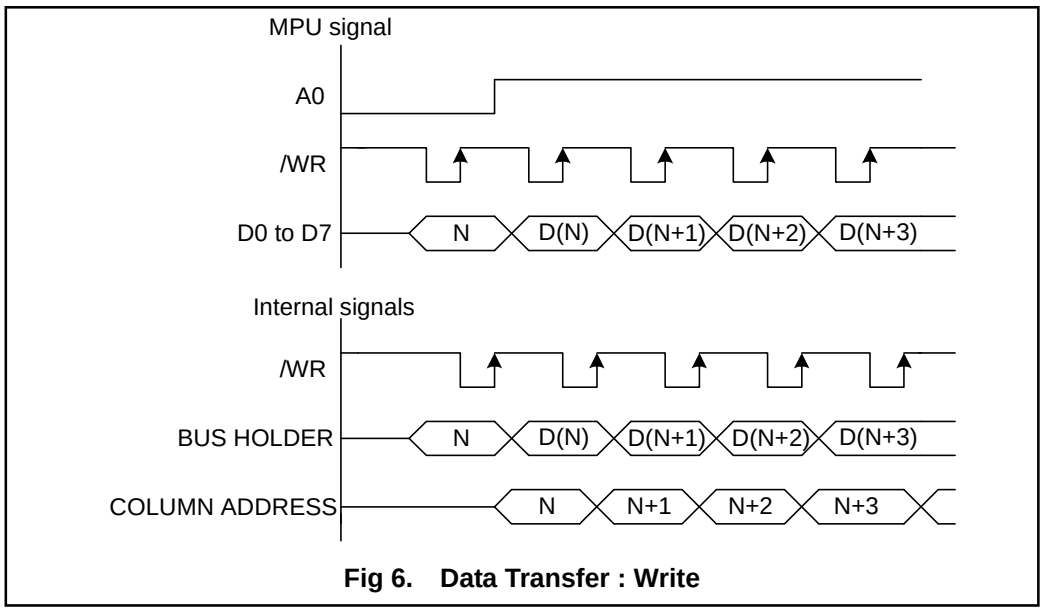


Fig 6. Data Transfer : Write

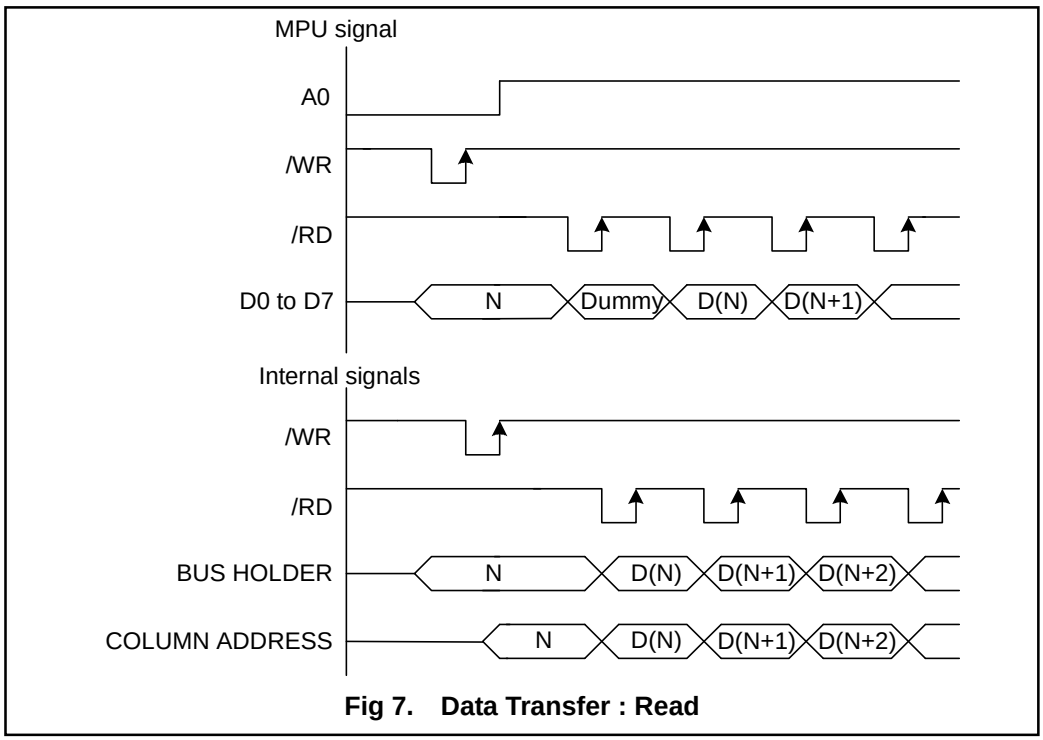


Fig 7. Data Transfer : Read

Display Data RAM (DDRAM)

ST7579 contains a 68X102 bit static RAM that stores the display data. The display data RAM (DDRAM) store the dot data for the LCD. It is an addressable array with 102 columns by 68 rows (8-page with 8-bit, 1-page with 3-bit and 1-page with 1-bit). The X-address is directly related to the column output number. Each pixel can be selected when the page and column addresses are specified. The rows are divided into: 8 pages (page 0~7) each with 8 lines (for COM0~63), the 8th page with 3 lines (for COM64~66) and the 9th page with only 1 line (the 67th row, COMS, for icon). The display data (D7~D0) corresponds to the LCD common-line direction (default: D0 at top when DO=0). Those pages with 8 lines can be accessed through D[7:0] directly. When accessing those pages with fewer than 8 lines, the valid bit(s) in D[7:0] should be checked. Refer to Fig 9 and Fig 10 for detailed illustration. The microprocessor can write to and read from (only Parallel interfaces) DDRAM by the I/O buffer. Since the LCD controller operates independently, data can be written into DDRAM at the same time as data is being displayed without causing the LCD flicker or data-conflict.

Page Address Circuit

This circuit is for providing a Page Address to Display Data RAM. It incorporates 4-bit Page Address register changed by only the “Set Page” instruction. Page Address 9 is a special RAM area for the icons and display data is only 1-bit valid (DO=0, D0 is valid; DO=1, D7 is valid).

Line Address Circuit

This circuit assigns DDRAM a Start Line Address corresponding to the first common output (COM0) of the LCD module. Therefore, by setting Line Address repeatedly, it is possible to realize the screen scrolling and page switching without changing the contents of on-chip RAM as shown in Fig 12. The Line Address Circuit incorporates 7-bit Line Counter and 7-bit Line Address Register (which can be changed by Set Start Line instruction). At the beginning of each LCD frame, the Line Address Register is copied into the Line Counter. The line which is specified by the counter will transfer 102-bit data to the display data latch circuit. At the next line period, the Line Counter is increased by one and the next line will transfer the next 102-bit data to the display data latch circuit. The 102-bit icon data are transferred at the last line period during each frame. The icon data cannot be scrolled as normal data because the icon data are fixed to transfer at the last line period during each frame.

Column Address Circuit

Column Address Circuit has an 8-bit preset counter that provides Column Address to the DDRAM. The display data RAM column address is specified by the Column Address Set command. The specified column address is incremented (+1) with each display data read/write command. This allows the MPU display data to be accessed continuously.

Register MX and MY makes it possible to invert the relationship between the addresses (Line Address and Column Address) and the outputs (COM/SEG). It is necessary to rewrite the display data into built-in RAM after changing MX setting.

The relation between DDRAM and outputs with different MX or MY setting is shown below.

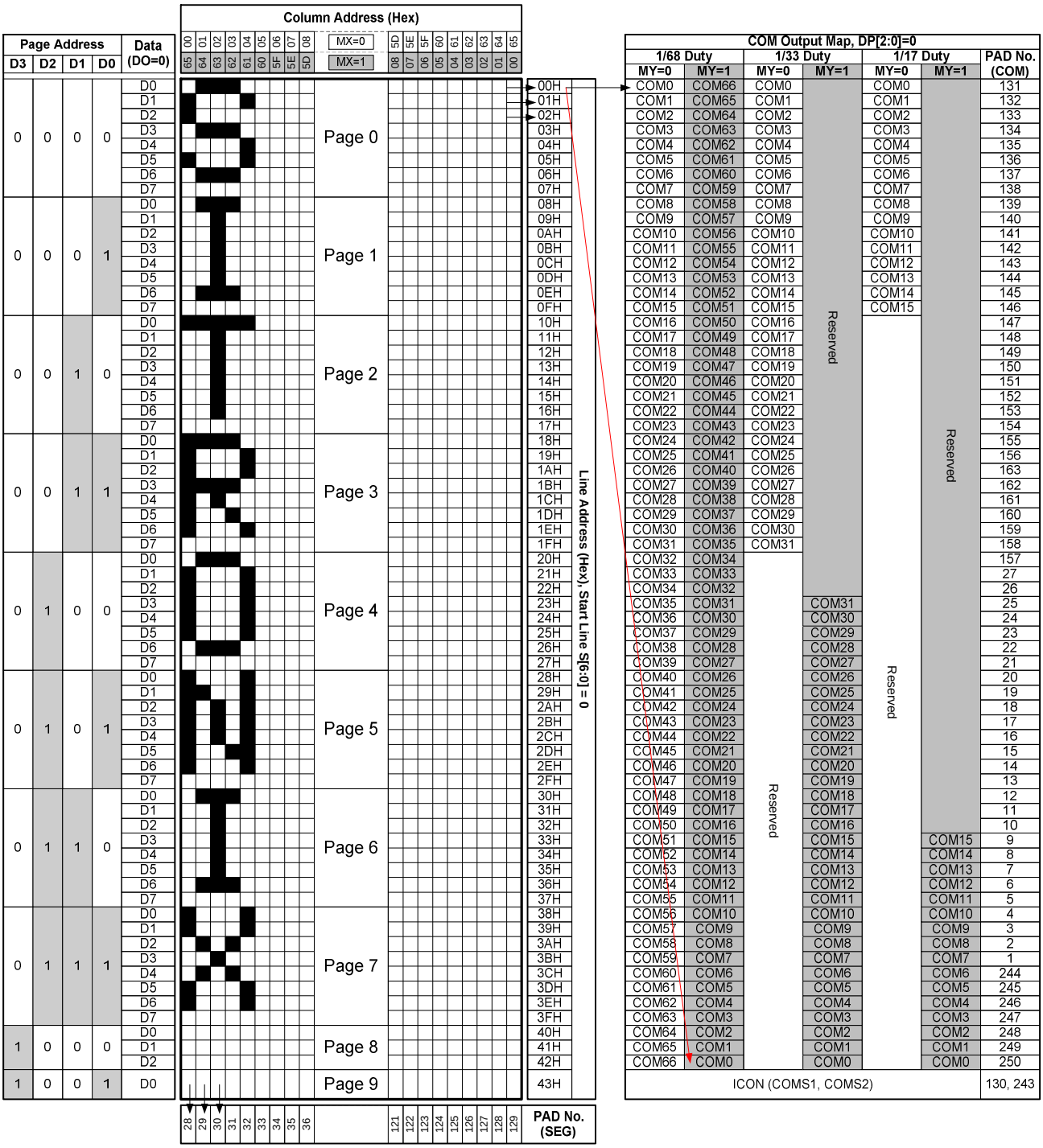


Fig 8. Relationship between DDRAM and Outputs (COM/SEG)

Addressing

Data is downloaded in bytes into the Display Data RAM matrix of ST7579 as shown below. The Display Data RAM has a matrix of 68 by 102 bits. The address pointer addresses the columns. The address ranges are: X 0 to 101 (1100101), Y 0 to 9 (1001) .Addresses outside these ranges are not allowed.

In horizontal addressing mode the X address increments after each byte (see Fig 11). After the last X address (X = 101), X wraps around to 0 and Y increments to address the next row.

After the very last address (X = 101, Y = 8) the address pointers wrap around to address (X = 0, Y =0)

Data Structure

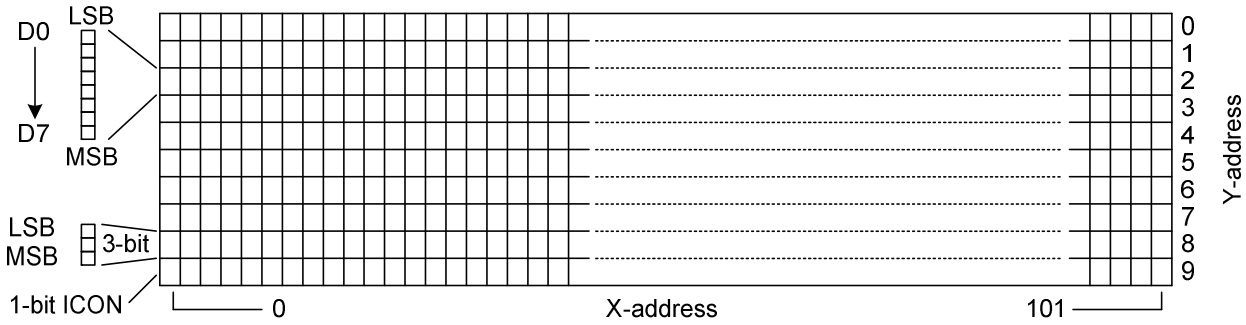


Fig 9. RAM format, if DO=0

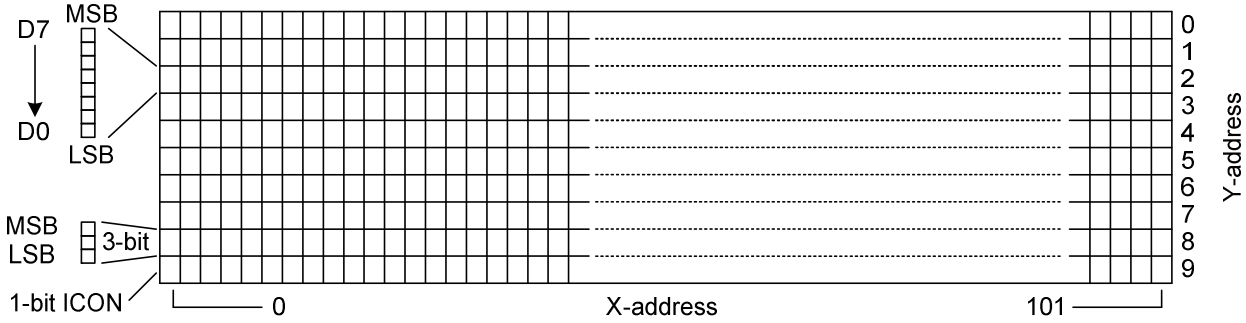


Fig 10. RAM format, if DO=1

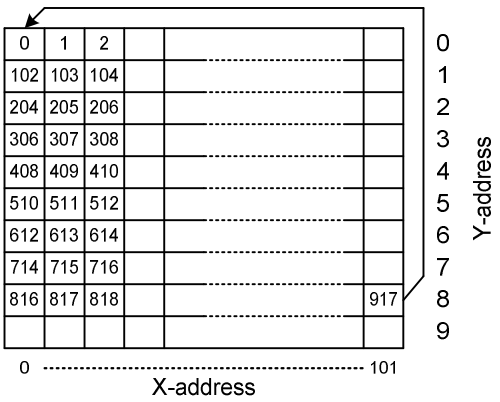


Fig 11. RAM Addressing : Horizontal Addressing

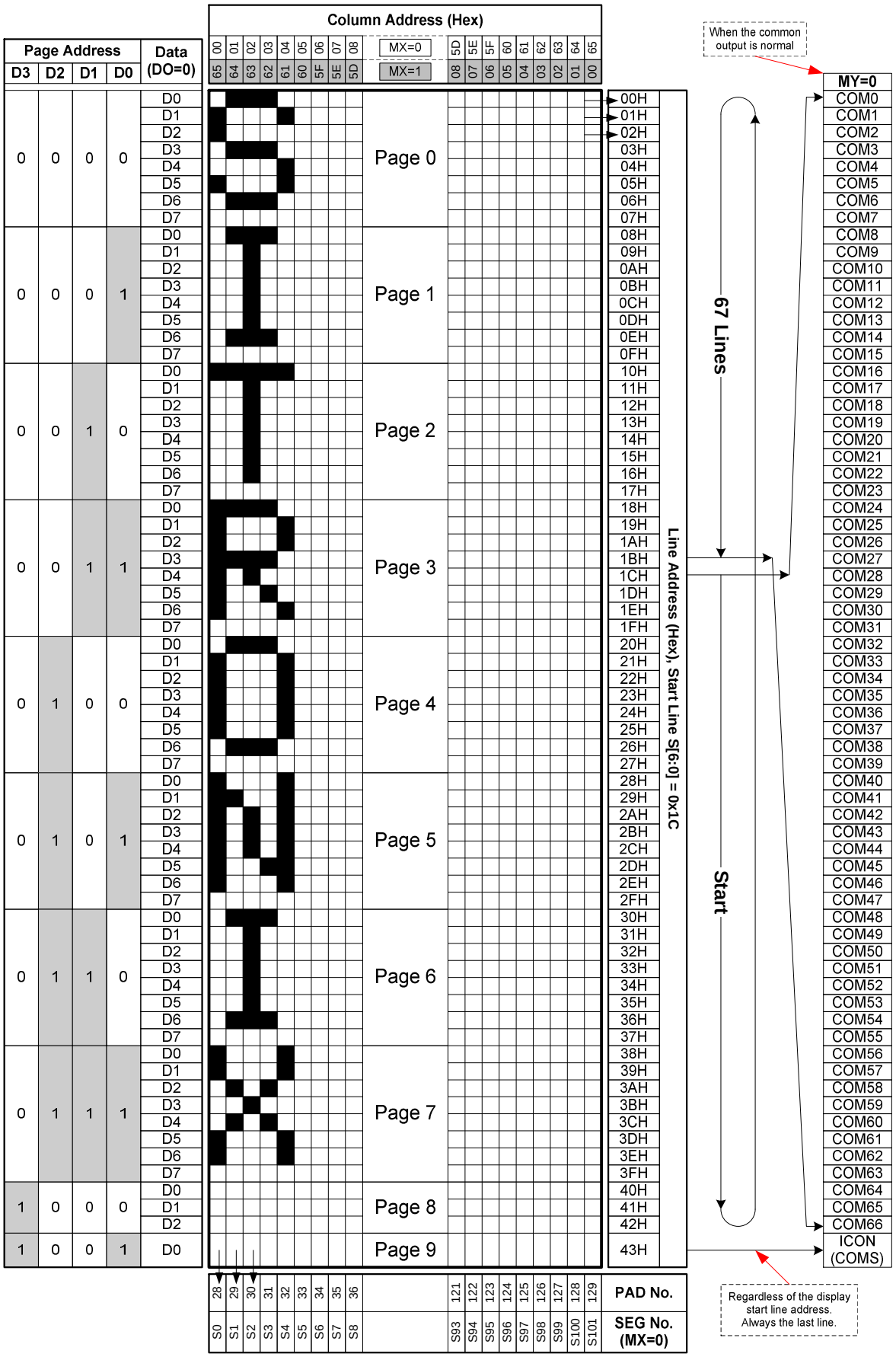


Fig 12. Display Data RAM Map (68 COM)

Partial Display on LCD

ST7579 realizes the Partial Display function on LCD with low-duty driving for saving power consumption and showing the various display duty. To show the various display duty on LCD, LCD driving duty and bias are programmable via the instruction. And, built-in power supply circuits are controlled by the instruction for adjusting the LCD driving voltages.

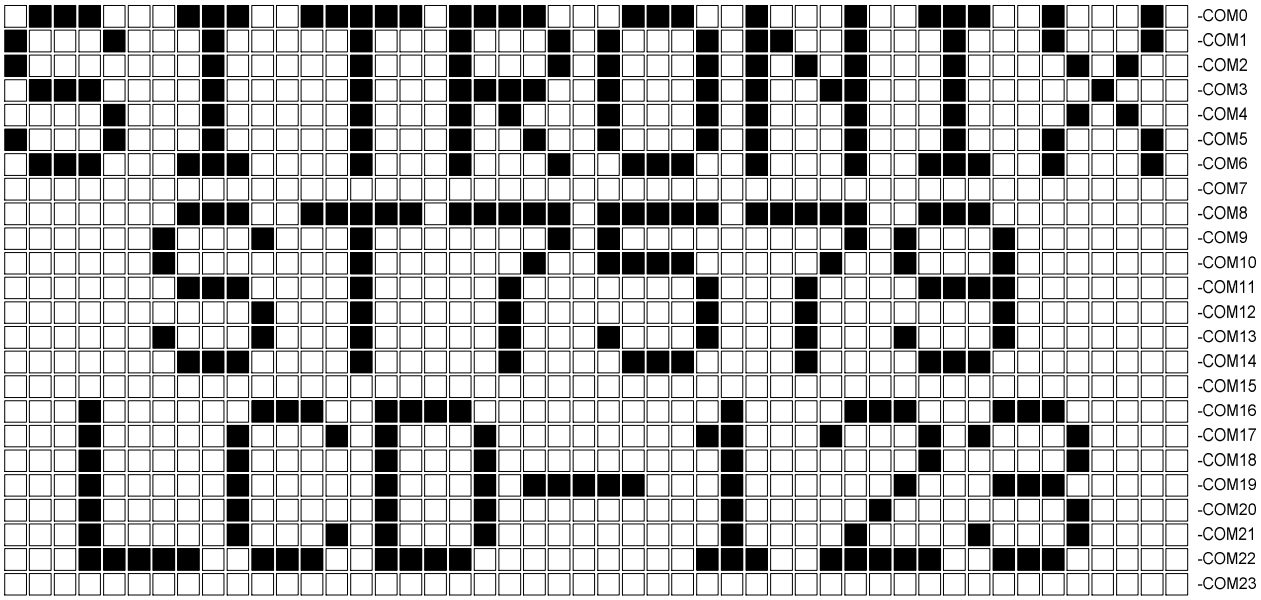


Fig 13. Reference Example for Partial Display

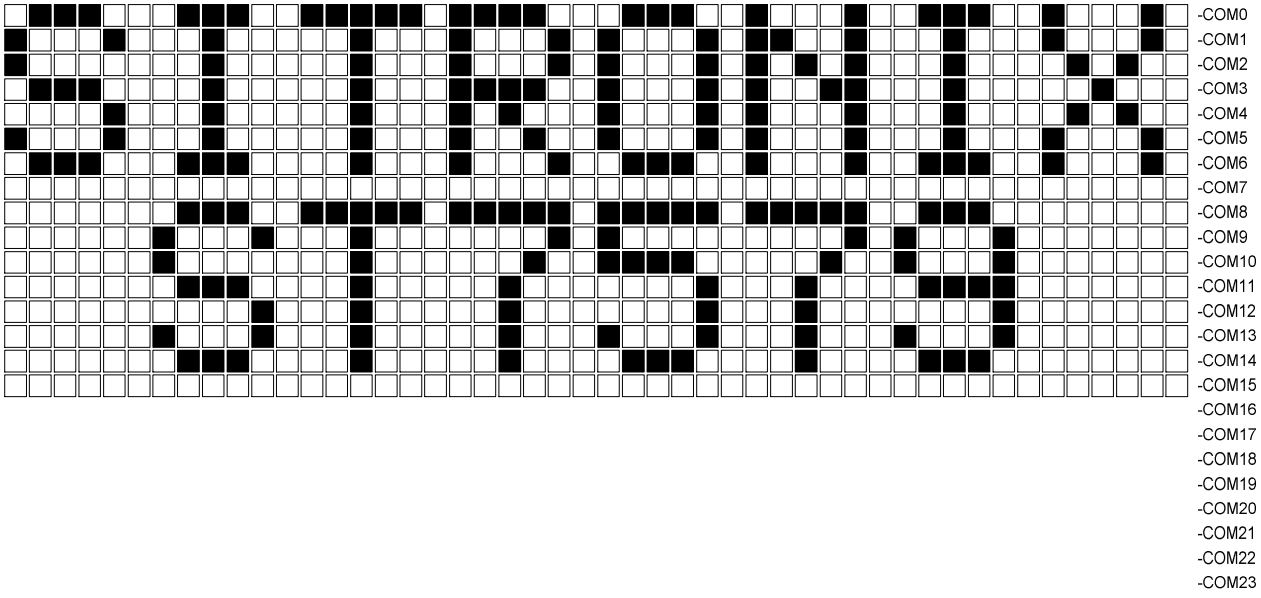


Fig 14. Partial Display (Partial Display Duty=1/17, Display Part=0)

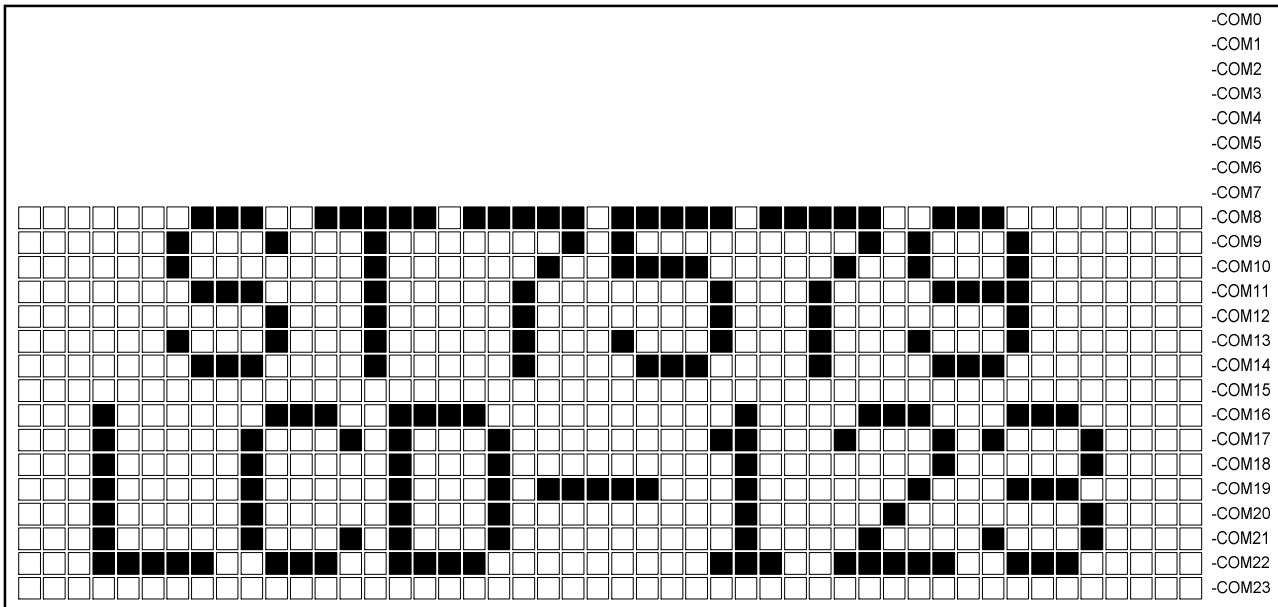


Fig 15. Move Partial Screen (Partial Display Duty=1/17, Display Part=1)

Liquid Crystal Driver Power Circuit

The Power Supply circuits generate the voltage levels necessary to drive liquid crystal driver circuits with low power consumption and the fewest components. There are voltage converter circuits, voltage regulator circuits, and voltage follower circuits. They are controlled by power control instruction.

External Power Components

The recommended external power components need only 2 capacitors. The detailed values of these two capacitors are determined by the panel size and loading.

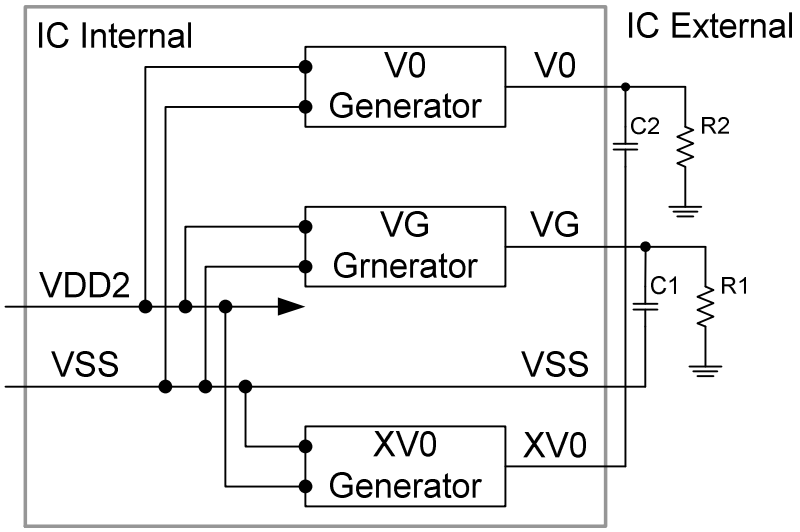


Fig 16. Power Circuit

The referential external component values are listed below (it is determined by the worse condition of 1.4" panel). Customer applications are not necessary the same as these values. The value should be determined by customer's LCD module (panel loading and ITO resistance) and application (VDD, V0, bias and etc.).

C1=0.1uF~1uF (Non-Polar/6V, default 0.1uF) C2=0.1uF~1uF (Non-Polar/16V, default 0.1uF)

R1=47KΩ~100KΩ (default 47KΩ) R2=500KΩ~1MΩ (default 500KΩ)

7. RESET CIRCUIT

Setting RESB to “L” or RESET instruction can initialize internal function. While RESB is “L”, no instruction except read status can be accepted. RESB pin must connect to the reset pin of MPU and initialization by RESB pin is essential before operating.

When RESB becomes “L”, the following procedures will start.
Power Down Mode: PD=1 (Analog Power OFF, Oscillator OFF & COM/SEG output at VSS)
Page Address: Y[3:0]=0
Column Address: X[6:0]=0
COM Scan Direction: MY=0
SEG Select Direction: MX=0
Data Orientation: DO=0
Display Control: Display OFF: D=E=0
Normal Instruction Set: H[1:0]=(0,0)
Frame Rate: FR[2:0]=(1,0,0) (73Hz)
Partial Display Mode: PS=0 (Partial Display OFF); WS=0
N-Line Inversion: NL[4:0]=0 (Disabled)
Booster setting: BE[1:0]=(10); PC[1:0] Depends on “CP” setting
Initial V0 Setting: V_{OP}[6:0]=0; PRS=0 (Regulator OFF)
Bias system: BS[2:0] Depends on “BR” setting

After power-on, RAM data are undefined and the display status is “Display OFF”. It’s better to initialize whole DDRAM (ex: fill all 00h or write the display pattern) before turning the Display ON.

8. INSTRUCTION TABLE

INSTRUCTION	A0	R/W (RWR)	COMMAND BYTE								DESCRIPTION
			D7	D6	D5	D4	D3	D2	D1	D0	
H[1:0] Independent Instruction											
NOP	0	0	0	0	0	0	0	0	0	0	No operation
Reserved	0	0	0	0	0	0	0	0	0	1	Do not use
Function Set	0	0	0	0	1	MX	MY	PD	H1	H0	Power down; entry mode; Select instruction table
Read Status	0	1	PD	0	0	D	E	MX	MY	DO	Read status byte
Read Data	1	1	D7	D6	D5	D4	D3	D2	D1	D0	Read data to RAM
Write Data	1	0	D7	D6	D5	D4	D3	D2	D1	D0	Write data to RAM
H[1:0] = (0,0)											
Reserved	0	0	0	0	0	0	0	0	1	X	Do not use
Set V0 Range	0	0	0	0	0	0	0	1	0	PRS	V0 range L/H select
END	0	0	0	0	0	0	0	1	1	0	Release read/modify/write
Read-modify-Write	0	0	0	0	0	0	0	1	1	1	RAM address at R:+0 , W:+1
Display Control	0	0	0	0	0	0	1	D	0	E	Sets display configuration
Reserved	0	0	0	0	0	1	0	0	X	X	Do not use
Set Y Address of RAM	0	0	0	1	0	0	Y3	Y2	Y1	Y0	Sets Y address of RAM 0≤Y≤9
Set X Address of RAM	0	0	1	X6	X5	X4	X3	X2	X1	X0	Sets X address of RAM 0≤X≤101
H[1:0] = (0,1)											
Reserved	0	0	0	0	0	0	0	0	1	X	Do not use
Display Configuration	0	0	0	0	0	0	1	DO	X	X	Top/bottom row mode set data order
Bias System	0	0	0	0	0	1	0	BS2	BS1	BS0	Set bias system (BSx)
Set Start Line (high)	0	0	0	0	0	0	0	1	0	S6	Specify the initial display line S6
Set Start Line (low)	0	0	0	1	S5	S4	S3	S2	S1	S0	Specify the initial display line to realize vertical scrolling
Set V0	0	0	1	V_{OP6}	V_{OP5}	V_{OP4}	V_{OP3}	V_{OP2}	V_{OP1}	V_{OP0}	Set V_{OP} parameter to register
H[1:0] = (1,0)											
Reserved	0	0	0	0	0	0	0	0	1	X	Do not use
Partial Screen Mode	0	0	0	0	0	0	0	1	0	PS	Partial screen enable
Partial Screen Size	0	0	0	0	0	0	1	0	0	WS	Set partial screen size
Display Part	0	0	0	0	0	1	0	DP2	DP1	DP0	Set display part for partial screen mode
H[1:0] = (1,1)											
Reserved	0	0	0	0	0	0	0	0	0	X	Do not use
RESET	0	0	0	0	0	0	0	0	1	1	Software reset
Frame Control	0	0	0	0	0	0	1	FR2	FR1	FR0	Frame rate control
N-Line Inversion	0	0	0	1	0	NL4	NL3	NL2	NL1	NL0	Sets N-Line inversion
Booster Efficiency & Booster Stage	0	0	1	0	0	1	BE1	BE0	PC1	PC0	Booster Efficiency Set
Reserved	0	0	1	X	X	X	X	X	X	X	Do not use

9. INSTRUCTION DESCRIPTION

H[1:0] Independent

Function Set

A0	R/W(RWR)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	1	MX	MY	PD	H1	H0

Flag	Description
MX	SEG bi-direction selection MX=0: normal direction (SEG0->SEG101) MX=1: reverse direction (SEG101->SEG0)
MY	COM bi-direction selection MY=0: normal direction (COM0->COM66) MY=1: reverse direction (COM66->COM0)
PD	PD=0: chip is active PD=1: chip is in power down mode All LCD outputs at VSS (display off), bias generator and V0 generator off, VOUT can be disconnected, oscillator off (external clock possible), RAM contents not cleared; RAM data can be written.
H1,H0	H[1:0] are used to select different instruction block Refer to the instruction table

Read Status

Indicates the internal status of ST7579

A0	R/W(RWR)	D7	D6	D5	D4	D3	D2	D1	D0
0	1	PD	0	0	D	E	MX	MY	DO

Flag	Description
PD	PD=0: chip is active PD=1: chip is in power down mode
D,E	D E The bits D and E select the display mode. 0 0 Display OFF 0 1 All display segments on 1 0 Normal mode 1 1 Inverse video mode
DO	DO=0: LSB is on top DO=1: MSB is on top Refer to page 23.

Read Data

8-bit data of Display Data from the RAM location specified by the column address and page address can be read to the microprocessor.

A0	R/W(RWR)	D7	D6	D5	D4	D3	D2	D1	D0
1	1	Read Data							

Write Data

8-bit data of Display Data from the microprocessor can be written to the RAM location specified by the column address and page address. The column address is increased by 1 automatically so that the microprocessor can continuously write data to the addressed page. During auto-increment, the column address wraps to 0 after the last column is written.

A0	R/W(RWR)	D7	D6	D5	D4	D3	D2	D1	D0
1	0	Write Data							

H[1:0]=[0:0]

Set V0 Range

V0 range L/H select

A0	R/W(RWR)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	0	1	0	PRS

PRS=0: V0 programming range LOW

PRS=1: V0 programming range HIGH

Display Control

This bits D and E selects the display mode.

A0	R/W(RWR)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	1	D	0	E

Flag	Description

D	E	The bits D and E select the display mode.
0	0	Display OFF
0	1	All display segments on
1	0	Normal mode
1	1	Inverse video mode

(Flag: D,E)

Set Y Address of RAM

Y [3:0] defines the Y address vector address of the display RAM.

A0	R/W(RWR)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	1	0	0	Y3	Y2	Y1	Y0

Y3	Y2	Y1	Y0	Content	Allowed X-Range	Valid Bit
0	0	0	0	Page0 (display RAM)	0 to 101	D0~ D7
0	0	0	1	Page1 (display RAM)	0 to 101	D0~ D7
0	0	1	0	Page2 (display RAM)	0 to 101	D0~ D7
0	0	1	1	Page3 (display RAM)	0 to 101	D0~ D7
0	1	0	0	Page4 (display RAM)	0 to 101	D0~ D7
0	1	0	1	Page5 (display RAM)	0 to 101	D0~ D7
0	1	1	0	Page6 (display RAM)	0 to 101	D0~ D7
0	1	1	1	Page7 (display RAM)	0 to 101	D0~ D7
1	0	0	0	Page8 (display RAM)	0 to 101	D0~ D2 (If DO=0)
1	0	0	1	Page9 (display RAM)	0 to 101	D0 (If DO=0) D7 (if DO=1)

Set X Address of RAM

The X address points to the columns. The range of X is 0…101.

A0	R/W(RWR)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	X6	X5	X4	X3	X2	X1	X0

X6	X5	X4	X3	X2	X1	X0	Column address
0	0	0	0	0	0	0	0
0	0	0	0	0	0	1	1
0	0	0	0	0	1	0	2
0	0	0	0	0	1	1	3
:	:	:	:	:	:	:	:
1	1	0	0	0	1	1	99
1	1	0	0	1	0	0	100
1	1	0	0	1	0	1	101

END

This command releases the read-modify-write mode and returns the column and page addresses to the address before receiving read-modify-write instruction.

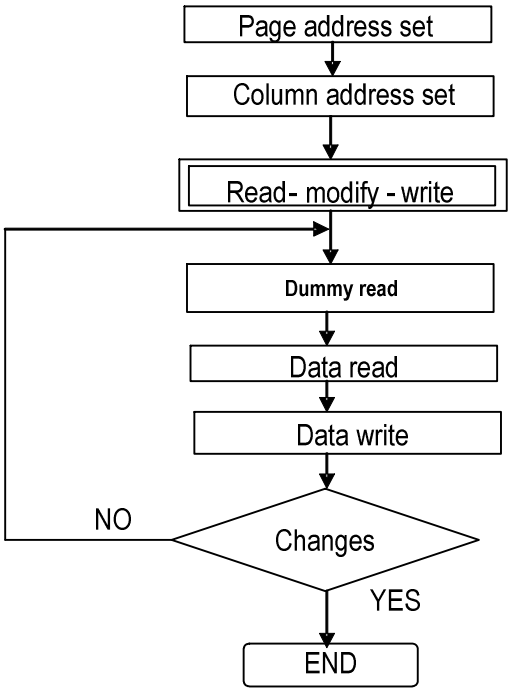
A0	R/W(RWR)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	0	1	1	0

Read-modify-Write

This command is used paired with the “END” instruction. Once this command has been input, the display data read command does not change the column and row address, but only the display data write command increments (+1) the address depend on V register setting. This mode is maintained until the END command is input. When the END command is input, the address returns to the address it was at when the read/modify/write command was entered. This function makes it possible to reduce the load on the MPU when there are repeating data changes in a specified display region, such as when there is a blanking cursor.

A0	R/W(RWR)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	0	1	1	1

* In Read-modify-Write mode, other commands aside from display data read/write commands can also be used.



H[1:0]=[0:1]

Display Configuration

Top/bottom row mode set data order

A0	R/W(RWR)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	1	DO	X	X

Flag	Description
DO	DO=0: LSB is on top DO=1: MSB is on top Refer to Page 23.

System Bias

Select LCD bias ratio of the voltage required for driving the LCD.

A0	R/W(RWR)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	1	0	BS2	BS1	BS0

BS2	BS1	BS0	Bias
0	0	0	11
0	0	1	10
0	1	0	9
0	1	1	8
1	0	0	7
1	0	1	6
1	1	0	5
1	1	1	4

Recommend LCD Bias Voltage

Symbol	Voltages for 1/9 Bias
V0	V0
VG	2/9 x V0
VM	1/9 x V0
VSS	VSS

* VG range: 1.24V ≤ VG < VDD2.
* VM range: 0.62V ≤ VM < VDD2.

Set Start Line

Sets the line address of display RAM to determine the initial display line instruction. The RAM display data is displayed at the top row (COM0) of the LCD panel.

A0	R/W(RWR)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	0	1	0	S6

A0	R/W(RWR)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	1	S5	S4	S3	S2	S1	S0

S6	S5	S4	S3	S2	S1	S0	Line address
0	0	0	0	0	0	0	0
0	0	0	0	0	0	1	1
0	0	0	0	0	1	0	2
0	0	0	0	0	1	1	3
:	:	:	:	:	:	:	:
1	0	0	0	0	0	0	64
1	0	0	0	0	0	1	65
1	0	0	0	0	1	0	66
1	0	0	0	0	1	1	No used
:	:	:	:	:	:	:	:
1	1	1	1	1	1	1	No used

Set V0

A0	R/W(RWR)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	V_{OP6}	V_{OP5}	V_{OP4}	V_{OP3}	V_{OP2}	V_{OP1}	V_{OP0}

The operation voltage V0 can be set by software.

$$V0=(a + V_{OPx} X b) \quad (1)$$

The parameters are explained in table 4. The maximum voltage that can be generated is depending on the VDD2 voltage and the display load current. Two overlapping V0 ranges are selectable via the command “Set V0 Range”. For the lower range (PRS=0), a=a1 and for the higher range (PRS=1), a=a2. The voltage steps in both ranges are equal to “b”. Note that the internal booster is turned off if V_{OP}[6:0] and the PRS bit are all set to zero. Please don’t operate this IC with this setting (PRS=0 & V_{OP}[6:0]=0).

*** The Vop must be operated in the range of 4V to 9.5V for the normal or partial display mode application, so that customer have some range(<4V; >9.5V) to adjust contrast by themselves.**

Table 4 Typical values for parameter for the HV-Generator programming

SYMBOL	VALUE	UNIT
a1	2.94 (PRS=0)	V
a2	6.75 (PRS=1)	V
b	0.03	V

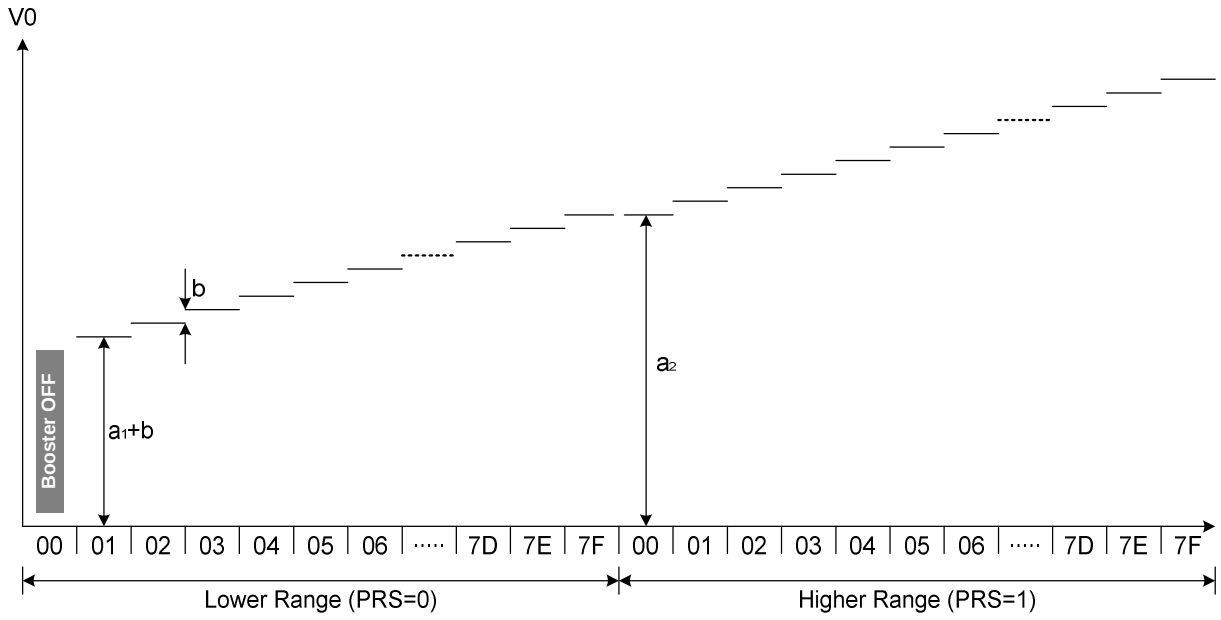


Fig 21 Setting V0 Voltage

H[1:0]=[1:0]

Partial Screen Mode

A0	R/W(RWR)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	0	1	0	PS

Flag	Description
PS	Full display mode or partial screen mode selection PS=0: Full display mode with 1/68 duty PS=1: Partial screen mode with 1/17 duty or 1/33 duty

In partial screen mode, COMS also works. The page address of COMS is Y=9 (D0).

Partial Screen Size

This instruction can select partial screen size

A0	R/W(RWR)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	1	0	0	WS

Flag	Description
WS	WS=0: Partial screen mode with 1/17 duty (16-Common + COMS) WS=1: Partial screen mode with 1/33 duty (32-Common + COMS)

Display Part

This instruction can select display area in partial screen mode.

A0	R/W(RWR)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	1	0	DP2	DP1	DP0

Flag	Content			Description	
				Display common	DDRAM position
DP[2:0]	0	0	0	Start from common 0	Start from page 0
	0	0	1	Start from common 8	Start from page 1
	0	1	0	Start from common 16	Start from page 2
	0	1	1	Start from common 24	Start from page 3
	1	0	0	Start from common 32	Start from page 4
	1	0	1	Start from common 40	Start from page 5
	1	1	0	Start from common 48	Start from page 6
	1	1	1	Start from common 56	Start from page 7

The range of display common and DDRAM depends on the “WS” register. For example, if WS=1 and DP[2:0]=001, then display commons are common 8~39 and COMS. DDRAM areas are page 1~4 and page 9 for COMS. Moreover, the last row is common 66, if the display range is over common 66, there will be no more common output to display.

H[1:0]=[1:1]

RESET

This instruction resets initial display line, column address, page address and common output status to their default setting .This instruction cannot initialize the LCD power supply which is initialized by the RESB pin.

A0	R/W(RWR)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	0	0	1	1

Frame Control

This command is used to set the frame frequency.

A0	R/W(RWR)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	1	FR2	FR1	FR0

FR2	FR1	FR0	FR Frequency
0	0	0	55 Hz
0	0	1	65 Hz
0	1	0	68 Hz
0	1	1	70 Hz
1	0	0	73 Hz (Default)
1	0	1	76 Hz
1	1	0	80 Hz
1	1	1	137 Hz

Set N-Line Inversion

The LCD operating voltage alters its polarization in different display phase. The display phase is changed after every frame as default. This instruction sets the scan line number so that the display phase will be changed after scanning the specified rows (3~33 lines).

A0	R/W(RWR)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	1	0	NL4	NL3	NL2	NL1	NL0

Note: The N-Line inversion mode will be disabled in partial screen mode. After exiting partial screen mode, the N-line inversion mode will return as it was.

NL4	NL3	NL2	NL1	NL0	Selected n-line inversion
0	0	0	0	0	Release N-Line Inversion (frame inversion)
0	0	0	0	1	3-line inversion
0	0	0	1	0	4-line inversion
0	0	0	1	1	5-line inversion
:	:	:	:	:	:
1	1	1	0	1	31-line inversion
1	1	1	1	0	32-line inversion
1	1	1	1	1	33-line inversion

Booster Efficiency & Booster Stage

A0	R/W(RWR)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	0	0	1	BE1	BE0	PC1	PC0

Booster Efficiency

ST7579 incorporates software configurable Booster Efficiency. It could be used with Voltage Booster to get the suitable boosted voltage and power consumption .Using lower Booster Efficiency level will get lower boosted voltage and lower power consumption. Default setting is Level 2 (suggest level).

Flag	Description

BE1	BE0	Booster Efficiency Level
0	0	Booster Efficiency Level 4
0	1	Booster Efficiency Level 3
1	0	Booster Efficiency Level 2 (default)
1	1	Booster Efficiency Level 1

BE[1:0]

Booster Stages

ST7579 incorporates a software configurable Voltage Booster. A hardware reset (RESB) will reset the booster stage to its default (depends on “CP” pin). After the reset is finished, the booster stage can be changed by this instruction.

Flag	Description

PC1	PC0	Booster Stage
0	1	3*voltage multiplier (Booster X3)
1	0	4*voltage multiplier (Booster X4)
1	1	5*voltage multiplier (Booster X5)

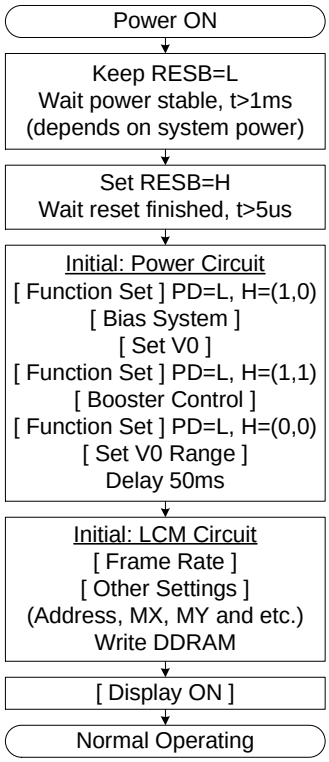
PC[1:0]

10. COMMAND SEQUENCE

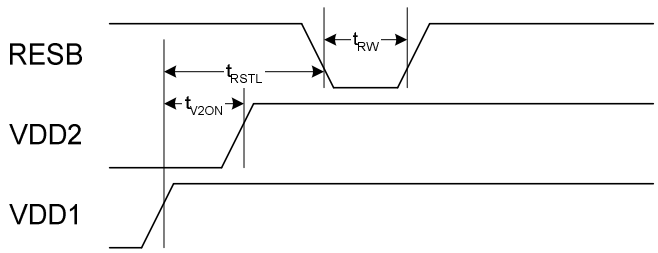
This section introduces some reference operation flows.

Power ON flow and instruction sequence:

Operating Flow



Power Sequence



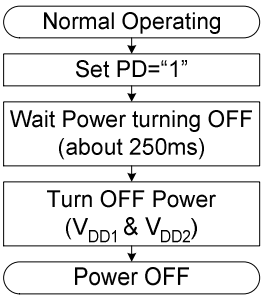
1. t_{V2ON}: VDD2 power ON delay.
   => 0 ≤ t_{V2ON} ≤ No Limitation.
2. t_{RSTL}: Reset Low time after VDD1 is stable.
   => 0 ≤ t_{RSTL} ≤ 50 ms[*1].
3. t_{RW}: Reset low pulse width.
   Please refer to RESB timing specification.

Note:

1. IC will NOT be damaged if either VDD1 or VDD2 is OFF while another is ON. The specification listed here is to prevent abnormal display on LCD module.
2. Be sure the power is stable and the internal reset is finished (refer to RESB timing specification).

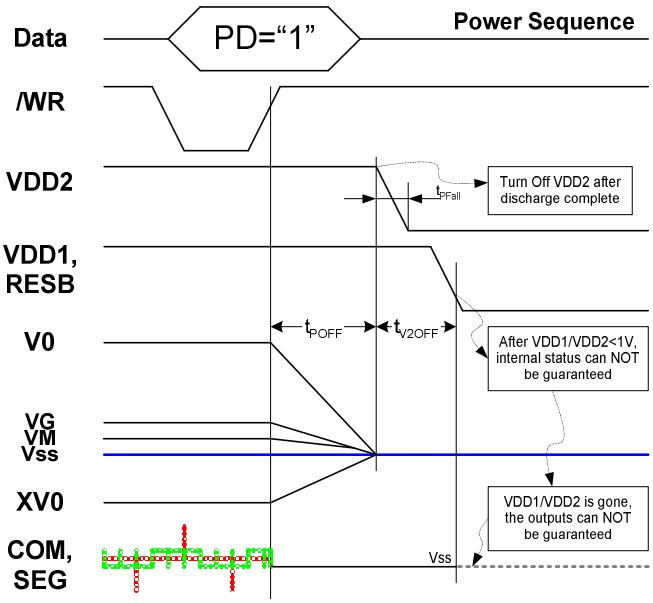
Power OFF Flow and Sequence

By setting PD="1", ST7579 will go into power save mode. The LCD driving outputs are fixed to VSS, built-in power circuits are turned OFF and a discharge process starts.

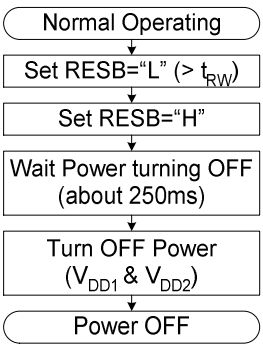


Instruction Flow

After the built-in power circuits are turned OFF and completely discharged, the power (VDD1 and VDD2) can be removed.

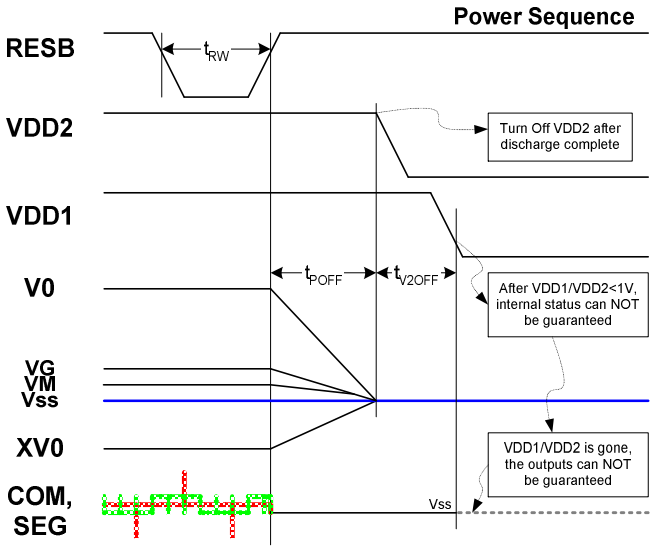


An alternate method is to use the RESB signal to set ST7579 into power save mode. After hardware reset, the PD flag is "1" and ST7579 is in power save mode (same as previous case).



Operating Flow

After the built-in power circuits are turned OFF and completely discharged, the power (VDD1 and VDD2) can be removed.



Note:

1. t_{IPOFF}: Internal Power discharge time. => 250ms (max).
2. t_{V2OFF}: Period between VDD1 and VDD2 OFF time. => 0 ms (min).
3. It is NOT recommended to turn VDD1 OFF before VDD2. Without VDD1, the internal status cannot be guaranteed and internal discharge-process maybe stopped. The un-discharged power maybe flows into COM/SEG output(s) and the liquid crystal in panel maybe polarized.
4. IC will NOT be damaged if either VDD1 or VDD2 is OFF while another is ON.
5. The timing is dependent on panel loading and the external capacitor(s).
6. The timing in these figures is base on the condition that: LCD Panel Size = 1.4" with C1=1uF, C2=1uF.

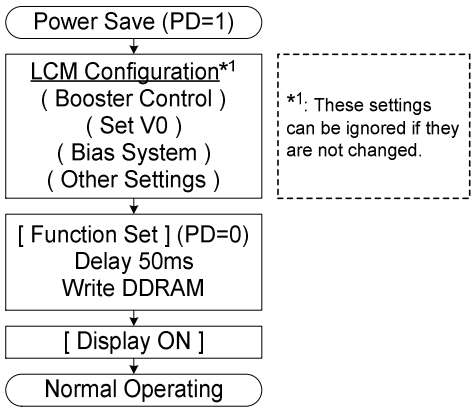
7. When turning VDD2 OFF, the falling time should follow the specification:
   300ms ≤ t_{PFall} ≤ 1sec
8. If the power OFF flow cannot meet this specification, it is recommended to use the resistor shown in application circuits (about 500KΩ ~ 1MΩ).

Power-Save Flow and Sequence

ENTERING THE POWER SAVE MODE

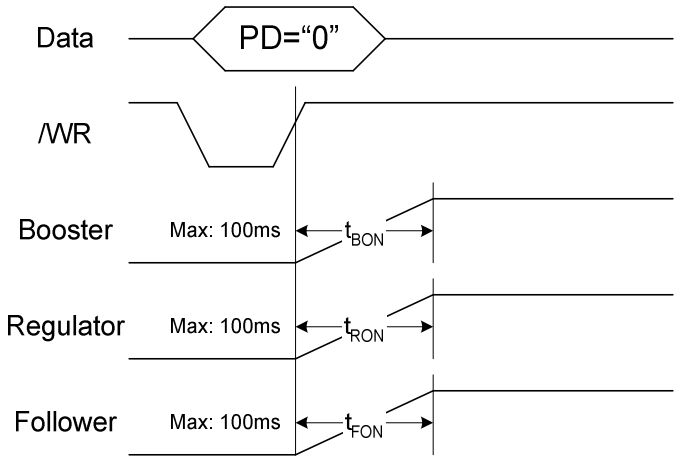
The power save mode is achieved by setting PD bit to be “1”. No specified instruction flow required.

EXITING THE POWER SAVE MODE



INTERNAL SEQUENCE of EXIT POWER SAVE MODE

After receiving “PD=0”, the internal circuits (Power) will starts the following procedure.



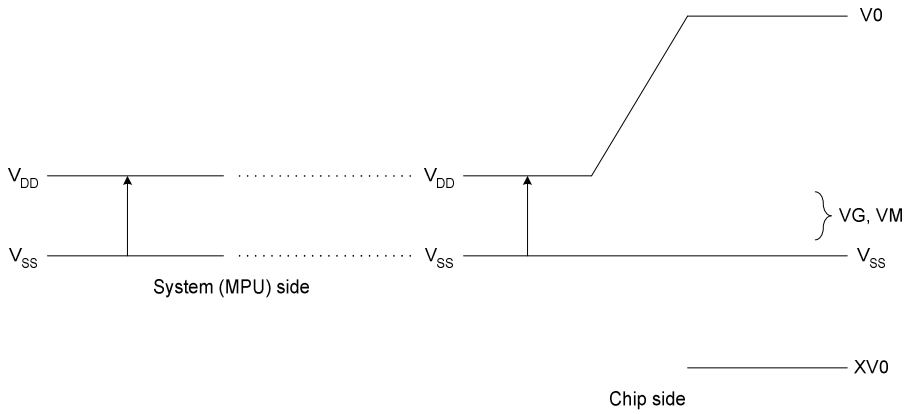
Note:

1. The power stable time is determined by LCD panel loading.
2. The power stable time in this figure is base on: LCD Panel Size = 1.4” with C1=1uF, C2=1uF.

11. LIMITING VALUES

In accordance with the Absolute Maximum Rating System; please refer to notes 1 and 2.

Parameter	Symbol	Conditions	Unit
Digital Power Supply Voltage	VDD1	-0.3 ~ 3.6	V
Analog Power supply voltage	VDD2	-0.3 ~ 3.6	V
LCD Power supply voltage	V0-XV0	-0.3~15	V
LCD Power driving voltage	VG, VM	-0.3 ~ VDD2	V
Operating temperature	TOPR	–30 to +85	°C
Storage temperature	TSTR	–65 to +150	°C



Notes

1. Stresses above those listed under Limiting Values may cause permanent damage to the device.
2. Parameters are valid over operating temperature range unless otherwise specified. All voltages are with respect to VSS unless otherwise noted.
3. Insure the voltage levels of V0, VDD2, VG, VM, VSS and XV0 always match the correct relation:
   V0 ≥ VDD2 > VG > VM > VSS ≥ XV0

12. HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices.

13. DC CHARACTERISTICS

VDD1=1.8V to 3.3V, VSS=0V; Tamb = -30°C to +85°C; unless otherwise specified.

Item	Symbol	Condition	Rating			Unit	Applicable Pin
			Min.	Typ.	Max.		
Operating Voltage (1)	VDD1		1.7	—	3.4	V	VDD1
Operating Voltage (2)	VDD2		2.4	—	3.4	V	VDD2
Input High-level Voltage	V_{IHC}		0.7 x VDD1	—	VDD1	V	MPU Interface
Input Low-level Voltage	V_{ILC}		VSS	—	0.3 x VDD1	V	MPU Interface
Output High-level Voltage	V_{OHC}	I_{OUT}=1mA, VDD1=1.8V	0.8 x VDD1	—	VDD1	V	D[7:0]
Output Low-level Voltage	V_{OLC}	I_{OUT}=-1mA, VDD1=1.8V	VSS	—	0.2 x VDD1	V	D[7:0]
Input Leakage Current	I_{LI}		-1.0	—	1.0	μA	MPU Interface
Output Leakage Current	I_{LO}		-3.0	—	3.0	μA	MPU Interface
Liquid Crystal Driver ON Resistance	R_{ON}	Ta=25°C, Vop=9V, △V=0.9V	—	0.7	—	KΩ	COMx
		Ta=25°C, VG=2V, △V=0.2V	—	0.7	—	KΩ	SEGx
Frame Frequency	FR	FR default (1,0,0), 1/68 Duty Ta = 25°C	68	73	81	Hz	

Note:

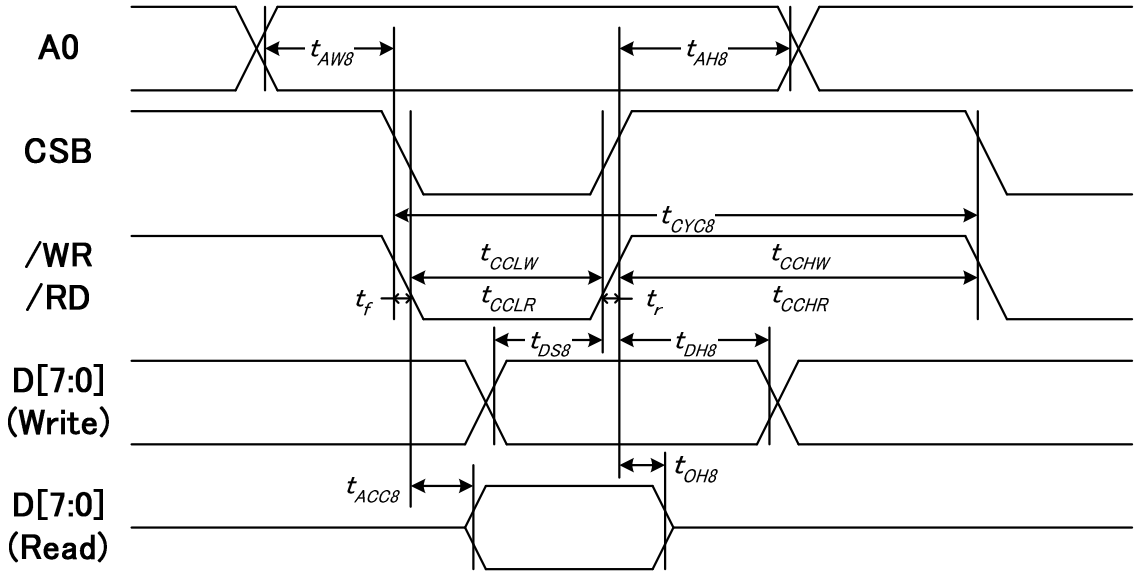
1. Recommend application Vop range : 4V ~ 9.5V.
2. LCD module size : 1.8” (max).

Current consumption: During Display, with internal power system, current consumed by whole IC (bare die).

Test Pattern	Symbol	Condition	Rating			Unit	Note
			Min.	Typ.	Max.		
Display Pattern: SNOW (Static)	ISS	VDD1=VDD2=3.0V, Booster X5, V_{OP} = 9.0 V, Bias=1/9, Ta=25°C	—	110	150	μA	
Power Down	ISS	VDD1=VDD2=3.0V, Ta=25°C	—	1	10	μA	

14. TIMING CHARACTERISTICS

System Bus Read/Write Characteristics (For the 8080 Series MPU)



(VDD = 3.3V , Ta =-30~85°C)

Item	Signal	Symbol	Condition	Min.	Max.	Unit
Address setup time	A0	tAW8		80	—	ns
Address hold time		tAH8		10	—	
System cycle time	/WR	tCYC8		350	—	
Write L pulse width		tCCLW		70	—	
Write H pulse width		tCCHW		50	—	
Read L pulse width	/RD	tCCLR		120	—	
Read H pulse width		tCCHR		50		
Data setup time (Write)	D[7:0]	tDS8		60	—	
Write Data hold time (Write)		tDH8		10	—	
Data access time (Read)		tACC8	CL = 16 pF	—	70	
Output disable time (Read)		tOH8	CL = 16 pF	10	50	

(VDD = 2.8V , Ta =-30~85°C)

Item	Signal	Symbol	Condition	Min.	Max.	Unit
Address setup time	A0	tAW8		120	—	ns
Address hold time		tAH8		15	—	
System cycle time	/WR	tCYC8		450	—	
Write L pulse width		tCCLW		120	—	
Write H pulse width		tCCHW		100	—	
Read L pulse width	/RD	tCCLR		120	—	
Read H pulse width		tCCHR		100	—	
Data setup time (Write)	D[7:0]	tDS8		90	—	
Write Data hold time (Write)		tDH8		15	—	
Data access time (Read)		tACC8	CL = 16 pF	—	140	
Output disable time (Read)		tOH8	CL = 16 pF	10	100	

(VDD = 1.8V , Ta =-30~85°C)

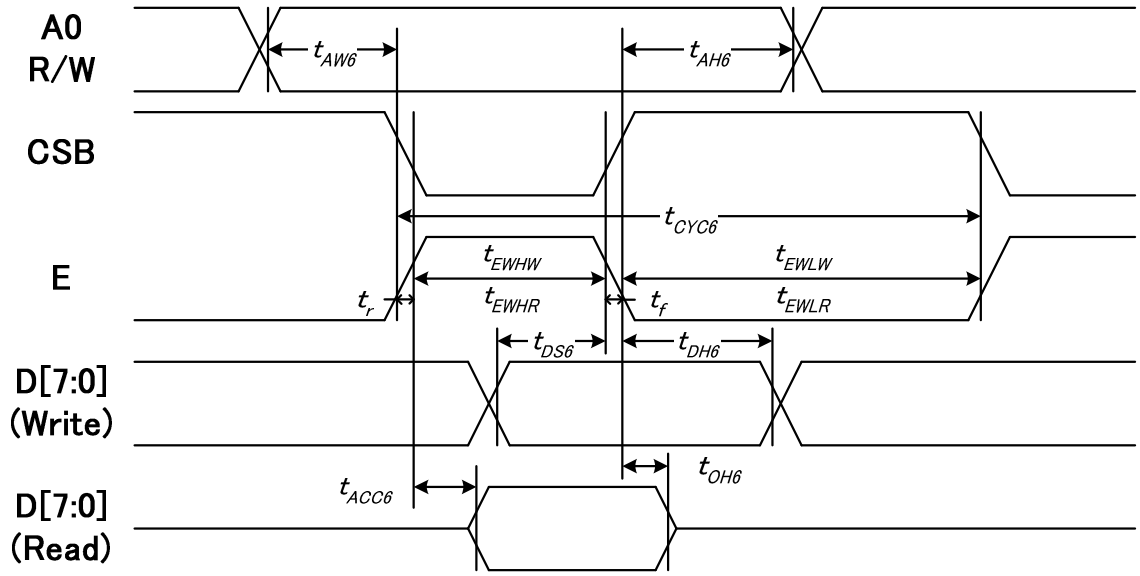
Item	Signal	Symbol	Condition	Min.	Max.	Unit
Address setup time	A0	tAW8		200	—	ns
Address hold time		tAH8		30	—	
System cycle time	/WR	tCYC8		1000	—	
Write L pulse width		tCCLW		360	—	
Write H pulse width		tCCHW		280	—	
Read L pulse width	/RD	tCCLR		360	—	
Read H pulse width		tCCHR		280		
Data setup time (Write)	D[7:0]	tDS8		200	—	
Write Data hold time (Write)		tDH8		30	—	
Data access time (Read)		tACC8	CL = 16 pF	—	240	
Output disable time (Read)		tOH8	CL = 16 pF	10	200	

*1 The input signal rise time and fall time (tr, tf) is specified at 15 ns or less. When the system cycle time is extremely fast, (tr + tf) ≦ (tCYC8 – tCCLW – tCCHW) for (tr + tf) ≦ (tCYC8 – tCCLR – tCCHR) are specified.

*2 All timing is specified using 20% and 80% of VDD1 as the reference.

*3 tCCLW and tCCLR are specified as the overlap between CSB being “L” and WR and RD being at the “L” level.

System Bus Read/Write Characteristics (For the 6800 Series MPU)



(VDD = 3.3V , Ta =-30~85°C)

Item	Signal	Symbol	Condition	Min.	Max.	Unit
Address setup time	A0	tAW6		80	—	ns
Address hold time		tAH6		10	—	
System cycle time	E	tCYC6		240	—	
Enable L pulse width (WRITE)		tEWLW		70	—	
Enable H pulse width (WRITE)		tEWHW		50	—	
Enable L pulse width (READ)		tEWLR		70	—	
Enable H pulse width (READ)		tEWHR		130		
Write data setup time	D[7:0]	tDS6		60	—	
Write data hold time		tDH6		10	—	
Read data access time		tACC6	CL = 16 pF	—	70	
Read data output disable time		tOH6	CL = 16 pF	10	50	

(VDD = 2.8V , Ta =-30~85°C)

Item	Signal	Symbol	Condition	Min.	Max.	Unit
Address setup time	A0	tAW6		100	—	ns
Address hold time		tAH6		15	—	
System cycle time	E	tCYC6		340	—	
Enable L pulse width (WRITE)		tEWLW		120	—	
Enable H pulse width (WRITE)		tEWHW		100	—	
Enable L pulse width (READ)		tEWLR		120	—	
Enable H pulse width (READ)		tEWHR		100	—	
Write data setup time	D[7:0]	tDS6		120	—	
Write data hold time		tDH6		15	—	
Read data access time		tACC6	CL = 16 pF	—	140	
Read data output disable time		tOH6	CL = 16 pF	10	100	

(VDD = 1.8V , Ta =-30~85°C)

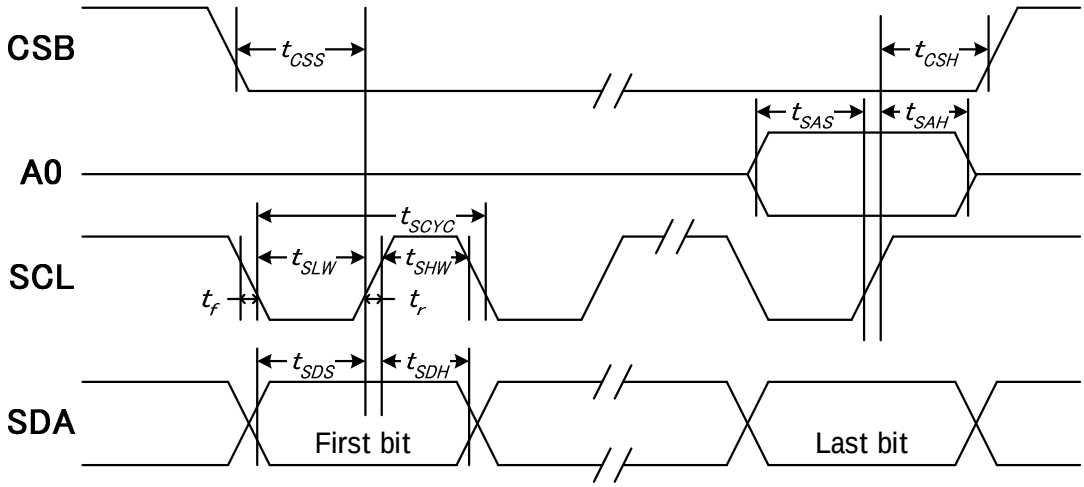
Item	Signal	Symbol	Condition	Min.	Max.	Unit
Address setup time	A0	tAW6		150	—	ns
Address hold time		tAH6		30	—	
System cycle time	E	tCYC6		440	—	
Enable L pulse width (WRITE)		tEWLW		170	—	
Enable H pulse width (WRITE)		tEWHW		150	—	
Enable L pulse width (READ)		tEWLR		170	—	
Enable H pulse width (READ)		tEWHR		150	—	
Write data setup time	D[7:0]	tDS6		180	—	
Write data hold time		tDH6		30	—	
Read data access time		tACC6	CL = 16 pF	—	240	
Read data output disable time		tOH6	CL = 16 pF	10	200	

*1 The input signal rise time and fall time (tr, tf) is specified at 15 ns or less. When the system cycle time is extremely fast, (tr + tf) ≦ (tCYC6 – tEWLW – tEWHW) for (tr + tf) ≦ (tCYC6 – tEWLR – tEWHR) are specified.

*2 All timing is specified using 20% and 80% of VDD1 as the reference.

*3 tEWLW and tEWLR are specified as the overlap between CSB being “L” and E.

Serial Interface (4-Line Interface)



(VDD = 3.3V , Ta =-30~85°C)

Item	Signal	Symbol	Condition	Min.	Max.	Unit
Serial clock period	SCLK	tSCYC		120	—	ns
SCLK “H” pulse width		tSHW		60	—	
SCLK “L” pulse width		tSLW		60	—	
Address setup time	A0	tSAS		20	—	
Address hold time		tSAH		90	—	
Data setup time	SDA	tSDS		20	—	
Data hold time		tSDH		10	—	
CSB-SCLK time	CSB	tCSS		20	—	
CSB-SCLK time		tCSH		120	—	

(VDD = 2.8V , Ta =-30~85°C)

Item	Signal	Symbol	Condition	Min.	Max.	Unit
Serial clock period	SCLK	tSCYC		200	—	ns
SCLK “H” pulse width		tSHW		100	—	
SCLK “L” pulse width		tSLW		100	—	
Address setup time	A0	tSAS		30	—	
Address hold time		tSAH		120	—	
Data setup time	SDA	tSDS		30	—	
Data hold time		tSDH		20	—	
CSB-SCLK time	CSB	tCSS		30	—	
CSB-SCLK time		tCSH		150	—	

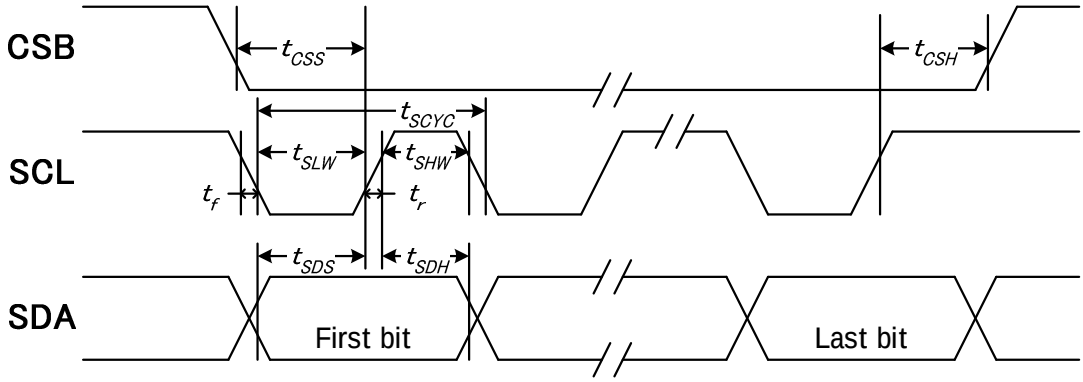
(VDD = 1.8V , Ta =-30~85°C)

Item	Signal	Symbol	Condition	Min.	Max.	Unit
Serial clock period	SCLK	tSCYC		280	—	ns
SCLK “H” pulse width		tSHW		140	—	
SCLK “L” pulse width		tSLW		140	—	
Address setup time	A0	tSAS		50	—	
Address hold time		tSAH		150	—	
Data setup time	SDA	tSDS		50	—	
Data hold time		tSDH		50	—	
CSB-SCLK time	CSB	tCSS		40	—	
CSB-SCLK time		tCSH		180	—	

*1 The input signal rise and fall time (tr, tf) are specified at 15 ns or less.

*2 All timing is specified using 20% and 80% of VDD1 as the standard.

Serial Interface (3-Line Interface)



(VDD = 3.3V , Ta =-30~85°C)

Item	Signal	Symbol	Condition	Min.	Max.	Unit
Serial clock period	SCLK	tSCYC		120	—	ns
SCLK “H” pulse width		tSHW		60	—	
SCLK “L” pulse width		tSLW		60	—	
Data setup time	SDA	tSDS		20	—	
Data hold time		tSDH		10	—	
CSB-SCLK time	CSB	tCSS		20	—	
CSB-SCLK time		tCSH		130	—	

(VDD = 2.8V , Ta =-30~85°C)

Item	Signal	Symbol	Condition	Min.	Max.	Unit
Serial clock period	SCLK	tSCYC		180	—	ns
SCLK “H” pulse width		tSHW		90	—	
SCLK “L” pulse width		tSLW		90	—	
Data setup time	SDA	tSDS		30	—	
Data hold time		tSDH		20	—	
CSB-SCLK time	CSB	tCSS		30	—	
CSB-SCLK time		tCSH		160	—	

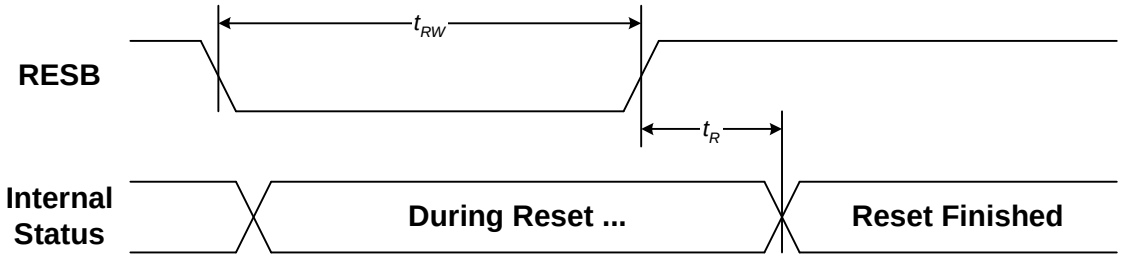
(VDD = 1.8V , Ta =-30~85°C)

Item	Signal	Symbol	Condition	Min.	Max.	Unit
Serial clock period	SCLK	tSCYC		240	—	ns
SCLK “H” pulse width		tSHW		120	—	
SCLK “L” pulse width		tSLW		120	—	
Data setup time	SDA	tSDS		60	—	
Data hold time		tSDH		50	—	
CSB-SCLK time	CSB	tCSS		40	—	
CSB-SCLK time		tCSH		190	—	

*1 The input signal rise and fall time (tr, tf) are specified at 15 ns or less.

*2 All timing is specified using 20% and 80% of VDD1 as the standard.

Reset Timing



(VDD = 3.3V , Ta =-30~85°C)

Item	Symbol	Condition	Min.	Max.	Unit
Reset time	tR		—	1.5	us
Reset “L” pulse width	tRW		1.5	—	

(VDD = 2.8V , Ta =-30~85°C)

Item	Symbol	Condition	Min.	Max.	Unit
Reset time	tR		—	2.0	us
Reset “L” pulse width	tRW		2.0		

(VDD = 1.8V , Ta =-30~85°C)

Item	Symbol	Condition	Min.	Max.	Unit
Reset time	tR		—	3.0	us
Reset “L” pulse width	tRW		3.0	—	

APPLICATION NOTE

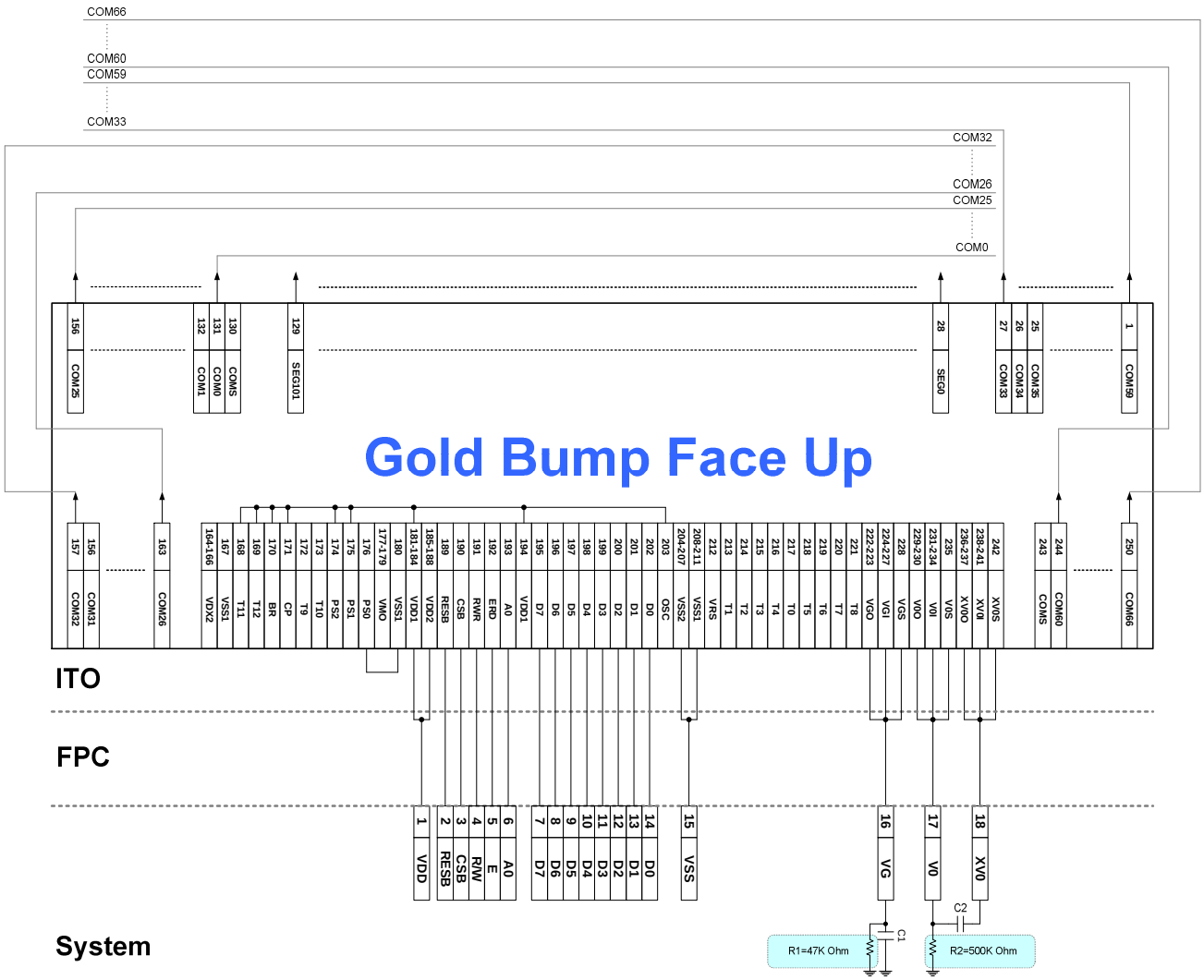
Application Circuits

The application circuits are for reference only and actual settings are dependent on LCD module characteristics.

ST7579

Interface : 6800 series
Resolution : 68(67COM+ICON)*102(SEG)
Internal analog circuit
Internal OSC
Booster : X5
Bias ratio default : 1/9
(bias ratio can be changed by instruction)
Vop=8.76V
C1=0.1uF, C2=0.1uF

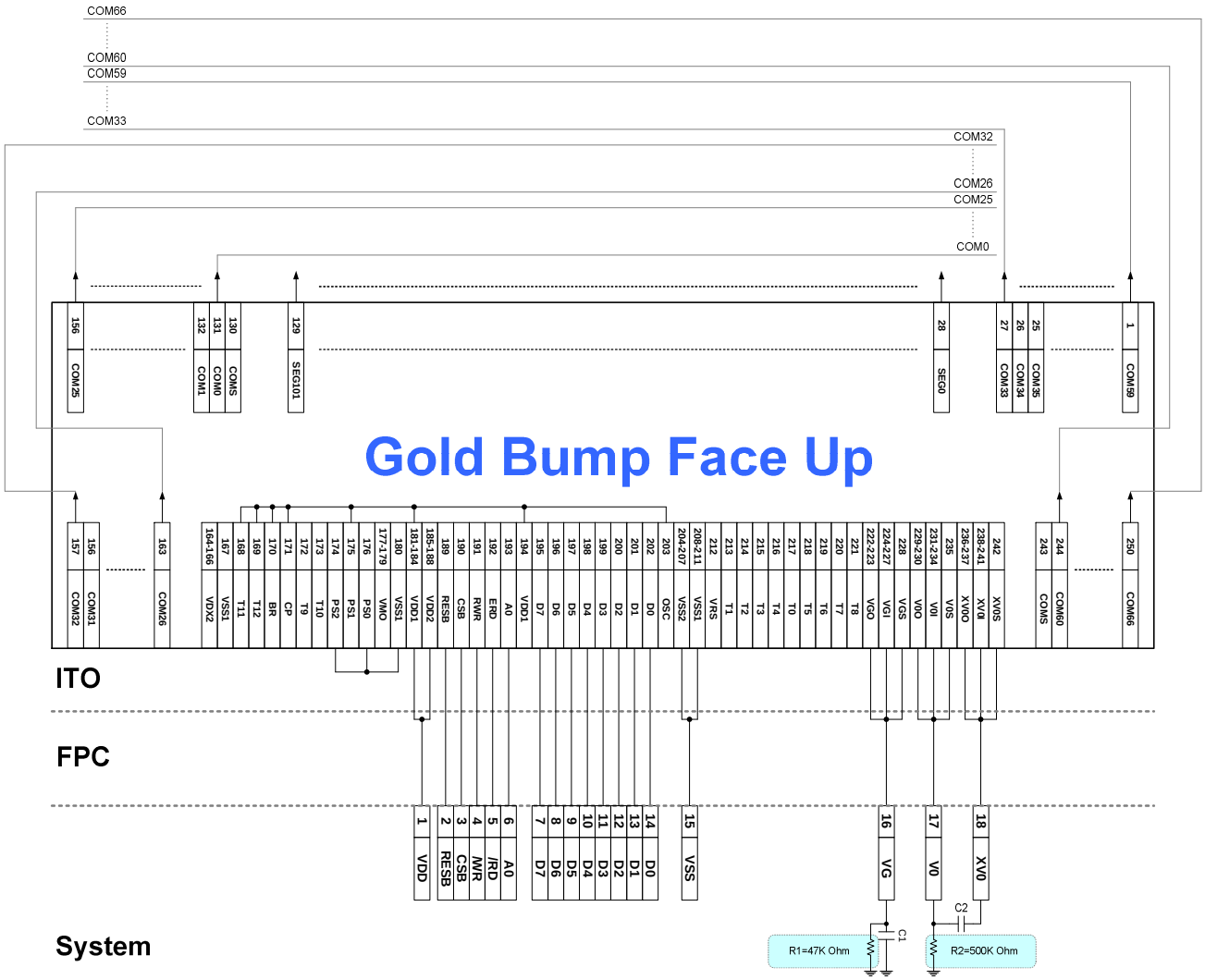
VDD1=VDD2=2.8V
OSC : VDD1
T11 : VDD1
T12 : VDD1
PS0 : VSS1
PS1 : VDD1
PS2 : VDD1
CP : VDD1
BR : VDD1



ST7579

Interface : 8080 series
Resolution : 68(67COM+ICON)*102(SEG)
Internal analog circuit
Internal OSC
Booster : X5
Bias ratio default : 1/9
(bias ratio can be changed by instruction)
Vop=8.76V
C1=0.1uF, C2=0.1uF

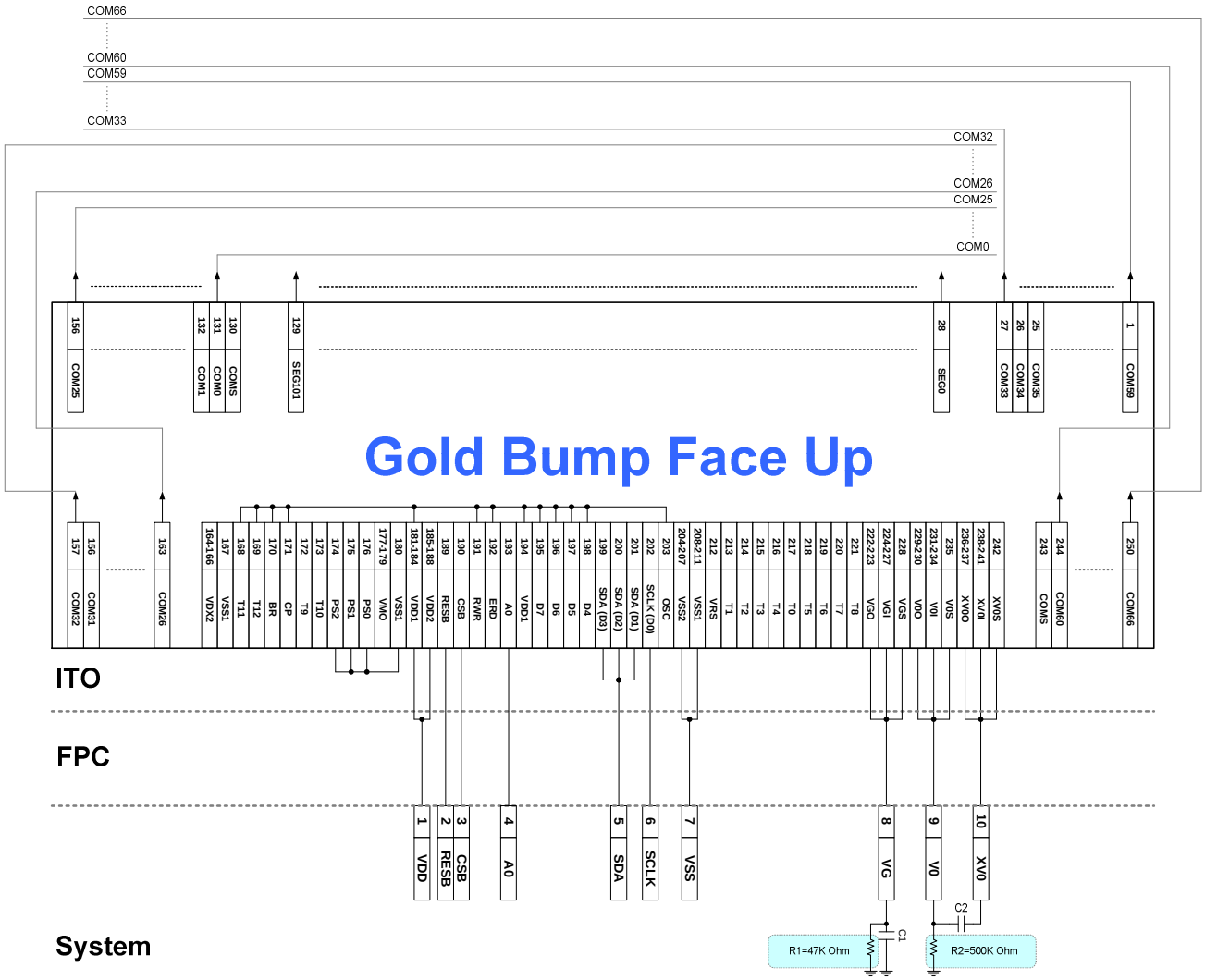
VDD1=VDD2=2.8V
OSC : VDD1
T11 : VDD1
T12 : VDD1
PS0 : VSS1
PS1 : VDD1
PS2 : VSS1
CP : VDD1
BR : VDD1



ST7579

Interface : 4-Line SPI
Resolution : 68(67COM+ICON)*102(SEG)
Internal analog circuit
Internal OSC
Booster : X5
Bias ratio default : 1/9
(bias ratio can be changed by instruction)
Vop=8.76V
C1=0.1uF, C2=0.1uF

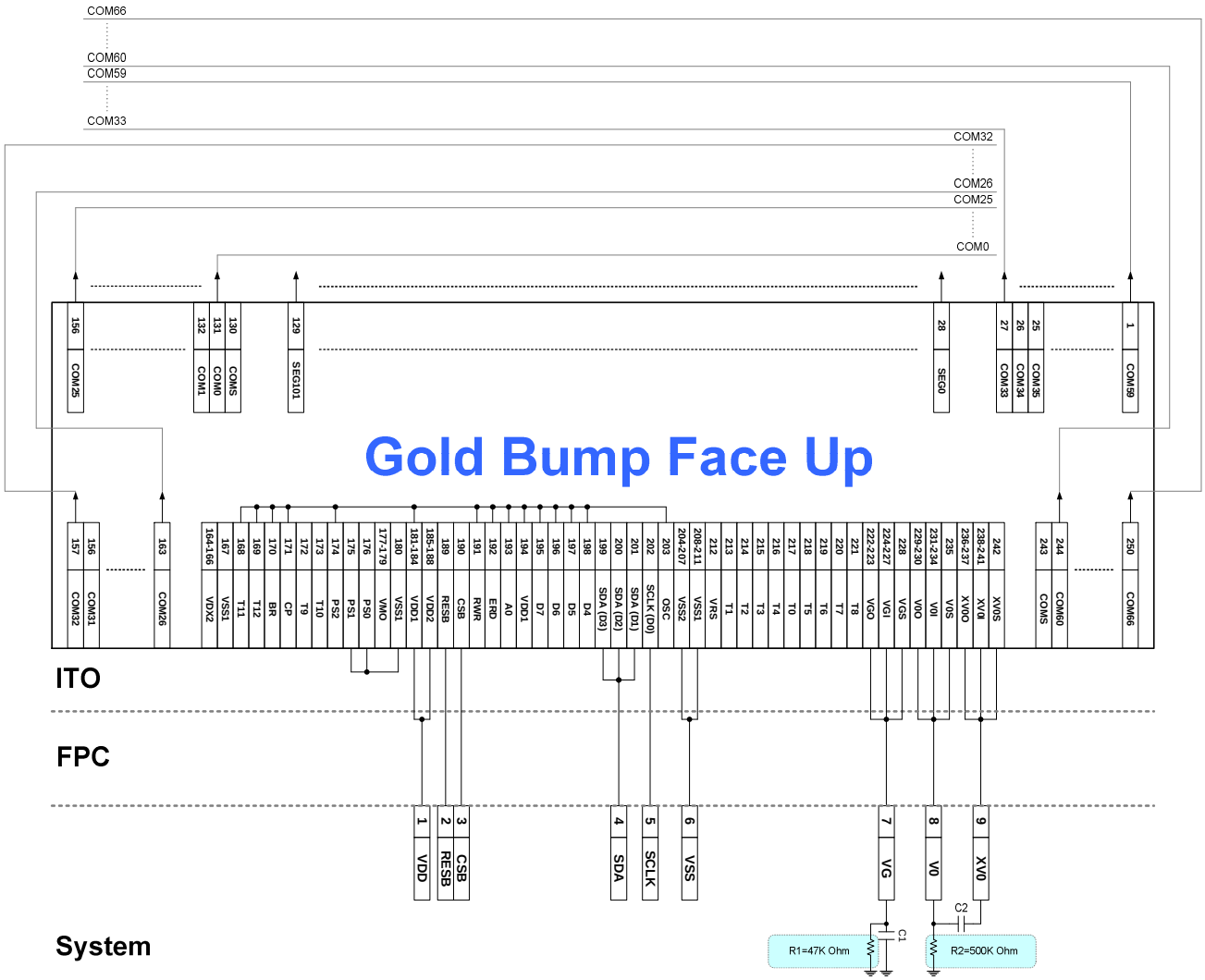
VDD1=VDD2=2.8V
OSC : VDD1
T11 : VDD1
T12 : VDD1
PS0 : VSS1
PS1 : VSS1
PS2 : VSS1
CP : VDD1
BR : VDD1



ST7579

Interface : 3-Line SPI
Resolution : 68(67COM+ICON)*102(SEG)
Internal analog circuit
Internal OSC
Booster : X5
Bias ratio default : 1/9
(bias ratio can be changed by instruction)
Vop=8.76V
C1=0.1uF, C2=0.1uF

VDD1=VDD2=2.8V
OSC : VDD1
T11 : VDD1
T12 : VDD1
PS0 : VSS1
PS1 : VSS1
PS2 : VDD1
CP : VDD1
BR : VDD1



Selection of Application Voltage

Power Range Summary

- Positive Booster: ***(VDD2 x PCn x BE) ≥ V0*** or ***(VDD2 x PCn x BE) ≥ Vop***;
- Negative Booster: ***[–VDD2 x (PCn - 1) x BE] ≤ XV0*** or ***[VDD2 x (PCn - 1) x BE] ≥ (Vop - VG)***,
  where VG = Vop x 2 / N;
- Vop requirement: ***[VDD2 x (PCn - 1) x BE] ≥ [Vop x (N - 2) / N]*** or ***[Vop ≤ VDD2 x (PCn – 1) x BE x N / (N - 2)]***.
- PCn is the booster stage and BE is the booster efficiency. Referential values are listed below: (assume VDD2=2.4V)
  Module Size ≤ 1.4”: BE=80% (min);
  Module Size = 1.4”~1.8”: BE=76% (min).
  Actual BE should be determined by module loading and ITO resistance value.
- 1.24 ≤ VG < VDD2. Recommend VG is: VDD2-VG around 0.5~0.8V.
- VM=VG/2 and 0.62V ≤ VM < VDD2.
- The worse condition should be considered:
  Low temperature effect and display on with snow pattern on panel (max: 1.8”).

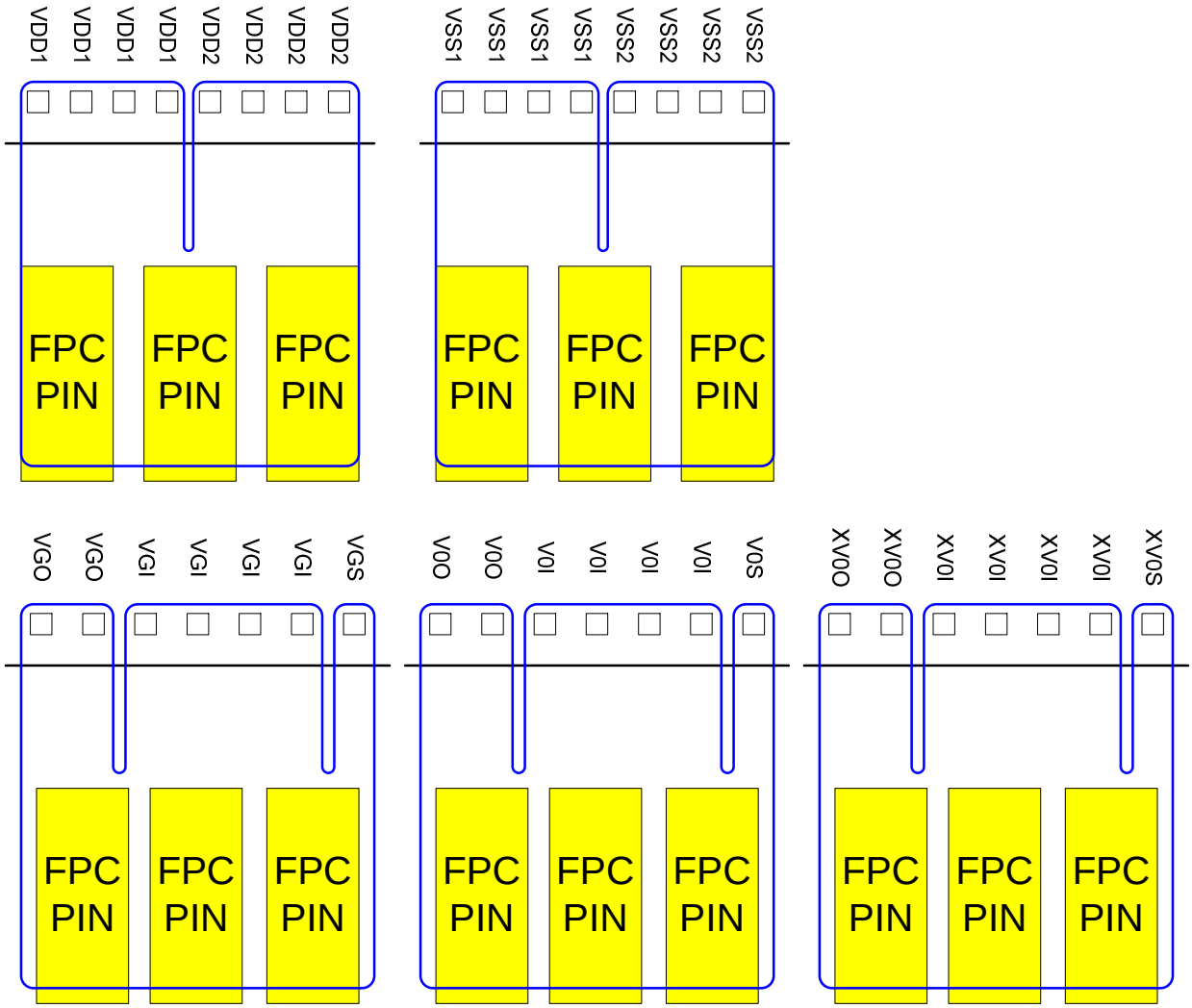
Referential LCD Module Setting

VDD1=VDD2=2.8V, Panel Size=1.4”

Duty	Booster	Vop	Bias
1/17, PS=1, WS=0	4X, CP=L	5.01V ~ 5.52V, PRS=0	1/5, BS[2:0]=1,1,0
1/33, PS=1, WS=1	4X, CP=L	6V ~ 6.51V, PRS=0	1/6, BS[2:0]=1,0,1
1/68, PS=0, WS=X	5X, CP=H	8.49V ~ 9V, PRS=1	1/9, BS[2:0]=0,1,1

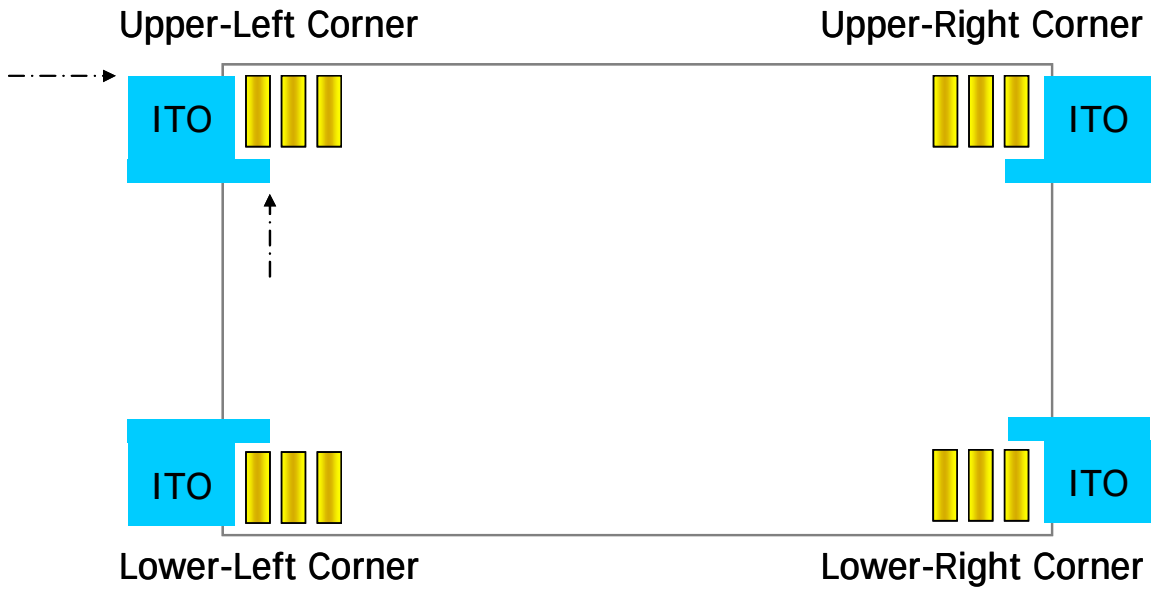
Note: It is recommended to reserve some range for user adjustment and temperature effect.

ITO Layout Reference



Manual Alignment by ITO Layout

Optional ITO alignment mark for manual COG machine (reference ITO mark).



Reversion History

Version	Date	Description
1.0	2007/01/18	Formal release.
1.1	2007/02/28	l Modify feature description.
1.2	2007/03/14	l Add detailed operating flows and power sequences. l Add application note for power selection. l Reserve Booster X2 function.
1.2a	2007/04/23	l Add Temperature Gradient of Regulator. l Update ITO Resistance suggestion: No Limitation => 5K. l Rearrange Microprocessor Interface section. l Fix typing mistake.
1.2b	2007/04/26	l Modify description of the reserved resistor. l More detailed ITO reference layout.
1.2c	2007/06/30	l Add an alternated power OFF operating flow. l Fix typing mistake (PAD167 & PAD180 are VSS1). l Modify Frame Rate Max. & Min. value to cover testing tolerance.
1.3	2007/11/12	l Fix typing mistake (PAD Coordinate of VRS). l Fix typing mistake of MPU interface (Page 18). l Fix typing mistake of 8080 timing (Page 42). l Add description of the external power components for critical case (Page 26, Page 50~53).
1.3a	2008/11/06	l Update pad pitch to the second decimal point. l Update pad center coordinate of VRS to the second decimal point.