ST7511U

640 x 320 Mono-color TFT-LCD Controller/Driver

ST7511U	**Parallel Interface: 8080,6800** **Serial Interface: 3-line, 4-line**	

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1. INTRODUCTION

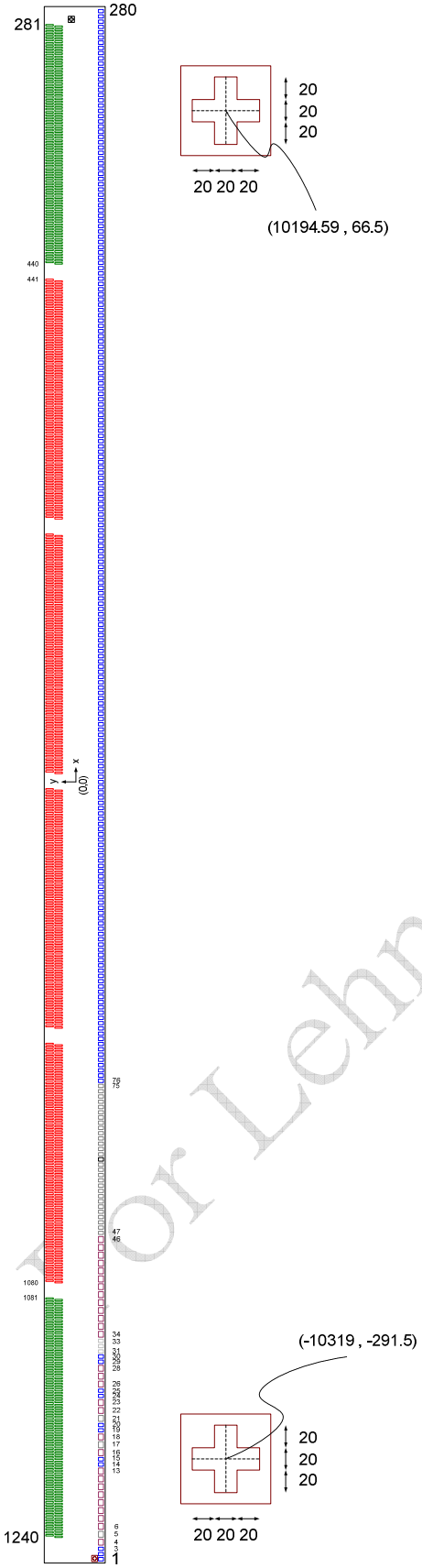
The ST7511U is a 1-chip driver for driving amorphous Si-TFT with built-in data RAM that contains 640 × 320 dots, supporting 16-, 4-, and 2-gray scale display. It includes built-in power supply circuit that all voltage level are generated for display, and it can be directly connected to MPU bus with 8bit parallel interface or 4-wire serial interface. ST7511U can drive the LCD panel without external clock, so that it is possible to make a display system with the fewest components and minimal power consumption.

2. FEATURES

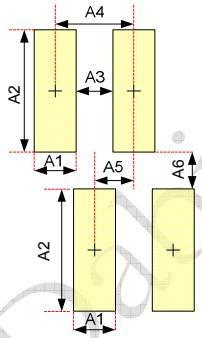
- **Single-chip Mono-color TFT-LCD Controller & Driver**
- **Gray Scale**
  - 16 Gray scale (4BPP)
  - 4 Gray scale (2BPP)
  - 2 Gray scale (1BPP)
- **Display RAM**
  - Capacity: 640x320x4 = 819,200 bits
    - 1BPP mode: 4 data frame are available.
    - 2BPP mode: 2 data frame are available.
    - 4BPP mode and 160 lines or less: 2 data frame are available
- **Interface**
  - 8-bit parallel bi-directional interface with 6800 and 8080
  - 4-line SPI
  - 3-line SPI
- **DC-VCOM Driving Methods**
  - Dot inversion
- **Temperature Compensation Functions**
  - Voltage
    - GVDD and GVCL temperature compensation
    - VCOM temperature compensation
    - VGH temperature compensation
  - Frame rate temperature compensation
- **Operation Voltage**
  - Input voltage:
    - Analog power supply: 3.0V ~ 5.0V
    - IO power supply: 3.0V ~ 5.0V
  - Output voltage:
    - Max. gate voltage: VGH – VGL = 30V
    - Max. source voltage: GVDD = 6.2V
    - VCOM voltage: -0.300V ~ -1.885V
- **None Volatility Memory**
  - MTP
    - VCOM offset: 7bits x 2
    - User ID: 8bits x 4
- **Backlight PWM Controller**
- **Temperature Range: -30℃ ~ 80℃**
- **Package Type: COG**

3. PIN ASSIGNMENT

3.1 ST7511U COG Outline (Gold Bump Face-up)

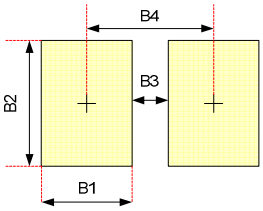


Item	Dimension(um)
Chip length (x)	20,786
Chip width (y)	841
Chip thickness	480
Bump height	15
Linear coefficient (α) of thermal expansion(10^{-6}/℃)	
2.6	
Type A	
Pin	281 ~ 1240



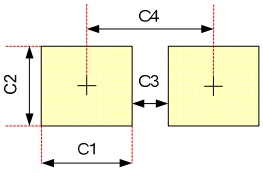
Item	Dimension(um)
A1	22
A2	100
A3	18
A4	40
A5	20
A6	20

Type B	
Pin	1~3,14,15,19,20,24,25,29~33,47~280



Item	Dimension(um)
B1	44
B2	70
B3	26
B4	70

Type C	
Pin	4~13,16~18,21~23,26~28,34~46



Item	Dimension(um)
C1	79
C2	70
C3	26
C4	105

3.2 Pad Center Coordinates

Pad	Name	X	Y
1	VPP	-10325	-369.5
2	VPP	-10255	-369.5
3	VPP	-10185	-369.5
4	EXTB	-10097.5	-369.5
5	TEST1	-9992.5	-369.5
6	PWM	-9887.5	-369.5
7	VSYNCO	-9782.5	-369.5
8	CL	-9677.5	-369.5
9	XEEWP	-9572.5	-369.5
10	EESO	-9467.5	-369.5
11	EESI	-9362.5	-369.5
12	EESCL	-9257.5	-369.5
13	XEECS	-9152.5	-369.5
14	VDDI	-9065	-369.5
15	VDDI	-8995	-369.5
16	RSTEN	-8907.5	-369.5
17	TEST2	-8802.5	-369.5
18	EEEN	-8697.5	-369.5
19	DGND	-8610	-369.5
20	DGND	-8540	-369.5
21	TEST3	-8452.5	-369.5
22	PX2SET	-8347.5	-369.5
23	EXAVDD	-8242.5	-369.5
24	VDDI	-8155	-369.5
25	VDDI	-8085	-369.5
26	IF0	-7997.5	-369.5
27	IF1	-7892.5	-369.5
28	CLS	-7787.5	-369.5
29	DGND	-7700	-369.5
30	DGND	-7630	-369.5
31	Dummy	-7560	-369.5
32	Dummy	-7490	-369.5
33	Dummy	-7420	-369.5
34	RSTB	-7332.5	-369.5
35	CSB	-7227.5	-369.5
36	A0	-7122.5	-369.5
37	RWR	-7017.5	-369.5
38	ERD	-6912.5	-369.5
39	D0	-6807.5	-369.5
40	D1	-6702.5	-369.5
41	D2	-6597.5	-369.5
42	D3	-6492.5	-369.5
43	D4	-6387.5	-369.5

Pad	Name	X	Y
44	D5	-6282.5	-369.5
45	D6	-6177.5	-369.5
46	D7	-6072.5	-369.5
47	T1	-5985	-369.5
48	T2	-5915	-369.5
49	T3	-5845	-369.5
50	T4	-5775	-369.5
51	TFCOM0	-5705	-369.5
52	T5	-5635	-369.5
53	T6	-5565	-369.5
54	T7	-5495	-369.5
55	T8	-5425	-369.5
56	T9	-5355	-369.5
57	T10	-5285	-369.5
58	T11	-5215	-369.5
59	T12	-5145	-369.5
60	T13	-5075	-369.5
61	TFCOM1	-5005	-369.5
62	T14	-4935	-369.5
63	T15	-4865	-369.5
64	T16	-4795	-369.5
65	T17	-4725	-369.5
66	T18	-4655	-369.5
67	T19	-4585	-369.5
68	T20	-4515	-369.5
69	T21	-4445	-369.5
70	T22	-4375	-369.5
71	TFCOM2	-4305	-369.5
72	T23	-4235	-369.5
73	T24	-4165	-369.5
74	T25	-4095	-369.5
75	T26	-4025	-369.5
76	VREFC	-3955	-369.5
77	VREFC	-3885	-369.5
78	VCCI	-3815	-369.5
79	VCCI	-3745	-369.5
80	VCCI	-3675	-369.5
81	VCCI	-3605	-369.5
82	VCCO	-3535	-369.5
83	VCCO	-3465	-369.5
84	DGND	-3395	-369.5
85	DGND	-3325	-369.5
86	DGND	-3255	-369.5

Pad	Name	X	Y
87	DGND	-3185	-369.5
88	DGND	-3115	-369.5
89	DGND	-3045	-369.5
90	DGND	-2975	-369.5
91	DGND	-2905	-369.5
92	DGND	-2835	-369.5
93	DGND	-2765	-369.5
94	VDDI	-2695	-369.5
95	VDDI	-2625	-369.5
96	VDDI	-2555	-369.5
97	VDDI	-2485	-369.5
98	VDDI	-2415	-369.5
99	VDDI	-2345	-369.5
100	VDDI	-2275	-369.5
101	VDDI	-2205	-369.5
102	VDDI	-2135	-369.5
103	VDDI	-2065	-369.5
104	VDDP	-1995	-369.5
105	VDDP	-1925	-369.5
106	PGND	-1855	-369.5
107	PGND	-1785	-369.5
108	AGND	-1715	-369.5
109	AGND	-1645	-369.5
110	AGND	-1575	-369.5
111	AGND	-1505	-369.5
112	VDDA	-1435	-369.5
113	VDDA	-1365	-369.5
114	VDDA	-1295	-369.5
115	VDDA	-1225	-369.5
116	VCOM	-1155	-369.5
117	VCOM	-1085	-369.5
118	VCOM	-1015	-369.5
119	VCOM	-945	-369.5
120	VCOM	-875	-369.5
121	GVCL	-805	-369.5
122	GVCL	-735	-369.5
123	GVCL	-665	-369.5
124	GVDD	-595	-369.5
125	GVDD	-525	-369.5
126	GVDD	-455	-369.5
127	VLDOA	-385	-369.5
128	VLDOA	-315	-369.5
129	VDDA	-245	-369.5
130	VDDA	-175	-369.5

Pad	Name	X	Y
131	VDDA	-105	-369.5
132	VDDA	-35	-369.5
133	VDDA	35	-369.5
134	VDDA	105	-369.5
135	VDDA	175	-369.5
136	VDDA	245	-369.5
137	VDDA	315	-369.5
138	VDDA	385	-369.5
139	VDDA	455	-369.5
140	VDDA	525	-369.5
141	VDDA	595	-369.5
142	VDDA	665	-369.5
143	C11N	735	-369.5
144	C11N	805	-369.5
145	C11N	875	-369.5
146	C11N	945	-369.5
147	C11N	1015	-369.5
148	C11N	1085	-369.5
149	C11P	1155	-369.5
150	C11P	1225	-369.5
151	C11P	1295	-369.5
152	C11P	1365	-369.5
153	C11P	1435	-369.5
154	C11P	1505	-369.5
155	C12N	1575	-369.5
156	C12N	1645	-369.5
157	C12N	1715	-369.5
158	C12N	1785	-369.5
159	C12N	1855	-369.5
160	C12N	1925	-369.5
161	C12P	1995	-369.5
162	C12P	2065	-369.5
163	C12P	2135	-369.5
164	C12P	2205	-369.5
165	C12P	2275	-369.5
166	C12P	2345	-369.5
167	AVDDO	2415	-369.5
168	AVDDO	2485	-369.5
169	AVDDO	2555	-369.5
170	AVDDO	2625	-369.5
171	AVDDO	2695	-369.5
172	AVDDO	2765	-369.5
173	VDDA	2835	-369.5
174	VDDA	2905	-369.5

Pad	Name	X	Y
175	AVDD	2975	-369.5
176	AVDD	3045	-369.5
177	AVDD	3115	-369.5
178	AVDD	3185	-369.5
179	AVDD	3255	-369.5
180	AVDD	3325	-369.5
181	AGND	3395	-369.5
182	AGND	3465	-369.5
183	AGND	3535	-369.5
184	AGND	3605	-369.5
185	AGND	3675	-369.5
186	AGND	3745	-369.5
187	AGND	3815	-369.5
188	AGND	3885	-369.5
189	AGND	3955	-369.5
190	AGND	4025	-369.5
191	AGND	4095	-369.5
192	AGND	4165	-369.5
193	AGND	4235	-369.5
194	AGND	4305	-369.5
195	C21N	4375	-369.5
196	C21N	4445	-369.5
197	C21N	4515	-369.5
198	C21N	4585	-369.5
199	C21N	4655	-369.5
200	C21N	4725	-369.5
201	C21P	4795	-369.5
202	C21P	4865	-369.5
203	C21P	4935	-369.5
204	C21P	5005	-369.5
205	C21P	5075	-369.5
206	C21P	5145	-369.5
207	C22N	5215	-369.5
208	C22N	5285	-369.5
209	C22N	5355	-369.5
210	C22N	5425	-369.5
211	C22N	5495	-369.5
212	C22N	5565	-369.5
213	C22P	5635	-369.5
214	C22P	5705	-369.5
215	C22P	5775	-369.5
216	C22P	5845	-369.5
217	C22P	5915	-369.5
218	C22P	5985	-369.5

Pad	Name	X	Y
219	AVCLO	6055	-369.5
220	AVCLO	6125	-369.5
221	AVCLO	6195	-369.5
222	AVCLO	6265	-369.5
223	AGND	6335	-369.5
224	AGND	6405	-369.5
225	AVCL	6475	-369.5
226	AVCL	6545	-369.5
227	AVCL	6615	-369.5
228	AVCL	6685	-369.5
229	AVCL	6755	-369.5
230	AVCL	6825	-369.5
231	AGND	6895	-369.5
232	AGND	6965	-369.5
233	VGHREG	7035	-369.5
234	VGHREG	7105	-369.5
235	VGLREG	7175	-369.5
236	VGLREG	7245	-369.5
237	VGL	7315	-369.5
238	VGL	7385	-369.5
239	VGL	7455	-369.5
240	VGL	7525	-369.5
241	VGL	7595	-369.5
242	C33N	7665	-369.5
243	C33N	7735	-369.5
244	C33N	7805	-369.5
245	C33N	7875	-369.5
246	C33P	7945	-369.5
247	C33P	8015	-369.5
248	C33P	8085	-369.5
249	C33P	8155	-369.5
250	C32N	8225	-369.5
251	C32N	8295	-369.5
252	C32N	8365	-369.5
253	C32N	8435	-369.5
254	C32P	8505	-369.5
255	C32P	8575	-369.5
256	C32P	8645	-369.5
257	C32P	8715	-369.5
258	C31N	8785	-369.5
259	C31N	8855	-369.5
260	C31N	8925	-369.5
261	C31N	8995	-369.5
262	C31P	9065	-369.5

Pad	Name	X	Y
263	C31P	9135	-369.5
264	C31P	9205	-369.5
265	C31P	9275	-369.5
266	AGND	9345	-369.5
267	AGND	9415	-369.5
268	VGH	9485	-369.5
269	VGH	9555	-369.5
270	VGH	9625	-369.5
271	VGH	9695	-369.5
272	VGH	9765	-369.5
273	C41N	9835	-369.5
274	C41N	9905	-369.5
275	C41N	9975	-369.5
276	C41N	10045	-369.5
277	C41P	10115	-369.5
278	C41P	10185	-369.5
279	C41P	10255	-369.5
280	C41P	10325	-369.5
281	GD[2]	10130	347.5
282	GD[4]	10110	227.5
283	GD[6]	10090	347.5
284	GD[8]	10070	227.5
285	GD[10]	10050	347.5
286	GD[12]	10030	227.5
287	GD[14]	10010	347.5
288	GD[16]	9990	227.5
289	GD[18]	9970	347.5
290	GD[20]	9950	227.5
291	GD[22]	9930	347.5
292	GD[24]	9910	227.5
293	GD[26]	9890	347.5
294	GD[28]	9870	227.5
295	GD[30]	9850	347.5
296	GD[32]	9830	227.5
297	GD[34]	9810	347.5
298	GD[36]	9790	227.5
299	GD[38]	9770	347.5
300	GD[40]	9750	227.5
301	GD[42]	9730	347.5
302	GD[44]	9710	227.5
303	GD[46]	9690	347.5
304	GD[48]	9670	227.5
305	GD[50]	9650	347.5
306	GD[52]	9630	227.5

Pad	Name	X	Y
307	GD[54]	9610	347.5
308	GD[56]	9590	227.5
309	GD[58]	9570	347.5
310	GD[60]	9550	227.5
311	GD[62]	9530	347.5
312	GD[64]	9510	227.5
313	GD[66]	9490	347.5
314	GD[68]	9470	227.5
315	GD[70]	9450	347.5
316	GD[72]	9430	227.5
317	GD[74]	9410	347.5
318	GD[76]	9390	227.5
319	GD[78]	9370	347.5
320	GD[80]	9350	227.5
321	GD[82]	9330	347.5
322	GD[84]	9310	227.5
323	GD[86]	9290	347.5
324	GD[88]	9270	227.5
325	GD[90]	9250	347.5
326	GD[92]	9230	227.5
327	GD[94]	9210	347.5
328	GD[96]	9190	227.5
329	GD[98]	9170	347.5
330	GD[100]	9150	227.5
331	GD[102]	9130	347.5
332	GD[104]	9110	227.5
333	GD[106]	9090	347.5
334	GD[108]	9070	227.5
335	GD[110]	9050	347.5
336	GD[112]	9030	227.5
337	GD[114]	9010	347.5
338	GD[116]	8990	227.5
339	GD[118]	8970	347.5
340	GD[120]	8950	227.5
341	GD[122]	8930	347.5
342	GD[124]	8910	227.5
343	GD[126]	8890	347.5
344	GD[128]	8870	227.5
345	GD[130]	8850	347.5
346	GD[132]	8830	227.5
347	GD[134]	8810	347.5
348	GD[136]	8790	227.5
349	GD[138]	8770	347.5
350	GD[140]	8750	227.5

Pad	Name	X	Y
351	GD[142]	8730	347.5
352	GD[144]	8710	227.5
353	GD[146]	8690	347.5
354	GD[148]	8670	227.5
355	GD[150]	8650	347.5
356	GD[152]	8630	227.5
357	GD[154]	8610	347.5
358	GD[156]	8590	227.5
359	GD[158]	8570	347.5
360	GD[160]	8550	227.5
361	GD[162]	8530	347.5
362	GD[164]	8510	227.5
363	GD[166]	8490	347.5
364	GD[168]	8470	227.5
365	GD[170]	8450	347.5
366	GD[172]	8430	227.5
367	GD[174]	8410	347.5
368	GD[176]	8390	227.5
369	GD[178]	8370	347.5
370	GD[180]	8350	227.5
371	GD[182]	8330	347.5
372	GD[184]	8310	227.5
373	GD[186]	8290	347.5
374	GD[188]	8270	227.5
375	GD[190]	8250	347.5
376	GD[192]	8230	227.5
377	GD[194]	8210	347.5
378	GD[196]	8190	227.5
379	GD[198]	8170	347.5
380	GD[200]	8150	227.5
381	GD[202]	8130	347.5
382	GD[204]	8110	227.5
383	GD[206]	8090	347.5
384	GD[208]	8070	227.5
385	GD[210]	8050	347.5
386	GD[212]	8030	227.5
387	GD[214]	8010	347.5
388	GD[216]	7990	227.5
389	GD[218]	7970	347.5
390	GD[220]	7950	227.5
391	GD[222]	7930	347.5
392	GD[224]	7910	227.5
393	GD[226]	7890	347.5
394	GD[228]	7870	227.5

Pad	Name	X	Y
395	GD[230]	7850	347.5
396	GD[232]	7830	227.5
397	GD[234]	7810	347.5
398	GD[236]	7790	227.5
399	GD[238]	7770	347.5
400	GD[240]	7750	227.5
401	GD[242]	7730	347.5
402	GD[244]	7710	227.5
403	GD[246]	7690	347.5
404	GD[248]	7670	227.5
405	GD[250]	7650	347.5
406	GD[252]	7630	227.5
407	GD[254]	7610	347.5
408	GD[256]	7590	227.5
409	GD[258]	7570	347.5
410	GD[260]	7550	227.5
411	GD[262]	7530	347.5
412	GD[264]	7510	227.5
413	GD[266]	7490	347.5
414	GD[268]	7470	227.5
415	GD[270]	7450	347.5
416	GD[272]	7430	227.5
417	GD[274]	7410	347.5
418	GD[276]	7390	227.5
419	GD[278]	7370	347.5
420	GD[280]	7350	227.5
421	GD[282]	7330	347.5
422	GD[284]	7310	227.5
423	GD[286]	7290	347.5
424	GD[288]	7270	227.5
425	GD[290]	7250	347.5
426	GD[292]	7230	227.5
427	GD[294]	7210	347.5
428	GD[296]	7190	227.5
429	GD[298]	7170	347.5
430	GD[300]	7150	227.5
431	GD[302]	7130	347.5
432	GD[304]	7110	227.5
433	GD[306]	7090	347.5
434	GD[308]	7070	227.5
435	GD[310]	7050	347.5
436	GD[312]	7030	227.5
437	GD[314]	7010	347.5
438	GD[316]	6990	227.5

Pad	Name	X	Y
439	GD[318]	6970	347.5
440	GD[320]	6950	227.5
441	SO[640]	6698	347.5
442	SO[639]	6678	227.5
443	SO[638]	6658	347.5
444	SO[637]	6638	227.5
445	SO[636]	6618	347.5
446	SO[635]	6598	227.5
447	SO[634]	6578	347.5
448	SO[633]	6558	227.5
449	SO[632]	6538	347.5
450	SO[631]	6518	227.5
451	SO[630]	6498	347.5
452	SO[629]	6478	227.5
453	SO[628]	6458	347.5
454	SO[627]	6438	227.5
455	SO[626]	6418	347.5
456	SO[625]	6398	227.5
457	SO[624]	6378	347.5
458	SO[623]	6358	227.5
459	SO[622]	6338	347.5
460	SO[621]	6318	227.5
461	SO[620]	6298	347.5
462	SO[619]	6278	227.5
463	SO[618]	6258	347.5
464	SO[617]	6238	227.5
465	SO[616]	6218	347.5
466	SO[615]	6198	227.5
467	SO[614]	6178	347.5
468	SO[613]	6158	227.5
469	SO[612]	6138	347.5
470	SO[611]	6118	227.5
471	SO[610]	6098	347.5
472	SO[609]	6078	227.5
473	SO[608]	6058	347.5
474	SO[607]	6038	227.5
475	SO[606]	6018	347.5
476	SO[605]	5998	227.5
477	SO[604]	5978	347.5
478	SO[603]	5958	227.5
479	SO[602]	5938	347.5
480	SO[601]	5918	227.5
481	SO[600]	5898	347.5
482	SO[599]	5878	227.5

Pad	Name	X	Y
483	SO[598]	5858	347.5
484	SO[597]	5838	227.5
485	SO[596]	5818	347.5
486	SO[595]	5798	227.5
487	SO[594]	5778	347.5
488	SO[593]	5758	227.5
489	SO[592]	5738	347.5
490	SO[591]	5718	227.5
491	SO[590]	5698	347.5
492	SO[589]	5678	227.5
493	SO[588]	5658	347.5
494	SO[587]	5638	227.5
495	SO[586]	5618	347.5
496	SO[585]	5598	227.5
497	SO[584]	5578	347.5
498	SO[583]	5558	227.5
499	SO[582]	5538	347.5
500	SO[581]	5518	227.5
501	SO[580]	5498	347.5
502	SO[579]	5478	227.5
503	SO[578]	5458	347.5
504	SO[577]	5438	227.5
505	SO[576]	5418	347.5
506	SO[575]	5398	227.5
507	SO[574]	5378	347.5
508	SO[573]	5358	227.5
509	SO[572]	5338	347.5
510	SO[571]	5318	227.5
511	SO[570]	5298	347.5
512	SO[569]	5278	227.5
513	SO[568]	5258	347.5
514	SO[567]	5238	227.5
515	SO[566]	5218	347.5
516	SO[565]	5198	227.5
517	SO[564]	5178	347.5
518	SO[563]	5158	227.5
519	SO[562]	5138	347.5
520	SO[561]	5118	227.5
521	SO[560]	5098	347.5
522	SO[559]	5078	227.5
523	SO[558]	5058	347.5
524	SO[557]	5038	227.5
525	SO[556]	5018	347.5
526	SO[555]	4998	227.5

Pad	Name	X	Y
527	SO[554]	4978	347.5
528	SO[553]	4958	227.5
529	SO[552]	4938	347.5
530	SO[551]	4918	227.5
531	SO[550]	4898	347.5
532	SO[549]	4878	227.5
533	SO[548]	4858	347.5
534	SO[547]	4838	227.5
535	SO[546]	4818	347.5
536	SO[545]	4798	227.5
537	SO[544]	4778	347.5
538	SO[543]	4758	227.5
539	SO[542]	4738	347.5
540	SO[541]	4718	227.5
541	SO[540]	4698	347.5
542	SO[539]	4678	227.5
543	SO[538]	4658	347.5
544	SO[537]	4638	227.5
545	SO[536]	4618	347.5
546	SO[535]	4598	227.5
547	SO[534]	4578	347.5
548	SO[533]	4558	227.5
549	SO[532]	4538	347.5
550	SO[531]	4518	227.5
551	SO[530]	4498	347.5
552	SO[529]	4478	227.5
553	SO[528]	4458	347.5
554	SO[527]	4438	227.5
555	SO[526]	4418	347.5
556	SO[525]	4398	227.5
557	SO[524]	4378	347.5
558	SO[523]	4358	227.5
559	SO[522]	4338	347.5
560	SO[521]	4318	227.5
561	SO[520]	4298	347.5
562	SO[519]	4278	227.5
563	SO[518]	4258	347.5
564	SO[517]	4238	227.5
565	SO[516]	4218	347.5
566	SO[515]	4198	227.5
567	SO[514]	4178	347.5
568	SO[513]	4158	227.5
569	SO[512]	4138	347.5
570	SO[511]	4118	227.5

Pad	Name	X	Y
571	SO[510]	4098	347.5
572	SO[509]	4078	227.5
573	SO[508]	4058	347.5
574	SO[507]	4038	227.5
575	SO[506]	4018	347.5
576	SO[505]	3998	227.5
577	SO[504]	3978	347.5
578	SO[503]	3958	227.5
579	SO[502]	3938	347.5
580	SO[501]	3918	227.5
581	SO[500]	3898	347.5
582	SO[499]	3878	227.5
583	SO[498]	3858	347.5
584	SO[497]	3838	227.5
585	SO[496]	3818	347.5
586	SO[495]	3798	227.5
587	SO[494]	3778	347.5
588	SO[493]	3758	227.5
589	SO[492]	3738	347.5
590	SO[491]	3718	227.5
591	SO[490]	3698	347.5
592	SO[489]	3678	227.5
593	SO[488]	3658	347.5
594	SO[487]	3638	227.5
595	SO[486]	3618	347.5
596	SO[485]	3598	227.5
597	SO[484]	3578	347.5
598	SO[483]	3558	227.5
599	SO[482]	3538	347.5
600	SO[481]	3518	227.5
601	SO[480]	3310	347.495
602	SO[479]	3290	227.5
603	SO[478]	3270	347.495
604	SO[477]	3250	227.5
605	SO[476]	3230	347.495
606	SO[475]	3210	227.5
607	SO[474]	3190	347.495
608	SO[473]	3170	227.5
609	SO[472]	3150	347.495
610	SO[471]	3130	227.5
611	SO[470]	3110	347.495
612	SO[469]	3090	227.5
613	SO[468]	3070	347.495
614	SO[467]	3050	227.5

Pad	Name	X	Y
615	SO[466]	3030	347.495
616	SO[465]	3010	227.5
617	SO[464]	2990	347.495
618	SO[463]	2970	227.5
619	SO[462]	2950	347.495
620	SO[461]	2930	227.5
621	SO[460]	2910	347.495
622	SO[459]	2890	227.5
623	SO[458]	2870	347.495
624	SO[457]	2850	227.5
625	SO[456]	2830	347.495
626	SO[455]	2810	227.5
627	SO[454]	2790	347.495
628	SO[453]	2770	227.5
629	SO[452]	2750	347.495
630	SO[451]	2730	227.5
631	SO[450]	2710	347.495
632	SO[449]	2690	227.5
633	SO[448]	2670	347.495
634	SO[447]	2650	227.5
635	SO[446]	2630	347.495
636	SO[445]	2610	227.5
637	SO[444]	2590	347.495
638	SO[443]	2570	227.5
639	SO[442]	2550	347.495
640	SO[441]	2530	227.5
641	SO[440]	2510	347.495
642	SO[439]	2490	227.5
643	SO[438]	2470	347.495
644	SO[437]	2450	227.5
645	SO[436]	2430	347.495
646	SO[435]	2410	227.5
647	SO[434]	2390	347.495
648	SO[433]	2370	227.5
649	SO[432]	2350	347.495
650	SO[431]	2330	227.5
651	SO[430]	2310	347.495
652	SO[429]	2290	227.5
653	SO[428]	2270	347.495
654	SO[427]	2250	227.5
655	SO[426]	2230	347.495
656	SO[425]	2210	227.5
657	SO[424]	2190	347.495
658	SO[423]	2170	227.5

Pad	Name	X	Y
659	SO[422]	2150	347.495
660	SO[421]	2130	227.5
661	SO[420]	2110	347.495
662	SO[419]	2090	227.5
663	SO[418]	2070	347.495
664	SO[417]	2050	227.5
665	SO[416]	2030	347.495
666	SO[415]	2010	227.5
667	SO[414]	1990	347.495
668	SO[413]	1970	227.5
669	SO[412]	1950	347.495
670	SO[411]	1930	227.5
671	SO[410]	1910	347.495
672	SO[409]	1890	227.5
673	SO[408]	1870	347.495
674	SO[407]	1850	227.5
675	SO[406]	1830	347.495
676	SO[405]	1810	227.5
677	SO[404]	1790	347.495
678	SO[403]	1770	227.5
679	SO[402]	1750	347.495
680	SO[401]	1730	227.5
681	SO[400]	1710	347.495
682	SO[399]	1690	227.5
683	SO[398]	1670	347.495
684	SO[397]	1650	227.5
685	SO[396]	1630	347.495
686	SO[395]	1610	227.5
687	SO[394]	1590	347.495
688	SO[393]	1570	227.5
689	SO[392]	1550	347.495
690	SO[391]	1530	227.5
691	SO[390]	1510	347.495
692	SO[389]	1490	227.5
693	SO[388]	1470	347.495
694	SO[387]	1450	227.5
695	SO[386]	1430	347.495
696	SO[385]	1410	227.5
697	SO[384]	1390	347.495
698	SO[383]	1370	227.5
699	SO[382]	1350	347.495
700	SO[381]	1330	227.5
701	SO[380]	1310	347.495
702	SO[379]	1290	227.5

Pad	Name	X	Y
703	SO[378]	1270	347.495
704	SO[377]	1250	227.5
705	SO[376]	1230	347.495
706	SO[375]	1210	227.5
707	SO[374]	1190	347.495
708	SO[373]	1170	227.5
709	SO[372]	1150	347.495
710	SO[371]	1130	227.5
711	SO[370]	1110	347.495
712	SO[369]	1090	227.5
713	SO[368]	1070	347.495
714	SO[367]	1050	227.5
715	SO[366]	1030	347.495
716	SO[365]	1010	227.5
717	SO[364]	990	347.495
718	SO[363]	970	227.5
719	SO[362]	950	347.495
720	SO[361]	930	227.5
721	SO[360]	910	347.495
722	SO[359]	890	227.5
723	SO[358]	870	347.495
724	SO[357]	850	227.5
725	SO[356]	830	347.495
726	SO[355]	810	227.5
727	SO[354]	790	347.495
728	SO[353]	770	227.5
729	SO[352]	750	347.495
730	SO[351]	730	227.5
731	SO[350]	710	347.495
732	SO[349]	690	227.5
733	SO[348]	670	347.495
734	SO[347]	650	227.5
735	SO[346]	630	347.495
736	SO[345]	610	227.5
737	SO[344]	590	347.495
738	SO[343]	570	227.5
739	SO[342]	550	347.495
740	SO[341]	530	227.5
741	SO[340]	510	347.495
742	SO[339]	490	227.5
743	SO[338]	470	347.495
744	SO[337]	450	227.5
745	SO[336]	430	347.495
746	SO[335]	410	227.5

Pad	Name	X	Y
747	SO[334]	390	347.495
748	SO[333]	370	227.5
749	SO[332]	350	347.495
750	SO[331]	330	227.5
751	SO[330]	310	347.495
752	SO[329]	290	227.5
753	SO[328]	270	347.495
754	SO[327]	250	227.5
755	SO[326]	230	347.495
756	SO[325]	210	227.5
757	SO[324]	190	347.495
758	SO[323]	170	227.5
759	SO[322]	150	347.495
760	SO[321]	130	227.5
761	SO[320]	-130	347.5
762	SO[319]	-150	227.5
763	SO[318]	-170	347.5
764	SO[317]	-190	227.5
765	SO[316]	-210	347.5
766	SO[315]	-230	227.5
767	SO[314]	-250	347.5
768	SO[313]	-270	227.5
769	SO[312]	-290	347.5
770	SO[311]	-310	227.5
771	SO[310]	-330	347.5
772	SO[309]	-350	227.5
773	SO[308]	-370	347.5
774	SO[307]	-390	227.5
775	SO[306]	-410	347.5
776	SO[305]	-430	227.5
777	SO[304]	-450	347.5
778	SO[303]	-470	227.5
779	SO[302]	-490	347.5
780	SO[301]	-510	227.5
781	SO[300]	-530	347.5
782	SO[299]	-550	227.5
783	SO[298]	-570	347.5
784	SO[297]	-590	227.5
785	SO[296]	-610	347.5
786	SO[295]	-630	227.5
787	SO[294]	-650	347.5
788	SO[293]	-670	227.5
789	SO[292]	-690	347.5
790	SO[291]	-710	227.5

Pad	Name	X	Y
791	SO[290]	-730	347.5
792	SO[289]	-750	227.5
793	SO[288]	-770	347.5
794	SO[287]	-790	227.5
795	SO[286]	-810	347.5
796	SO[285]	-830	227.5
797	SO[284]	-850	347.5
798	SO[283]	-870	227.5
799	SO[282]	-890	347.5
800	SO[281]	-910	227.5
801	SO[280]	-930	347.5
802	SO[279]	-950	227.5
803	SO[278]	-970	347.5
804	SO[277]	-990	227.5
805	SO[276]	-1010	347.5
806	SO[275]	-1030	227.5
807	SO[274]	-1050	347.5
808	SO[273]	-1070	227.5
809	SO[272]	-1090	347.5
810	SO[271]	-1110	227.5
811	SO[270]	-1130	347.5
812	SO[269]	-1150	227.5
813	SO[268]	-1170	347.5
814	SO[267]	-1190	227.5
815	SO[266]	-1210	347.5
816	SO[265]	-1230	227.5
817	SO[264]	-1250	347.5
818	SO[263]	-1270	227.5
819	SO[262]	-1290	347.5
820	SO[261]	-1310	227.5
821	SO[260]	-1330	347.5
822	SO[259]	-1350	227.5
823	SO[258]	-1370	347.5
824	SO[257]	-1390	227.5
825	SO[256]	-1410	347.5
826	SO[255]	-1430	227.5
827	SO[254]	-1450	347.5
828	SO[253]	-1470	227.5
829	SO[252]	-1490	347.5
830	SO[251]	-1510	227.5
831	SO[250]	-1530	347.5
832	SO[249]	-1550	227.5
833	SO[248]	-1570	347.5
834	SO[247]	-1590	227.5

Pad	Name	X	Y
835	SO[246]	-1610	347.5
836	SO[245]	-1630	227.5
837	SO[244]	-1650	347.5
838	SO[243]	-1670	227.5
839	SO[242]	-1690	347.5
840	SO[241]	-1710	227.5
841	SO[240]	-1730	347.5
842	SO[239]	-1750	227.5
843	SO[238]	-1770	347.5
844	SO[237]	-1790	227.5
845	SO[236]	-1810	347.5
846	SO[235]	-1830	227.5
847	SO[234]	-1850	347.5
848	SO[233]	-1870	227.5
849	SO[232]	-1890	347.5
850	SO[231]	-1910	227.5
851	SO[230]	-1930	347.5
852	SO[229]	-1950	227.5
853	SO[228]	-1970	347.5
854	SO[227]	-1990	227.5
855	SO[226]	-2010	347.5
856	SO[225]	-2030	227.5
857	SO[224]	-2050	347.5
858	SO[223]	-2070	227.5
859	SO[222]	-2090	347.5
860	SO[221]	-2110	227.5
861	SO[220]	-2130	347.5
862	SO[219]	-2150	227.5
863	SO[218]	-2170	347.5
864	SO[217]	-2190	227.5
865	SO[216]	-2210	347.5
866	SO[215]	-2230	227.5
867	SO[214]	-2250	347.5
868	SO[213]	-2270	227.5
869	SO[212]	-2290	347.5
870	SO[211]	-2310	227.5
871	SO[210]	-2330	347.5
872	SO[209]	-2350	227.5
873	SO[208]	-2370	347.5
874	SO[207]	-2390	227.5
875	SO[206]	-2410	347.5
876	SO[205]	-2430	227.5
877	SO[204]	-2450	347.5
878	SO[203]	-2470	227.5

Pad	Name	X	Y
879	SO[202]	-2490	347.5
880	SO[201]	-2510	227.5
881	SO[200]	-2530	347.5
882	SO[199]	-2550	227.5
883	SO[198]	-2570	347.5
884	SO[197]	-2590	227.5
885	SO[196]	-2610	347.5
886	SO[195]	-2630	227.5
887	SO[194]	-2650	347.5
888	SO[193]	-2670	227.5
889	SO[192]	-2690	347.5
890	SO[191]	-2710	227.5
891	SO[190]	-2730	347.5
892	SO[189]	-2750	227.5
893	SO[188]	-2770	347.5
894	SO[187]	-2790	227.5
895	SO[186]	-2810	347.5
896	SO[185]	-2830	227.5
897	SO[184]	-2850	347.5
898	SO[183]	-2870	227.5
899	SO[182]	-2890	347.5
900	SO[181]	-2910	227.5
901	SO[180]	-2930	347.5
902	SO[179]	-2950	227.5
903	SO[178]	-2970	347.5
904	SO[177]	-2990	227.5
905	SO[176]	-3010	347.5
906	SO[175]	-3030	227.5
907	SO[174]	-3050	347.5
908	SO[173]	-3070	227.5
909	SO[172]	-3090	347.5
910	SO[171]	-3110	227.5
911	SO[170]	-3130	347.5
912	SO[169]	-3150	227.5
913	SO[168]	-3170	347.5
914	SO[167]	-3190	227.5
915	SO[166]	-3210	347.5
916	SO[165]	-3230	227.5
917	SO[164]	-3250	347.5
918	SO[163]	-3270	227.5
919	SO[162]	-3290	347.5
920	SO[161]	-3310	227.5
921	SO[160]	-3518	347.5
922	SO[159]	-3538	227.5

Pad	Name	X	Y
923	SO[158]	-3558	347.5
924	SO[157]	-3578	227.5
925	SO[156]	-3598	347.5
926	SO[155]	-3618	227.5
927	SO[154]	-3638	347.5
928	SO[153]	-3658	227.5
929	SO[152]	-3678	347.5
930	SO[151]	-3698	227.5
931	SO[150]	-3718	347.5
932	SO[149]	-3738	227.5
933	SO[148]	-3758	347.5
934	SO[147]	-3778	227.5
935	SO[146]	-3798	347.5
936	SO[145]	-3818	227.5
937	SO[144]	-3838	347.5
938	SO[143]	-3858	227.5
939	SO[142]	-3878	347.5
940	SO[141]	-3898	227.5
941	SO[140]	-3918	347.5
942	SO[139]	-3938	227.5
943	SO[138]	-3958	347.5
944	SO[137]	-3978	227.5
945	SO[136]	-3998	347.5
946	SO[135]	-4018	227.5
947	SO[134]	-4038	347.5
948	SO[133]	-4058	227.5
949	SO[132]	-4078	347.5
950	SO[131]	-4098	227.5
951	SO[130]	-4118	347.5
952	SO[129]	-4138	227.5
953	SO[128]	-4158	347.5
954	SO[127]	-4178	227.5
955	SO[126]	-4198	347.5
956	SO[125]	-4218	227.5
957	SO[124]	-4238	347.5
958	SO[123]	-4258	227.5
959	SO[122]	-4278	347.5
960	SO[121]	-4298	227.5
961	SO[120]	-4318	347.5
962	SO[119]	-4338	227.5
963	SO[118]	-4358	347.5
964	SO[117]	-4378	227.5
965	SO[116]	-4398	347.5
966	SO[115]	-4418	227.5

Pad	Name	X	Y
967	SO[114]	-4438	347.5
968	SO[113]	-4458	227.5
969	SO[112]	-4478	347.5
970	SO[111]	-4498	227.5
971	SO[110]	-4518	347.5
972	SO[109]	-4538	227.5
973	SO[108]	-4558	347.5
974	SO[107]	-4578	227.5
975	SO[106]	-4598	347.5
976	SO[105]	-4618	227.5
977	SO[104]	-4638	347.5
978	SO[103]	-4658	227.5
979	SO[102]	-4678	347.5
980	SO[101]	-4698	227.5
981	SO[100]	-4718	347.5
982	SO[99]	-4738	227.5
983	SO[98]	-4758	347.5
984	SO[97]	-4778	227.5
985	SO[96]	-4798	347.5
986	SO[95]	-4818	227.5
987	SO[94]	-4838	347.5
988	SO[93]	-4858	227.5
989	SO[92]	-4878	347.5
990	SO[91]	-4898	227.5
991	SO[90]	-4918	347.5
992	SO[89]	-4938	227.5
993	SO[88]	-4958	347.5
994	SO[87]	-4978	227.5
995	SO[86]	-4998	347.5
996	SO[85]	-5018	227.5
997	SO[84]	-5038	347.5
998	SO[83]	-5058	227.5
999	SO[82]	-5078	347.5
1000	SO[81]	-5098	227.5
1001	SO[80]	-5118	347.5
1002	SO[79]	-5138	227.5
1003	SO[78]	-5158	347.5
1004	SO[77]	-5178	227.5
1005	SO[76]	-5198	347.5
1006	SO[75]	-5218	227.5
1007	SO[74]	-5238	347.5
1008	SO[73]	-5258	227.5
1009	SO[72]	-5278	347.5
1010	SO[71]	-5298	227.5

Pad	Name	X	Y
1011	SO[70]	-5318	347.5
1012	SO[69]	-5338	227.5
1013	SO[68]	-5358	347.5
1014	SO[67]	-5378	227.5
1015	SO[66]	-5398	347.5
1016	SO[65]	-5418	227.5
1017	SO[64]	-5438	347.5
1018	SO[63]	-5458	227.5
1019	SO[62]	-5478	347.5
1020	SO[61]	-5498	227.5
1021	SO[60]	-5518	347.5
1022	SO[59]	-5538	227.5
1023	SO[58]	-5558	347.5
1024	SO[57]	-5578	227.5
1025	SO[56]	-5598	347.5
1026	SO[55]	-5618	227.5
1027	SO[54]	-5638	347.5
1028	SO[53]	-5658	227.5
1029	SO[52]	-5678	347.5
1030	SO[51]	-5698	227.5
1031	SO[50]	-5718	347.5
1032	SO[49]	-5738	227.5
1033	SO[48]	-5758	347.5
1034	SO[47]	-5778	227.5
1035	SO[46]	-5798	347.5
1036	SO[45]	-5818	227.5
1037	SO[44]	-5838	347.5
1038	SO[43]	-5858	227.5
1039	SO[42]	-5878	347.5
1040	SO[41]	-5898	227.5
1041	SO[40]	-5918	347.5
1042	SO[39]	-5938	227.5
1043	SO[38]	-5958	347.5
1044	SO[37]	-5978	227.5
1045	SO[36]	-5998	347.5
1046	SO[35]	-6018	227.5
1047	SO[34]	-6038	347.5
1048	SO[33]	-6058	227.5
1049	SO[32]	-6078	347.5
1050	SO[31]	-6098	227.5
1051	SO[30]	-6118	347.5
1052	SO[29]	-6138	227.5
1053	SO[28]	-6158	347.5
1054	SO[27]	-6178	227.5

Pad	Name	X	Y
1055	SO[26]	-6198	347.5
1056	SO[25]	-6218	227.5
1057	SO[24]	-6238	347.5
1058	SO[23]	-6258	227.5
1059	SO[22]	-6278	347.5
1060	SO[21]	-6298	227.5
1061	SO[20]	-6318	347.5
1062	SO[19]	-6338	227.5
1063	SO[18]	-6358	347.5
1064	SO[17]	-6378	227.5
1065	SO[16]	-6398	347.5
1066	SO[15]	-6418	227.5
1067	SO[14]	-6438	347.5
1068	SO[13]	-6458	227.5
1069	SO[12]	-6478	347.5
1070	SO[11]	-6498	227.5
1071	SO[10]	-6518	347.5
1072	SO[9]	-6538	227.5
1073	SO[8]	-6558	347.5
1074	SO[7]	-6578	227.5
1075	SO[6]	-6598	347.5
1076	SO[5]	-6618	227.5
1077	SO[4]	-6638	347.5
1078	SO[3]	-6658	227.5
1079	SO[2]	-6678	347.5
1080	SO[1]	-6698	227.5
1081	GD[319]	-6950	347.5
1082	GD[317]	-6970	227.5
1083	GD[315]	-6990	347.5
1084	GD[313]	-7010	227.5
1085	GD[311]	-7030	347.5
1086	GD[309]	-7050	227.5
1087	GD[307]	-7070	347.5
1088	GD[305]	-7090	227.5
1089	GD[303]	-7110	347.5
1090	GD[301]	-7130	227.5
1091	GD[299]	-7150	347.5
1092	GD[297]	-7170	227.5
1093	GD[295]	-7190	347.5
1094	GD[293]	-7210	227.5
1095	GD[291]	-7230	347.5
1096	GD[289]	-7250	227.5
1097	GD[287]	-7270	347.5
1098	GD[285]	-7290	227.5

Pad	Name	X	Y
1099	GD[283]	-7310	347.5
1100	GD[281]	-7330	227.5
1101	GD[279]	-7350	347.5
1102	GD[277]	-7370	227.5
1103	GD[275]	-7390	347.5
1104	GD[273]	-7410	227.5
1105	GD[271]	-7430	347.5
1106	GD[269]	-7450	227.5
1107	GD[267]	-7470	347.5
1108	GD[265]	-7490	227.5
1109	GD[263]	-7510	347.5
1110	GD[261]	-7530	227.5
1111	GD[259]	-7550	347.5
1112	GD[257]	-7570	227.5
1113	GD[255]	-7590	347.5
1114	GD[253]	-7610	227.5
1115	GD[251]	-7630	347.5
1116	GD[249]	-7650	227.5
1117	GD[247]	-7670	347.5
1118	GD[245]	-7690	227.5
1119	GD[243]	-7710	347.5
1120	GD[241]	-7730	227.5
1121	GD[239]	-7750	347.5
1122	GD[237]	-7770	227.5
1123	GD[235]	-7790	347.5
1124	GD[233]	-7810	227.5
1125	GD[231]	-7830	347.5
1126	GD[229]	-7850	227.5
1127	GD[227]	-7870	347.5
1128	GD[225]	-7890	227.5
1129	GD[223]	-7910	347.5
1130	GD[221]	-7930	227.5
1131	GD[219]	-7950	347.5
1132	GD[217]	-7970	227.5
1133	GD[215]	-7990	347.5
1134	GD[213]	-8010	227.5
1135	GD[211]	-8030	347.5
1136	GD[209]	-8050	227.5
1137	GD[207]	-8070	347.5
1138	GD[205]	-8090	227.5
1139	GD[203]	-8110	347.5
1140	GD[201]	-8130	227.5
1141	GD[199]	-8150	347.5
1142	GD[197]	-8170	227.5

Pad	Name	X	Y
1143	GD[195]	-8190	347.5
1144	GD[193]	-8210	227.5
1145	GD[191]	-8230	347.5
1146	GD[189]	-8250	227.5
1147	GD[187]	-8270	347.5
1148	GD[185]	-8290	227.5
1149	GD[183]	-8310	347.5
1150	GD[181]	-8330	227.5
1151	GD[179]	-8350	347.5
1152	GD[177]	-8370	227.5
1153	GD[175]	-8390	347.5
1154	GD[173]	-8410	227.5
1155	GD[171]	-8430	347.5
1156	GD[169]	-8450	227.5
1157	GD[167]	-8470	347.5
1158	GD[165]	-8490	227.5
1159	GD[163]	-8510	347.5
1160	GD[161]	-8530	227.5
1161	GD[159]	-8550	347.5
1162	GD[157]	-8570	227.5
1163	GD[155]	-8590	347.5
1164	GD[153]	-8610	227.5
1165	GD[151]	-8630	347.5
1166	GD[149]	-8650	227.5
1167	GD[147]	-8670	347.5
1168	GD[145]	-8690	227.5
1169	GD[143]	-8710	347.5
1170	GD[141]	-8730	227.5
1171	GD[139]	-8750	347.5
1172	GD[137]	-8770	227.5
1173	GD[135]	-8790	347.5
1174	GD[133]	-8810	227.5
1175	GD[131]	-8830	347.5
1176	GD[129]	-8850	227.5
1177	GD[127]	-8870	347.5
1178	GD[125]	-8890	227.5
1179	GD[123]	-8910	347.5
1180	GD[121]	-8930	227.5
1181	GD[119]	-8950	347.5
1182	GD[117]	-8970	227.5
1183	GD[115]	-8990	347.5
1184	GD[113]	-9010	227.5
1185	GD[111]	-9030	347.5
1186	GD[109]	-9050	227.5

Pad	Name	X	Y
1187	GD[107]	-9070	347.5
1188	GD[105]	-9090	227.5
1189	GD[103]	-9110	347.5
1190	GD[101]	-9130	227.5
1191	GD[99]	-9150	347.5
1192	GD[97]	-9170	227.5
1193	GD[95]	-9190	347.5
1194	GD[93]	-9210	227.5
1195	GD[91]	-9230	347.5
1196	GD[89]	-9250	227.5
1197	GD[87]	-9270	347.5
1198	GD[85]	-9290	227.5
1199	GD[83]	-9310	347.5
1200	GD[81]	-9330	227.5
1201	GD[79]	-9350	347.5
1202	GD[77]	-9370	227.5
1203	GD[75]	-9390	347.5
1204	GD[73]	-9410	227.5
1205	GD[71]	-9430	347.5
1206	GD[69]	-9450	227.5
1207	GD[67]	-9470	347.5
1208	GD[65]	-9490	227.5
1209	GD[63]	-9510	347.5
1210	GD[61]	-9530	227.5
1211	GD[59]	-9550	347.5
1212	GD[57]	-9570	227.5
1213	GD[55]	-9590	347.5
1214	GD[53]	-9610	227.5
1215	GD[51]	-9630	347.5
1216	GD[49]	-9650	227.5
1217	GD[47]	-9670	347.5
1218	GD[45]	-9690	227.5
1219	GD[43]	-9710	347.5
1220	GD[41]	-9730	227.5
1221	GD[39]	-9750	347.5
1222	GD[37]	-9770	227.5
1223	GD[35]	-9790	347.5
1224	GD[33]	-9810	227.5
1225	GD[31]	-9830	347.5
1226	GD[29]	-9850	227.5
1227	GD[27]	-9870	347.5
1228	GD[25]	-9890	227.5
1229	GD[23]	-9910	347.5
1230	GD[21]	-9930	227.5

Pad	Name	X	Y
1231	GD[19]	-9950	347.5
1232	GD[17]	-9970	227.5
1233	GD[15]	-9990	347.5
1234	GD[13]	-10010	227.5
1235	GD[11]	-10030	347.5

Pad	Name	X	Y
1236	GD[9]	-10050	227.5
1237	GD[7]	-10070	347.5
1238	GD[5]	-10090	227.5
1239	GD[3]	-10110	347.5
1240	GD[1]	-10130	227.5

4. BLOCK DIAGRAM

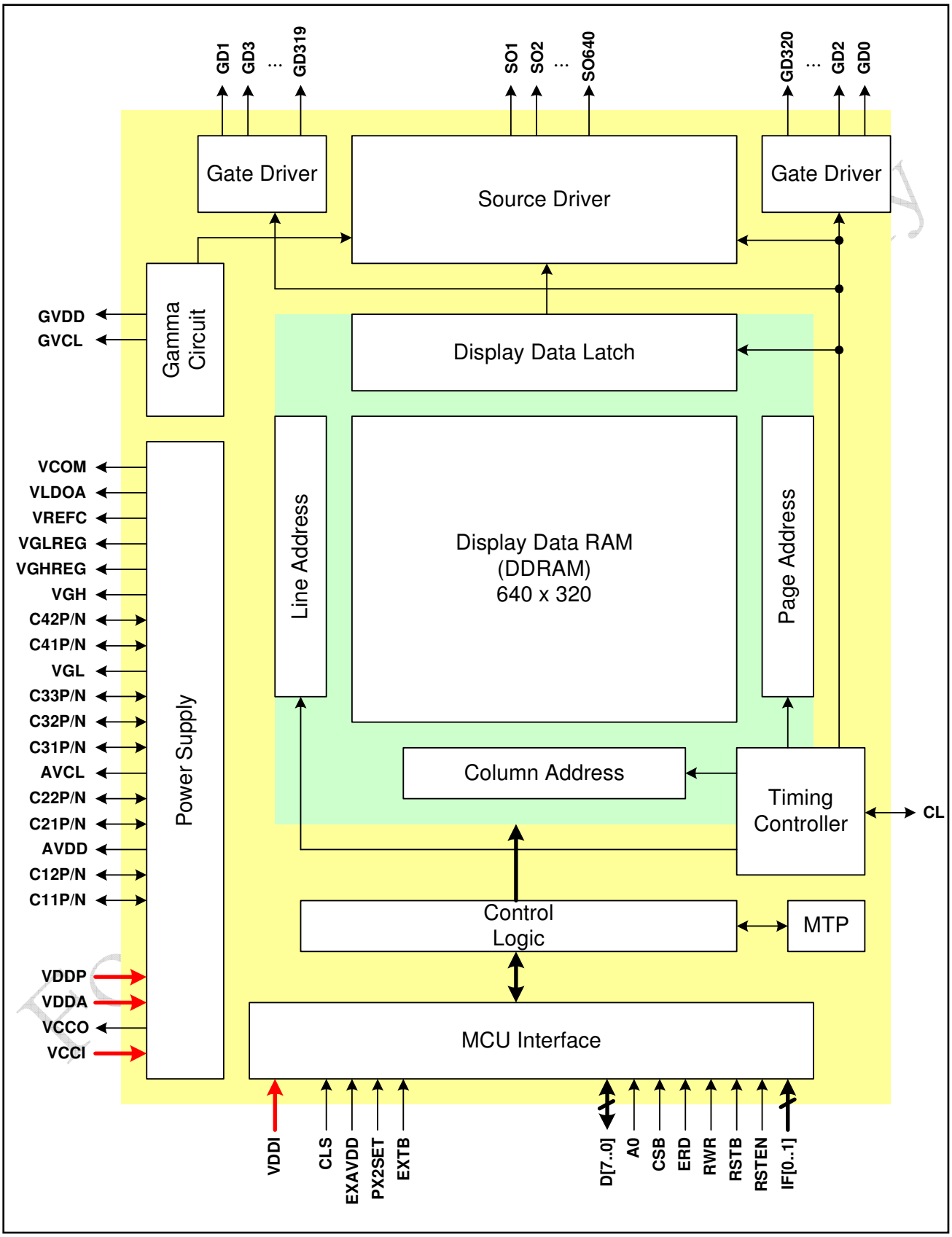


Fig 1. Block Diagram

5. PIN DESCRIPTION

5.1 Microprocessor Interface Pins

<table>
<tr><th>Pin Name</th><th>Type</th><th>Description</th></tr>
<tr><td>IF[1:0]</td><td>I</td><td>IF1 selects the interface mode (Serial or Parallel), and IF0 selects the microprocessor type in parallel interface mode (8080-series or 6800-series).
<table>
<tr><th>IF1</th><th>IF0</th><th>Selected Interface</th></tr>
<tr><td>“L”</td><td>“L”</td><td>8-bit 8080 parallel interface</td></tr>
<tr><td>“L”</td><td>“H”</td><td>8-bit 6800 parallel interface</td></tr>
<tr><td>“H”</td><td>“L”</td><td>3-line serial interface</td></tr>
<tr><td>“H”</td><td>“H”</td><td>4-line serial interface</td></tr>
</table></td></tr>
<tr><td>RSTB</td><td>I</td><td>Reset input pin. Active when it is low. This pin is effective when RSTEN pin is High.
Initialization is executed when this pin is set to Low. SWRESET command must be required after initialization.</td></tr>
<tr><td>RSTEN</td><td>I</td><td>Distinction pin of the RSTB pin signal.
RESEN=Hi: RSTB pin is effective.
RESEN=Low: RSTB pin is not effective.</td></tr>
<tr><td>CSB</td><td>I</td><td>Chip select input pin.
Interface access is enabled when CSB is “L” in parallel, SPI interface.
When CSB is non-active (CSB=“H”), D[7:0] pins are high impedance.</td></tr>
<tr><td>A0</td><td>I</td><td>Data/Command identification pin.
A0=Hi: Display data or parameter
A0=Low: Command
When using 3-line serial interface:
A0=Hi</td></tr>
<tr><td rowspan="2">D[7:0]</td><td>I/O</td><td>When using 8-bit parallel interface: (6800 or 8080 mode)
8-bit bi-directional data bus. Connect to the data bus of 8-bit microprocessor.
When chip select pins are not active (CSB=“H), D[7:0] pins are high impedance.</td></tr>
<tr><td>I/O</td><td>When using serial interface: 3-line or 4-line
D7: Serial input clock (SCL).
D0: Serial data (SDA).
D[6:1]: fix to “H” by VDDI.
When chip select pin (CSB) is not active, D[7:0] are high impedance.</td></tr>
<tr><td>ERD</td><td>I</td><td>Read/Write execution control pin. When IF1 is “L”,
<table>
<tr><th>IF0</th><th>MPU Type</th><th>ERD</th><th>Description</th></tr>
<tr><td>H</td><td>6800 series</td><td>E</td><td>Read/Write control input pin.
R/W=”H“: When E is “H”, D[7:0] are in output mode.
R/W=”L“: Signals on D[7:0] are latched at the falling edge of E signal.</td></tr>
<tr><td>L</td><td>8080 series</td><td>/RD</td><td>Read enable input pin.
When /RD is “L”, D[7:0] are in output mode.</td></tr>
</table>
ERD is not used in serial interface and should fix to “H” by VDDI.</td></tr>
</table>

<table>
<tr><th>Pin Name</th><th>Type</th><th>Description</th></tr>
<tr><td>RWR</td><td>I</td><td>Read/Write execution control pin. When IF1 is “L”,
<table>
<tr><th>IF0</th><th>MPU Type</th><th>RWR</th><th>Description</th></tr>
<tr><td>H</td><td>6800 series</td><td>R/W</td><td>Read/Write control input pin.
R/W=“H”: read.
R/W=“L”: write.</td></tr>
<tr><td>L</td><td>8080 series</td><td>/WR</td><td>Write enable input pin.
Signals on D[7:0] will be latched at the rising edge of /WR signal.</td></tr>
</table>
RWR is not used in serial interface and should fix to “H” by VDDI.</td></tr>
<tr><td>EXAVDD</td><td>I</td><td>Select pin of AVDD for external power supply.
<table>
<tr><th>EXAVDD</th><th>AVDD power supply</th><th>Description</th></tr>
<tr><td>H</td><td>External</td><td>AVDD is connected to external power supply.</td></tr>
<tr><td>L</td><td>Internal</td><td>AVDD is generated by internal power circuit.</td></tr>
</table></td></tr>
<tr><td>PX2SET</td><td>I</td><td>Select pin of AVDD pump multiplier.
<table>
<tr><th>PX2SET</th><th>AVDD pump multiplier.</th><th>Description</th></tr>
<tr><td>H</td><td>x 2</td><td>VDDA = 5.0V</td></tr>
<tr><td>L</td><td>x 3</td><td>VDDA = 3.3V</td></tr>
</table></td></tr>
<tr><td>PWM</td><td>O</td><td>PWM output pin</td></tr>
<tr><td>VSYNCO</td><td>O</td><td>Vertical synchronization signal output pin.</td></tr>
<tr><td>EXTB</td><td>O</td><td>For MTP enable pin. (Internal pull-up)</td></tr>
</table>

Note:

1. After VDDI is turned ON, any MPU interface pins cannot be left floating.

5.2 LCD Driver Related Pins

Pin Name	Type	Description
SO[640:1]	**O**	TFT-LCD Source Driver Outputs.
GD[320:1]	**O**	TFT-LCD Gate Driver Outputs.

5.3 Clock System Pins

Pin Name	Type	Description
CLS	**I**	Clock source selection pin. CLS=“H”: enable internal clock. CLS=“L”: disable internal clock and use external clock.
CL	**I/O**	If CLS=“H”, internal clock output. If CLS=“L”, external clock input.

5.4 Power Supply Pins

Pin Name	Type	Description
VDDA	**Power**	Power supply for analog and booster circuit.
VDDP	**Power**	Power supply for analog power system.
VDDI	**Power**	Power supply for IO system.
AGND	**Power**	System ground for analog and booster circuit.
PGND	**Power**	System ground for analog power system.
DGND	**Power**	System ground for IO and digital circuit.
VPP	**Power**	Power supply for MTP burning.

5.5 LCD Power System Pins

Pin Name	Type	Description
VLDOA	**O**	Monitor pin for internal regulator VLDOA
VREFC	**O**	Monitor pin for internal regulator VREFC
VGLREG	**O**	Monitor pin for internal regulator VGLREG
VGHREG	**O**	Monitor pin for internal regulator VGHREG
AVDD	**Power**	Power pin for analog circuits. Connect to a capacitor for stabilization.
AVDDO	**O**	Power pin for analog circuits. Connect to a capacitor for stabilization.
AVCL	**Power**	Power supply pin for generating GVCL. Connect to a capacitor for stabilization.
AVCLO	**O**	Power supply pin for generating GVCL. Connect to a capacitor for stabilization.
VGL	**O**	Power supply pin for gate driver. Connect to a capacitor for stabilization.
VGH	**O**	Power supply pin for gate driver. Connect to a capacitor for stabilization.
GVDD	**O**	Power output of positive grayscale voltage generator. When internal GVDD generator is not used, connect an external power supply (AVDD – 0.5V) to this pin.
GVCL	**O**	Power output of negative grayscale voltage generator. When internal GVCL generator is not used, connect an external power supply (AVCL+0.5V) to this pin.
VCOM	**Power**	Power supply for the TFT-LCD common electrode.
VCCO	**O**	Digital reference power voltage output. Connect to a capacitor for stabilization.
VCCI	**Power**	Digital reference power voltage input
C11P C12P	**Power**	Flying Capacitor for generating AVDD Output Connecting pins on the positive side. If 1st booster is not used, please open them.
C11N C12N	**Power**	Flying Capacitor for generating AVDD Output Connecting pins on the negative side. If 1st booster is not used, please open them.
C21P C22P	**Power**	Flying Capacitor for generating AVCL Output Connecting pins on the positive side. If 2nd booster is not used, please open them.
C21N C22N	**Power**	Flying Capacitor for generating AVCL Output Connecting pins on the negative side. If 2nd booster is not used, please open them.
C31P C32P C33P	**Power**	Flying Capacitor for generating VGL Output Connecting pins on the positive side.
C31N C32N C33N	**Power**	Flying Capacitor for generating VGL Output Connecting pins on the negative side.
C41P	**Power**	Flying Capacitor for generating VGH Output
C41N	**Power**	Flying Capacitor for generating VGH Output

5.6 Test Pins

Pin Name	Type	Description
T1~T26	**Open**	Reserved for testing only. Leave these pins open.
TFCOM[2:0]	**Open**	Reserved for testing only. Leave these pins open.
TEST1	**Open**	Reserved for testing only. Leave this pin open.
TEST2, TEST3	**GND**	Reserved for testing only. Connect to ground.
EEEN	**GND**	Reserved for testing only. Connect to ground.
EESI	**VDDI**	Reserved for testing only. Connect to VDDI.
XEECS	**Open**	Reserved for testing only. Leave this pin open.
EESCL	**Open**	Reserved for testing only. Leave this pin open.
EESO	**Open**	Reserved for testing only. Leave this pin open.
XEEWP	**Open**	Reserved for testing only. Leave this pin open.

5.7 Dummy Pins

Pin Name	Type	Description
Dummy	**Open**	Dummy pins. Leave these pins open.

5.8 Recommend Resistance

Item	Pin name	Resistance
Powers	VDDA, VDDP, VDDI, AGND, PGND, DGND	< 10 ohm
Boosters	CxxN/P, VLDOA, AVxxO	< 10 ohm
Regulators	VCOM, GVxx, VxxREG, VGx	< 10 ohm
Logics	D[7:0], CSB, RSTB, A0, RWR, ERD,IF[1:0], EXAVDD, etc.	< 50 ohm
MTP	VPP	< 20 ohm

6. FUNCTION DESCRIPTION

6.1 Microprocessor Interface

6.1.1 Chip Selection

CSB pin is used for chip selection. ST7511U can communicate with an MCU when CSB is “L”. If CSB is “H”, the inputs of A0, ERD and RWR with any combination will be ignored and D[7:0] are high impedance. In 3-Line and 4-Line serial interfaces, the internal shift register and serial counter are reset when CSB is “H”.

6.1.2 Interface Selection

The interface selection is controlled by IF[1:0] pins. Please refer to the table below:

Table 1

Setting		MCU Type	Interface Pin Function				
IF1	IF0		CSB	A0	RWR	ERD	D[7:0]
L	L	Parallel 8080 series MCU	CSB	A0	/WR	/RD	D[7:0]
L	H	Parallel 6800 series MCU			R/W	E	
H	H	Serial 4-Line series MCU			-	-	D7=SCL, D0=SDA, D[6:1] are not used
H	L	Serial 3-Line series MCU		-	-	-	

Note: The un-used pins are marked as “-” and should be connected to “H” by VDDI.

6.1.3 Parallel Interface

When parallel interface is selected, the interface transmission type will be determined by the combination of the control signals. Please refer to the table below:

Table 2

8080 series MCU		6800 series MCU		A0	CSB	Interface Transmission Type
/WR	/RD	R/W	E			
↑	H	L	↓	L	L	Write Command
↑	H	L	↓	H		Write Display Data or Parameter
H	↓	H	↑	H		Read Display Data or Parameter Start
H	↑	H	↓	H		Read Display Data or Parameter Stop

Note:

1. Reading Display Data or Parameter is specified by the instruction before the read operation.
2. When reading Display Data (DDRAM contents), the first output byte is dummy byte.
3. When reading Parameter (temperature, status and PROM data), the first output byte is valid.

6.1.4 Serial Interface

In serial interface (4-Line or 3-Line), IC is active and the control signals (SDI, SDO, SCL and A0 for 4-Line) are enabled when CSB is “L”. When CSB is “H”, the MCU interface is not active and the internal shift-register and serial-counter are reset.

If CSB is set to “H” before all data bits (8 bits) are entered completely, the data concerned is invalidated. Before entering succeeding sets of data, you must input the data concerned again. In order to avoid transfer error due to incoming noise when writing command or data, it is recommended to set CSB at “H” on byte basis, so that the serial-to-parallel counter and the shift-register can be cleared after each byte of transmission.

6.1.4a 4-Line Serial Interface

In 4-Line serial interface, A0 signal is latched at the 8th rising edge of the SCL signal (refer to Fig 1).

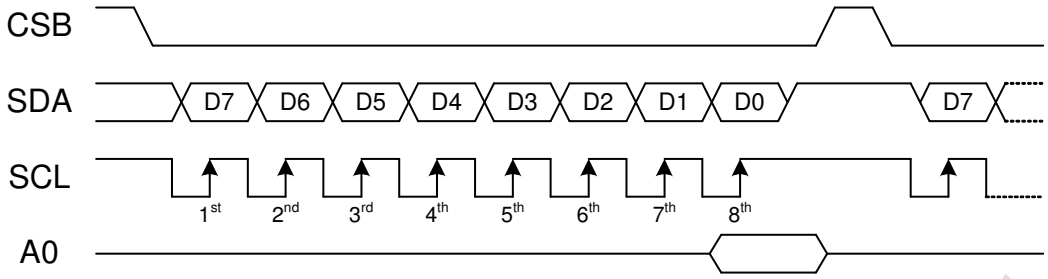


Fig 1 Write-Operation of 4-Line Serial Interface

After entering the Read Status instruction to read IC status, the information is shifted out as shown below. CSB signal must be kept at “L” during this period. All read out data will be 8 bits.

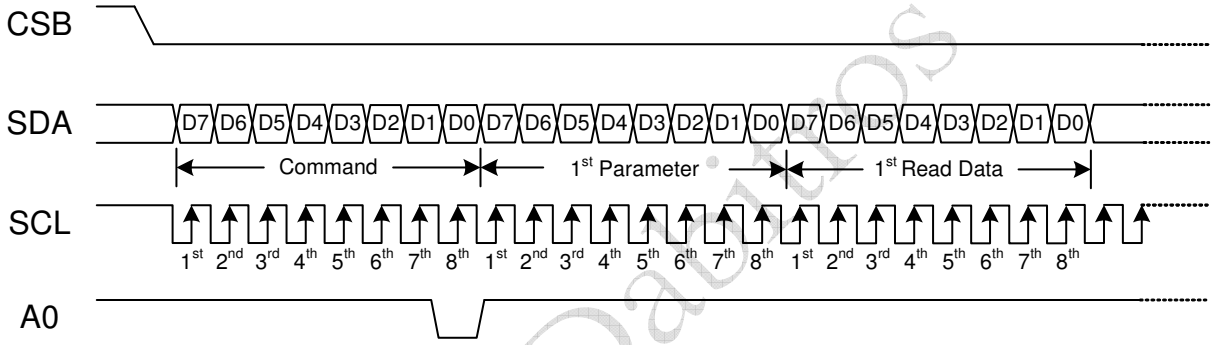


Fig 2 Read-Operation of 4-Line Serial Interface

6.1.4b 3-Line Serial Interface

In 3-Line interface, A0 signal is not available. The 1st output bit defines command byte or parameter byte (refer to Fig 3).

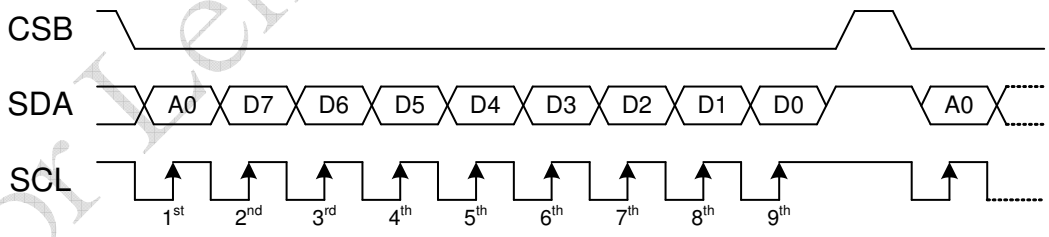


Fig 3 Write-Operation of 3-Line Serial Interface

After entering the Read Status instruction to read IC status, the information is shifted out as shown below. CSB signal must be kept at “L” during this period. All read out data will be 8 bits.

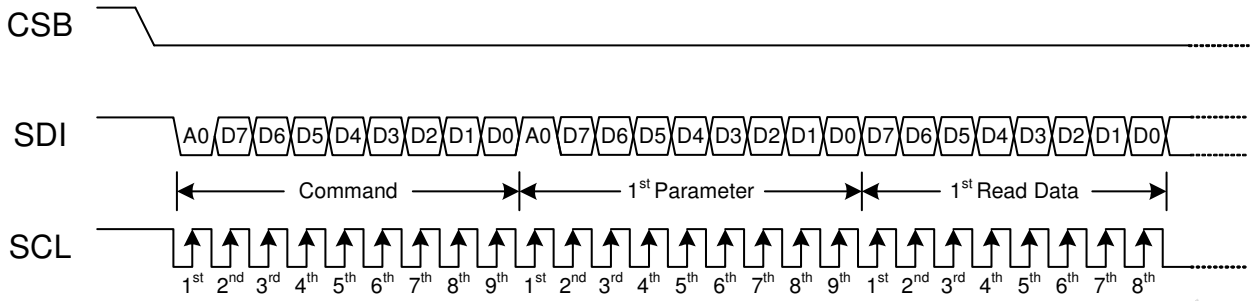


Fig 4 Read-Operation of 3-Line Serial Interface

6.1.5 Data Transfer

ST7511U uses bus latch and internal data bus for interface data transfer. When writing data from MPU to the DDRAM, data is automatically transferred from the bus latch to the DDRAM. When reading data from the on-chip DDRAM to MPU, the first read cycle reads the content in bus latch (dummy read) and the data that MPU should read will be output at the next read cycle. That means: after setting the target address, a dummy read cycle is required before the following read-operation. Therefore, the data of the specified address cannot be read at the first read of display data right after setting the address, but can be read at the second read of display data.

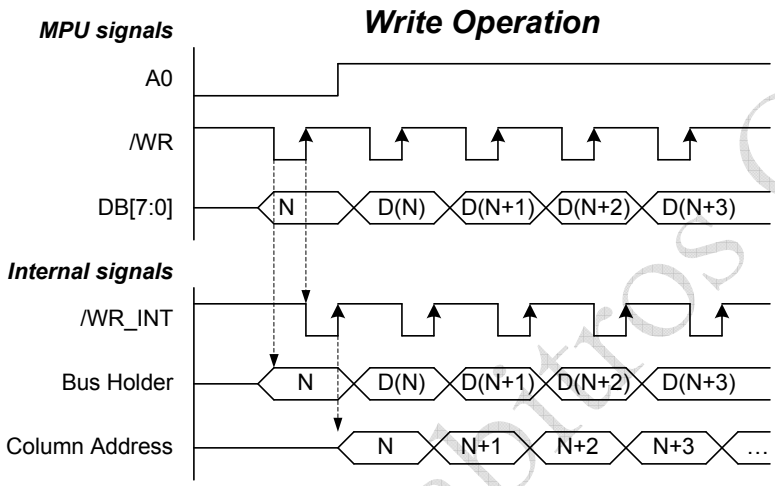


Fig 5 Data Transfer : Write

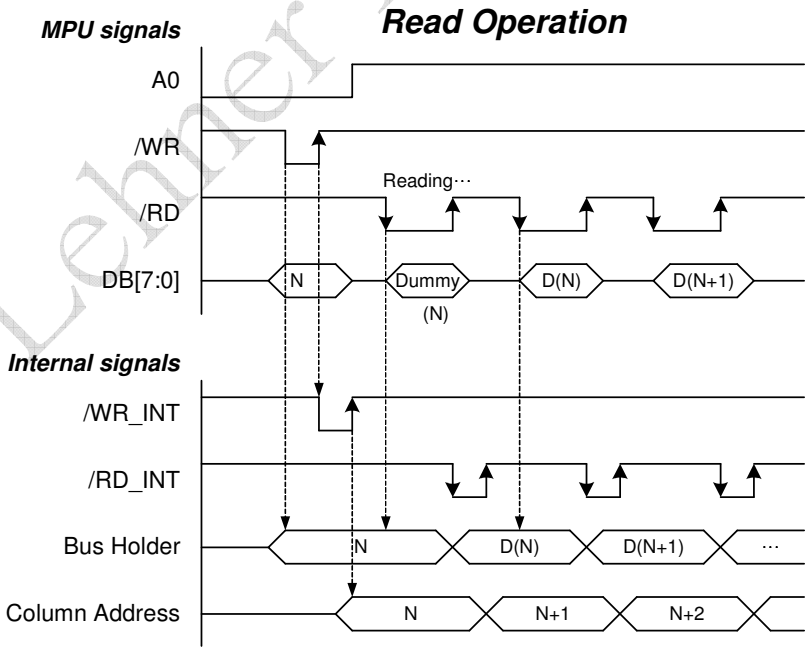


Fig 6 Data Transfer : Read

6.2 Display Data RAM (DDRAM)

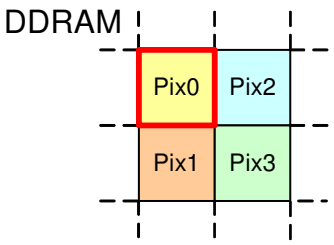
6.2.1 4bpp DDRAM Map

Page address		0	1	2	..	637	638	639	normal	**Column address**
normal	invert	639	638	637	..	2	1	0	invert	
0	159	D[0:3]	D[0:3]	D[0:3]	..	D[0:3]	D[0:3]	D[0:3]	**G1**	
		D[4:7]	D[4:7]	D[4:7]	..	D[4:7]	D[4:7]	D[4:7]	**G2**	
1	158	D[0:3]	D[0:3]	D[0:3]	..	D[0:3]	D[0:3]	D[0:3]	**G3**	
		D[4:7]	D[4:7]	D[4:7]	..	D[4:7]	D[4:7]	D[4:7]	**G4**	
:	:	:	:	:		:	:	:	:	
158	1	D[0:3]	D[0:3]	D[0:3]	..	D[0:3]	D[0:3]	D[0:3]	**G317**	
		D[4:7]	D[4:7]	D[4:7]	..	D[4:7]	D[4:7]	D[4:7]	**G318**	
159	0	D[0:3]	D[0:3]	D[0:3]	..	D[0:3]	D[0:3]	D[0:3]	**G319**	
		D[4:7]	D[4:7]	D[4:7]	..	D[4:7]	D[4:7]	D[4:7]	**G320**	
Source		**S1**	**S2**	**S3**	..	**S638**	**S639**	**S640**	**Gate**	

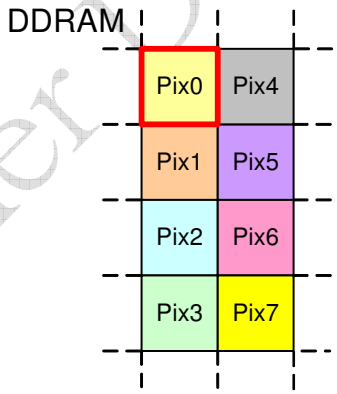
Gate	4bpp mode(>160 lines)		4bpp mode(<=160 lines)		2bpp mode		1bpp mode	
	Page address	Frame address	Page address	Frame address	Page address	Frame address	Page address	Frame address
G1	0	0	0	0/1	0	0/1	0	0/1/2/3
G2								
G3	1		1					
G4								
G5	2		2		1			
G6								
G7	3		3					
G8								
G9	4		4		2		1	
G10								
G311	155	0	75	0/1	77	0/1	38	0/1/2/3
G312								
G313	156		76		78		39	
G314								
G315	157		77					
G316								
G317	158		78		79			
G318								
G319	159		79					
G320								

6.2.2 Addressing

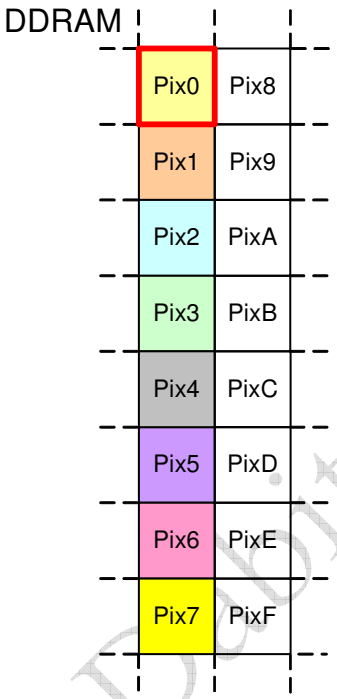
4bpp mode	A1	D7	D6	D5	D4	D3	D2	D1	D0
DDRAM write	0	0	0	1	0	1	1	0	0
command	1	1	0	1	0	0	1	0	1
1st write	1	Pix13	Pix12	Pix11	Pix10	Pix03	Pix02	Pix01	Pix00
2nd write	1	Pix33	Pix32	Pix31	Pix30	Pix23	Pix22	Pix21	Pix20



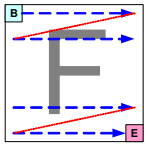
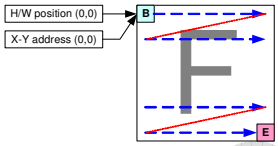
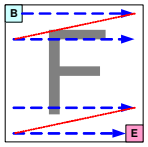
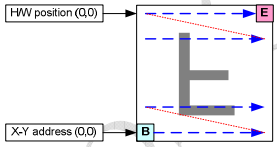
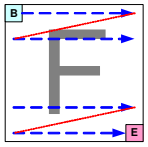
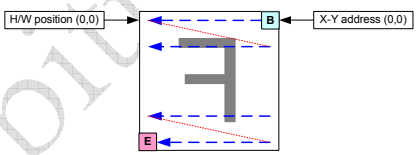
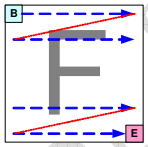
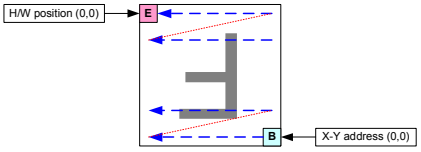
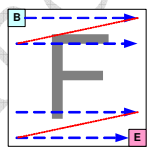
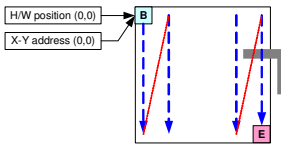
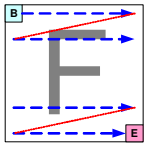
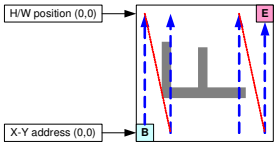
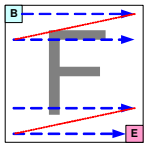
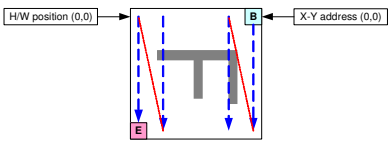
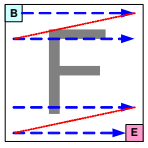
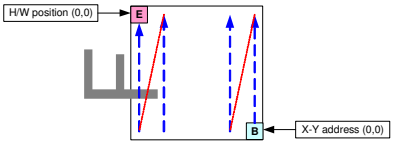
2bpp mode	A1	D7	D6	D5	D4	D3	D2	D1	D0
DDRAM write	0	0	0	1	0	1	1	0	0
command	1	1	0	1	0	0	1	0	1
1st write	1	Pix31	Pix30	Pix21	Pix20	Pix11	Pix10	Pix01	Pix00
2nd write	1	Pix71	Pix70	Pix61	Pix60	Pix51	Pix50	Pix41	Pix40



1bpp mode	A1	D7	D6	D5	D4	D3	D2	D1	D0
DDRAM write	0	0	0	1	0	1	1	0	0
command	1	1	0	1	0	0	1	0	1
1st write	1	Pix7	Pix6	Pix5	Pix4	Pix3	Pix2	Pix1	Pix0
2nd write		PixF	PixE	PixD	PixC	PixB	PixA	Pix9	Pix8

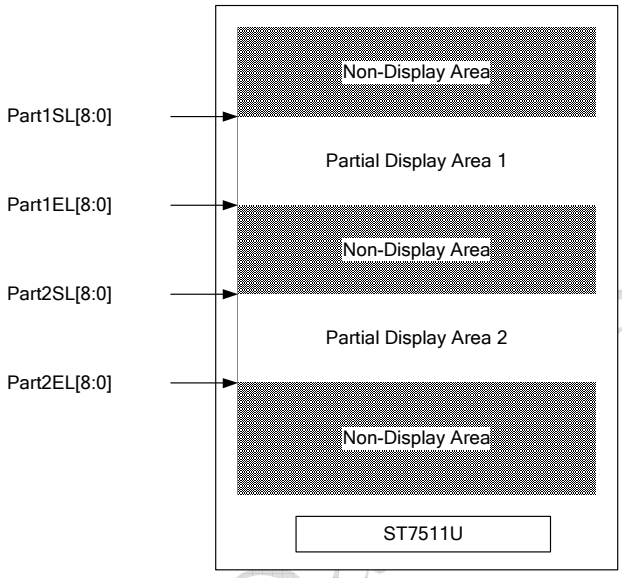


6.2.3 Page Address Circuit and Column Address Circuit

Display data direction	Memory access control			Image in the host	Image in the driver (DDRAM)
	MV	MX	MY		
Normal	0	0	0		
Y-Mirror	0	0	1		
X-Mirror	0	1	0		
X-Mirror Y-Mirror	0	1	1		
X-Y Exchange	1	0	0		
X-Y Exchange Y-Mirror	1	0	1		
X-Y Exchange X-Mirror	1	1	0		
X-Y Exchange X-Mirror Y-Mirror	1	1	1		

6.2.4 Partial Display

The ST7511U can support two regions of partial display area in an LCD module. For the first partial display area, the start and end lines are set by the command, Part1SL[8:0] and Part1EL[8:0], respectively. The second partial display area is set by the same way with the command, Part2SL[8:0] and Part2EL[8:0]. The partial display function in the ST7511U is activated by the command, PTLIN(AAh). When the application of normal display is required, the ST7511U can escape from the partial display mode by the command, PTLOUT(A9h).

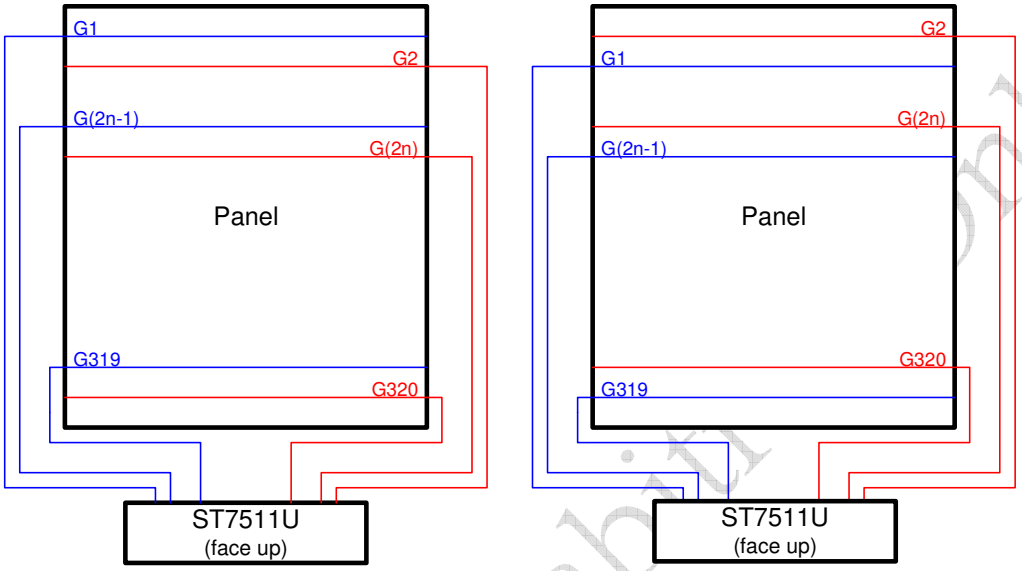


6.3 Oscillation Circuit

This is on-chip Oscillator without external resistor. When the internal oscillator is used, connect CLS to VDDI; when the external oscillator is used, connect CLS to VSS and input external clock to CL pin. This oscillator signal is used by the voltage booster and display timing generation circuit.

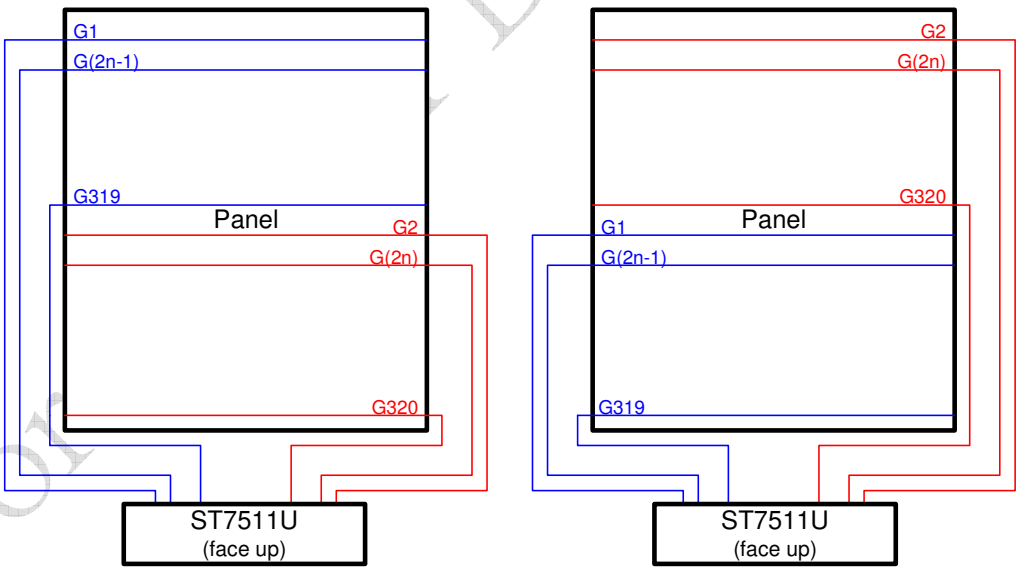
6.4 Setting Gate Line Scan Mode

ST7511U can support 4 kinds of scan mode.



Scan Mode 1

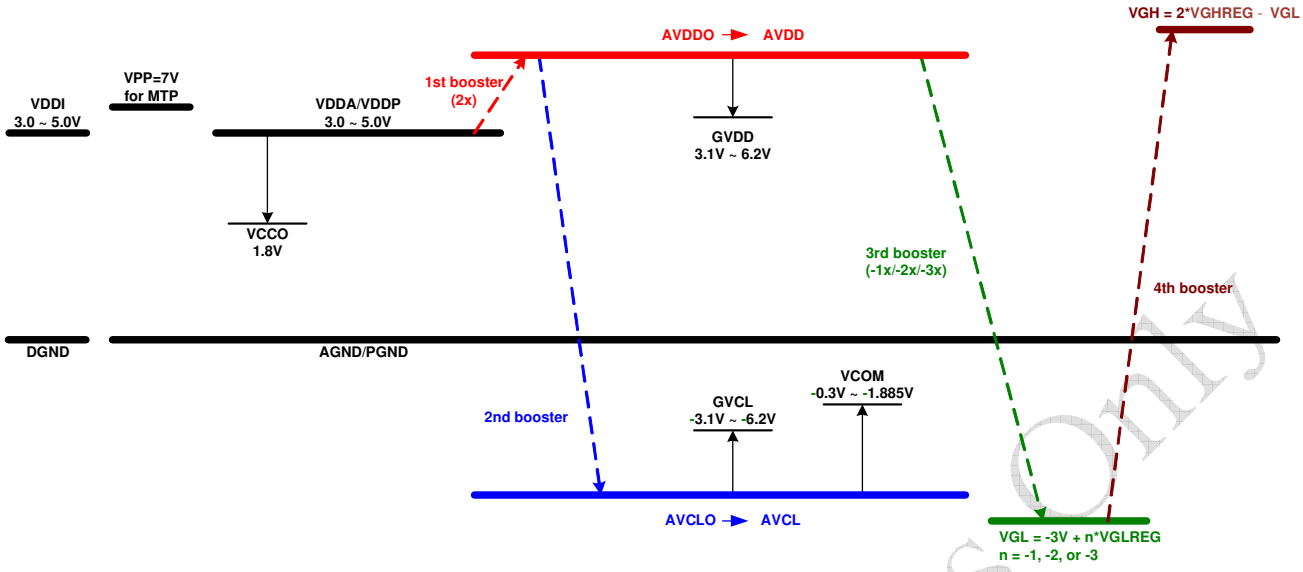
Scan Mode 2



Scan Mode 3

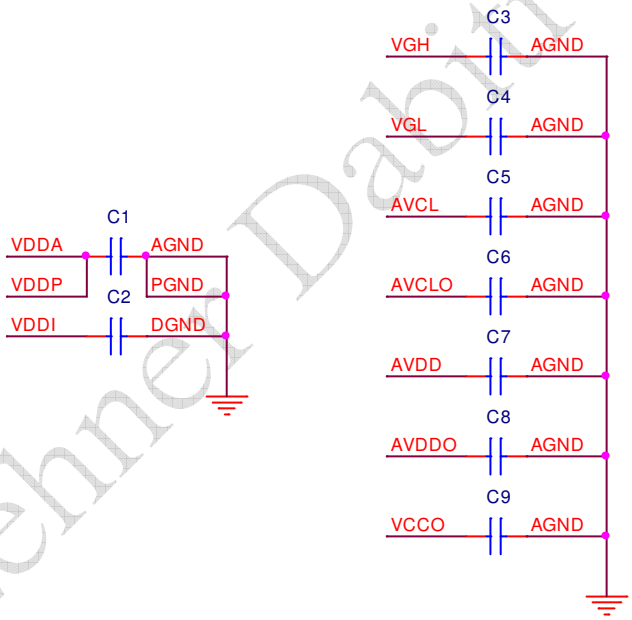
Scan Mode 4

6.5 Power System

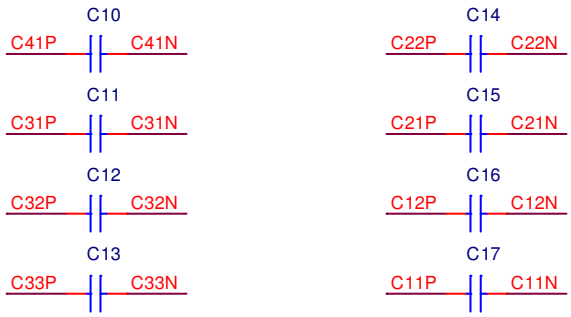


6.6 Connection Diagram of External Components

6.6.1 Connection of Stabilization Capacitors



6.6.2 Connection of Charge Pump Capacitors



6.6.3 Requirement of External Capacitors

Item	Capacitance (uF)	Rated voltage (V)	Remarks
C1,C2	4.7	6.3	X7R
C3	4.7	25	X7R
C4	4.7	16	X7R
C5,C6,C7,C8	4.7	10	X7R
C9	4.7	6.3	X7R
C10,C11,C12,C13	2.2	16	X7R
C14,C15	2.2	10	X7R
C16,C17	2.2	6.3	X7R

6.7 Gamma Circuit

This gamma circuit determines 64-level x 2-polarity voltages for grayscale.

For 4bpp mode, these gray levels can be determined by GAMSET4P1~GAMSET4P4 or GAMSET4N1~GAMSET4N4.

For 2bpp mode, these gray levels can be determined by GAMSET2P or GAMSET2N.

For 1bpp mode, these gray levels can be determined by GAMSET1.

G*x*BPV*y*[5:0] *x* = 1 ~ 4, *y* = 0 ~ F	Equation of voltages	G*x*BPV*y*[5:0] *x* = 1 ~ 4, *y* = 0 ~ F	Equation of voltages
000000	AGND	100000	GVDD x 32R/63R
000001	GVDD x 1R/63R	100001	GVDD x 33R/63R
000010	GVDD x 2R/63R	100010	GVDD x 34R/63R
000011	GVDD x 3R/63R	100011	GVDD x 35R/63R
000100	GVDD x 4R/63R	100100	GVDD x 36R/63R
000101	GVDD x 5R/63R	100101	GVDD x 37R/63R
000110	GVDD x 6R/63R	100110	GVDD x 38R/63R
000111	GVDD x 7R/63R	100111	GVDD x 39R/63R
001000	GVDD x 8R/63R	101000	GVDD x 40R/63R
001001	GVDD x 9R/63R	101001	GVDD x 41R/63R
001010	GVDD x 10R/63R	101010	GVDD x 42R/63R
001011	GVDD x 11R/63R	101011	GVDD x 43R/63R
001100	GVDD x 12R/63R	101100	GVDD x 44R/63R
001101	GVDD x 13R/63R	101101	GVDD x 45R/63R
001110	GVDD x 14R/63R	101110	GVDD x 46R/63R
001111	GVDD x 15R/63R	101111	GVDD x 47R/63R
010000	GVDD x 16R/63R	110000	GVDD x 48R/63R
010001	GVDD x 17R/63R	110001	GVDD x 49R/63R
010010	GVDD x 18R/63R	110010	GVDD x 50R/63R
010011	GVDD x 19R/63R	110011	GVDD x 51R/63R
010100	GVDD x 20R/63R	110100	GVDD x 52R/63R
010101	GVDD x 21R/63R	110101	GVDD x 53R/63R
010110	GVDD x 22R/63R	110110	GVDD x 54R/63R
010111	GVDD x 23R/63R	110111	GVDD x 55R/63R
011000	GVDD x 24R/63R	111000	GVDD x 56R/63R
011001	GVDD x 25R/63R	111001	GVDD x 57R/63R

G*x*BPV*y*[5:0] *x* = 1 ~ 4, *y* = 0 ~ F	Equation of voltages	G*x*BPV*y*[5:0] *x* = 1 ~ 4, *y* = 0 ~ F	Equation of voltages
011010	GVDD x 26R/63R	111010	GVDD x 58R/63R
011011	GVDD x 27R/63R	111011	GVDD x 59R/63R
011100	GVDD x 28R/63R	111100	GVDD x 60R/63R
011101	GVDD x 29R/63R	111101	GVDD x 61R/63R
011110	GVDD x 30R/63R	111110	GVDD x 62R/63R
011111	GVDD x 31R/63R	111111	GVDD

G*x*BNV*y*[5:0] *x* =1 ~ 4, *y* =0 ~ F	Equation of voltages	G*x*BNV*y*[5:0] *x* = 1 ~ 4, *y* = 0 ~ F	Equation of voltages
000000	AGND	100000	GVCL x 32R/63R
000001	GVCL x 1R/63R	100001	GVCL x 33R/63R
000010	GVCL x 2R/63R	100010	GVCL x 34R/63R
000011	GVCL x 3R/63R	100011	GVCL x 35R/63R
000100	GVCL x 4R/63R	100100	GVCL x 36R/63R
000101	GVCL x 5R/63R	100101	GVCL x 37R/63R
000110	GVCL x 6R/63R	100110	GVCL x 38R/63R
000111	GVCL x 7R/63R	100111	GVCL x 39R/63R
001000	GVCL x 8R/63R	101000	GVCL x 40R/63R
001001	GVCL x 9R/63R	101001	GVCL x 41R/63R
001010	GVCL x 10R/63R	101010	GVCL x 42R/63R
001011	GVCL x 11R/63R	101011	GVCL x 43R/63R
001100	GVCL x 12R/63R	101100	GVCL x 44R/63R
001101	GVCL x 13R/63R	101101	GVCL x 45R/63R
001110	GVCL x 14R/63R	101110	GVCL x 46R/63R
001111	GVCL x 15R/63R	101111	GVCL x 47R/63R
010000	GVCL x 16R/63R	110000	GVCL x 48R/63R
010001	GVCL x 17R/63R	110001	GVCL x 49R/63R
010010	GVCL x 18R/63R	110010	GVCL x 50R/63R
010011	GVCL x 19R/63R	110011	GVCL x 51R/63R
010100	GVCL x 20R/63R	110100	GVCL x 52R/63R
010101	GVCL x 21R/63R	110101	GVCL x 53R/63R
010110	GVCL x 22R/63R	110110	GVCL x 54R/63R
010111	GVCL x 23R/63R	110111	GVCL x 55R/63R
011000	GVCL x 24R/63R	111000	GVCL x 56R/63R
011001	GVCL x 25R/63R	111001	GVCL x 57R/63R
011010	GVCL x 26R/63R	111010	GVCL x 58R/63R
011011	GVCL x 27R/63R	111011	GVCL x 59R/63R
011100	GVCL x 28R/63R	111100	GVCL x 60R/63R
011101	GVCL x 29R/63R	111101	GVCL x 61R/63R
011110	GVCL x 30R/63R	111110	GVCL x 62R/63R
011111	GVCL x 31R/63R	111111	GVCL

6.8 Reset

Setting RSTB pin to “L” (hardware reset) can initialize internal function. Generally, VDDI is not stable at the time that the system power is just turned ON. The hardware reset or software reset is required to initialize internal registers after VDDI is stable. Initialization by RSTB pin or command SWRESET is essential before operating.

6.9 Temperature Compensation Circuit

6.9.1 Set GVDD/GVCL with Temperature Compensation (Temperature ≠ 24℃)

There are 14-line slopes in each temperature step, and customer can select one line slope of temperature compensation coefficient for each temperature step. Each temperature step is 8℃. Please see Fig 7. as below.

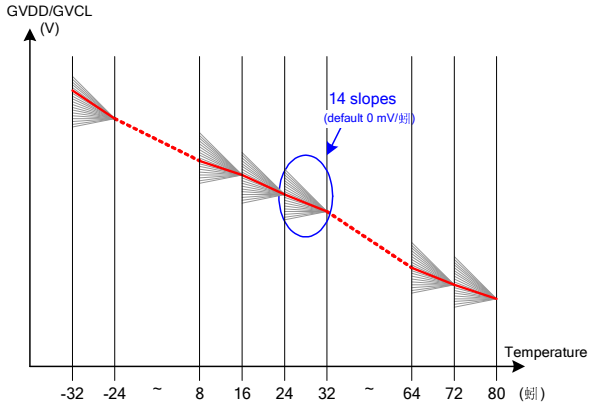


Fig 7. Temperature Compensation Coefficient Selection

The temperature compensation circuit includes negative and positive temperature gradient slope coefficient. The parameter (MTGVxyy) of Temperature Gradient Set instruction (where x=GV or GC, yy=01, 02, 03,…11) has a setting value between 0 and 15. MTGVxyy[3]=0 means the sign for the slope of temperature gradient is positive. Otherwise, MTGVxyy[3]=1 means the sign for the slope of temperature gradient is negative. MTGVxyy[2:0] determines the multiplier of the temperature increment by 12.5mV/℃. For example, MTGVxyy[2:0]=1 results the slope of temperature gradient in 1x12.5mV/℃. In other words, if MTGVxyy[3:0]=15, the slope of temperature gradient will be -7x12.5 mV/℃.

Note that each MTGVxyy individually corresponds to a temperature interval; the MTGVxyy means temperature gradient slope coefficient. The relations between MTGVxyy and GVDD/GVCL quantity due to temperature V0(T) are described in the equation shown in Table 3.

Temperature Range	Equation GVDD/GVCL(V0) at temperature=T℃
-32℃ ≤ T < -24℃	V0(T) = V0(T24) + (-16 – T) x M0 + (M1 + M2 + M3 + M4 + M5 + M6) x 8
-24℃ ≤ T < -16℃	V0(T) = V0(T24) + (-16 – T) x M1 + (M2 + M3 + M4 + M5 + M6) x 8
-16℃ ≤ T < -8℃	V0(T) = V0(T24) + (-8 – T) x M2 + (M3 + M4 + M5 + M6) x 8
-8℃ ≤ T < 0℃	V0(T) = V0(T24) + (0 – T) x M3 + (M4 + M5 + M6) x 8
0℃ ≤ T < 8℃	V0(T) = V0(T24) + (8 – T) x M4 + (M5 + M6) x 8
8℃ ≤ T < 16℃	V0(T) = V0(T24) + (16 – T) x M5 + M6 x 8
16℃ ≤ T < 24℃	V0(T) = V0(T24) + (24 – T) x M6
24℃ ≤ T < 32℃	V0(T) = V0(T24) – (T – 24) x M7
32℃ ≤ T < 40℃	V0(T) = V0(T24) – (T – 32) x M8 – M7 x 8
40℃ ≤ T < 48℃	V0(T) = V0(T24) – (T – 40) x M9– (M8 + M7) x 8
48℃ ≤ T < 56℃	V0(T) = V0(T24) – (T – 48) x MA – (M9 + M8 + M7) x 8
56℃ ≤ T < 64℃	V0(T) = V0(T24) – (T – 56) x MB – (MA + M9 + M8 + M7) x 8
64℃ ≤ T < 72℃	V0(T) = V0(T24) – (T – 64) x MC – (MB + MA + M9 + M8 + M7) x 8
72℃ ≤ T < 80℃	V0(T) = V0(T24) – (T – 72) x MD – (MC + MB + MA + M9 + M8 + M7) x 8

Table 3

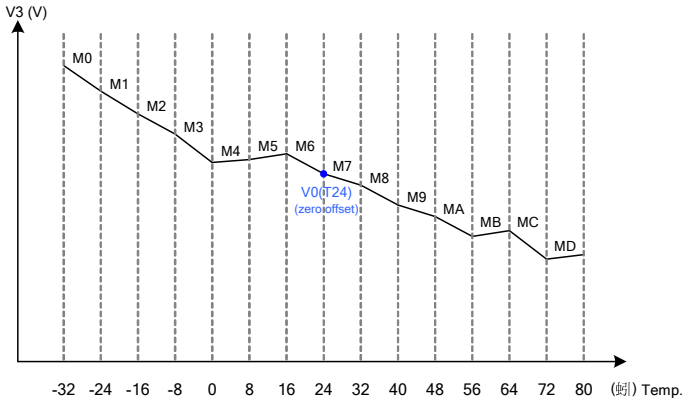
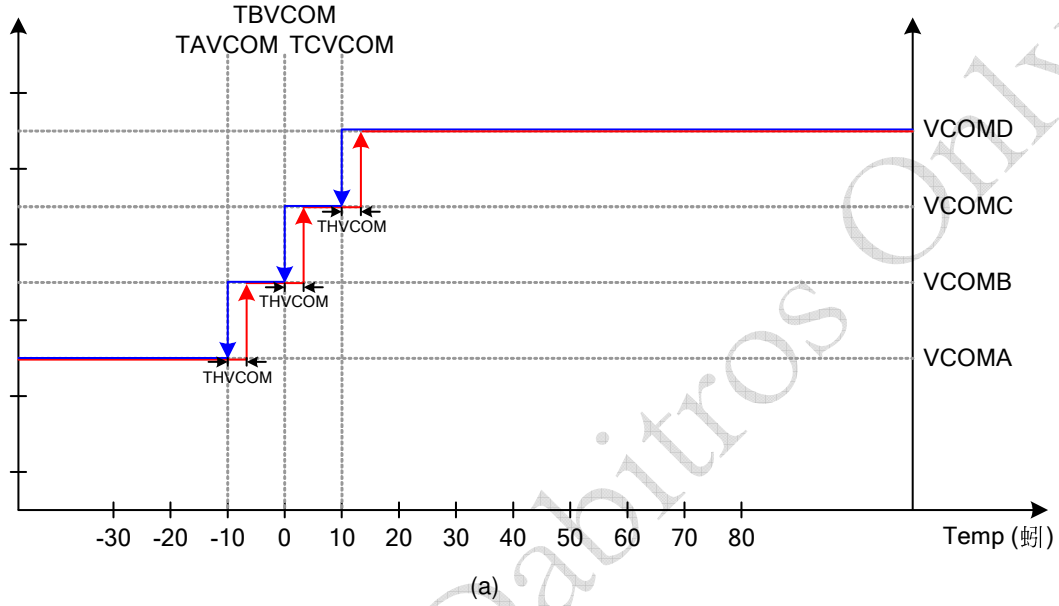


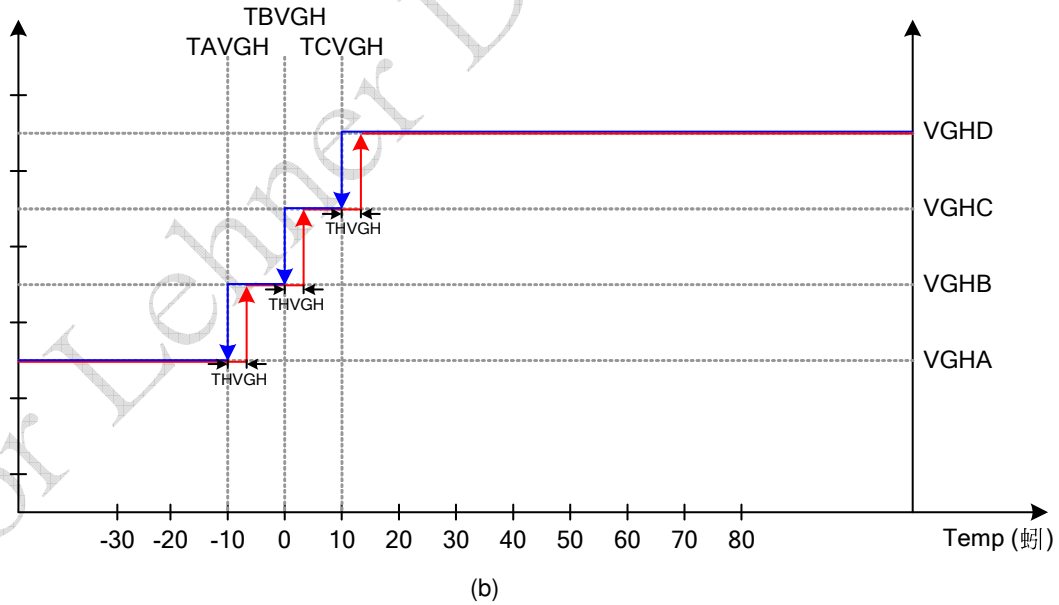
Fig.8

6.9.2 Temperature Gradient Compensation Coefficient of VCOM, VGH, and Frame Rate

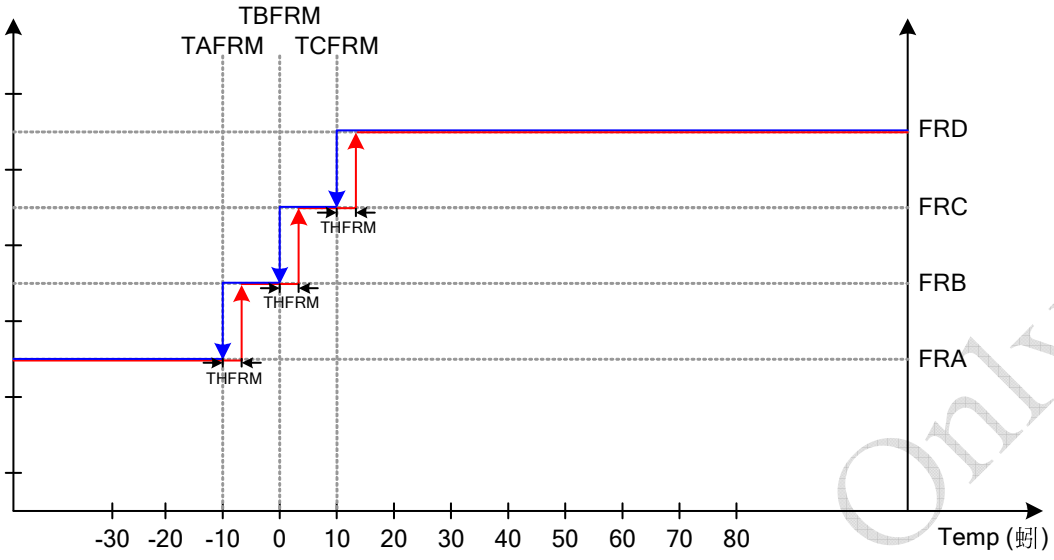
ST7511U will auto-switch VCOM in different temperature, such as Fig. 9(a). TA, TB and TC are VCOM switching temperature which can be defined by customer with instruction (C8h). VCOMA, VCOMB, VCOMC and VCOMD are switched VCOM, which also can be defined by customer with instruction (B1h). The temperature hysteresis “THVCOM” in the Fig.9(a) that defines the sensitivity of internal temperature sensor and the value can be altered by instruction. The settings of temperature compensation about VGH and frame rate are in the same way with VCOM.



(a)



(b)



(c)

Fig.9

7. COMMAND

7.1 Command List

Instruction	Add. (hex)	A0	ERD	RWR	D7	D6	D5	D4	D3	D2	D1	D0	Default (hex)	Function
NOP	00	0	1	↑	0	0	0	0	0	0	0	0		Non-Operation
		1	1	↑	1	0	1	0	0	1	0	1		
SLPOUT	12	0	1	↑	0	0	0	1	0	0	1	0		Sleep Out
		1	1	↑	1	0	1	0	0	1	0	1		
SLPIN	13	0	1	↑	0	0	0	1	0	0	1	1		Sleep In
		1	1	↑	1	0	1	0	0	1	0	1		
DISOFF	14	0	1	↑	0	0	0	1	0	1	0	0		Display Off
		1	1	↑	1	0	1	0	0	1	0	1		
DISON	15	0	1	↑	0	0	0	1	0	1	0	1		Display On
		1	1	↑	1	0	1	0	0	1	0	1		
DINVOUT	1A	0	1	↑	0	0	0	1	1	0	1	0		Display Invert Out
		1	1	↑	1	0	1	0	0	1	0	1		
DINVIN	1B	0	1	↑	0	0	0	1	1	0	1	1		Display Invert In
		1	1	↑	1	0	1	0	0	1	0	1		
BLOUT	1C	0	1	↑	0	0	0	1	1	1	0	0		Blinking Out
		1	1	↑	1	0	1	0	0	1	0	1		
BLIN	1D	0	1	↑	0	0	0	1	1	1	0	1		Blinking In
		1	1	↑	1	0	1	0	0	1	0	1		
STFRAME	21	0	1	↑	0	0	1	0	0	0	0	1		Start Frame Address
		1	1	↑	0	0	0	0	0	0	SFrmA1	SFrmA0	00	
		1	1	↑	1	0	1	0	0	1	0	1		
		1	1	↑	1	0	1	0	0	1	0	1		
		1	1	↑	1	0	1	0	0	1	0	1		
BPPSEL	22	0	1	↑	0	0	1	0	0	0	1	0		BPP Select
		1	1	↑	0	0	0	0	0	0	BppSel1	BppSel0	02	
		1	1	↑	1	0	1	0	0	1	0	1		
		1	1	↑	1	0	1	0	0	1	0	1		
		1	1	↑	1	0	1	0	0	1	0	1		
MADCTL	24	0	1	↑	0	0	1	0	0	1	0	0		Memory Address Control
		1	1	↑	0	0	0	0	0	MV	MY	MX	00	
		1	1	↑	1	0	1	0	0	1	0	1		
		1	1	↑	1	0	1	0	0	1	0	1		
		1	1	↑	1	0	1	0	0	1	0	1		
PASET	25	0	1	↑	0	0	1	0	0	1	0	1		Page Address Set
		1	1	↑	PSA7	PSA6	PSA5	PSA4	PSA3	PSA2	PSA1	PSA0	00	
		1	1	↑	PEA7	PEA6	PEA5	PEA4	PEA3	PEA2	PEA1	PEA0	9F	
		1	1	↑	0	0	0	0	0	0	FrmA1	FrmA0	00	
		1	1	↑	1	0	1	0	0	1	0	1		
CASET	26	0	1	↑	0	0	1	0	0	1	1	0		Column

		1	1	↑	0	0	0	0	0	0	CSA9	CSA8	00	Address Set
		1	1	↑	CSA7	CSA6	CSA5	CSA4	CSA3	CSA2	CSA1	CSA0	00	
		1	1	↑	0	0	0	0	0	0	CEA9	CEA8	02	
		1	1	↑	CEA7	CEA6	CEA5	CEA4	CEA3	CEA2	CEA1	CEA0	7F	
		0	1	↑	0	0	1	0	1	0	0	1		
		1	1	↑	0	0	0	0	BFData3	BFData2	BFData1	BFData0	00	
BLKFIL	29	1	1	↑	1	0	1	0	0	1	0	1		Block Fill
		1	1	↑	1	0	1	0	0	1	0	1		
		1	1	↑	1	0	1	0	0	1	0	1		
		0	1	↑	0	0	1	0	1	0	1	1		
		1	1	↑	BlinkCyc7	BlinkCyc6	BlinkCyc5	BlinkCyc4	BlinkCyc3	BlinkCyc2	BlinkCyc1	BlinkCyc0	1D	
BLSET	2B	1	1	↑	0	0	0	0	B1stF1	B1stF0	B2ndF1	B2ndF0	01	Blinking Set
		1	1	↑	1	0	1	0	0	1	0	1		
		1	1	↑	1	0	1	0	0	1	0	1		
		0	1	↑	0	0	1	0	1	1	0	0		
WRRAM	2C	1	1	↑	1	0	1	0	0	1	0	1		Write RAM
		1	1	↑	Data7	Data6	Data5	Data4	Data3	Data2	Data1	Data0		
		0	1	↑	0	0	1	0	1	1	0	1		
		1	1	↑	1	0	1	0	0	1	0	1		
RDRAM	2D	1	↑	1	X	X	X	X	X	X	X	X		Read RAM
		1	↑	1	Data7	Data6	Data5	Data4	Data3	Data2	Data1	Data0		
		0	1	↑	0	0	1	1	0	0	0	1		
		1	1	↑	0	0	0	0	0	0	0	DisLin8	01	
DISAR	31	1	1	↑	DisLin7	DisLin6	DisLin5	DisLin4	DisLin3	DisLin2	DisLin1	DisLin0	3F	Display Area
		1	1	↑	0	0	0	0	0	0	1	0	02	
		1	1	↑	0	1	1	1	1	1	1	1	7F	
		0	1	↑	0	0	1	1	0	0	1	0		
		1	1	↑	HClkNo7	HClkNo6	HClkNo5	HClkNo4	HClkNo3	HClkNo2	HClkNo1	HClkNo0	32	
DISSET1	32	1	1	↑	BPNo7	BPNo6	BPNo5	BPNo4	BPNo3	BPNo2	BPNo1	BPNo0	02	Display Set1
		1	1	↑	NorBlk	OSCO	0	0	FPNo11	FPNo10	FPNo9	FPNo8	00	
		1	1	↑	FPNo7	FPNo6	FPNo5	FPNo4	FPNo3	FPNo2	FPNo1	FPNo0	01	
		0	1	↑	0	0	1	1	0	0	1	1		
		1	1	↑	SOnT7	SOnT6	SOnT5	SOnT4	SOnT3	SOnT2	SOnT1	SOnT0	0A	
DISSET2	33	1	1	↑	SOffT7	SOffT6	SOffT5	SOffT4	SOffT3	SOffT2	SOffT1	SOffT0	28	Display Set2
		1	1	↑	GOnT7	GOnT6	GOnT5	GOnT4	GOnT3	GOnT2	GOnT1	GOnT0	0C	
		1	1	↑	GOffT7	GOffT6	GOffT5	GOffT4	GOffT3	GOffT2	GOffT1	GOffT0	26	
		0	1	↑	0	0	1	1	0	1	0	0		
		1	1	↑	0	0	0	0	0	0	0	Part1SL8	00	
PTLSET1	34	1	1	↑	Part1SL7	Part1SL6	Part1SL5	Part1SL4	Part1SL3	Part1SL2	Part1SL1	Part1SL0	00	Partial Set 1
		1	1	↑	0	0	0	0	0	0	0	Part1EL8	00	
		1	1	↑	Part1EL7	Part1EL6	Part1EL5	Part1EL4	Part1EL3	Part1EL2	Part1EL1	Part1EL0	00	
PTLSET2	35	0	1	↑	0	0	1	1	0	1	0	1		Partial Set 2
		1	1	↑	0	0	0	0	0	0	0	Part2SL8	00	
		1	1	↑	Part2SL7	Part2SL6	Part2SL5	Part2SL4	Part2SL3	Part2SL2	Part2SL1	Part2SL0	00	
		1	1	↑	0	0	0	0	0	0	0	Part2EL8	00	

		1	1	↑	Part2EL7	Part2EL6	Part2EL5	Part2EL4	Part2EL3	Part2EL2	Part2EL1	Part2EL0	00	
PTLSET3	36	0	1	↑	0	0	1	1	0	1	1	0		Partial Set 3
		1	1	↑	0	NDisRefR6	NDisRefR5	NDisRefR4	NDisRefR3	NDisRefR2	NDisRefR1	NDisRefR0	00	
		1	1	↑	0	0	0	0	0	RTBFreq2	RTBFreq1	RTBFreq0	00	
		1	1	↑	0	0	0	0	0	0	NDisDM1	NDisDM0	00	
		1	1	↑	1	0	1	0	0	1	0	1		
VCMDAT	54	0	1	↑	0	1	0	1	0	1	0	0		VCOM Offset Data
		1	1	↑	0	0	0	0	VcomS3	VcomS2	VcomS1	VcomS0	00	
		1	1	↑	0	VcomD16	VcomD15	VcomD14	VcomD13	VcomD12	VcomD11	VcomD10	00	
		1	1	↑	0	VcomD26	VcomD25	VcomD24	VcomD23	VcomD22	VcomD21	VcomD20	00	
		1	1	↑	1	0	1	0	0	1	0	1		
UIDSET	55	0	1	↑	0	1	0	1	0	1	0	1		User ID
		1	1	↑	UID117	UID116	UID115	UID114	UID113	UID112	UID111	UID110	00	
		1	1	↑	UID127	UID126	UID125	UID124	UID123	UID122	UID121	UID120	00	
		1	1	↑	UID217	UID216	UID215	UID214	UID213	UID212	UID211	UID210	00	
		1	1	↑	UID227	UID226	UID225	UID224	UID223	UID222	UID221	UID220	00	
MTPMOD	5A	0	1	↑	0	1	0	1	1	0	1	0		Multi Time PROM Mode
		1	1	↑	MTPMOD7	MTPMOD6	MTPMOD5	MTPMOD4	MTPMOD3	MTPMOD2	MTPMOD1	MTPMOD0	00	
		1	1	↑	1	0	1	0	0	1	0	1		
		1	1	↑	1	0	1	0	0	1	0	1		
		1	1	↑	1	0	1	0	0	1	0	1		
MTPOP	5B	0	1	↑	0	1	0	1	1	0	1	1		Multi Time PROM Operation
		1	1	↑	0	0	0	0	0	MTP_Sel	0	Prog_Mod	00	
		1	1	↑	1	0	1	0	0	1	0	1		
		1	1	↑	1	0	1	0	0	1	0	1		
		1	1	↑	1	0	1	0	0	1	0	1		
SPI3WRCNT	5C	0	1	↑	0	1	0	1	1	1	0	0		SPI3 Write Memory Byte Counter
		1	1	↑	Si3Mw15	Si3Mw14	Si3Mw13	Si3Mw12	Si3Mw11	Si3Mw10	Si3Mw9	Si3Mw8	02	
		1	1	↑	Si3Mw7	Si3Mw6	Si3Mw5	5Si3Mw4	Si3Mw3	Si3Mw2	Si3Mw1	Si3Mw0	7F	
		1	1	↑										
		1	1	↑										
PWRCTL	61	0	1	↑	0	1	1	0	0	0	0	1		Power Control
		1	1	↑	BST3SR1	BST3SR0	0	0	BST4ON	BST3ON	BST2ON	BST1ON	40	
		1	1	↑	FOFNo3	FOFNo2	FOFNo1	FOFNo0	0	SAMPSet2	SAMPSet1	SAMPSet0	04	
		1	1	↑	0	0	0	0	0	0	1	0	02	
		1	1	↑	1	0	1	0	0	1	0	1		
EVSET1	62	0	1	↑	0	1	1	0	0	0	1	0		Electronic Volume Set 1
		1	1	↑	0	VCOM6	VCOM5	VCOM4	VCOM3	VCOM2	VCOM1	VCOM0	0A	
		1	1	↑	0	0	VGHREG5	VGHREG4	VGHREG3	VGHREG2	VGHREG1	VGHREG0	06	
		1	1	↑	0	0	0	VGLREG4	VGLREG3	VGLREG2	VGLREG1	VGLREG0	0F	
		1	1	↑	1	0	1	0	0	1	0	1		
EVSET2	63	0	1	↑	0	1	1	0	0	0	1	1		Electronic Volume Set 2
		1	1	↑	0	0	0	GVDD4	GVDD3	GVDD2	GVDD1	GVDD0	0F	
		1	1	↑	0	0	0	GVCL4	GVCL3	GVCL2	GVCL1	GVCL0	0F	
		1	1	↑	1	0	1	0	0	1	0	1		

		1	1	↑	1	0	1	0	0	1	0	1		
BCLKSET	64	0	1	↑	0	1	1	0	0	1	0	0		Booster Clock Setting
		1	1	↑	0	AVclClk2	AVclClk1	AVclClk0	0	AVdClk2	AVdClk2	AVdClk2	44	
		1	1	↑	0	VglClk2	VglClk1	VglClk0	0	Vghclk2	Vghclk1	VghClk0	44	
		1	1	↑	0	AVclClk_nd2	AVclClk_nd1	AVclClk_nd2	0	AVdClk_nd2	AVdClk_nd1	AVdClk_nd0	44	
		1	1	↑	0	VglClk_nd2	VglClk_nd1	VglClk_nd0	0	Vghclk_nd2	Vghclk_nd1	VghClk_nd0	44	
GATESET	66	0	1	↑	0	1	1	0	0	1	1	0		Gate Set
		1	1	↑	VGPP	0	0	ScanDir	0	0	ScanMod1	ScanMod0	00	
		1	1	↑	1	0	1	0	0	1	0	1		
		1	1	↑	1	0	1	0	0	1	0	1		
		1	1	↑	1	0	1	0	0	1	0	1		
PWMCTRL	6C	0	1	↑	0	1	1	0	1	1	0	0		PWM Control
		1	1	↑	0	0	0	0	0	LOnTyp	0	LEDMD	00	
		1	1	↑	SLEDOn7	SLEDOn6	SLEDOn5	SLEDOn4	SLEDOn3	SLEDOn2	SLEDOn1	SLEDOn0		
		1	1	↑	ASLEDOn7	ASLEDOn6	ASLEDOn5	ASLEDOn4	ASLEDOn3	ASLEDOn2	ASLEDOn1	ASLEDOn0		
		1	1	↑	ASLEDOf7	ASLEDOf6	ASLEDOf5	ASLEDOf4	ASLEDOf3	ASLEDOf2	ASLEDOf1	ASLEDOf0		
RDSTAT	72	0	1	↑	0	1	1	1	0	0	1	0		Read Status
		1	1	↑	1	0	1	0	0	1	0	1		
		1	↑	1	R17	R16	R15	0	R13	R12	R11	R10		
		1	↑	1	0	R26	R25	R24	R23	R22	R21	R20		
		1	↑	1	R37	R36	R35	R34	R33	R32	R31	R30		
		1	↑	1	R47	R46	R45	R44	R43	R42	R41	R40		
		1	↑	1	0	0	0	0	0	R52	R51	R50		
		1	↑	1	0	R66	R65	R64	0	R62	R61	R60		
RDREV	73	0	1	↑	0	1	1	1	0	0	1	1		Read Revision
		1	1	↑	1	0	1	0	0	1	0	1		
		1	↑	1	R17	R16	R15	R14	R13	R12	R11	R10		
RDUID	75	0	1	↑	0	1	1	1	0	1	0	1		Read User ID
		1	1	↑	1	0	1	0	0	1	0	1		
		1	↑	1	R17	R16	R15	R14	R13	R12	R11	R10		
		1	↑	1	R27	R26	R25	R24	R23	R22	R21	R20		
		1	↑	1	R37	R36	R35	R34	R33	R32	R31	R30		
		1	↑	1	R47	R46	R45	R44	R43	R42	R41	R40		
		1	↑	1	R57	R56	R55	R54	R53	R52	R51	R50		
		1	↑	1	R67	R66	R65	R64	R63	R62	R61	R60		
		1	↑	1	R77	R76	R75	R74	R73	R72	R71	R70		
		1	↑	1	R87	R86	R85	R84	R83	R82	R81	R80		
		1	↑	1	R97	R96	R95	R94	R93	R92	R91	R90		
		1	↑	1	RA7	RA6	RA5	RA4	RA3	RA2	RA1	RA0		
		1	↑	1	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0		
		1	↑	1	RC7	RC6	RC5	RC4	RC3	RC2	RC1	RC0		
RDVCMDAT	79	0	1	↑	0	1	1	1	1	0	0	1		Read VCOM Data
		1	1	↑	1	0	1	0	0	1	0	1		
		1	↑	1	x	x	R15	R14	R13	R12	R11	R10		
		1	↑	1	x	x	R25	R24	R23	R22	R21	R20		

		1	↑	1	x	x	R35	R34	R33	R32	R31	R30		
		1	↑	1	x	x	R45	R44	R43	R42	R41	R40		
		1	↑	1	x	x	R55	R54	R53	R52	R51	R50		
		1	↑	1	x	x	R65	R64	R63	R62	R61	R60		
		1	↑	1	x	x	R75	R74	R73	R72	R71	R70		
		1	↑	1	0	0	0	0	R83	R82	R81	R80		
GAMSET4P1	91	0	1	↑	1	0	0	1	0	0	0	1		Gamma Set 4bpp Positive 1
		1	1	↑	0	0	G4BPV05	G4BPV04	G4BPV03	G4BPV02	G4BPV01	G4BPV00	00	
		1	1	↑	0	0	G4BPV15	G4BPV14	G4BPV13	G4BPV12	G4BPV11	G4BPV10	04	
		1	1	↑	0	0	G4BPV25	G4BPV24	G4BPV23	G4BPV22	G4BPV21	G4BPV20	08	
		1	1	↑	0	0	G4BPV35	G4BPV34	G4BPV33	G4BPV32	G4BPV31	G4BPV30	0C	
GAMSET4P2	92	0	1	↑	1	0	0	1	0	0	1	0		Gamma Set 4bpp Positive 2
		1	1	↑	0	0	G4BPV45	G4BPV44	G4BPV43	G4BPV42	G4BPV41	G4BPV40	10	
		1	1	↑	0	0	G4BPV55	G4BPV54	G4BPV53	G4BPV52	G4BPV51	G4BPV50	14	
		1	1	↑	0	0	G4BPV65	G4BPV64	G4BPV63	G4BPV62	G4BPV61	G4BPV60	18	
		1	1	↑	0	0	G4BPV75	G4BPV74	G4BPV73	G4BPV72	G4BPV71	G4BPV70	1C	
GAMSET4P3	93	0	1	↑	1	0	0	1	0	0	1	1		Gamma Set 4bpp Positive 3
		1	1	↑	0	0	G4BPV85	G4BPV84	G4BPV83	G4BPV82	G4BPV81	G4BPV80	23	
		1	1	↑	0	0	G4BPV95	G4BPV94	G4BPV93	G4BPV92	G4BPV91	G4BPV90	27	
		1	1	↑	0	0	G4BPVA5	G4BPVA4	G4BPVA3	G4BPVA2	G4BPVA1	G4BPVA0	2B	
		1	1	↑	0	0	G4BPVB5	G4BPVB4	G4BPVB3	G4BPVB2	G4BPVB1	G4BPVB0	2F	
GAMSET4P4	94	0	1	↑	1	0	0	1	0	1	0	0		Gamma Set 4bpp Positive 4
		1	1	↑	0	0	G4BPVC5	G4BPVC4	G4BPVC3	G4BPVC2	G4BPVC1	G4BPVC0	33	
		1	1	↑	0	0	G4BPVD5	G4BPVD4	G4BPVD3	G4BPVD2	G4BPVD1	G4BPVD0	37	
		1	1	↑	0	0	G4BPVE5	G4BPVE4	G4BPVE3	G4BPVE2	G4BPVE1	G4BPVE0	3B	
		1	1	↑	0	0	G4BPVF5	G4BPVF4	G4BPVF3	G4BPVF2	G4BPVF1	G4BPVF0	3F	
GAMSET2P	95	0	1	↑	1	0	0	1	0	1	0	1		Gamma Set 2bpp Positive
		1	1	↑	0	0	G2BPV05	G2BPV04	G2BPV03	G2BPV02	G2BPV01	G2BPV00	00	
		1	1	↑	0	0	G2BPV15	G2BPV14	G2BPV13	G2BPV12	G2BPV11	G2BPV10	15	
		1	1	↑	0	0	G2BPV25	G2BPV24	G2BPV23	G2BPV22	G2BPV21	G2BPV20	2A	
		1	1	↑	0	0	G2BPV35	G2BPV34	G2BPV33	G2BPV32	G2BPV31	G2BPV30	3F	
GAMSET1	96	0	1	↑	1	0	0	1	0	1	1	0		Gamma Set 1bpp
		1	1	↑	0	0	G1BPV05	G1BPV04	G1BPV03	G1BPV02	G1BPV01	G1BPV00	00	
		1	1	↑	0	0	G1BPV15	G1BPV14	G1BPV13	G1BPV12	G1BPV11	G1BPV10	3F	
		1	1	↑	0	0	G1BNV05	G1BNV04	G1BNV03	G1BNV02	G1BNV01	G1BNV00	00	
		1	1	↑	0	0	G1BNV15	G1BNV14	G1BNV13	G1BNV12	G1BNV11	G1BNV10	3F	
GAMSET4N1	99	0	1	↑	1	0	0	1	1	0	0	1		Gamma Set 4bpp Negative 1
		1	1	↑	0	0	G4BNV05	G4BNV04	G4BNV03	G4BNV02	G4BNV01	G4BNV00	00	
		1	1	↑	0	0	G4BNV15	G4BNV14	G4BNV13	G4BNV12	G4BNV11	G4BNV10	04	
		1	1	↑	0	0	G4BNV25	G4BNV24	G4BNV23	G4BNV22	G4BNV21	G4BNV20	08	
		1	1	↑	0	0	G4BNV35	G4BNV34	G4BNV33	G4BNV32	G4BNV31	G4BNV30	0C	
GAMSET4N2	9A	0	1	↑	1	0	0	1	1	0	1	0		Gamma Set 4bpp Negative 2
		1	1	↑	0	0	G4BNV45	G4BNV44	G4BNV43	G4BNV42	G4BNV41	G4BNV40	10	
		1	1	↑	0	0	G4BNV55	G4BNV54	G4BNV53	G4BNV52	G4BNV51	G4BNV50	14	
		1	1	↑	0	0	G4BNV65	G4BNV64	G4BNV63	G4BNV62	G4BNV61	G4BNV60	18	

		1	1	↑	0	0	G4BNV75	G4BNV74	G4BNV73	G4BNV72	G4BNV71	G4BNV70	1C	
GAMSET4N3	9B	0	1	↑	1	0	0	1	1	0	1	1		Gamma Set 4bpp Negative 3
		1	1	↑	0	0	G4BNV85	G4BNV84	G4BNV83	G4BNV82	G4BNV81	G4BNV80	23	
		1	1	↑	0	0	G4BNV95	G4BNV94	G4BNV93	G4BNV92	G4BNV91	G4BNV90	27	
		1	1	↑	0	0	G4BNVA5	G4BNVA4	G4BNVA3	G4BNVA2	G4BNVA1	G4BNVA0	2B	
		1	1	↑	0	0	G4BNVB5	G4BNVB4	G4BNVB3	G4BNVB2	G4BNVB1	G4BNVB0	2F	
GAMSET4N4	9C	0	1	↑	1	0	0	1	1	1	0	0		Gamma Set 4bpp Negative 4
		1	1	↑	0	0	G4BNVC5	G4BNVC4	G4BNVC3	G4BNVC2	G4BNVC1	G4BNVC0	33	
		1	1	↑	0	0	G4BNVD5	G4BNVD4	G4BNVD3	G4BNVD2	G4BNVD1	G4BNVD0	37	
		1	1	↑	0	0	G4BNVE5	G4BNVE4	G4BNVE3	G4BNVE2	G4BNVE1	G4BNVE0	3B	
		1	1	↑	0	0	G4BNVF5	G4BNVF4	G4BNVF3	G4BNVF2	G4BNVF1	G4BNVF0	3F	
GAMSET2N	9D	0	1	↑	1	0	0	1	1	1	0	1		Gamma Set 2bpp Negative
		1	1	↑	0	0	G2BNV05	G2BNV04	G2BNV03	G2BNV02	G2BNV01	G2BNV00	00	
		1	1	↑	0	0	G2BNV15	G2BNV14	G2BNV13	G2BNV12	G2BNV11	G2BNV10	15	
		1	1	↑	0	0	G2BNV25	G2BNV24	G2BNV23	G2BNV22	G2BNV21	G2BNV20	2A	
		1	1	↑	0	0	G2BNV35	G2BNV34	G2BNV33	G2BNV32	G2BNV31	G2BNV30	3F	
RMWIN	A1	0	1	↑	1	0	1	0	0	0	0	1		Read Modify Write In
		1	1	↑	1	0	1	0	0	1	0	1		
MTPRDEN	A2	0	1	↑	1	0	1	0	0	0	1	0		MTP Read Enable
		1	1	↑	1	0	1	0	0	1	0	1		
MTPWREN	A3	0	1	↑	1	0	1	0	0	0	1	1		MTP Write Enable
		1	1	↑	1	0	1	0	0	1	0	1		
PTLOUT	A9	0	1	↑	1	0	1	0	1	0	0	1		Partial Out
		1	1	↑	1	0	1	0	0	1	0	1		
PTLIN	AA	0	1	↑	1	0	1	0	1	0	1	0		Partial In
		1	1	↑	1	0	1	0	0	1	0	1		
RMWOUT	AC	0	1	↑	1	0	1	0	1	1	0	0		Read Modify Write Out
		1	1	↑	1	0	1	0	0	1	0	1		
SWRESET	AE	0	1	↑	1	0	1	0	1	1	1	0		Software Reset
		1	1	↑	1	0	1	0	0	1	0	1		
RDTC	76	0	1	↑	0	1	1	1	0	1	1	0		Read TC Data
		1	1	↑	1	0	1	0	0	1	0	1		
		1	↑	1	0	0	0	0	0	0	0	R10		
		1	↑	1	R27	R26	R25	R24	R23	R22	R21	R20		
TCVCOM	B1	0	1	↑	1	0	1	1	0	0	0	1		TCVCOM Offset Set
		1	1	↑	0	0	0	TCAVCM4	TCAVCM3	TCAVCM2	TCAVCM1	TCAVCM0	00	
		1	1	↑	0	0	0	TCBVCM4	TCBVCM3	TCBVCM2	TCBVCM1	TCBVCM0	00	
		1	1	↑	0	0	0	TCCVCM4	TCCVCM3	TCCVCM2	TCCVCM1	TCCVCM0	00	
		1	1	↑	0	0	0	TCDVCM4	TCDVCM3	TCDVCM2	TCDVCM1	TCDVCM0	00	
TCPWMSY	B2	0	1	↑	1	0	1	1	0	0	1	0		TC PWM Sync Offset Set
		1	1	↑	TCAPS7	TCAPS6	TCAPS5	TCAPS4	TCAPS3	TCAPS2	TCAPS1	TCAPS0	00	
		1	1	↑	TCBPS7	TCBPS6	TCBPS5	TCBPS4	TCBPS3	TCBPS2	TCBPS1	TCBPS0	00	
		1	1	↑	TCCPS7	TCCPS6	TCCPS5	TCCPS4	TCCPS3	TCCPS2	TCCPS1	TCCPS0	00	
		1	1	↑	TCDPS7	TCDPS6	TCDPS5	TCDPS4	TCDPS3	TCDPS2	TCDPS1	TCDPS0	00	
TCPWMASON	B3	0	1	↑	1	0	1	1	0	0	1	1		

		1	1	↑	TCAPAsOn7	TCAPAsOn6	TCAPAsOn5	TCAPAsOn4	TCAPAsOn3	TCAPAsOn2	TCAPAsOn1	TCAPAsOn0	00	
		1	1	↑	TCBPAsOn7	TCBPAsOn6	TCBPAsOn5	TCBPAsOn4	TCBPAsOn3	TCBPAsOn2	TCBPAsOn1	TCBPAsOn0	00	
		1	1	↑	TCCPAsOn7	TCCPAsOn6	TCCPAsOn5	TCCPAsOn4	TCCPAsOn3	TCCPAsOn2	TCCPAsOn1	TCCPAsOn0	00	
		1	1	↑	TCDPAsOn7	TCDPAsOn6	TCDPAsOn5	TCDPAsOn4	TCDPAsOn3	TCDPAsOn2	TCDPAsOn1	TCDPAsOn0	00	
TCPWMASOF	B4	0	1	↑	1	0	1	1	0	1	0	0		
		1	1	↑	TCAPAsOf7	TCAPAsOf6	TCAPAsOf5	TCAPAsOf4	TCAPAsOf3	TCAPAsOf2	TCAPAsOf1	TCAPAsOf0	00	
		1	1	↑	TCBPAsOf7	TCBPAsOf6	TCBPAsOf5	TCBPAsOf4	TCBPAsOf3	TCBPAsOf2	TCBPAsOf1	TCBPAsOf0	00	
		1	1	↑	TCCPAsOf7	TCCPAsOf6	TCCPAsOf5	TCCPAsOf4	TCCPAsOf3	TCCPAsOf2	TCCPAsOf1	TCCPAsOf0	00	
		1	1	↑	TCDPAsOf7	TCDPAsOf6	TCDPAsOf5	TCDPAsOf4	TCDPAsOf3	TCDPAsOf2	TCDPAsOf1	TCDPAsOf0	00	
TCVGH1	B5	0	1	↑	1	0	1	1	0	1	0	1		TC VGHREG Offset Set
		1	1	↑	0	TCAVGH6	TCAVGH5	TCAVGH4	TCAVGH3	TCAVGH2	TCAVGH1	TCAVGH0	00	
		1	1	↑	0	TCBVGH6	TCBVGH5	TCBVGH4	TCBVGH3	TCBVGH2	TCBVGH1	TCBVGH0	00	
		1	1	↑	0	TCCVGH6	TCCVGH5	TCCVGH4	TCCVGH3	TCCVGH2	TCCVGH1	TCCVGH0	00	
		1	1	↑	0	TCDVGH6	TCDVGH5	TCDVGH4	TCDVGH3	TCDVGH2	TCDVGH1	TCDVGH0	00	
TCVGH2	B6	0	1	↑	1	0	1	1	0	1	1	0		TC VGLREG Offset Set
		1	1	↑	TCAGlx1	TCAGlx0	TCAVGL5	TCAVGL4	TCAVGL3	TCAVGL2	TCAVGL1	TCAVGL0	00	
		1	1	↑	TCBGlx1	TCBGlx0	TCBVGL5	TCBVGL4	TCBVGL3	TCBVGL2	TCBVGL1	TCBVGL0	00	
		1	1	↑	TCCGlx1	TCCGlx0	TCCVGL5	TCCVGL4	TCCVGL3	TCCVGL2	TCCVGL1	TCCVGL0	00	
		1	1	↑	TCDGlx1	TCDGlx0	TCDVGL5	TCDVGL4	TCDVGL3	TCDVGL2	TCDVGL1	TCDVGL0	00	
TC2GPAB	B9	0	1	↑	1	0	1	1	0	1	0	1		
		1	1	↑	TCA2GP13	TCA2GP12	TCA2GP11	TCA2GP10	TCA2GP03	TCA2GP02	TCA2GP01	TCA2GP00	00	Gamma 2BPP TC Range A/B Positive polarity
		1	1	↑	TCA2GP33	TCA2GP32	TCA2GP31	TCA2GP30	TCA2GP23	TCA2GP22	TCA2GP21	TCA2GP20	00	
		1	1	↑	TCB2GP13	TCB2GP12	TCB2GP11	TCB2GP10	TCB2GP03	TCB2GP02	TCB2GP01	TCB2GP00	00	
		1	1	↑	TCB2GP33	TCB2GP32	TCB2GP31	TCB2GP30	TCB2GP23	TCB2GP22	TCB2GP21	TCB2GP20	00	
TC2GPCD	BA	0	1	↑	1	0	1	1	0	1	0	1		
		1	1	↑	TCC2GP13	TCC2GP12	TCC2GP11	TCC2GP10	TCC2GP03	TCC2GP02	TCC2GP01	TCC2GP00	00	Gamma 2BPP TC Range C/D Positive polarity
		1	1	↑	TCC2GP33	TCC2GP32	TCC2GP31	TCC2GP30	TCC2GP23	TCC2GP22	TCC2GP21	TCC2GP20	00	
		1	1	↑	TCD2GP13	TCD2GP12	TCD2GP11	TCD2GP10	TCD2GP03	TCD2GP02	TCD2GP01	TCD2GP00	00	
		1	1	↑	TCD2GP33	TCD2GP32	TCD2GP31	TCD2GP30	TCD2GP23	TCD2GP22	TCD2GP21	TCD2GP20	00	
TC2GNAB	BB	0	1	↑	1	0	1	1	0	1	0	1		Gamma 2BPP TC Range A/B Negative polarity
		1	1	↑	TCA2GN13	TCA2GN12	TCA2GN11	TCA2GN10	TCA2GN03	TCA2GN02	TCA2GN01	TCA2GN00	00	
		1	1	↑	TCA2GN33	TCA2GN32	TCA2GN31	TCA2GN30	TCA2GN23	TCA2GN22	TCA2GN21	TCA2GN20	00	
		1	1	↑	TCB2GN13	TCB2GN12	TCB2GN11	TCB2GN10	TCB2GN03	TCB2GN02	TCB2GN01	TCB2GN00	00	
		1	1	↑	TCB2GN33	TCB2GN32	TCB2GN31	TCB2GN30	TCB2GN23	TCB2GN22	TCB2GN21	TCB2GN20	00	
TC2GNCD	BC	0	1	↑	1	0	1	1	0	1	0	1		Gamma 2BPP TC Range C/D Negative polarity
		1	1	↑	TCC2GN13	TCC2GN12	TCC2GN11	TCC2GN10	TCC2GN03	TCC2GN02	TCC2GN01	TCC2GN00	00	
		1	1	↑	TCC2GN33	TCC2GN32	TCC2GN31	TCC2GN30	TCC2GN23	TCC2GN22	TCC2GN21	TCC2GN20	00	
		1	1	↑	TCD2GN13	TCD2GN12	TCD2GN11	TCD2GN10	TCD2GN03	TCD2GN02	TCD2GN01	TCD2GN00	00	
		1	1	↑	TCD2GN33	TCD2GN32	TCD2GN31	TCD2GN30	TCD2GN23	TCD2GN22	TCD2GN21	TCD2GN20	00	
TC1GP	BD	0	1	↑	1	0	1	1	0	1	0	1		Gamma 1BPP TC Range A/B/C/D Positive polarity
		1	1	↑	TCA1GP13	TCA1GP12	TCA1GP11	TCA1GP10	TCA1GP03	TCA1GP02	TCA1GP01	TCA1GP00	00	
		1	1	↑	TCB1GP13	TCB1GP12	TCB1GP11	TCB1GP10	TCB1GP03	TCB1GP02	TCB1GP01	TCB1GP00	00	
		1	1	↑	TCC1GP13	TCC1GP12	TCC1GP11	TCC1GP10	TCC1GP03	TCC1GP02	TCC1GP01	TCC1GP00	00	
		1	1	↑	TCD1GP13	TCD1GP12	TCD1GP11	TCD1GP10	TCD1GP03	TCD1GP02	TCD1GP01	TCD1GP00	00	
TC1GN	BE	0	1	↑	1	0	1	1	0	1	0	1		Gamma 1BPP

		1	1	↑	TCA1GN13	TCA1GN12	TCA1GN11	TCA1GN10	TCA1GN03	TCA1GN02	TCA1GN01	TCA1GN00	00	TC Range
		1	1	↑	TCB1GN13	TCB1GN12	TCB1GN11	TCB1GN10	TCB1GN03	TCB1GN02	TCB1GN01	TCB1GN00	00	A/B/C/D
		1	1	↑	TCC1GN13	TCC1GN12	TCC1GN11	TCC1GN10	TCC1GN03	TCC1GN02	TCC1GN01	TCC1GN00	00	Negative
		1	1	↑	TCD1GN13	TCD1GN12	TCD1GN11	TCD1GN10	TCD1GN03	TCD1GN02	TCD1GN01	TCD1GN00	00	polarity
SETTCGVD1	C1	0	1	↑	1	1	0	0	0	0	0	1		
		1	1	↑	MTGVD03	MTGVD02	MTGVD01	MTGVD00	0	0	0	0	00	Set GVDD TC
		1	1	↑	MTGVD23	MTGVD22	MTGVD21	MTGVD20	MTGVD13	MTGVD12	MTGVD11	MTGVD10	00	Gradient
		1	1	↑	MTGVD43	MTGVD42	MTGVD41	MTGVD40	MTGVD33	MTGVD32	MTGVD31	MTGVD30	00	Curves1
		1	1	↑	MTGVD63	MTGVD62	MTGVD61	MTGVD60	MTGVD53	MTGVD52	MTGVD51	MTGVD50	00	
SETTCGVD2	C2	0	1	↑	1	1	0	0	0	0	1	0		
		1	1	↑	MTGVD83	MTGVD82	MTGVD81	MTGVD80	MTGVD73	MTGVD72	MTGVD71	MTGVD70	00	Set GVDD TC
		1	1	↑	MTGVDA3	MTGVDA2	MTGVDA1	MTGVDA0	MTGVD93	MTGVD92	MTGVD91	MTGVD90	00	Gradient
		1	1	↑	MTGVDC3	MTGVDC2	MTGVDC1	MTGVDC0	MTGVDB3	MTGVDB2	MTGVDB1	MTGVDB0	00	Curves2
		1	1	↑	0	0	0	0	MTGVDD3	MTGVDD2	MTGVDD1	MTGVDD0	00	
SETTCGVD3	C3	0	1	↑	1	1	0	0	0	0	1	1		
		1	1	↑	0	0	0	0	0	0	0	0	00	Set GVDD TC
		1	1	↑	0	0	THGVD5	THGVD4	THGVD3	THGVD2	THGVD1	THGVD0	00	Gradient
		1	1	↑	1	0	1	0	0	1	0	1		Curves3
		1	1	↑	1	0	1	0	0	1	0	1		
SETTCGVC1	C4	0	1	↑	1	1	0	0	0	1	0	0		
		1	1	↑	MTGVC03	MTGVC02	MTGVC01	MTGVC00	0	0	0	0	00	Set GVCL TC
		1	1	↑	MTGVC23	MTGVC22	MTGVC21	MTGVC20	MTGVC13	MTGVC12	MTGVC11	MTGVC10	00	Gradient
		1	1	↑	MTGVC43	MTGVC42	MTGVC41	MTGVC40	MTGVC33	MTGVC32	MTGVC31	MTGVC30	00	Curves1
		1	1	↑	MTGVC63	MTGVC62	MTGVC61	MTGVC60	MTGVC53	MTGVC52	MTGVC51	MTGVC50	00	
SETTCGVC2	C5	0	1	↑	1	1	0	0	0	1	0	1		
		1	1	↑	MTGVC83	MTGVC82	MTGVC81	MTGVC80	MTGVC73	MTGVC72	MTGVC71	MTGVC70	00	Set GVCL TC
		1	1	↑	MTGVCA3	MTGVCA2	MTGVCA1	MTGVCA0	MTGVC93	MTGVC92	MTGVC91	MTGVC90	00	Gradient
		1	1	↑	MTGVCC3	MTGVCC2	MTGVCC1	MTGVCC0	MTGVCB3	MTGVCB2	MTGVCB1	MTGVCB0	00	Curves2
		1	1	↑	0	0	0	0	MTGVCD3	MTGVCD2	MTGVCD1	MTGVCD0	00	
SETTCGVC3	C6	0	1	↑	1	1	0	0	0	1	1	0		
		1	1	↑	0	0	0	0	0	0	0	0	00	Set GVCL TC
		1	1	↑	1	0	1	0	0	1	0	1		Gradient
		1	1	↑	1	0	1	0	0	1	0	1		Curves3
		1	1	↑	1	0	1	0	0	1	0	1		
SETTCVGH	C7	0	1	↑	1	1	0	0	0	1	1	1		
		1	1	↑	TAVGH7	TAVGH6	TAVGH5	TAVGH4	TAVGH3	TAVGH2	TAVGH1	TAVGH0	00	Set TC VGH
		1	1	↑	TBVGH7	TBVGH6	TBVGH5	TBVGH4	TBVGH3	TBVGH2	TBVGH1	TBVGH0	00	Flag
		1	1	↑	TCVGH7	TCVGH6	TCVGH5	TCVGH4	TCVGH3	TCVGH2	TCVGH1	TCVGH0	00	
		1	1	↑	0	0	0	0	THVGH3	THVGH2	THVGH1	THVGH0	00	
SETTCVCOM	C8	0	1	↑	1	1	0	0	1	0	0	0		
		1	1	↑	0	TAVCOM6	TAVCOM5	TAVCOM4	TAVCOM3	TAVCOM2	TAVCOM1	TAVCOM0	00	Set TC VCOM
		1	1	↑	0	TBVCOM6	TBVCOM5	TBVCOM4	TBVCOM3	TBVCOM2	TBVCOM1	TBVCOM0	00	Flag
		1	1	↑	0	TCVCOM6	TCVCOM5	TCVCOM4	TCVCOM3	TCVCOM2	TCVCOM1	TCVCOM0	00	
		1	1	↑	0	0	0	0	THVCOM3	THVCOM2	THVCOM1	THVCOM0	00	
SETTCFRM	C9	0	1	↑	1	1	0	0	1	0	0	1		Set TC FRC

		1	1	↑	0	TAFRM6	TAFRM5	TAFRM4	TAFRM3	TAFRM2	TAFRM1	TAFRM0	00	Flag
		1	1	↑	0	TBFRM6	TBFRM5	TBFRM4	TBFRM3	TBFRM2	TBFRM1	TBFRM0	00	
		1	1	↑	0	TCFRM6	TCFRM5	TCFRM4	TCFRM3	TCFRM2	TCFRM1	TCFRM0	00	
		1	1	↑	0	0	0	0	THFRM3	THFRM2	THFRM1	THFRM0	00	
SETTCGMA	CA	0	1	↑	1	1	0	0	1	0	1	0		Set TC Gamma Flag
		1	1	↑	0	TAGMA6	TAGMA5	TAGMA4	TAGMA3	TAGMA2	TAGMA1	TAGMA0	00	
		1	1	↑	0	TBGMA6	TBGMA5	TBGMA4	TBGMA3	TBGMA2	TBGMA1	TBGMA0	00	
		1	1	↑	0	TCGMA6	TCGMA5	TCGMA4	TCGMA3	TCGMA2	TCGMA1	TCGMA0	00	
		1	1	↑	0	0	0	0	THGMA3	THGMA2	THGMA1	THGMA0	00	
SETTCPWM	CB	0	1	↑	1	1	0	0	1	0	1	1		Set TC PWM Flag
		1	1	↑	0	TAPWM6	TAPWM5	TAPWM4	TAPWM3	TAPWM2	TAPWM1	TAPWM0	00	
		1	1	↑	0	TBPWM6	TBPWM5	TBPWM4	TBPWM3	TBPWM2	TBPWM1	TBPWM0	00	
		1	1	↑	0	TCPWM6	TCPWM5	TCPWM4	TCPWM3	TCPWM2	TCPWM1	TCPWM0	00	
		1	1	↑	0	0	0	0	THPWM3	THPWM2	THPWM1	THPWM0	00	
TCFP	CC	0	1	↑	1	1	0	0	1	1	0	0		Front Porch of Frame Rate TC Range Setting
		1	1	↑	TCAFP7	TCAFP6	TCAFP5	TCAFP4	TCAFP3	TCAFP2	TCAFP1	TCAFP0	00	
		1	1	↑	TCBFP7	TCBFP6	TCBFP5	TCBFP4	TCBFP3	TCBFP2	TCBFP1	TCBFP0	00	
		1	1	↑	TCCFP7	TCCFP6	TCCFP5	TCCFP4	TCCFP3	TCCFP2	TCCFP1	TCCFP0	00	
		1	1	↑	TCDFP7	TCDFP6	TCDFP5	TCDFP4	TCDFP3	TCDFP2	TCDFP1	TCDFP0	00	
TC1H	CD	0	1	↑	1	1	0	0	1	1	0	1		1H of Frame Rate TC Range Setting
		1	1	↑	TCAGLW7	TCAGLW6	TCAGLW5	TCAGLW4	TCAGLW3	TCAGLW2	TCAGLW1	TCAGLW0	00	
		1	1	↑	TCBGLW7	TCBGLW6	TCBGLW5	TCBGLW4	TCBGLW3	TCBGLW2	TCBGLW1	TCBGLW0	00	
		1	1	↑	TCCGLW7	TCCGLW6	TCCGLW5	TCCGLW4	TCCGLW3	TCCGLW2	TCCGLW1	TCCGLW0	00	
		1	1	↑	TCDGLW7	TCDGLW6	TCDGLW5	TCDGLW4	TCDGLW3	TCDGLW2	TCDGLW1	TCDGLW0	00	
TCBP	CE	0	1	↑	1	1	0	0	1	1	1	0		Back Porch of Frame Rate TC Range Setting
		1	1	↑	TCABP7	TCABP6	TCABP5	TCABP4	TCABP3	TCABP2	TCABP1	TCABP0	00	
		1	1	↑	TCBBP7	TCBBP6	TCBBP5	TCBBP4	TCBBP3	TCBBP2	TCBBP1	TCBBP0	00	
		1	1	↑	TCCBP7	TCCBP6	TCCBP5	TCCBP4	TCCBP3	TCCBP2	TCCBP1	TCCBP0	00	
		1	1	↑	F	TCDBP6	TCDBP5	TCDBP4	TCDBP3	TCDBP2	TCDBP1	TCDBP0	00	
TC4GPA1	D0	0	1	↑	1	1	0	1	0	0	0	0		Gamma 4BPP TC Range A Positive polarity
		1	1	↑	TCA4GP13	TCA4GP12	TCA4GP11	TCA4GP10	TCA4GP03	TCA4GP02	TCA4GP01	TCA4GP00	00	
		1	1	↑	TCA4GP33	TCA4GP32	TCA4GP31	TCA4GP30	TCA4GP23	TCA4GP22	TCA4GP21	TCA4GP20	00	
		1	1	↑	TCA4GP53	TCA4GP52	TCA4GP51	TCA4GP50	TCA4GP43	TCA4GP42	TCA4GP41	TCA4GP40	00	
		1	1	↑	TCA4GP73	TCA4GP72	TCA4GP71	TCA4GP70	TCA4GP63	TCA4GP62	TCA4GP61	TCA4GP60	00	
TC4GPA2	D1	0	1	↑	1	1	0	1	0	0	0	1		Gamma 4BPP TC Range A Positive polarity
		1	1	↑	TCA4GP93	TCA4GP92	TCA4GP91	TCA4GP90	TCA4GP83	TCA4GP82	TCA4GP81	TCA4GP80	00	
		1	1	↑	TCA4GPB3	TCA4GPB2	TCA4GPB1	TCA4GPB0	TCA4GPA3	TCA4GPA2	TCA4GPA1	TCA4GPA0	00	
		1	1	↑	TCA4GPD3	TCA4GPD2	TCA4GPD1	TCA4GPD0	TCA4GPC3	TCA4GPC2	TCA4GPC1	TCA4GPC0	00	
		1	1	↑	TCA4GPF3	TCA4GPF2	TCA4GPF1	TCA4GPF0	TCA4GPE3	TCA4GPE2	TCA4GPE1	TCA4GPE0	00	
TC4GNA1	D2	0	1	↑	1	1	0	1	0	0	1	0		Gamma 4BPP TC Range A Negative polarity
		1	1	↑	TCA4GN13	TCA4GN12	TCA4GN11	TCA4GN10	TCA4GN03	TCA4GN02	TCA4GN01	TCA4GN00	00	
		1	1	↑	TCA4GN33	TCA4GN32	TCA4GN31	TCA4GN30	TCA4GN23	TCA4GN22	TCA4GN21	TCA4GN20	00	
		1	1	↑	TCA4GN53	TCA4GN52	TCA4GN51	TCA4GN50	TCA4GN43	TCA4GN42	TCA4GN41	TCA4GN40	00	
		1	1	↑	TCA4GN73	TCA4GN72	TCA4GN71	TCA4GN70	TCA4GN63	TCA4GN62	TCA4GN61	TCA4GN60	00	
TC4GNA2	D3	0	1	↑	1	1	0	1	0	0	1	1		Gamma 4BPP

		1	1	↑	TCA4GN93	TCA4GN92	TCA4GN91	TCA4GN90	TCA4GN83	TCA4GN82	TCA4GN81	TCA4GN80	00	TC Range A
		1	1	↑	TCA4GNB3	TCA4GNB2	TCA4GNB1	TCA4GNB0	TCA4GNA3	TCA4GNA2	TCA4GNA1	TCA4GNA0	00	Negative
		1	1	↑	TCA4GND3	TCA4GND2	TCA4GND1	TCA4GND0	TCA4GNC3	TCA4GNC2	TCA4GNC1	TCA4GNC0	00	polarity
		1	1	↑	TCA4GNF3	TCA4GNF2	TCA4GNF1	TCA4GNF0	TCA4GNE3	TCA4GNE2	TCA4GNE1	TCA4GNE0	00	
TC4GPB1	D4	0	1	↑	1	1	0	1	0	1	0	0		
		1	1	↑	TCB4GP13	TCB4GP12	TCB4GP11	TCB4GP10	TCB4GP03	TCB4GP02	TCB4GP01	TCB4GP00	00	Gamma 4BPP
		1	1	↑	TCB4GP33	TCB4GP32	TCB4GP31	TCB4GP30	TCB4GP23	TCB4GP22	TCB4GP21	TCB4GP20	00	TC Range B
		1	1	↑	TCB4GP53	TCB4GP52	TCB4GP51	TCB4GP50	TCB4GP43	TCB4GP42	TCB4GP41	TCB4GP40	00	Positive polarity
		1	1	↑	TCB4GP73	TCB4GP72	TCB4GP71	TCB4GP70	TCB4GP63	TCB4GP62	TCB4GP61	TCB4GP60	00	
TC4GPB2	D5	0	1	↑	1	1	0	1	0	1	0	1		
		1	1	↑	TCB4GP93	TCB4GP92	TCB4GP91	TCB4GP90	TCB4GP83	TCB4GP82	TCB4GP81	TCB4GP80	00	Gamma 4BPP
		1	1	↑	TCB4GPB3	TCB4GPB2	TCB4GPB1	TCB4GPB0	TCB4GPA3	TCB4GPA2	TCB4GPA1	TCB4GPA0	00	TC Range B
		1	1	↑	TCB4GPD3	TCB4GPD2	TCB4GPD1	TCB4GPD0	TCB4GPC3	TCB4GPC2	TCB4GPC1	TCB4GPC0	00	Positive polarity
		1	1	↑	TCB4GPF3	TCB4GPF2	TCB4GPF1	TCB4GPF0	TCB4GPE3	TCB4GPE2	TCB4GPE1	TCB4GPE0	00	
TC4GNB1	D6	0	1	↑	1	1	0	1	0	1	1	0		
		1	1	↑	TCB4GN13	TCB4GN12	TCB4GN11	TCB4GN10	TCB4GN03	TCB4GN02	TCB4GN01	TCB4GN00	00	Gamma 4BPP
		1	1	↑	TCB4GN33	TCB4GN32	TCB4GN31	TCB4GN30	TCB4GN23	TCB4GN22	TCB4GN21	TCB4GN20	00	TC Range B
		1	1	↑	TCB4GN53	TCB4GN52	TCB4GN51	TCB4GN50	TCB4GN43	TCB4GN42	TCB4GN41	TCB4GN40	00	Negative
		1	1	↑	TCB4GN73	TCB4GN72	TCB4GN71	TCB4GN70	TCB4GN63	TCB4GN62	TCB4GN61	TCB4GN60	00	polarity
TC4GNB2	D7	0	1	↑	1	1	0	1	0	1	1	1		
		1	1	↑	TCB4GN93	TCB4GN92	TCB4GN91	TCB4GN90	TCB4GN83	TCB4GN82	TCB4GN81	TCB4GN80	00	Gamma 4BPP
		1	1	↑	TCB4GNB3	TCB4GNB2	TCB4GNB1	TCB4GNB0	TCB4GNA3	TCB4GNA2	TCB4GNA1	TCB4GNA0	00	TC Range B
		1	1	↑	TCB4GND3	TCB4GND2	TCB4GND1	TCB4GND0	TCB4GNC3	TCB4GNC2	TCB4GNC1	TCB4GNC0	00	Negative
		1	1	↑	TCB4GNF3	TCB4GNF2	TCB4GNF1	TCB4GNF0	TCB4GNE3	TCB4GNE2	TCB4GNE1	TCB4GNE0	00	polarity
TC4GPC1	D8	0	1	↑	1	1	0	1	1	0	0	0		
		1	1	↑	TCC4GP13	TCC4GP12	TCC4GP11	TCC4GP10	TCC4GP03	TCC4GP02	TCC4GP01	TCC4GP00	00	Gamma 4BPP
		1	1	↑	TCC4GP33	TCC4GP32	TCC4GP31	TCC4GP30	TCC4GP23	TCC4GP22	TCC4GP21	TCC4GP20	00	TC Range C
		1	1	↑	TCC4GP53	TCC4GP52	TCC4GP51	TCC4GP50	TCC4GP43	TCC4GP42	TCC4GP41	TCC4GP40	00	Positive polarity
		1	1	↑	TCC4GP73	TCC4GP72	TCC4GP71	TCC4GP70	TCC4GP63	TCC4GP62	TCC4GP61	TCC4GP60	00	
TC4GPC2	D9	0	1	↑	1	1	0	1	1	0	0	1		
		1	1	↑	TCC4GP93	TCC4GP92	TCC4GP91	TCC4GP90	TCC4GP83	TCC4GP82	TCC4GP81	TCC4GP80	00	Gamma 4BPP
		1	1	↑	TCC4GPB3	TCC4GPB2	TCC4GPB1	TCC4GPB0	TCC4GPA3	TCC4GPA2	TCC4GPA1	TCC4GPA0	00	TC Range C
		1	1	↑	TCC4GPD3	TCC4GPD2	TCC4GPD1	TCC4GPD0	TCC4GPC3	TCC4GPC2	TCC4GPC1	TCC4GPC0	00	Positive polarity
		1	1	↑	TCC4GPF3	TCC4GPF2	TCC4GPF1	TCC4GPF0	TCC4GPE3	TCC4GPE2	TCC4GPE1	TCC4GPE0	00	
TC4GNC1	DA	0	1	↑	1	1	0	1	1	0	1	0		
		1	1	↑	TCC4GN13	TCC4GN12	TCC4GN11	TCC4GN10	TCC4GN03	TCC4GN02	TCC4GN01	TCC4GN00	00	Gamma 4BPP
		1	1	↑	TCC4GN33	TCC4GN32	TCC4GN31	TCC4GN30	TCC4GN23	TCC4GN22	TCC4GN21	TCC4GN20	00	TC Range C
		1	1	↑	TCC4GN53	TCC4GN52	TCC4GN51	TCC4GN50	TCC4GN43	TCC4GN42	TCC4GN41	TCC4GN40	00	Negative
		1	1	↑	TCC4GN73	TCC4GN72	TCC4GN71	TCC4GN70	TCC4GN63	TCC4GN62	TCC4GN61	TCC4GN60	00	polarity
TC4GNC2	DB	0	1	↑	1	1	0	1	1	0	1	1		
		1	1	↑	TCC4GN93	TCC4GN92	TCC4GN91	TCC4GN90	TCC4GN83	TCC4GN82	TCC4GN81	TCC4GN80	00	Gamma 4BPP
		1	1	↑	TCC4GNB3	TCC4GNB2	TCC4GNB1	TCC4GNB0	TCC4GNA3	TCC4GNA2	TCC4GNA1	TCC4GNA0	00	TC Range C
		1	1	↑	TCC4GND3	TCC4GND2	TCC4GND1	TCC4GND0	TCC4GNC3	TCC4GNC2	TCC4GNC1	TCC4GNC0	00	Negative
		1	1	↑	TCC4GNF3	TCC4GNF2	TCC4GNF1	TCC4GNF0	TCC4GNE3	TCC4GNE2	TCC4GNE1	TCC4GNE0	00	polarity
TC4GPD1	DC	0	1	↑	1	1	0	1	1	1	0	0		Gamma 4BPP

		1	1	↑	TCD4GP13	TCD4GP12	TCD4GP11	TCD4GP10	TCD4GP03	TCD4GP02	TCD4GP01	TCD4GP00	00	TC Range D
		1	1	↑	TCD4GP33	TCD4GP32	TCD4GP31	TCD4GP30	TCD4GP23	TCD4GP22	TCD4GP21	TCD4GP20	00	Positive polarity
		1	1	↑	TCD4GP53	TCD4GP52	TCD4GP51	TCD4GP50	TCD4GP43	TCD4GP42	TCD4GP41	TCD4GP40	00	
		1	1	↑	TCD4GP73	TCD4GP72	TCD4GP71	TCD4GP70	TCD4GP63	TCD4GP62	TCD4GP61	TCD4GP60	00	
TC4GPD2	DD	0	1	↑	1	1	0	1	1	1	0	1		Gamma 4BPP TC Range D Positive polarity
		1	1	↑	TCD4GP93	TCD4GP92	TCD4GP91	TCD4GP90	TCD4GP83	TCD4GP82	TCD4GP81	TCD4GP80	00	
		1	1	↑	TCD4GPB3	TCD4GPB2	TCD4GPB1	TCD4GPB0	TCD4GPA3	TCD4GPA2	TCD4GPA1	TCD4GPA0	00	
		1	1	↑	TCD4GPD3	TCD4GPD2	TCD4GPD1	TCD4GPD0	TCD4GPC3	TCD4GPC2	TCD4GPC1	TCD4GPC0	00	
		1	1	↑	TCD4GPF3	TCD4GPF2	TCD4GPF1	TCD4GPF0	TCD4GPE3	TCD4GPE2	TCD4GPE1	TCD4GPE0	00	
TC4GND1	DE	0	1	↑	1	1	0	1	1	1	1	0		Gamma 4BPP TC Range D Negative polarity
		1	1	↑	TCD4GN13	TCD4GN12	TCD4GN11	TCD4GN10	TCD4GN03	TCD4GN02	TCD4GN01	TCD4GN00	00	
		1	1	↑	TCD4GN33	TCD4GN32	TCD4GN31	TCD4GN30	TCD4GN23	TCD4GN22	TCD4GN21	TCD4GN20	00	
		1	1	↑	TCD4GN53	TCD4GN52	TCD4GN51	TCD4GN50	TCD4GN43	TCD4GN42	TCD4GN41	TCD4GN40	00	
		1	1	↑	TCD4GN73	TCD4GN72	TCD4GN71	TCD4GN70	TCD4GN63	TCD4GN62	TCD4GN61	TCD4GN60	00	
TC4GND2	DF	0	1	↑	1	1	0	1	1	1	1	1		Gamma 4BPP TC Range D Negative polarity
		1	1	↑	TCD4GN93	TCD4GN92	TCD4GN91	TCD4GN90	TCD4GN83	TCD4GN82	TCD4GN81	TCD4GN80	00	
		1	1	↑	TCD4GNB3	TCD4GNB2	TCD4GNB1	TCD4GNB0	TCD4GNA3	TCD4GNA2	TCD4GNA1	TCD4GNA0	00	
		1	1	↑	TCD4GND3	TCD4GND2	TCD4GND1	TCD4GND0	TCD4GNC3	TCD4GNC2	TCD4GNC1	TCD4GNC0	00	
		1	1	↑	TCD4GNF3	TCD4GNF2	TCD4GNF1	TCD4GNF0	TCD4GNE3	TCD4GNE2	TCD4GNE1	TCD4GNE0	00	
TOSC	F4	0	1	↑	1	1	1	1	0	1	0	0		Command for MTP Autoload Control
		1	1	↑	0	0	0	0	0	0	0	0	00	
		1	1	↑	0	1	1	0	0	1	1	1	67	
		1	1	↑	1	1	1	MTPAuto	1	1	1	0	FE	
		1	1	↑	1	1	1	0	1	0	1	0	EA	
TCSET	F6	0	1	↑	1	1	1	1	0	1	1	0		Command for TC Temperature Control
		1	1	↑	0	0	0	0	TSON	TCSEL	0	0	00	
		1	1	↑	0	0	0	0	0	0	0	0	00	
		1	1	↑	0	0	0	0	0	0	0	0	00	
		1	1	↑	0	0	1	0	0	0	0	1	21	

7.2 Command Description

7.2.1 Non-Operation

00H	Non-Operation											
Ins./Par.	**A1**	**ERD**	**RWR**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**HEX**
NOP	0	1	↑	0	0	0	0	0	0	0	0	00
1st parameter	1	1	↑	1	0	1	0	0	1	0	1	A5
Description	▪ Non-operation. This command does not affect any operation.											

7.2.2 Sleep Out

12H	Sleep out											
Ins./Par.	**A1**	**ERD**	**RWR**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**HEX**
SLPOUT	0	1	↑	0	0	0	1	0	0	1	0	12
1st parameter	1	1	↑	1	0	1	0	0	1	0	1	A5
Description	▪ It is required hardware reset at power-on. ▪ **It is always required to input this command after hardware reset.**											

7.2.3 Sleep In

13H	Sleep in											
Ins./Par.	**A1**	**ERD**	**RWR**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**HEX**
SLPIN	0	1	↑	0	0	0	1	0	0	1	1	13
1st parameter	1	1	↑	1	0	1	0	0	1	0	1	A5
Description	▪ It is required Hardware reset at power-on reset. ▪ **It is always required to input this command after hardware reset.**											

7.2.4 Display Off

14H	Display off											
Ins./Par.	**A1**	**ERD**	**RWR**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**HEX**
DISOFF	0	1	↑	0	0	0	1	0	1	0	0	14
1st parameter	1	1	↑	1	0	1	0	0	1	0	1	A5
Description	▪ Display off.											

7.2.5 Display On

15H	Display on											
Ins./Par.	**A1**	**ERD**	**RWR**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**HEX**
DISON	0	1	↑	0	0	0	1	0	1	0	1	15
1st parameter	1	1	↑	1	0	1	0	0	1	0	1	A5
Description	▪ Start to display. ▪ SLPOUT command must be input before this command. ▪ After SLPOUT command, DISON command is waited until “display possible state” and this command is executed after wait time set by PWRCTL command.											

7.2.6 Display Invert Out

1AH	Display Invert out											
Ins./Par.	**A1**	**ERD**	**RWR**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**HEX**
DINVIN	0	1	↑	0	0	0	1	1	0	1	0	1A
1st parameter	1	1	↑	1	0	1	0	0	1	0	1	A5
Description	▪ Quit from display inverting state. ▪ It is enabled next frame after receiving the command.											

7.2.7 Display Invert In

1BH	Display Invert in											
Ins./Par.	**A1**	**ERD**	**RWR**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**HEX**
DINVIN	0	1	↑	0	0	0	1	1	0	1	1	1B
1st parameter	1	1	↑	1	0	1	0	0	1	0	1	A5
Description	▪ Inverts Display without re-writing display RAM. ▪ It is enabled next frame after receiving the command.											

7.2.8 Blinking Out

1CH	Blinking out											
Ins./Par.	**A1**	**ERD**	**RWR**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**HEX**
BLOUT	0	1	↑	0	0	0	1	1	1	0	0	1C
1st parameter	1	1	↑	1	0	1	0	0	1	0	1	A5
Description	▪ Exit blinking display state. ▪ Frame address after exit is address set by 7.3.10 STFRAME command. ▪ It is enable at frame changing of blinking cycle after the command. **▪ When WRRAM command is input after BLOUT, 2 NOP commands must be required before WRRAM.**											

7.2.9 Blinking In

1DH	Blinking in											
Ins./Par.	**A1**	**ERD**	**RWR**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**HEX**
BLIN	0	1	↑	0	0	0	1	1	1	0	1	1D
1st parameter	1	1	↑	1	0	1	0	0	1	0	1	A5
Description	▪ This command is used for blinking display by changing frame address. ▪ The blinking state is set by BLSET command. ▪ It is enable in next frame of the command input. ▪ During executing this command, RAM writing is invalid. ▪ In 1bpp mode with 4frames, other frames that is used by this command are valid to write RAM.											

7.2.10 Start Frame Address

21H	Start Frame Address											
Ins./Par.	**A1**	**ERD**	**RWR**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**HEX**
STFRAME	0	1	↑	0	0	1	0	0	0	0	1	21
1st parameter	1	1	↑	0	0	0	0	0	0	SFrmA1	SFrmA0	00
2nd parameter	1	1	↑	1	0	1	0	0	1	0	1	A5
3rd parameter	1	1	↑	1	0	1	0	0	1	0	1	A5
4th parameter	1	1	↑	1	0	1	0	0	1	0	1	A5
Description	▪ Set frame address. ▪ SFrmA: Set start frame address											

7.2.11 BPP Select

22H	BPP Selection											
Ins./Par.	**A1**	**ERD**	**RWR**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**HEX**
BPPSEL	0	1	↑	0	0	1	0	0	0	1	0	22
1st parameter	1	1	↑	0	0	0	0	0	0	BppSel1	BppSel0	02
2nd parameter	1	1	↑	1	0	1	0	0	1	0	1	A5
3rd parameter	1	1	↑	1	0	1	0	0	1	0	1	A5
4th parameter	1	1	↑	1	0	1	0	0	1	0	1	A5
Description	▪ Set data format (bit per pixel) ▪ It is enabled next frame after receiving the command. ▪ It is possible to change 4bpp / 2bpp / 1bpp. ▪ **It must be input during display off state, and display data must be written after changing** ▪ BppSel[1:0] : Set data format (bit per pixel) 00: 1bpp (2 gray scale) 01: 2bpp (4 gray scale) 10: 4bpp (16 gray scale)											

7.2.12 Memory Address Control

24H	Memory Address Control											
Ins./Par.	**A1**	**ERD**	**RWR**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**HEX**
MADCTL	0	1	↑	0	0	1	0	0	1	0	0	24
1st parameter	1	1	↑	0	0	0	0	0	MV	MY	MX	00
2nd parameter	1	1	↑	1	0	1	0	0	1	0	1	A5
3rd parameter	1	1	↑	1	0	1	0	0	1	0	1	A5
4th parameter	1	1	↑	1	0	1	0	0	1	0	1	A5
Description	▪ Set about display data RAM. ▪ To access display RAM, it is required 1ms or more wait after input this command. ▪ MV: Select address incremental direction.(refer to 6.2.3) 0: Incremental column addr. 1: Incremental page addr. ▪ MY: Display data RAM page address (refer to 6.2.3) 0: Normal 1: Reverse ▪ MX: Display data RAM column address (refer to 6.2.3) 0: Normal 1: Reverse											

7.2.13 Page Address Set

25H	Page Address Set											
Ins./Par.	**A1**	**ERD**	**RWR**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**HEX**
PASET	0	1	↑	0	0	1	0	0	1	0	1	25
1st parameter	1	1	↑	PSA7	PSA6	PSA5	PSA4	PSA3	PSA2	PSA1	PSA0	00
2nd parameter	1	1	↑	PEA7	PEA6	PEA5	PEA4	PEA3	PEA2	PEA1	PEA0	9F
3rd parameter	1	1	↑	0	0	0	0	0	0	FrmA1	FrmA0	00
4th parameter	1	1	↑	1	0	1	0	0	1	0	1	A5
Description	▪ Set page start address and page end address of display data RAM. ▪ PSA: Set page START address ▪ PEA: Set page END address ▪ FrmA: Set frame address ▪ Frame address range set by PASET command is depend on setting of BPPSEL command ▪ **PSA < PEA**											

7.2.14 Column Address Set

26H	Column Address Set											
Ins./Par.	**A1**	**ERD**	**RWR**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**HEX**
CASET	0	1	↑	0	0	1	0	0	1	1	0	26
1st parameter	1	1	↑	0	0	0	0	0	0	CSA9	CSA8	00
2nd parameter	1	1	↑	CSA7	CSA6	CSA5	CSA4	CSA3	CSA2	CSA1	CSA0	00
3rd parameter	1	1	↑	0	0	0	0	0	0	CEA9	CEA8	02
4th parameter	1	1	↑	CEA7	CEA6	CEA5	CEA4	CEA3	CEA2	CEA1	CEA0	7F
Description	▪ Set column start address and column end address of display data RAM. ▪ CSA: Set column START address ▪ CEA: Set column END address ▪ **CSA < CEA**											

7.2.15 Block Fill

29H	Block Fill											
Ins./Par.	**A1**	**ERD**	**RWR**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**HEX**
BLKFIL	0	1	↑	0	0	1	0	1	0	0	1	29
1st parameter	1	1	↑	0	0	0	0	BFData3	BFData2	BFData1	BFData0	00
2nd parameter	1	1	↑	1	0	1	0	0	1	0	1	A5
3rd parameter	1	1	↑	1	0	1	0	0	1	0	1	A5
4th parameter	1	1	↑	1	0	1	0	0	1	0	1	A5

Description

- Write set data to display data RAM area which set by CASET and PASET command.
- 60ms waiting time is required after BLKFIL command input.
- R23 of RDSTAT command is available to confirm display data RAM writing by BLKFIL command or not.
- During this term, prohibit DISAR, CASET, PASET, BPPSEL, WRRAM and RDRAM commands.
- When WRRAM or RDRAM command is input after BLKFIL, two NOP commands are required before
- WRRAM, RDRAM.

BFData[3:0]	4bit data	2bit data	1bit data
0h	0h	0h	0h
1h	1h	1h	1h
2h	2h	2h	0h
3h	3h	3h	1h
4h	4h	0h	0h
5h	5h	1h	1h
6h	6h	2h	0h
7h	7h	3h	1h
8h	8h	0h	0h
9h	9h	1h	1h
Ah	Ah	2h	0h
Bh	Bh	3h	1h
Ch	Ch	0h	0h
Dh	Dh	1h	1h
Eh	Eh	2h	0h
Fh	Fh	3h	1h

7.2.16 Blinking Set

2BH	Blinking Set											
Ins./Par.	**A1**	**ERD**	**RWR**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**HEX**
BLSET	0	1	↑	0	0	1	0	1	0	1	1	2B
1st parameter	1	1	↑	BlinkCyc7	BlinkCyc6	BlinkCyc5	BlinkCyc4	BlinkCyc3	BlinkCyc2	BlinkCyc1	BlinkCyc0	1D
2nd parameter	1	1	↑	0	0	0	0	B1stF1	B1stF0	B2ndF1	B2ndF0	01
3rd parameter	1	1	↑	1	0	1	0	0	1	0	1	A5
4th parameter	1	1	↑	1	0	1	0	0	1	0	1	A5

Description

- This command is used to blink display to exchange frame RAMs.
- The blinking is fixed between 1st and 2nd frame addresses in 4bpp mode (160 lines or less are used) or 2bpp mode, and blinking is set by parameter 2 in 1bpp mode.
- It is enable in next frame of the command input.
- B1stF[1:0] and B2ndF[1:0]: Select blinking frame addresses.
- If invalid frame address is selected, it is return to initial value in 4bpp and 2bpp mode.

BlinkCyc[7:0]	Blinking Period
00h	2 frame
01h	2 frame
02h	4 frame
03h	4 frame
:	:
FDh	254 frame
FEh	256 frame
FFh	256 frame

B1stF[1:0]	1st frame addr.
0h	0
1h	1
2h	2
3h	3

B2ndF[1:0]	2nd frame addr.
0h	0
1h	1
2h	2
3h	3

7.2.17 Write RAM

2CH	Write RAM											
Ins./Par.	**A1**	**ERD**	**RWR**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**HEX**
WRRAM	0	1	↑	0	0	1	0	1	1	0	0	2C
1st parameter	1	1	↑	1	0	1	0	0	1	0	1	A5
Write data	1	1	↑	Data7	Data6	Data5	Data4	Data3	Data2	Data1	Data0	
Description	▪ After this WRRAM command, data is input at display area which is set by CASET and PASET command. ▪ RAM address is incremented automatically by WR signal. ▪ Column address, page address and frame address are set to start addresses by WRRAM command input. ▪ There is no limit to input data, and it is continued to be written until next command input. ▪ When the address arrives to end address, it is return to start address.											

7.2.18 Read RAM

2DH	Read RAM											
Ins./Par.	**A1**	**ERD**	**RWR**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**HEX**
RDRAM	0	1	↑	0	0	1	0	1	1	0	1	2D
1st parameter	1	1	↑	1	0	1	0	0	1	0	1	A5
Dummy	1	↑	1	X	X	X	X	X	X	X	X	XX
Read data	1	↑	1	Data7	Data6	Data5	Data4	Data3	Data2	Data1	Data0	
Description	▪ After this RDRAM command, data is read at display area which is set by CASET and PASET command. ▪ RAM address is incremented automatically by RD signal. ▪ Column address, page address and frame address are set to start addresses by RDRAM command input. ▪ There is no limit to read data, and it is continued to be read until next command input. ▪ When the address arrives to end address, it is return to start address. ▪ During BLKFIL command, data reading by RDRAM command is cancelled.											

7.2.19 Display Area

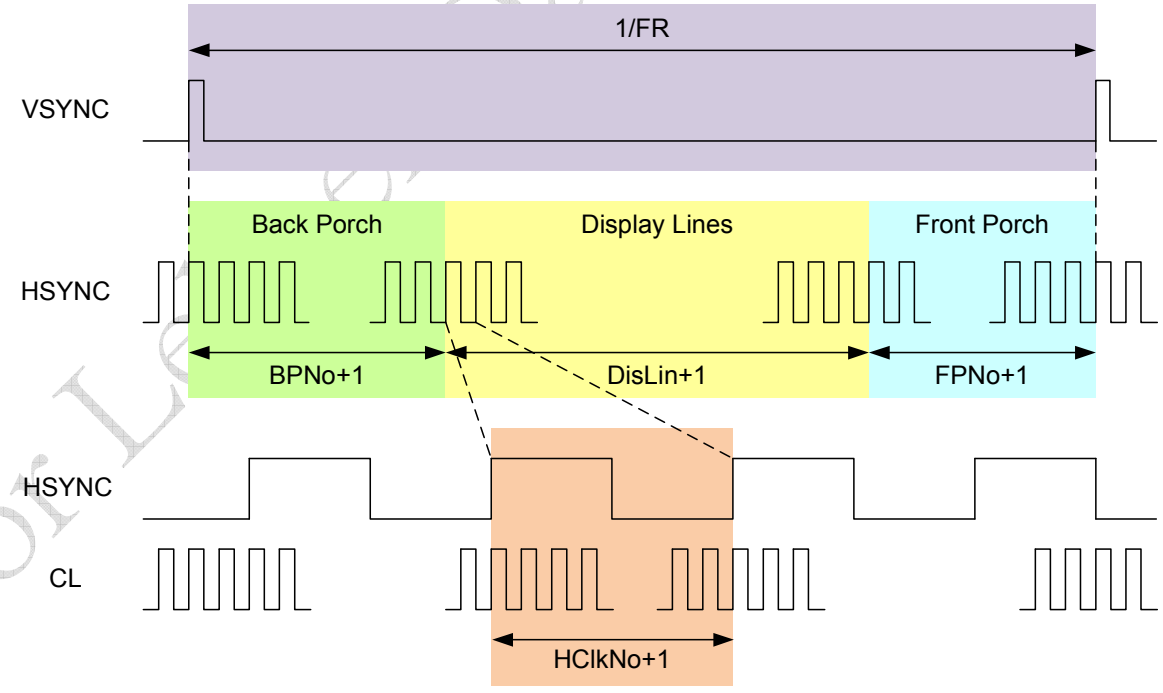
31H	Display Area											
Ins./Par.	**A1**	**ERD**	**RWR**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**HEX**
DISAR	0	1	↑	0	0	1	1	0	0	0	1	31
1st parameter	1	1	↑	0	0	0	0	0	0	0	DisLin8	01
2nd parameter	1	1	↑	DisLin7	DisLin6	DisLin5	DisLin4	DisLin3	DisLin2	DisLin1	DisLin0	3F
3rd parameter	1	1	↑	0	0	0	0	0	0	1	0	02
4th parameter	1	1	↑	0	1	1	1	1	1	I1	1	7F
Description	▪ Set display area (number of display lines, number of display columns) ▪ DisLin = number of display lines – 1 ▪ When number of display lines is decreased, porch term should be adjusted by DISET1 command to satisfy “1H =< 150us. ▪ **10 < DisLin < 320**											

7.2.20 Display Set1

32H	Display Set 1											
Ins./Par.	**A1**	**ERD**	**RWR**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**HEX**
DISSET1	0	1	↑	0	0	1	1	0	0	1	0	32
1st parameter	1	1	↑	HClkNo7	HClkNo6	HClkNo5	HClkNo4	HClkNo3	HClkNo2	HClkNo1	HClkNo0	32
2nd parameter	1	1	↑	BPNo7	BPNo6	BPNo5	BPNo4	BPNo3	BPNo2	BPNo1	BPNo0	02
3rd parameter	1	1	↑	NorBlk	OSCO	0	0	FPNo11	FPNo10	FPNo9	FPNo8	00
4th parameter	1	1	↑	FPNo7	FPNo6	FPNo5	FPNo4	FPNo3	FPNo2	FPNo1	FPNo0	01

Description

- Set display conditions
- HClkNo = number of clocks in 1H – 1
- BPNo = number of back porch – 1
- FPNo = number of front porch – 1
- NorBlk: Select LCD type
  - 0: Normally black
  - 1: Normally white
- OSCO: OSCO pin function
  - 0: VSS output
  - 1: Clock output
- Frame rate $= \frac{10^6}{(BPNo + DisLin + FPNo + 3) \cdot (HClkNo + 1)} (Hz)$



7.2.21 Display Set2

33H	Display Set 2											
Ins./Par.	**A1**	**ERD**	**RWR**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**HEX**
DISSET2	0	1	↑	0	0	1	1	0	0	1	1	33
1st parameter	1	1	↑	SOnT7	SOnT6	SOnT5	SOnT4	SOnT3	SOnT2	SOnT1	SOnT0	0A
2nd parameter	1	1	↑	SOffT7	SOffT6	SOffT5	SOffT4	SOffT3	SOffT2	SOffT1	SOffT0	28
3rd parameter	1	1	↑	GOnT7	GOnT6	GOnT5	GOnT4	GOnT3	GOnT2	GOnT1	GOnT0	0C
4th parameter	1	1	↑	GOffT7	GOffT6	GOffT5	GOffT4	GOffT3	GOffT2	GOffT1	GOffT0	26
Description	▪ Set source and gate ON/OFF timing ▪ SOnT: Set source on timing by "number of clock from start – 1" ▪ SOffT: Set source off timing by "number of clock from start – 1" ▪ GOnT: Set gate on timing by "number of clock from start – 1" ▪ GOffT: Set gate off timing by "number of clock from start – 1"											

7.2.22 Partial Set 1

34H	Partial Set 1											
Ins./Par.	**A1**	**ERD**	**RWR**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**HEX**
PTLSET1	0	1	↑	0	0	1	1	0	1	0	0	34
1st parameter	1	1	↑	0	0	0	0	0	0	0	Part1SL8	00
2nd parameter	1	1	↑	Part1SL7	Part1SL6	Part1SL5	Part1SL4	Part1SL3	Part1SL2	Part1SL1	Part1SL0	00
3rd parameter	1	1	↑	0	0	0	0	0	0	0	Part1EL8	01
4th parameter	1	1	↑	Part1EL7	Part1EL6	Part1EL5	Part1EL4	Part1EL3	Part1EL2	Part1EL1	Part1EL0	3F
Description	▪ It is used to display partially (line divided) in order to reduce power consumption. ▪ 2 display areas are settable. It is used with PTLSET2 and PTLSET3 command. ▪ 2 partial display areas are set within display lines set P1 and P2 of DISAR command. ▪ When 2nd area is not used, the start line and end line of the 2nd area must be set 511. ▪ Part1SL[8:0]: 1st partial display START line ▪ Part1EL[8:0]: 1st partial display END line **▪ When interlace is set, 1st partial display end line and 2nd partial display end line must not be set to 0, 1 and 2.**											

7.2.23 Partial Set 2

35H	Partial Set 2											
Ins./Par.	**A1**	**ERD**	**RWR**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**HEX**
PTLSET2	0	1	↑	0	0	1	1	0	1	0	1	35
1st parameter	1	1	↑	0	0	0	0	0	0	0	Part2SL8	00
2nd parameter	1	1	↑	Part2SL7	Part2SL6	Part2SL5	Part2SL4	Part2SL3	Part2SL2	Part2SL1	Part2SL0	00
3rd parameter	1	1	↑	0	0	0	0	0	0	0	Part2EL8	01
4th parameter	1	1	↑	Part2EL7	Part2EL6	Part2EL5	Part2EL4	Part2EL3	Part2EL2	Part2EL1	Part2EL0	3F
Description	▪ It is used to display partially (line divided) in order to reduce power consumption. ▪ 2 display areas are settable. It is used with PTLSET1 and PTLSET3 command.											

7.2.24 Partial Set 3

36H	Partial Set 3											
Ins./Par.	**A1**	**ERD**	**RWR**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**HEX**
PTLSET3	0	1	↑	0	0	1	1	0	1	1	0	36
1st parameter	1	1	↑	0	NDisRefR6	NDisRefR5	NDisRefR4	NDisRefR3	NDisRefR2	NDisRefR1	NDisRefR0	00
2nd parameter	1	1	↑	0	0	0	0	0	RTBFreq2	RTBFreq1	RTBFreq0	9F
3rd parameter	1	1	↑	0	0	0	0	0	0	NDisDM1	NDisDM0	00
4th parameter	1	1	↑	1	0	1	0	0	1	0	1	A5
Description	It is used to display partially (line devided) in order to reduce power consumption. 2 display areas are settable. It is used with PTLSET1 and PTLSET2 command.											

7.2.25 VCOM Offset Data

54H	VCOM Offset Data											
Ins./Par.	**A1**	**ERD**	**RWR**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**HEX**
VCMDAT	0	1	↑	0	1	0	1	0	1	0	0	54
1st parameter	1	1	↑	0	0	0	0	VcomS3	VcomS2	VcomS1	VcomS0	00
2nd parameter	1	1	↑	0	VcomD16	VcomD15	VcomD14	VcomD13	VcomD12	VcomD11	VcomD10	00
3rd parameter	1	1	↑	0	VcomD26	VcomD25	VcomD24	VcomD23	VcomD22	VcomD21	VcomD20	01
4th parameter	1	1	↑	1	0	1	0	0	1	0	1	A5

Description

VcomS[3:0]	VCOM offset data select
0xxx	No offset adjustment
1x00	Parameter 2 of this command (VCOM offset data1)
1x01	Parameter 3 of this command (VCOM offset data2)
1110	External MTP VCOM offset data1
1111	External MTP VCOM offset data2
else	TBD

VcomD1[6:0] and VcomD2[6:0]	Offset
1000000	-64
1000001	-63
1000010	-62
:	:
1111111	-1
0000000	0
0000001	+1
:	:
0111110	+62
0111111	+63

7.2.26 User ID

55H	User ID Set											
Ins./Par.	**A1**	**ERD**	**RWR**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**HEX**
UIDSET	0	1	↑	0	1	0	1	0	1	0	1	55
1st parameter	1	1	↑	UID117	UID116	UID115	UID114	UID113	UID112	UID111	UID110	00
2nd parameter	1	1	↑	UID127	UID126	UID125	UID124	UID123	UID122	UID121	UID120	00
3rd parameter	1	1	↑	UID217	UID216	UID215	UID214	UID213	UID212	UID211	UID210	00
4th parameter	1	1	↑	UID227	UID226	UID225	UID224	UID223	UID222	UID221	UID220	00
Description	▪ Set user ID data to write Multi Time PROM ▪ UID11[7:0]: User ID1-1 data to write Multi Time PROM ▪ UID12[7:0]: User ID1-2 data to write Multi Time PROM ▪ UID21[7:0]: User ID2-1 data to write Multi Time PROM ▪ UID22[7:0]: User ID2-2 data to write Multi Time PROM											

7.2.27 Multi Time PROM Mode

5AH	Multi Time PROM Mode											
Ins./Par.	**A1**	**ERD**	**RWR**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**HEX**
MTPMOD	0	1	↑	0	1	0	1	1	0	1	0	5A
1st parameter	1	1	↑	MTPMOD7	MTPMOD6	MTPMOD5	MTPMOD4	MTPMOD3	MTPMOD2	MTPMOD1	MTPMOD0	00
2nd parameter	1	1	↑	1	0	1	0	0	1	0	1	A5
3rd parameter	1	1	↑	1	0	1	0	0	1	0	1	A5
4th parameter	1	1	↑	1	0	1	0	0	1	0	1	A5
Description	▪ MTPMOD[7:0]: Mode select Read mode: BRM: F5h CAM: CFh FAM: 3Fh Program mode: 3Ah Erase mode: C5h											

7.2.28 Multi Time PROM Operation

5BH	Multi Time PROM Operation											
Ins./Par.	**A1**	**ERD**	**RWR**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**HEX**
MTPOP	0	1	↑	0	1	0	1	1	0	1	1	5B
1st parameter	1	1	↑	0	0	0	0	0	MTP_Sel	0	Prog_Mod	00
2nd parameter	1	1	↑	1	0	1	0	0	1	0	1	A5
3rd parameter	1	1	↑	1	0	1	0	0	1	0	1	A5
4th parameter	1	1	↑	1	0	1	0	0	1	0	1	A5
Description	▪ Prog_Mod: Program Mode 1: Enable 0: Disable ▪ MTP_SEL: 1: Select MTP1 0: Select MTP0											

7.2.29 SPI3 Write Memory Byte Counter

5CH	SPI3 Write Memory Byte Counter											
Ins./Par.	**A1**	**ERD**	**RWR**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**HEX**
SPI3WRCNT	0	1	↑	0	1	0	1	1	1	0	0	5C
1st parameter	1	1	↑	Si3Mw15	Si3Mw14	Si3Mw13	Si3Mw12	Si3Mw11	Si3Mw10	Si3Mw9	Si3Mw8	02
2nd parameter	1	1	↑	Si3Mw7	Si3Mw6	Si3Mw5	Si3Mw4	Si3Mw3	Si3Mw2	Si3Mw1	Si3Mw0	7F
3rd parameter	1	1	↑	1	0	1	0	0	1	0	1	A5
4th parameter	1	1	↑	1	0	1	0	0	1	0	1	A5
Description	▪ This command defines the numbers of data bytes written to DDRAM with 3-line SPI. ▪ Length of data byte = Si3Mw[15:0]+1											

7.2.30 Power Control

61H	Power Control											
Ins./Par.	**A1**	**ERD**	**RWR**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**HEX**
PWRCTL	0	1	↑	0	1	1	0	0	0	0	1	61
1st parameter	1	1	↑	BST3SR1	BST3SR0	0	0	BST4ON	BST3ON	BST2ON	BST1ON	40
2nd parameter	1	1	↑	FOFNo3	FOFNo2	FOFNo1	FOFNo0	0	SAMPSet2	SAMPSet1	SAMPSet0	04
3rd parameter	1	1	↑	0	0	0	0	0	0	1	0	02
4th parameter	1	1	↑	1	0	1	0	0	1	0	1	A5
Description	▪ Booster circuit control, source amp setting and booster clock frequency settings. ▪ This command must be input before SLPOUT command. ▪ BST3SR[1:0]: Step-up Rate of the 3rd booster setting 00, 01:"-1" 10: "-2" 11: "-3" ▪ BST4ON ~ BST1ON: 4th ~ 1st booster On/Off setting 0: Booster off 1: Booster on ▪ FOFNo[3:0]: Force off frame, set waiting time by number of frames from sleep out to display on. ▪ SAMPSet[2:0]: Source Amplifier Setting											

7.2.31 Electronic Volume Set 1

62H	Electronic Volume Set 1											
Ins./Par.	**A1**	**ERD**	**RWR**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**HEX**
EVSET1	0	1	↑	0	1	1	0	0	0	1	0	62
1st parameter	1	1	↑	0	VCOM6	VCOM5	VCOM4	VCOM3	VCOM2	VCOM1	VCOM0	0A
2nd parameter	1	1	↑	0	0	VGHREG5	VGHREG4	VGHREG3	VGHREG2	VGHREG1	VGHREG0	06
3rd parameter	1	1	↑	0	0	0	VGLREG4	VGLREG3	VGLREG2	VGLREG1	VGLREG0	0F
4th parameter	1	1	↑	1	0	1	0	0	1	0	1	A5

Description

- Set each output voltages of built-in voltage regulators.
- $\begin{cases} VGL = BST3SR[2:0] \times VGLREG - 3V \\ VGH = 2 \times VGHREG - VGL \end{cases}$
- The voltage of VGL must be lower than AVCLO.

VCOM[6:0]	VCOM (V)
00h	-0.3000
01h	-0.3125
02h	-0.3250
03h	-0.3375
:	:
3Dh	-1.0625
3Eh	-1.0750
3Fh	-1.0875
:	:
7Dh	-1.8625
7Eh	-1.8750
7Fh	-1.8875

VGHREG[5:0]	VGHREG (V)
00h	0
01h	1.5
02h	1.6
03h	1.7
:	:
2Eh	6.0
2Fh	6.1
30h	6.2
31h	6.2
:	:
3Eh	6.2
3Fh	6.2

VGLREG[4:0]	VGLREG (V)
00h	2.4
01h	2.5
02h	2.6

		03h	2.7	
		:	:	
		1Dh	5.3	
		1Eh	5.4	
		1Fh	5.5	

7.2.32 Electronic Volume Set 2

63H	Electronic Volume Set 1											
Ins./Par.	**A1**	**ERD**	**RWR**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**HEX**
EVSET2	0	1	↑	0	1	1	0	0	0	1	1	63
1st parameter	1	1	↑	0	0	0	GVDD4	GVDD3	GVDD2	GVDD1	GVDD0	0F
2nd parameter	1	1	↑	0	0	0	GVCL4	GVCL3	GVCL2	GVCL1	GVCL0	0F
3rd parameter	1	1	↑	1	0	1	0	0	1	0	1	A5
4th parameter	1	1	↑	1	0	1	0	0	1	0	1	A5

Description

▪ Set each output voltages of built-in voltage regulators.

GVDD[4:0]	GVDD(V)
00h	3.1
01h	3.2
02h	3.3
03h	3.4
:	:
1Dh	6.0
1Eh	6.1
1Fh	6.2

GVCL[4:0]	GVCL(V)
00h	-3.1
01h	-3.2
02h	-3.3
03h	-3.4
:	:
1Dh	-6.0
1Eh	-6.1
1Fh	-6.2

7.2.33 Booster Clock Setting

64H	Booster Clock Setting											
Ins./Par.	**A1**	**ERD**	**RWR**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**HEX**
BCLKSET	0	1	↑	0	1	1	0	0	1	0	0	64
1st parameter	1	1	↑	0	AVclClk2	AVclClk1	AVclClk0	0	AVdClk2	AVdClk2	AVdClk2	44
2nd parameter	1	1	↑	0	VglClk2	VglClk1	VglClk0	0	Vghclk2	Vghclk1	VghClk0	44
3rd parameter	1	1	↑	0	AVclClk_nd2	AVclClk_nd1	AVclClk_nd2	0	AVdClk_nd2	AVdClk_nd1	AVdClk_nd0	44
4th parameter	1	1	↑	0	VglClk_nd2	VglClk_nd1	VglClk_nd0	0	Vghclk_nd2	Vghclk_nd1	VghClk_nd0	44

Description

AVclClk: AVCL normal display booster clock select
AVdClk: AVDD normal display booster clock select
VGHCK: VGH normal display booster clock select
VGLCK: VGL normal display booster clock select
AVclClk: AVCL partial non-display booster clock select
AVdClk: AVDD partial non-display booster clock select
VGHCK: VGH partial non-display booster clock select
VGLCK: VGL partial non-display booster clock select

HEX	booster clock freq.
0	4K
1	7K
2	10K
3	15K
4	20K
5	31K
6	40K
7	62K

7.2.34 Gate Set

66H	Gate Set											
Ins./Par.	**A1**	**ERD**	**RWR**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**HEX**
GATESET	0	1	↑	0	1	1	0	0	1	1	0	66
1st parameter	1	1	↑	VGPP	0	0	ScanDir	0	0	ScanMod1	ScanMod0	00
2nd parameter	1	1	↑	1	0	1	0	0	1	0	1	A5
3rd parameter	1	1	↑	1	0	1	0	0	1	0	1	A5
4th parameter	1	1	↑	1	0	1	0	0	1	0	1	A5
Description	▪ Set line scan mode of gate driver. ▪ This command must be input before SLPOUT command. ▪ VGPP: Valid gate pin postion 0: Inside 1: Outside ▪ ScanDir: Scan direction 0: Normal 1: Reverse ▪ ScanMode[1:0]: Scan mode (refer to 6.4) 00: scan mode 1 01: scan mode 2 10: scan mode 3 11: scan mode 4											

7.2.35 Read Status

72H	Read Status											
Ins./Par.	**A1**	**ERD**	**RWR**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**HEX**
RDSTAT	0	1	↑	0	1	1	1	0	0	1	0	72
1st parameter	1	1	↑	1	0	1	0	0	1	0	1	A5
2nd parameter	1	↑	1	0	R16	R15	0	R13	R12	R11	R10	
3rd parameter	1	↑	1	0	R26	R25	R24	R23	R22	R21	R20	
4th parameter	1	↑	1	R37	R36	R35	R34	R33	R32	R31	R30	
5th parameter	1	↑	1	R47	R46	R45	R44	R43	R42	R41	R40	
6th parameter	1	↑	1	0	0	0	0	0	R52	R51	R50	
7th parameter	1	↑	1	0	R66	R65	R64	0	R62	R61	R60	
Description	▪ Display Status (1/0) R10: ’0’: DISOFF ‘1’: DISON R11: ‘0’: SLPIN ‘1’: SLPOUT R12: ‘0’: PTLOUT ‘1’: PTLIN R[17, 16, 15] = [1bpp, 2bpp, 4bpp] ▪ RAM Status R20: Page address increment ‘0’: Normal ‘1’: Reverse R21: Column address increment ‘0’: Normal ‘1’: Reverse R23: Scan direction ‘0’: Column ‘1’: Page R23: BLKFIL ‘0’ Command not executed ‘1’: Command executed R24: ‘0’: BLOUT ‘1’: BLIN R26, R25: Bit operation of start and end page (01: AND, 10: OR) ▪ R3[7:0]: Mask data of writing start page ▪ R4[7:0]: Mask data of writing end page											

7.2.36 Read Revision

73H	Read Revision											
Ins./Par.	**A1**	**ERD**	**RWR**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**HEX**
RDREV	0	1	↑	0	1	1	1	0	0	1	1	73
1st parameter	1	1	↑	1	0	1	0	0	1	0	1	A5
2nd parameter	1	↑	1	R17	R16	R15	R14	R13	R12	R11	R10	
Description	▪ R1[7:0]: Read IC Revision											

7.2.37 Read User ID

75H	Read User ID											
Ins./Par.	**A1**	**ERD**	**RWR**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**HEX**
RDUID	0	1	↑	0	1	1	1	0	1	0	1	75
1st parameter	1	1	↑	1	0	1	0	0	1	0	1	A5
2nd parameter	1	↑	1	R17	R16	R15	R14	R13	R12	R11	R10	
3rd parameter	1	↑	1	R27	R26	R25	R24	R23	R22	R21	R20	
4th parameter	1	↑	1	R37	R36	R35	R34	R33	R32	R31	R30	
5th parameter	1	↑	1	R47	R46	R45	R44	R43	R42	R41	R40	
6th parameter	1	↑	1	R57	R56	R55	R54	R53	R52	R51	R50	
7th parameter	1	↑	1	R67	R66	R65	R64	R63	R62	R61	R60	
8th parameter	1	↑	1	R77	R76	R75	R74	R73	R72	R71	R70	
9th parameter	1	↑	1	R87	R86	R85	R84	R83	R82	R81	R80	
10th parameter	1	↑	1	R97	R96	R95	R94	R93	R92	R91	R90	
11th parameter	1	↑	1	RA7	RA6	RA5	RA4	RA3	RA2	RA1	RA0	
12th parameter	1	↑	1	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0	
13th parameter	1	↑	1	RC7	RC6	RC5	RC4	RC3	RC2	RC1	RC0	
Description	▪ R1[7:0]: MTP UID1-1 ▪ R2[7:0]: MTP UID1-2 ▪ R3[7:0]: MTP UID2-1 ▪ R4[7:0]: MTP UID2-2 ▪ R5[7:0]: Don't Care ▪ R6[7:0]: Don't Care ▪ R7[7:0]: Don't Care ▪ R8[7:0]: Don't Care ▪ R9[7:0]: UIDSET Register UID1-1 ▪ RA[7:0]: UIDSET Register UID1-2 ▪ RB[7:0]: UIDSET Register UID2-1 ▪ RC[7:0]: UIDSET Register UID2-2											

7.2.38 Read VCOM Data

79H	Read VCOM Data											
Ins./Par.	**A1**	**ERD**	**RWR**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**HEX**
RDVCMDAT	0	1	↑	0	1	1	1	1	0	0	1	79
1st parameter	1	1	↑	1	0	1	0	0	1	0	1	A5
2nd parameter	1	↑	1	x	x	R15	R14	R13	R12	R11	R10	
3rd parameter	1	↑	1	x	x	R25	R24	R23	R22	R21	R20	
4th parameter	1	↑	1	x	x	R35	R34	R33	R32	R31	R30	
5th parameter	1	↑	1	x	x	R45	R44	R43	R42	R41	R40	
6th parameter	1	↑	1	x	x	R55	R54	R53	R52	R51	R50	
7th parameter	1	↑	1	x	x	R65	R64	R63	R62	R61	R60	
8th parameter	1	↑	1	x	x	R75	R74	R73	R72	R71	R70	
9th parameter	1	↑	1	0	0	0	0	R83	R82	R81	R80	
Description	▪ R1[5:0]: MTP VCOM offset value1 ▪ R2[5:0]: MTP VCOM offset value2 ▪ R3[5:0]: Don't Care ▪ R4[5:0]: Don't Care ▪ R5[5:0]: VCMDAT register VCOM offset value1 ▪ R6[5:0]: VCMDAT register VCOM offset value2 ▪ R7[5:0]: VCOM electric volume (EVSET1 2nd parameter + VCMDAT) ▪ R8[3:0]: VCOM offset data reference point											

7.2.39 Gamma Set 4bpp Positive 1

91H	Gamma Set 4bpp Positive 1											
Ins./Par.	**A1**	**ERD**	**RWR**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**HEX**
GAMSET4P1	0	1	↑	1	0	0	1	0	0	0	1	91
1st parameter	1	1	↑	0	0	G4BPV05	G4BPV04	G4BPV03	G4BPV02	G4BPV01	G4BPV00	00
2nd parameter	1	1	↑	0	0	G4BPV15	G4BPV14	G4BPV13	G4BPV12	G4BPV11	G4BPV10	04
3rd parameter	1	1	↑	0	0	G4BPV25	G4BPV24	G4BPV23	G4BPV22	G4BPV21	G4BPV20	08
4th parameter	1	1	↑	0	0	G4BPV35	G4BPV34	G4BPV33	G4BPV32	G4BPV31	G4BPV30	0C
Description	▪ Set LCD gamma voltage setting of positive polarity in 4bpp mode. ▪ This command must be input before SLPOUT. ▪ G4BPV0: V0 voltage setting (positive polarity) ▪ G4BPV1: V1 voltage setting (positive polarity) ▪ G4BPV2: V2 voltage setting (positive polarity) ▪ G4BPV3: V3 voltage setting (positive polarity)											

7.2.40 Gamma Set 4bpp Positive 2

92H	Gamma Set 4bpp Positive 2											
Ins./Par.	**A1**	**ERD**	**RWR**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**HEX**
GAMSET4P2	0	1	↑	1	0	0	1	0	0	1	0	92
1st parameter	1	1	↑	0	0	G4BPV45	G4BPV44	G4BPV43	G4BPV42	G4BPV41	G4BPV40	10
2nd parameter	1	1	↑	0	0	G4BPV55	G4BPV54	G4BPV53	G4BPV52	G4BPV51	G4BPV50	14
3rd parameter	1	1	↑	0	0	G4BPV65	G4BPV64	G4BPV63	G4BPV62	G4BPV61	G4BPV60	18
4th parameter	1	1	↑	0	0	G4BPV75	G4BPV74	G4BPV73	G4BPV72	G4BPV71	G4BPV70	1C
Description	▪ Set LCD gamma voltage setting of positive polarity in 4bpp mode. ▪ This command must be input before SLPOUT. ▪ G4BPV4: V4 voltage setting (positive polarity) ▪ G4BPV5: V5 voltage setting (positive polarity) ▪ G4BPV6: V6 voltage setting (positive polarity) ▪ G4BPV7: V7 voltage setting (positive polarity)											

7.2.41 Gamma Set 4bpp Positive 3

93H	Gamma Set 4bpp Positive 3											
Ins./Par.	**A1**	**ERD**	**RWR**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**HEX**
GAMSET4P3	0	1	↑	1	0	0	1	0	0	1	1	93
1st parameter	1	1	↑	0	0	G4BPV85	G4BPV84	G4BPV83	G4BPV82	G4BPV81	G4BPV80	23
2nd parameter	1	1	↑	0	0	G4BPV95	G4BPV94	G4BPV93	G4BPV92	G4BPV91	G4BPV90	27
3rd parameter	1	1	↑	0	0	G4BPVA5	G4BPVA4	G4BPVA3	G4BPVA2	G4BPVA1	G4BPVA0	2B
4th parameter	1	1	↑	0	0	G4BPVB5	G4BPVB4	G4BPVB3	G4BPVB2	G4BPVB1	G4BPVB0	2F
Description	▪ Set LCD gamma voltage setting of positive polarity in 4bpp mode. ▪ This command must be input before SLPOUT. ▪ G4BPV8: V8 voltage setting (positive polarity) ▪ G4BPV9: V9 voltage setting (positive polarity) ▪ G4BPV10: V10 voltage setting (positive polarity) ▪ G4BPV11: V11 voltage setting (positive polarity)											

7.2.42 Gamma Set 4bpp Positive 4

94H	Gamma Set 4bpp Positive 4											
Ins./Par.	**A1**	**ERD**	**RWR**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**HEX**
GAMSET4P4	0	1	↑	1	0	0	1	0	1	0	0	94
1st parameter	1	1	↑	0	0	G4BPVC5	G4BPVC4	G4BPVC3	G4BPVC2	G4BPVC1	G4BPVC0	33
2nd parameter	1	1	↑	0	0	G4BPVD5	G4BPVD4	G4BPVD3	G4BPVD2	G4BPVD1	G4BPVD0	37
3rd parameter	1	1	↑	0	0	G4BPVE5	G4BPVE4	G4BPVE3	G4BPVE2	G4BPVE1	G4BPVE0	3B
4th parameter	1	1	↑	0	0	G4BPVF5	G4BPVF4	G4BPVF3	G4BPVF2	G4BPVF1	G4BPVF0	3F
Description	▪ Set LCD gamma voltage setting of positive polarity in 4bpp mode. ▪ This command must be input before SLPOUT. ▪ G4BPV12: V12 voltage setting (positive polarity) ▪ G4BPV13: V13 voltage setting (positive polarity) ▪ G4BPV14: V14 voltage setting (positive polarity) ▪ G4BPV15: V15 voltage setting (positive polarity)											

7.2.43 Gamma Set 2bpp Positive

95H	Gamma Set 2bpp Positive											
Ins./Par.	**A1**	**ERD**	**RWR**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**HEX**
GAMSET2P	0	1	↑	1	0	0	1	0	1	0	1	95
1st parameter	1	1	↑	0	0	G2BPV05	G2BPV04	G2BPV03	G2BPV02	G2BPV01	G2BPV00	00
2nd parameter	1	1	↑	0	0	G2BPV15	G2BPV14	G2BPV13	G2BPV12	G2BPV11	G2BPV10	15
3rd parameter	1	1	↑	0	0	G2BPV25	G2BPV24	G2BPV23	G2BPV22	G2BPV21	G2BPV20	2A
4th parameter	1	1	↑	0	0	G2BPV35	G2BPV34	G2BPV33	G2BPV32	G2BPV31	G2BPV30	3F
Description	▪ Set LCD gamma voltage setting of positive polarity in 2bpp mode. ▪ This command must be input before SLPOUT. ▪ G2BPV0: V0 voltage setting (positive polarity) ▪ G2BPV1: V1 voltage setting (positive polarity) ▪ G2BPV2: V2 voltage setting (positive polarity) ▪ G2BPV3: V3 voltage setting (positive polarity)											

7.2.44 Gamma Set 1bpp

96H	Gamma Set 1bpp											
Ins./Par.	**A1**	**ERD**	**RWR**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**HEX**
GAMSET	0	1	↑	1	0	0	1	0	1	1	0	96
1st parameter	1	1	↑	0	0	G1BPV05	G1BPV04	G1BPV03	G1BPV02	G1BPV01	G1BPV00	00
2nd parameter	1	1	↑	0	0	G1BPV15	G1BPV14	G1BPV13	G1BPV12	G1BPV11	G1BPV10	3F
3rd parameter	1	1	↑	0	0	G1BNV05	G1BNV04	G1BNV03	G1BNV02	G1BNV01	G1BNV00	00
4th parameter	1	1	↑	0	0	G1BNV15	G1BNV14	G1BNV13	G1BNV12	G1BNV11	G1BNV10	3F
Description	▪ Set LCD gamma voltage setting of positive and negative polarity in 1bpp mode. ▪ This command must be input before SLPOUT. ▪ G1BPV0: V0 voltage setting (positive polarity) ▪ G1BPV1: V1 voltage setting (positive polarity) ▪ G1BNV0: V0 voltage setting (negative polarity) ▪ G1BNV1: V1 voltage setting (negative polarity)											

7.2.45 Gamma Set 4bpp Negative 1

99H	Gamma Set 4bpp Negative 1											
Ins./Par.	**A1**	**ERD**	**RWR**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**HEX**
GAMSET4N1	0	1	↑	1	0	0	1	1	0	0	1	99
1st parameter	1	1	↑	0	0	G4BNV05	G4BNV04	G4BNV03	G4BNV02	G4BNV01	G4BNV00	00
2nd parameter	1	1	↑	0	0	G4BNV15	G4BNV14	G4BNV13	G4BNV12	G4BNV11	G4BNV10	04
3rd parameter	1	1	↑	0	0	G4BNV25	G4BNV24	G4BNV23	G4BNV22	G4BNV21	G4BNV20	08
4th parameter	1	1	↑	0	0	G4BNV35	G4BNV34	G4BNV33	G4BNV32	G4BNV31	G4BNV30	0C
Description	▪ Set LCD gamma voltage setting of negative polarity in 4bpp mode. ▪ This command must be input before SLPOUT. ▪ G4BNV0: V0 voltage setting (negative polarity) ▪ G4BNV1: V1 voltage setting (negative polarity) ▪ G4BNV2: V2 voltage setting (negative polarity) ▪ G4BNV3: V3 voltage setting (negative polarity)											

7.2.46 Gamma Set 4bpp Negative 2

9AH	Gamma Set 4bpp Negative 2											
Ins./Par.	**A1**	**ERD**	**RWR**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**HEX**
GAMSET4N2	0	1	↑	1	0	0	1	1	0	1	0	9A
1st parameter	1	1	↑	0	0	G4BNV45	G4BNV44	G4BNV43	G4BNV42	G4BNV41	G4BNV40	10
2nd parameter	1	1	↑	0	0	G4BNV55	G4BNV54	G4BNV53	G4BNV52	G4BNV51	G4BNV50	14
3rd parameter	1	1	↑	0	0	G4BNV65	G4BNV64	G4BNV63	G4BNV62	G4BNV61	G4BNV60	18
4th parameter	1	1	↑	0	0	G4BNV75	G4BNV74	G4BNV73	G4BNV72	G4BNV71	G4BNV70	1C
Description	▪ Set LCD gamma voltage setting of negative polarity in 4bpp mode. ▪ This command must be input before SLPOUT. ▪ G4BNV4: V4 voltage setting (negative polarity) ▪ G4BNV5: V5 voltage setting (negative polarity) ▪ G4BNV6: V6 voltage setting (negative polarity) ▪ G4BNV7: V7 voltage setting (negative polarity)											

7.2.47 Gamma Set 4bpp Negative 3

9BH	Gamma Set 4bpp Negative 3											
Ins./Par.	**A1**	**ERD**	**RWR**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**HEX**
GAMSET4N3	0	1	↑	1	0	0	1	1	0	1	1	9B
1st parameter	1	1	↑	0	0	G4BNV85	G4BNV84	G4BNV83	G4BNV82	G4BNV81	G4BNV80	23
2nd parameter	1	1	↑	0	0	G4BNV95	G4BNV94	G4BNV93	G4BNV92	G4BNV91	G4BNV90	27
3rd parameter	1	1	↑	0	0	G4BNVA5	G4BNVA4	G4BNVA3	G4BNVA2	G4BNVA1	G4BNVA0	2B
4th parameter	1	1	↑	0	0	G4BNVB5	G4BNVB4	G4BNVB3	G4BNVB2	G4BNVB1	G4BNVB0	2F
Description	▪ Set LCD gamma voltage setting of negative polarity in 4bpp mode. ▪ This command must be input before SLPOUT. ▪ G4BNV8: V8 voltage setting (negative polarity) ▪ G4BNV9: V9 voltage setting (negative polarity) ▪ G4BNVA: V10 voltage setting (negative polarity) ▪ G4BNVB: V11 voltage setting (negative polarity)											

7.2.48 Gamma Set 4bpp Negative 4

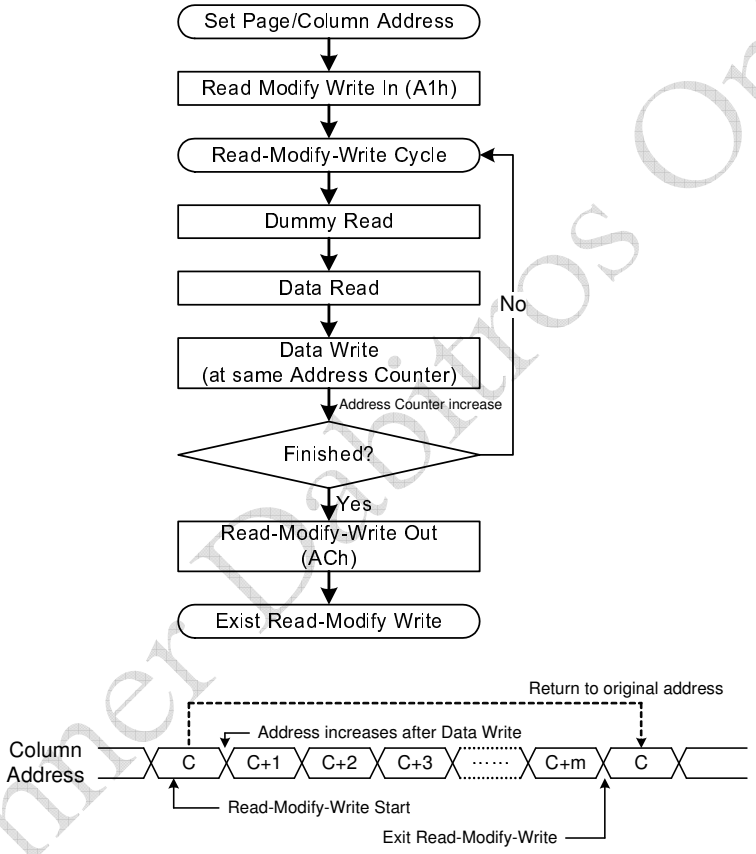
9CH	Gamma Set 4bpp Negative 4											
Ins./Par.	**A1**	**ERD**	**RWR**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**HEX**
GAMSET4N4	0	1	↑	1	0	0	1	1	1	0	0	9C
1st parameter	1	1	↑	0	0	G4BNVC5	G4BNVC4	G4BNVC3	G4BNVC2	G4BNVC1	G4BNVC0	33
2nd parameter	1	1	↑	0	0	G4BNVD5	G4BNVD4	G4BNVD3	G4BNVD2	G4BNVD1	G4BNVD0	37
3rd parameter	1	1	↑	0	0	G4BNVE5	G4BNVE4	G4BNVE3	G4BNVE2	G4BNVE1	G4BNVE0	3B
4th parameter	1	1	↑	0	0	G4BNVF5	G4BNVF4	G4BNVF3	G4BNVF2	G4BNVF1	G4BNVF0	3F
Description	▪ Set LCD gamma voltage setting of negative polarity in 4bpp mode. ▪ This command must be input before SLPOUT. ▪ G4BNVC: V12 voltage setting (negative polarity) ▪ G4BNVD: V13 voltage setting (negative polarity) ▪ G4BNVE: V14 voltage setting (negative polarity) ▪ G4BNVF: V15 voltage setting (negative polarity)											

7.2.49 Gamma Set 2bpp Negative

9DH	Gamma Set 2bpp Negative											
Ins./Par.	**A1**	**ERD**	**RWR**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**HEX**
GAMSET2N	0	1	↑	1	0	0	1	1	1	0	1	9D
1st parameter	1	1	↑	0	0	G2BNV05	G2BNV04	G2BNV03	G2BNV02	G2BNV01	G2BNV00	00
2nd parameter	1	1	↑	0	0	G2BNV15	G2BNV14	G2BNV13	G2BNV12	G2BNV11	G2BNV10	15
3rd parameter	1	1	↑	0	0	G2BNV25	G2BNV24	G2BNV23	G2BNV22	G2BNV21	G2BNV20	2A
4th parameter	1	1	↑	0	0	G2BNV35	G2BNV34	G2BNV33	G2BNV32	G2BNV31	G2BNV30	3F
Description	▪ Set LCD gamma voltage setting of negative polarity in 2bpp mode. ▪ This command must be input before SLPOUT. ▪ G2BNV0: V0 voltage setting (negative polarity) ▪ G2BNV1: V1 voltage setting (negative polarity) ▪ G2BNV2: V2 voltage setting (negative polarity) ▪ G2BNV3: V3 voltage setting (negative polarity)											

7.2.50 Read Modify Write In

A1H	Read Modify Write in											
Ins./Par.	**A1**	**ERD**	**RWR**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**HEX**
RMWIN	0	1	↑	0	1	1	0	0	1	0	0	A1
1st parameter	1	1	↑	1	0	1	0	0	1	0	1	A5
Description	▪ Read modify write mode in ▪ Only valid in 6800/8080											



7.2.51 MTP Read Enable

A2H	MTP Read Enable											
Ins./Par.	**A1**	**ERD**	**RWR**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**HEX**
MTPRDEN	0	1	↑	1	0	1	0	0	0	1	0	A2
1st parameter	1	1	↑	1	0	1	0	0	1	0	1	A5
Description	▪ MTP read enable											

7.2.52 MTP Write Enable

A3H	MTP White Enable											
Ins./Par.	A1	ERD	RWR	D7	D6	D5	D4	D3	D2	D1	D0	HEX
MTPWREN	0	1	↑	1	0	1	0	0	0	1	1	A3
1st parameter	1	1	↑	1	0	1	0	0	1	0	1	A5
Description	▪ MTP write enable											

7.2.53 Partial Out

A9H	Partial out											
Ins./Par.	A1	ERD	RWR	D7	D6	D5	D4	D3	D2	D1	D0	HEX
PTLOUT	0	1	↑	1	0	1	0	1	0	0	1	A9
1st parameter	1	1	↑	1	0	1	0	0	1	0	1	A5
Description	▪ Escape from partial display mode.											

7.2.54 Partial In

AAH	Partial in											
Ins./Par.	A1	ERD	RWR	D7	D6	D5	D4	D3	D2	D1	D0	HEX
PTLIN	0	1	↑	1	0	1	0	1	0	1	0	AA
1st parameter	1	1	↑	1	0	1	0	0	1	0	1	A5
Description	▪ Enter into partial display mode.											

7.2.55 Read Modify Write Out

ACH	Read Modify Write out											
Ins./Par.	A1	ERD	RWR	D7	D6	D5	D4	D3	D2	D1	D0	HEX
RMWOUT	0	1	↑	0	1	1	0	0	1	0	0	AC
1st parameter	1	1	↑	1	0	1	0	0	1	0	1	A5
Description	▪ Read modify write mode out ▪ Only valid in 6800/8080											

7.2.56 Software Reset

AEH	Software Reset											
Ins./Par.	A1	ERD	RWR	D7	D6	D5	D4	D3	D2	D1	D0	HEX
SWRESET	0	1	↑	1	0	1	0	1	1	1	0	AE
1st parameter	1	1	↑	1	0	1	0	0	1	0	1	A5
Description	▪ This command make a reset as same as hardware reset. ▪ It is required Hardware reset at power-on reset. ▪ **It is always required to input this command after hardware reset.**											

7.2.57 Read TC Data

76H	Read TC Data											
Ins./Par.	**A1**	**ERD**	**RWR**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**HEX**
RDTC	0	1	↑	0	1	1	1	0	1	1	0	76
1st parameter	1	1	↑	1	0	1	0	0	1	0	1	A5
2nd parameter	1	↑	1	0	0	0	0	0	0	0	R10	
3rd parameter	1	↑	1	R27	R26	R25	R24	R23	R22	R21	R20	
Description	▪ R1[0]: XDTA[8] ▪ R2[7:0]: XDTA[7:0] ▪ Temperature = -40 + 0.5 x XDTA[8:0] (±4*) ℃ * The variation of temperature read from the internal sensor may be affected by the conditions of IC operation.											

7.2.58 Command for MTP Autoload Control

F4H	Command for MTP Autoload Control											
Ins./Par.	**A1**	**ERD**	**RWR**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**HEX**
TCSET	0	1	↑	1	1	1	1	0	1	0	0	F4
1st parameter	1	↑	1	0	0	0	0	0	0	0	0	00
2nd parameter	1	↑	1	0	1	1	0	0	1	1	1	67
3rd parameter	1	↑	1	1	1	1	MTPAuto	1	1	1	0	FE
4th parameter	1	↑	1	1	1	1	0	1	0	1	0	EA
Description	▪ MTPAuto: MTP autoload 0: off 1: on											

7.2.59 Command for Temperature Control

F6H	Command for Temperature Control											
Ins./Par.	**A1**	**ERD**	**RWR**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**HEX**
TCSET	0	1	↑	1	1	1	1	0	1	1	0	F6
1st parameter	1	↑	1	0	0	0	0	TSON	TCSEL	0	0	00
2nd parameter	1	↑	1	0	0	0	0	0	0	0	0	00
3rd parameter	1	↑	1	0	0	0	0	0	0	0	0	00
4th parameter	1	↑	1	0	0	1	0	0	0	0	1	21
Description	▪ Temperature sensor “on” TSON=TCSEL=1 ▪ Temperature sensor “off” TSON=TCSEL=0											

7.2.60 TCVCOM Offset Set

B1H	TCVCOM Offset Set											
Ins./Par.	**A1**	**ERD**	**RWR**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**HEX**
TCSET	0	1	↑	1	0	1	1	0	0	0	1	B1
1st parameter	1	1	↑	0	0	0	TCAVCM4	TCAVCM3	TCAVCM2	TCAVCM1	TCAVCM0	00
2nd parameter	1	1	↑	0	0	0	TCBVCM4	TCBVCM3	TCBVCM2	TCBVCM1	TCBVCM0	00
3rd parameter	1	1	↑	0	0	0	TCCVCM4	TCCVCM3	TCCVCM2	TCCVCM1	TCCVCM0	00
4th parameter	1	1	↑	0	0	0	TCDVCM4	TCDVCM3	TCDVCM2	TCDVCM1	TCDVCM0	00

Description

- TCAVCM[4:0]: TC offset for VCOM of temperature zone A
- TCBVCM[4:0]: TC offset for VCOM of temperature zone B
- TCCVCM[4:0]: TC offset for VCOM of temperature zone C
- TCDVCM[4:0]: TC offset for VCOM of temperature zone D

TCxVCM[4:0] x=A, B, C, D	Offset
10000	-16
10001	-15
10010	-14
:	:
11111	-1
00000	0
00001	+1
:	:
01110	+14
01111	+15

7.2.61 TC VGHREG Offset Set

B5H	TC VGHREG Offset Set											
Ins./Par.	**A1**	**ERD**	**RWR**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**HEX**
TCVGH1	0	1	↑	1	0	1	1	0	1	0	1	B5
1st parameter	1	1	↑	0	TCAVGH6	TCAVGH5	TCAVGH4	TCAVGH3	TCAVGH2	TCAVGH1	TCAVGH0	00
2nd parameter	1	1	↑	0	TCBVGH6	TCBVGH5	TCBVGH4	TCBVGH3	TCBVGH2	TCBVGH1	TCBVGH0	00
3rd parameter	1	1	↑	0	TCCVGH6	TCCVGH5	TCCVGH4	TCCVGH3	TCCVGH2	TCCVGH1	TCCVGH0	00
4th parameter	1	1	↑	0	TCDVGH6	TCDVGH5	TCDVGH4	TCDVGH3	TCDVGH2	TCDVGH1	TCDVGH0	00
Description	▪ TCAVGH[6:0]: TC offset for VGHREG of temperature zone A ▪ TCBVGH[6:0]: TC offset for VGHREG of temperature zone B ▪ TCCVGH[6:0]: TC offset for VGHREG of temperature zone C ▪ TCDVGH[6:0]: TC offset for VGHREG of temperature zone D											

TCxVCM[6:0] x=A, B, C, D	Offset
1000000	-64
1000001	-63
1000010	-62
:	:
1111111	-1
0000000	0
0000001	+1
:	:
0111110	+62
0111111	+63

7.2.62 Set GVDD Temperature Compensation Gradient Curves1

C1H	Set GVDD Temperature Compensation Gradient Curves1											
Ins./Par.	**A1**	**ERD**	**RWR**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**HEX**
SETTCGVD1	0	1	↑	1	1	0	0	0	0	0	1	C1
1st parameter	1	1	↑	MTGVD03	MTGVD02	MTGVD01	MTGVD00	0	0	0	0	00
2nd parameter	1	1	↑	MTGVD23	MTGVD22	MTGVD21	MTGVD20	MTGVD13	MTGVD12	MTGVD11	MTGVD10	00
3rd parameter	1	1	↑	MTGVD43	MTGVD42	MTGVD41	MTGVD40	MTGVD33	MTGVD32	MTGVD31	MTGVD30	00
4th parameter	1	1	↑	MTGVD63	MTGVD62	MTGVD61	MTGVD60	MTGVD53	MTGVD52	MTGVD51	MTGVD50	00
Description	▪ MTGVDx[3]: TCx(x=0~7) polarity 1: Positive, 0: Negative ▪ MTGVD0[2:0]: Set GVDD Gradient of TC0 Curves -32~-24℃ ▪ MTGVD1[2:0]: Set GVDD Gradient of TC0 Curves -24~-16℃ ▪ MTGVD2[2:0]: Set GVDD Gradient of TC1 Curves -16~-8℃ ▪ MTGVD3[2:0]: Set GVDD Gradient of TC2 Curves -8~0℃ ▪ MTGVD4[2:0]: Set GVDD Gradient of TC3 Curves 0~8℃ ▪ MTGVD5[2:0]: Set GVDD Gradient of TC4 Curves 8~16℃ ▪ MTGVD6[2:0]: Set GVDD Gradient of TC5 Curves 16~24℃											

7.2.63 Set GVDD Temperature Compensation Gradient Curves2

C2H	Set GVDD Temperature Compensation Gradient Curves2											
Ins./Par.	**A1**	**ERD**	**RWR**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**HEX**
SETTCGVD2	0	1	↑	1	1	0	0	0	0	1	0	C2
1st parameter	1	1	↑	MTGVD83	MTGVD82	MTGVD81	MTGVD80	MTGVD73	MTGVD72	MTGVD71	MTGVD70	00
2nd parameter	1	1	↑	MTGVDA3	MTGVDA2	MTGVDA1	MTGVDA0	MTGVD93	MTGVD92	MTGVD91	MTGVD90	00
3rd parameter	1	1	↑	MTGVDC3	MTGVDC2	MTGVDC1	MTGVDC0	MTGVDB3	MTGVDB2	MTGVDB1	MTGVDB0	00
4th parameter	1	1	↑	0	0	0	0	MTGVDD3	MTGVDD2	MTGVDD1	MTGVDD0	00
Description	▪ MTGVDx[3]: TCx(x=8~F) polarity 1: Positive, 0: Negative ▪ MTGVD7[2:0]: Set GVDD Gradient of TC6 Curves 24~32℃ ▪ MTGVD8[2:0]: Set GVDD Gradient of TC7 Curves 32~40℃ ▪ MTGVD9[2:0]: Set GVDD Gradient of TC8 Curves 40~48℃ ▪ MTGVDA[2:0]: Set GVDD Gradient of TC9 Curves 48~56℃ ▪ MTGVDB[2:0]: Set GVDD Gradient of TCA Curves 56~64℃ ▪ MTGVDC[2:0]: Set GVDD Gradient of TCB Curves 64~72℃ ▪ MTGVDD[2:0]: Set GVDD Gradient of TCC Curves 72~80℃											

7.2.64 Set GVDD Temperature Compensation Gradient Curves3

C2H	Set GVDD Temperature Compensation Gradient Curves3											
Ins./Par.	**A1**	**ERD**	**RWR**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**HEX**
SETTCGVD3	0	1	↑	1	1	0	0	0	0	1	1	C3
1st parameter	1	1	↑	0	0	0	0	0	0	0	0	00
2nd parameter	1	1	↑	0	0	THGVD5	THGVD4	THGVD3	THGVD2	THGVD1	THGVD0	00
3rd parameter	1	1	↑	1	0	1	0	0	1	0	1	00
4th parameter	1	1	↑	1	0	1	0	0	1	0	1	00
Description	▪ THGVD [5:0]: Set temperature hysteresis value											

THGVD [5:0]	temperature hysteresis value
000000	0 ℃
000001	0.5 ℃
000010	1.0 ℃
:	:
111110	31.0 ℃
111111	31.5 ℃

7.2.65 Set GVCL Temperature Compensation Gradient Curves1

C4H	Set GVCL Temperature Compensation Gradient Curves1											
Ins./Par.	**A1**	**ERD**	**RWR**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**HEX**
SETTCGVD1	0	1	↑	1	1	0	0	0	1	0	0	C4
1st parameter	1	1	↑	MTGVC03	MTGVC02	MTGVC01	MTGVC00	0	0	0	0	00
2nd parameter	1	1	↑	MTGVC23	MTGVC22	MTGVC21	MTGVC20	MTGVC13	MTGVC12	MTGVC11	MTGVC10	00
3rd parameter	1	1	↑	MTGVC43	MTGVC42	MTGVC41	MTGVC40	MTGVC33	MTGVC32	MTGVC31	MTGVC30	00
4th parameter	1	1	↑	MTGVC63	MTGVC62	MTGVC61	MTGVC60	MTGVC53	MTGVC52	MTGVC51	MTGVC50	00
Description	▪ MTGVCx[3]: TCx(x=0~7) polarity 1: Positive, 0: Negative ▪ MTGVC0[2:0]: Set GVCL Gradient of TC0 Curves -32~-24℃ ▪ MTGVC1[2:0]: Set GVCL Gradient of TC0 Curves -24~-16℃ ▪ MTGVC2[2:0]: Set GVCL Gradient of TC1 Curves -16~-8℃ ▪ MTGVC3[2:0]: Set GVCL Gradient of TC2 Curves -8~0℃ ▪ MTGVC4[2:0]: Set GVCL Gradient of TC3 Curves 0~8℃ ▪ MTGVC5[2:0]: Set GVCL Gradient of TC4 Curves 8~16℃ ▪ MTGVC6[2:0]: Set GVCL Gradient of TC5 Curves 16~24℃											

7.2.66 Set GVCL Temperature Compensation Gradient Curves2

C5H	Set GVCL Temperature Compensation Gradient Curves2											
Ins./Par.	**A1**	**ERD**	**RWR**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**HEX**
SETTCGVD2	0	1	↑	1	1	0	0	0	1	0	1	C5
1st parameter	1	1	↑	MTGVC83	MTGVC82	MTGVC81	MTGVC80	MTGVC73	MTGVC72	MTGVC71	MTGVC70	00
2nd parameter	1	1	↑	MTGVCA3	MTGVCA2	MTGVCA1	MTGVCA0	MTGVC93	MTGVC92	MTGVC91	MTGVC90	00
3rd parameter	1	1	↑	MTGVCC3	MTGVCC2	MTGVCC1	MTGVCC0	MTGVCB3	MTGVCB2	MTGVCB1	MTGVCB0	00
4th parameter	1	1	↑	0	0	0	0	MTGVCD3	MTGVCD2	MTGVCD1	MTGVCD0	00
Description	▪ MTGVCx[3]: TCx(x=8~F) polarity 1: Positive, 0: Negative ▪ MTGVC7[2:0]: Set GVCL Gradient of TC6 Curves 24~32℃ ▪ MTGVC8[2:0]: Set GVCL Gradient of TC7 Curves 32~40℃ ▪ MTGVC9[2:0]: Set GVCL Gradient of TC8 Curves 40~48℃ ▪ MTGVCA[2:0]: Set GVCL Gradient of TC9 Curves 48~56℃ ▪ MTGVCB[2:0]: Set GVCL Gradient of TCA Curves 56~64℃ ▪ MTGVCC[2:0]: Set GVCL Gradient of TCB Curves 64~72℃ ▪ MTGVCD[2:0]: Set GVCL Gradient of TCC Curves 72~80℃											

7.2.67 Set GVCL Temperature Compensation Gradient Curves3

C6H	Set GVCL Temperature Compensation Gradient Curves3											
Ins./Par.	**A1**	**ERD**	**RWR**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**HEX**
SETTCGVD3	0	1	↑	1	1	0	0	0	1	1	0	C6
1st parameter	1	1	↑	0	0	0	0	0	0	0	0	00
2nd parameter	1	1	↑	1	0	1	0	0	1	0	1	A5
3rd parameter	1	1	↑	1	0	1	0	0	1	0	1	A5
4th parameter	1	1	↑	1	0	1	0	0	1	0	1	A5
Description	▪ Reserved											

7.2.68 Set TC VGH Flag

C7H	Set TC VGH Flag											
Ins./Par.	**A1**	**ERD**	**RWR**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**HEX**
SETTCVGH	0	1	↑	1	1	0	0	0	1	1	1	C7
1st parameter	1	1	↑	TAVGH7	TAVGH6	TAVGH5	TAVGH4	TAVGH3	TAVGH2	TAVGH1	TAVGH0	00
2nd parameter	1	1	↑	TBVGH7	TBVGH6	TBVGH5	TBVGH4	TBVGH3	TBVGH2	TBVGH1	TBVGH0	00
3rd parameter	1	1	↑	TCVGH7	TCVGH6	TCVGH5	TCVGH4	TCVGH3	TCVGH2	TCVGH1	TCVGH0	00
4th parameter	1	1	↑	0	0	0	0	THVGH3	THVGH2	THVGH1	THVGH0	00

Description

- ▪ TAVGH[7:0]: set the TC zone boundary between zone A and B
- ▪ TBVGH[7:0]: set the TC zone boundary between zone B and C
- ▪ TCVGH[7:0]: set the TC zone boundary between zone C and D
- ▪ THVGH [3:0]: Set temperature hysteresis value
- ▪ TxVGH=TxVGH[7:0] – 40(℃)
- ▪ -30 < TAVGH< TBVGH < TCVGH < 80

THVGH [3:0]	temperature hysteresis value
0000	0 ℃
0001	1 ℃
0010	2 ℃
:	:
1110	14 ℃
1111	15 ℃

7.2.69 Set TC VCOM Flag

C8H	Set TC VCOM Flag											
Ins./Par.	**A1**	**ERD**	**RWR**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**HEX**
SETTCVCOM	0	1	↑	1	1	0	0	1	0	0	0	C8
1st parameter	1	1	↑	TAVCOM7	TAVCOM6	TAVCOM5	TAVCOM4	TAVCOM3	TAVCOM2	TAVCOM1	TAVCOM0	00
2nd parameter	1	1	↑	TBVCOM7	TBVCOM6	TBVCOM5	TBVCOM4	TBVCOM3	TBVCOM2	TBVCOM1	TBVCOM0	00
3rd parameter	1	1	↑	TCVCOM7	TCVCOM6	TCVCOM5	TCVCOM4	TCVCOM3	TCVCOM2	TCVCOM1	TCVCOM0	00
4th parameter	1	1	↑	0	0	0	0	THVCOM3	THVCOM2	THVCOM1	THVCOM0	00

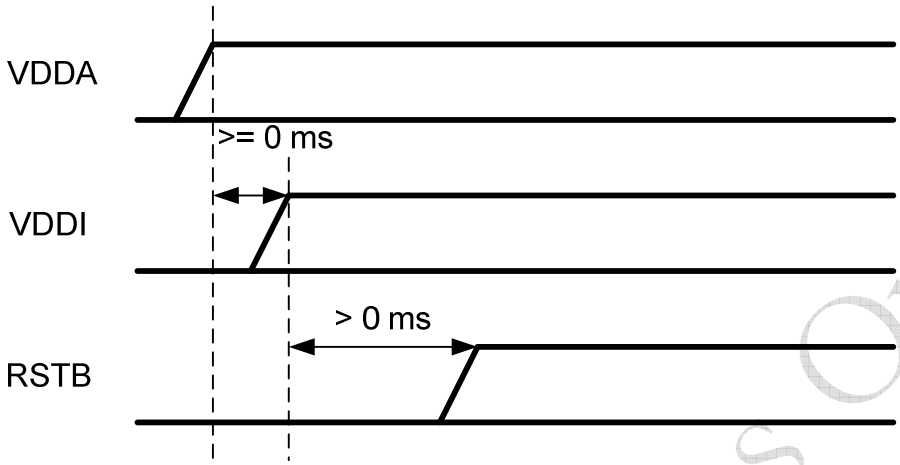
Description

- TAVCOM [7:0]: set the TC zone boundary between zone A and B
- TBVCOM [7:0]: set the TC zone boundary between zone B and C
- TCVCOM [7:0]: set the TC zone boundary between zone C and D
- THVCOM [3:0]: Set temperature hysteresis value
- TxVCOM=TxVGH[7:0] – 40(℃)
- -30 < TAVCOM< TBVCOM < TCVCOM < 80

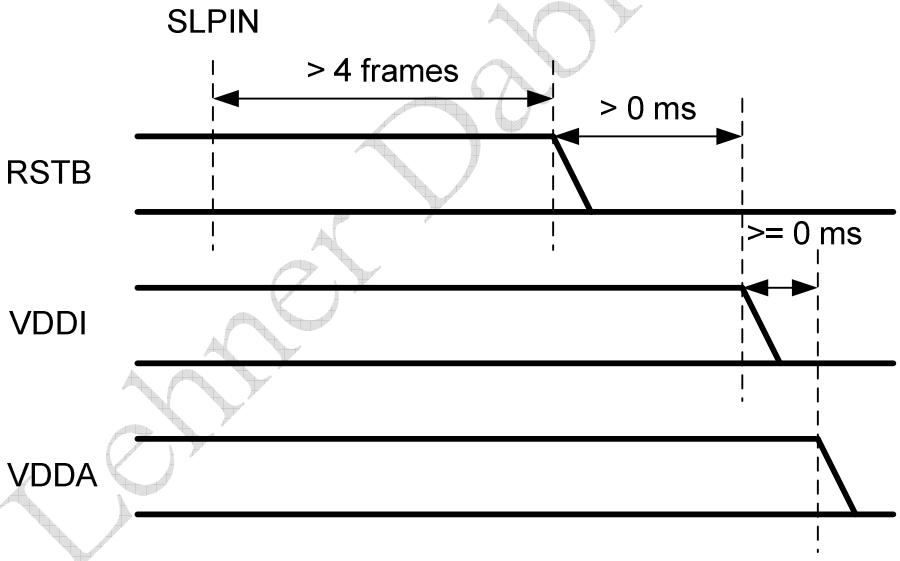
THVCOM [3:0]	temperature hysteresis value
0000	0 ℃
0001	1 ℃
0010	2 ℃
:	:
1110	14 ℃
1111	15 ℃

8. OPERATION FLOW

8.1 Power on/off Sequence

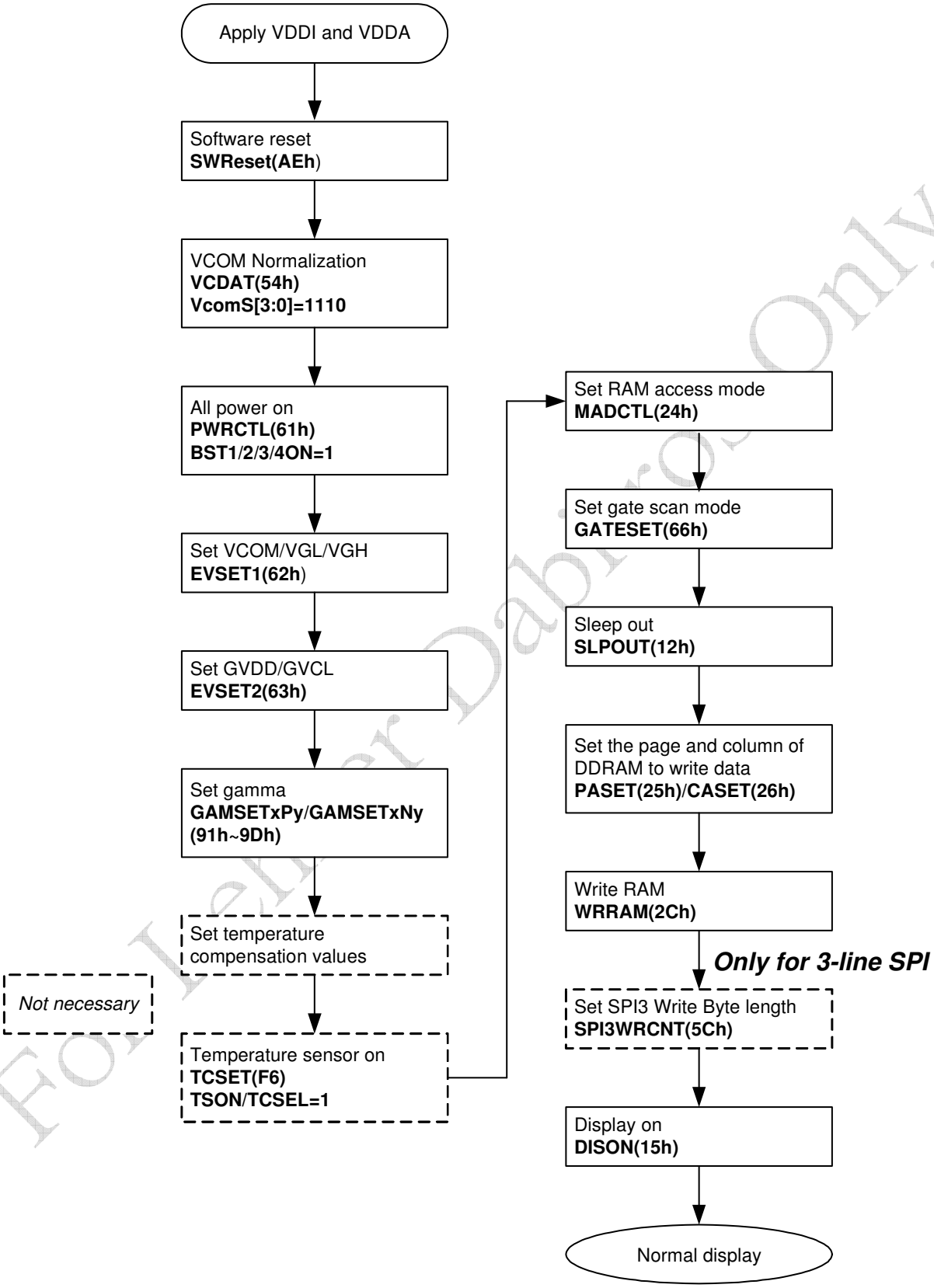


Power on sequence

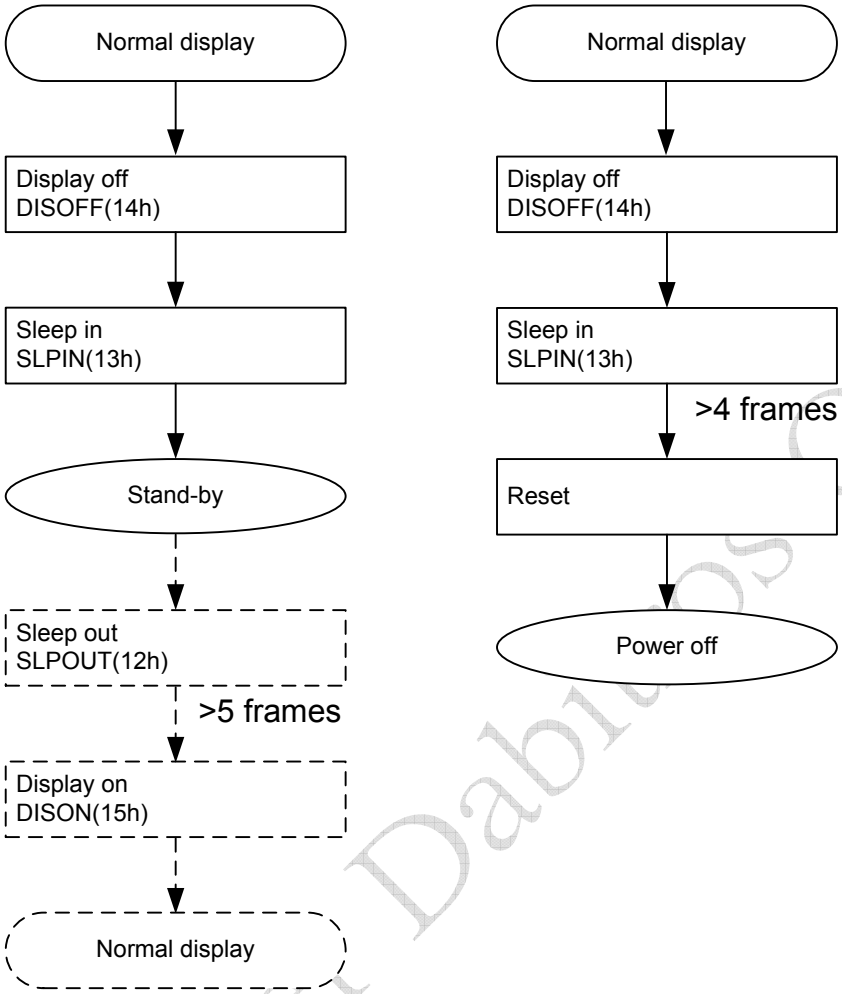


Power off sequence

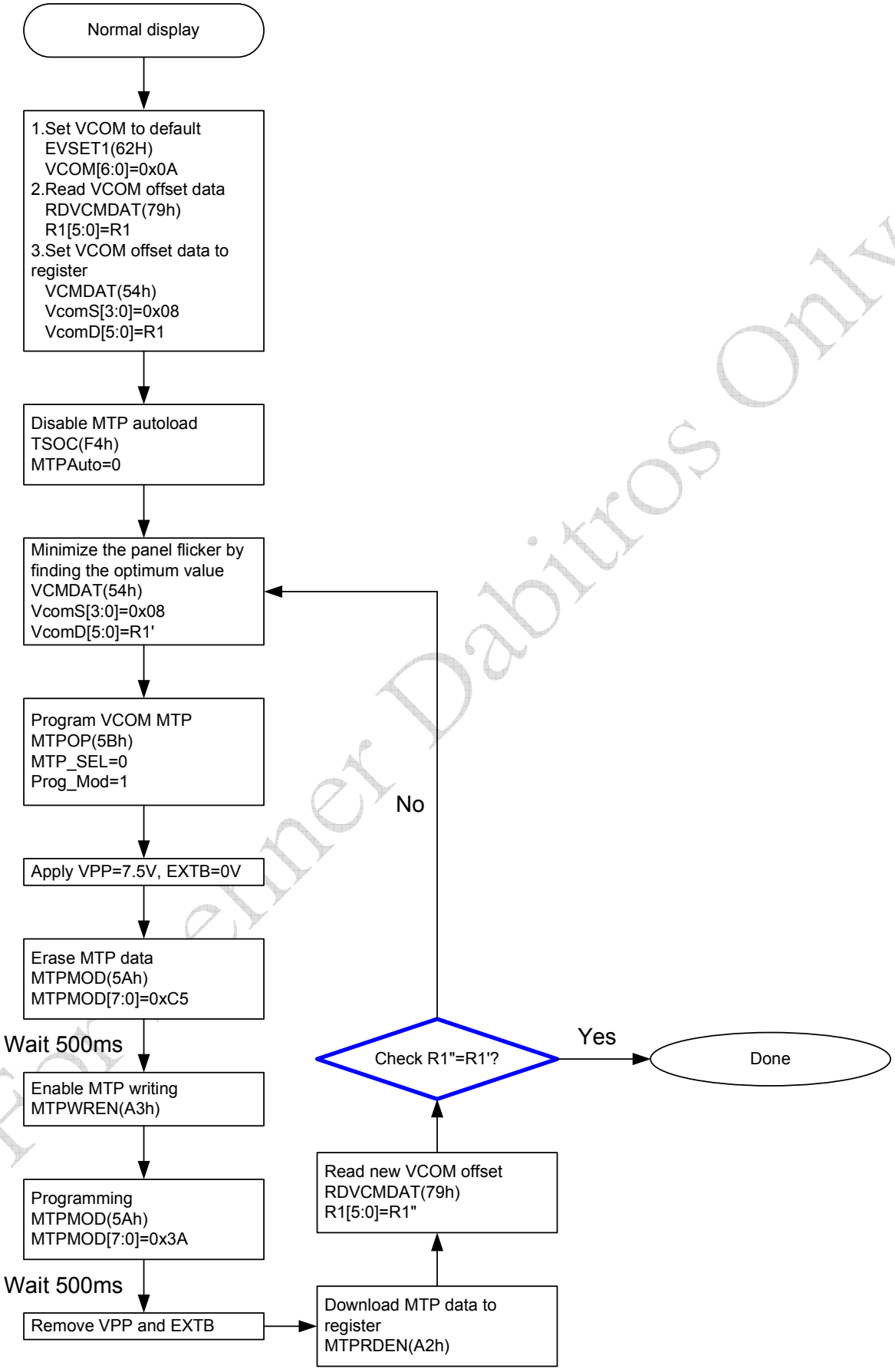
8.2 Initial Flow



8.3 Stand-by and Power-off Flow



8.4 MTP Flow



9. ABSOLUTE MAXIMUM RATINGS

In accordance with the Absolute Maximum Rating System; please refer to notes 1 and 2.

Parameter	Symbol	Conditions	Unit
I/O Power Supply Voltage	VDDI	-0.3 ~ 6.0	V
Analog Power supply voltage	VDDA	-0.3 ~ 6.5	V
Analog Power supply voltage	VDDP	-0.3 ~ 6.0	V
LCD Power supply voltage	AVDD, GVDD	7.0	V
	AVCL, GVCL, VCOM	-7.0	V
	VGH – VGL	35	V
MPU Interface Input Voltage	V_{IN}	-0.3 ~ VDDI +0.3	V
Operating temperature	TOPR	-30 ~ 80	°C
Storage temperature	TSTR (TCP) TSTR (Dice)	-55 ~ 100 -55 ~ 120	°C

Notes:

1. Stresses exceed the absolute maximum ratings listed above may cause permanent damage to IC. The IC should be operated under the condition of DC/AC characteristics for normal operation. If this condition is not met, the IC may be malfunctioned, or the reliability may drop.
2. Parameters are valid in the operating temperature range unless otherwise specified. All voltages are with respect to VSS unless otherwise noted.

10. DC CHARACTERISTICS

VSS = AGND = PGND =DGND = 0V; Temp = -20 ~ 80℃;

Item	Symbol	Condition	Rating			Unit	Applicable Pin
			Min.	Typ.	Max.		
Operating Voltage	VDDI	External Supply	2.7	—	5.5	V	VDDI
Operating Voltage	VDDA	External Supply	2.7	—	5.5	V	VDDA
Operating Voltage	VDDP	External Supply	2.7	—	5.5	V	VDDP
Operating Voltage	VCCO	Built-In Power Supply	—	1.8	—	V	VCCO
Operating Voltage	AVDDO	Built-In Power Supply	6.1	—	9	V	AVDDO
Operating Voltage	AVCLO	Built-In Power Supply	-9	—	-6.1	V	AVCLO
Operating Voltage	GVDD	Built-In Power Supply	3.1	—	6.2	V	GVDD
Operating Voltage	GVCL	Built-In Power Supply	-6.2	—	-3.1	V	GVCL
Operating Voltage	VGH	Built-In Power Supply	8.0	—	19.0	V	VGH
Operating Voltage	VGL	Built-In Power Supply	-15.0	—	-8.0	V	VGL
Operating Voltage	VCOM	Built-In Power Supply	-1.885	—	-0.3	V	VCOM
Input High-level Voltage	V_{IH}		0.8 VDDI	—	VDDI	V	MPU Interface
Input Low-level Voltage	V_{IL}		VSS	—	0.2 VDDI	V	MPU Interface
Output High-level Voltage	V_{OH}	VDDI=2.7V, IOL=1mA	0.8 VDDI	—	VDDI	V	D[7:0]
Output Low-level Voltage	V_{OL}	VDDI=2.7V, IOL=1mA	VSS	—	0.2 VDDI	V	D[7:0]
Input Leakage Current	I_{LI}	V_{IN}=VDDI or DGND	-1.0	—	1.0	μA	MPU Interface
Output Voltage Deviation	ΔVS	Ta=25°C	—	±10	±20	mV	Source Pad
Read Temperature Offset	ΔT_{RD}	VDD=3.3V, Ta=25℃	–	-2	–	2	℃
		VDD=3.3V, Ta=-40~105℃	–	-4 *1	–	4 *1	

*1: Temperature accuracy is for reference only now. The target for all temperature range is ± 4℃ and it is still under yield improvement stage.

The current consumed by whole IC (bare die) with internal power system:

Item	Symbol	Condition	Rating			Unit
			Min.	Typ.	Max.	
Display Current (Digital)	IDDI	VDDA=VDDP=VDDI=3.3V, Internal Power, 4bpp mode, Display ON Pattern: 1x1 Checker (Static), fFR= 60Hz Ta=-40~105℃	–	<1	–	μA
Display Current (Analog)	IDDA + IDDP			18,000		
Standby	ISS	VDDA=VDDP=VDDI=3.3V, Internal Power, Ta=-40~105℃	–	250	–	μA

Note: The current is DC characteristic of a "Bare Chip".

11. AC CHARACTERISTICS

11.1 Oscillation Frequency

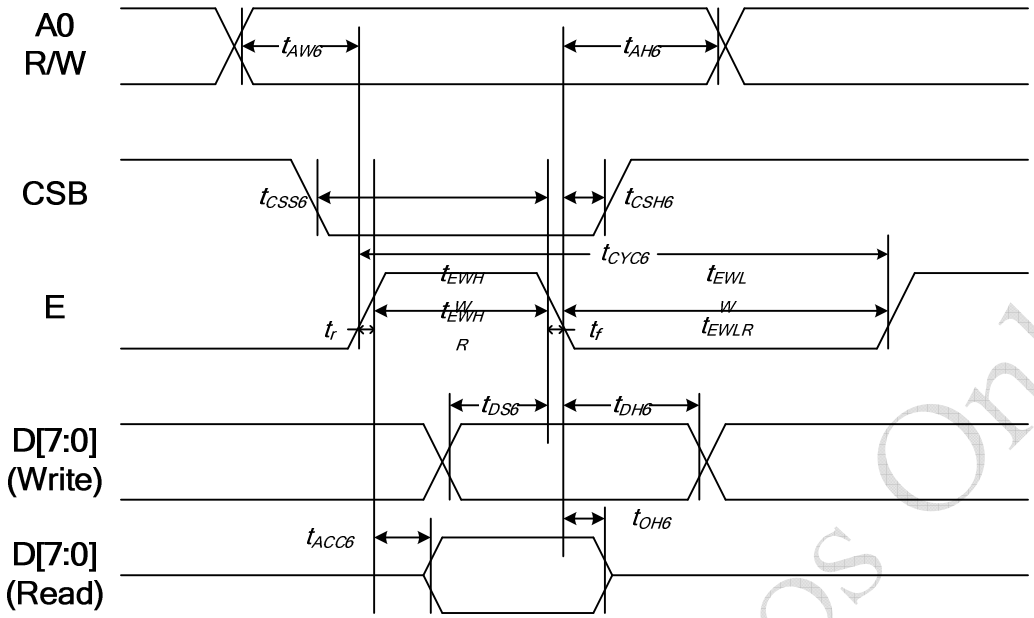
AGND = PGND =DGND = 0V, VDDA = VDDP= VDDI = 3.0 ~ 5.0V, Ta = -30 ~ 80℃

Item	Symbol	Condition	Rating			Unit	Applicable Pin
			Min.	Typ.	Max.		
Oscillation Frequency	fosc	Built in oscillator circuit is used	900	1000	1100	KHz	CL
External Clock Input Frequency	fosci		900	1000	1100	KHz	CL

Note:

1. External clock timing are specified based on the 20% and 80% of VDDI
2. The rise and fall times (tr and tf) of the input signal are specified for less than 10ns.

11.2 System Bus Timing for 6800 Series MPU



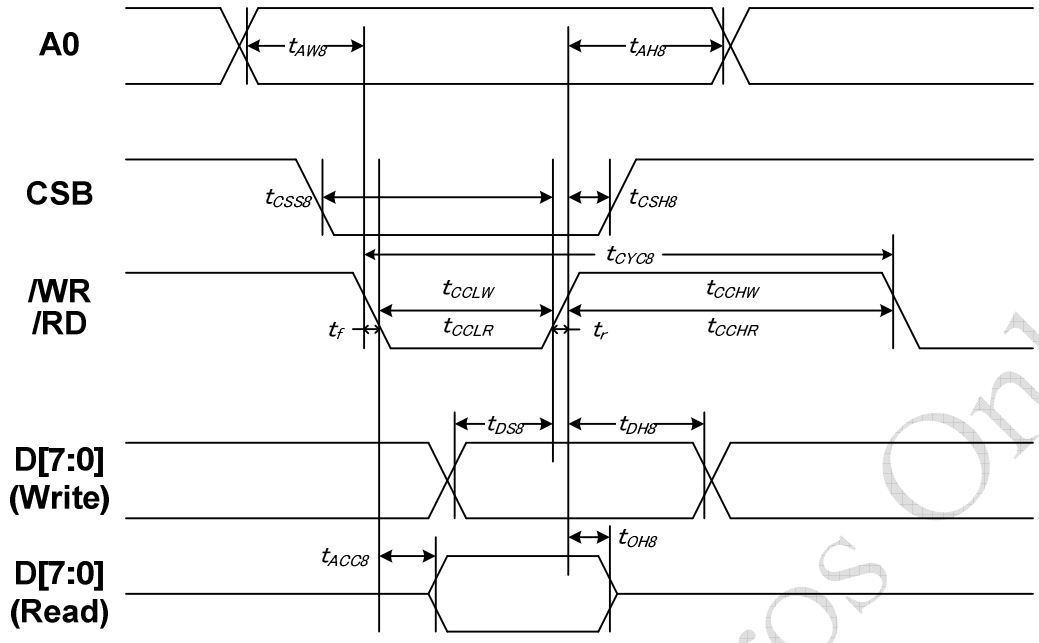
AGND = PGND =DGND = 0V, VDDA = VDDP= VDDI = 3.0 ~ 5.0V , Ta = -30 ~ 80℃

Item	Signal	Symbol	Condition	Min.	Max.	Unit
Address setup time	A0	tAW6		10	—	ns
Address hold time		tAH6		0	—	
System cycle time	E	tCYC6		200	—	
Enable L pulse width (WRITE)		tEWLW		100	—	
Enable H pulse width (WRITE)		tEWHW		100	—	
Enable L pulse width (READ)		tEWLR		130	—	
Enable H pulse width (READ)		tEWHR		130	—	
CSB setup time	CSB	tCSS6		100	—	
CSB hold time		tCSH6		100	—	
Write data setup time	D[7:0]	tDS6		70	—	
Write data hold time		tDH6		20	—	
Read data access time		tACC6	CL = 100 pF	—	80	
Read data output disable time		tOH6	CL = 100 pF	15	80	

Note:

1. The input signal rise time and fall time (tr, tf) is specified at 15 ns or less. When the system cycle time is extremely fast, (tr + tf) ≤ (tCYC8 – tCCLW – tCCHW) for (tr + tf) ≤ (tCYC8 – tCCLR – tCCHR) are specified.
2. All timing is specified using 20% and 80% of VDDI as the reference.
3. tCCLW and tCCLR are specified as the overlap between CSB being “L” and /WR and /RD being at the “L” level. CSB and /WR (or /RD) cannot act at the same time and CSB should be 100ns wider than /WR (or /RD).

11.3 System Bus Timing for 8080 Series MPU



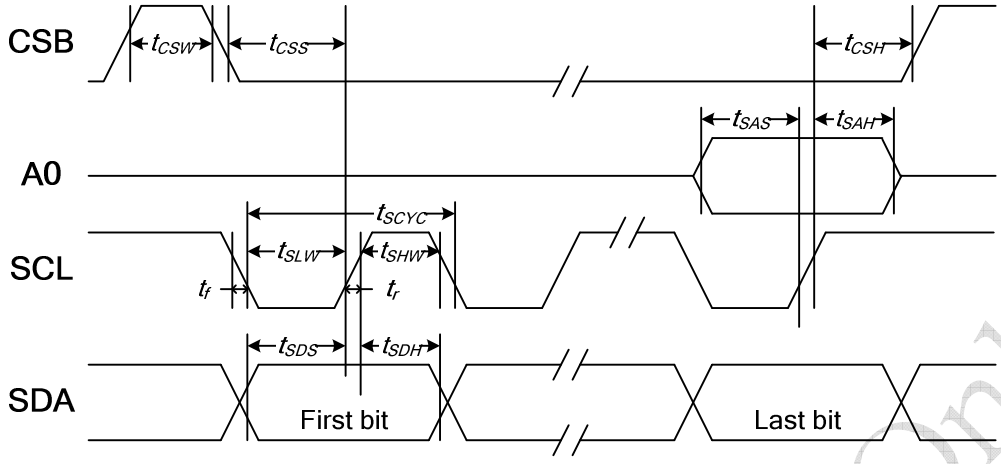
AGND = PGND =DGND = 0V, VDDA = VDDP= VDDI = 3.0 ~ 5.0V , Ta = -30 ~ 80℃

Item	Signal	Symbol	Condition	Min.	Max.	Unit
Address setup time	A0	tAW8		10	—	ns
Address hold time		tAH8		0	—	
System cycle time	/WR	tCYC8		200	—	
/WR L pulse width (WRITE)		tCCLW		100	—	
/WR H pulse width (WRITE)		tCCHW		100	—	
/RD L pulse width (READ)	/RD	tCCLR		120	—	
/RD H pulse width (READ)		tCCHR		120	—	
CSB setup time	CSB	tCSS8		100	—	
CSB hold time		tCSH8		100	—	
WRITE Data setup time	D[7:0]	tDS8		70	—	
WRITE Data hold time		tDH8		20	—	
READ access time		tACC8	CL = 100 pF	—	80	
READ Output disable time		tOH8	CL = 100 pF	15	80	

Note:

1. The input signal rise time and fall time (tr, tf) is specified at 15 ns or less. When the system cycle time is extremely fast, (tr + tf) ≤ (tCYC8 – tCCLW – tCCHW) for (tr + tf) ≤ (tCYC8 – tCCLR – tCCHR) are specified.
2. All timing is specified using 20% and 80% of VDDI as the reference.
3. tCCLW and tCCLR are specified as the overlap between CSB being “L” and /WR and /RD being at the “L” level. CSB and /WR (or /RD) cannot act at the same time and CSB should be 100ns wider than /WR (or /RD).

11.4 System Bus Timing for 4-Line Serial Interface



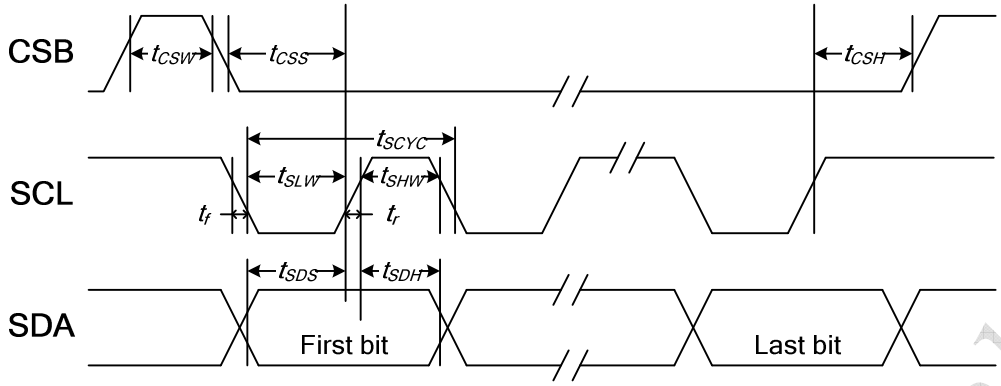
AGND = PGND =DGND = 0V, VDDA = VDDP= VDDI = 3.0 ~ 5.0V, Ta = -30 ~ 80℃

Item	Signal	Symbol	Condition	Min.	Max.	Unit
Serial clock period	SCL	tSCYC		80	—	ns
SCL “H” pulse width		tSHW		40	—	
SCL “L” pulse width		tSLW		40	—	
Address setup time	A0	tSAS		40	—	
Address hold time		tSAH		40	—	
Data setup time	SDA	tSDS		15	—	
Data hold time		tSDH		20	—	
CSB-SCL time	CSB	tCSS		40	—	
CSB-SCL time		tCSH		40	—	
CSB “H” pulse width		tCSW		15	—	

Note:

1. The input signal rise and fall time (tr, tf) are specified at 15 ns or less.
2. All timing is specified using 20% and 80% of VDDI as the standard.

11.5 System Bus Timing for 3-Line Serial Interface



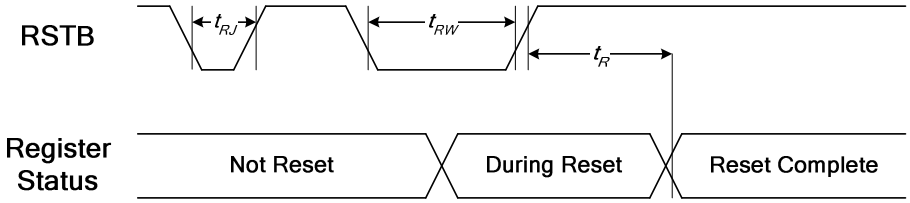
AGND = PGND =DGND = 0V, VDDA = VDDP= VDDI = 3.0 ~ 5.0V, -30 ~ 80℃

Item	Signal	Symbol	Condition	Min.	Max.	Unit
Serial Clock Period	SCL	tSCYC		80	—	ns
SCL “H” pulse width		tSHW		40	—	
SCL “L” pulse width		tSLW		40	—	
Data setup time	SDA	tSDS		15	—	
Data hold time		tSDH		20	—	
CSB-SCL time	CSB	tCSS		40	—	
CSB-SCL time		tCSH		40	—	
CSB “H” pulse width		tCSW		15	—	

Note:

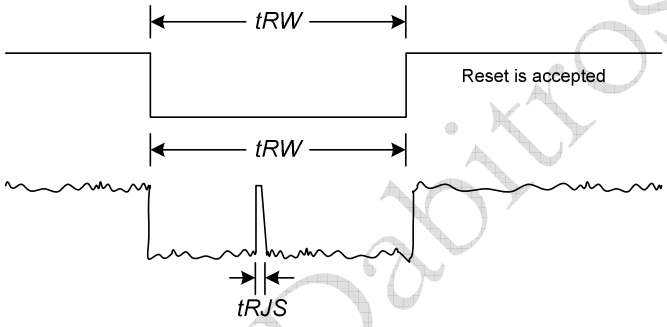
1. The input signal rise and fall time (tr, tf) are specified at 15 ns or less.
2. All timing is specified using 20% and 80% of VDDI as the standard.

11.6 Hardware Reset Timing



AGND = PGND =DGND = 0V, VDDA = VDDP= VDDI = 3.0 ~ 5.0V, Ta = -30 ~ 80℃

Item	Signal	Symbol	Condition	Rating		Unit
				Min.	Max.	
Reset time	RSTB	tR		—	5 *1	us
Reset “L” pulse width		tRW		15	—	
Reset rejection		tRJ		—	5	
Reset rejection (for noise spike)		tRJS		—	10	ns

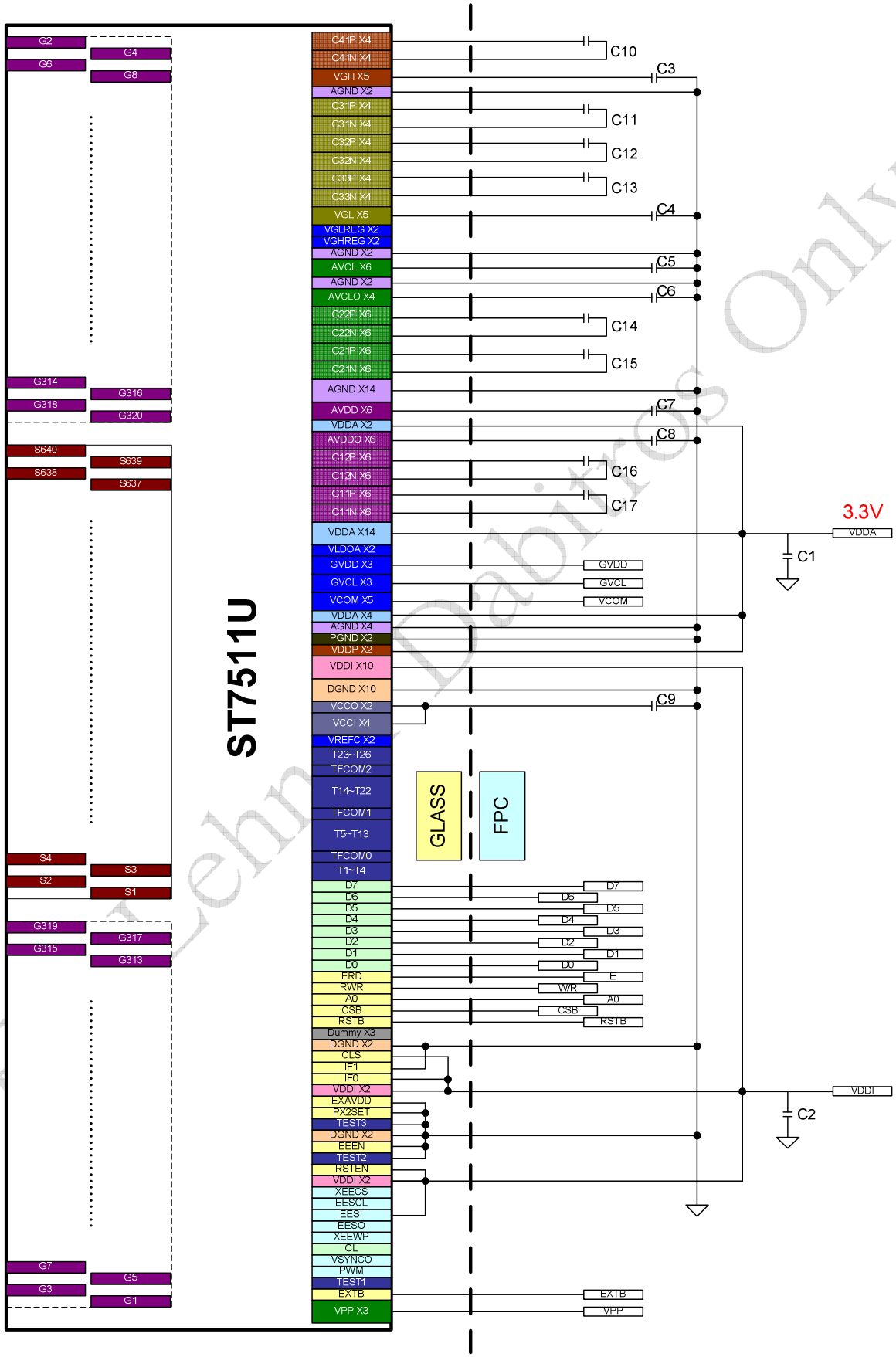


Note:

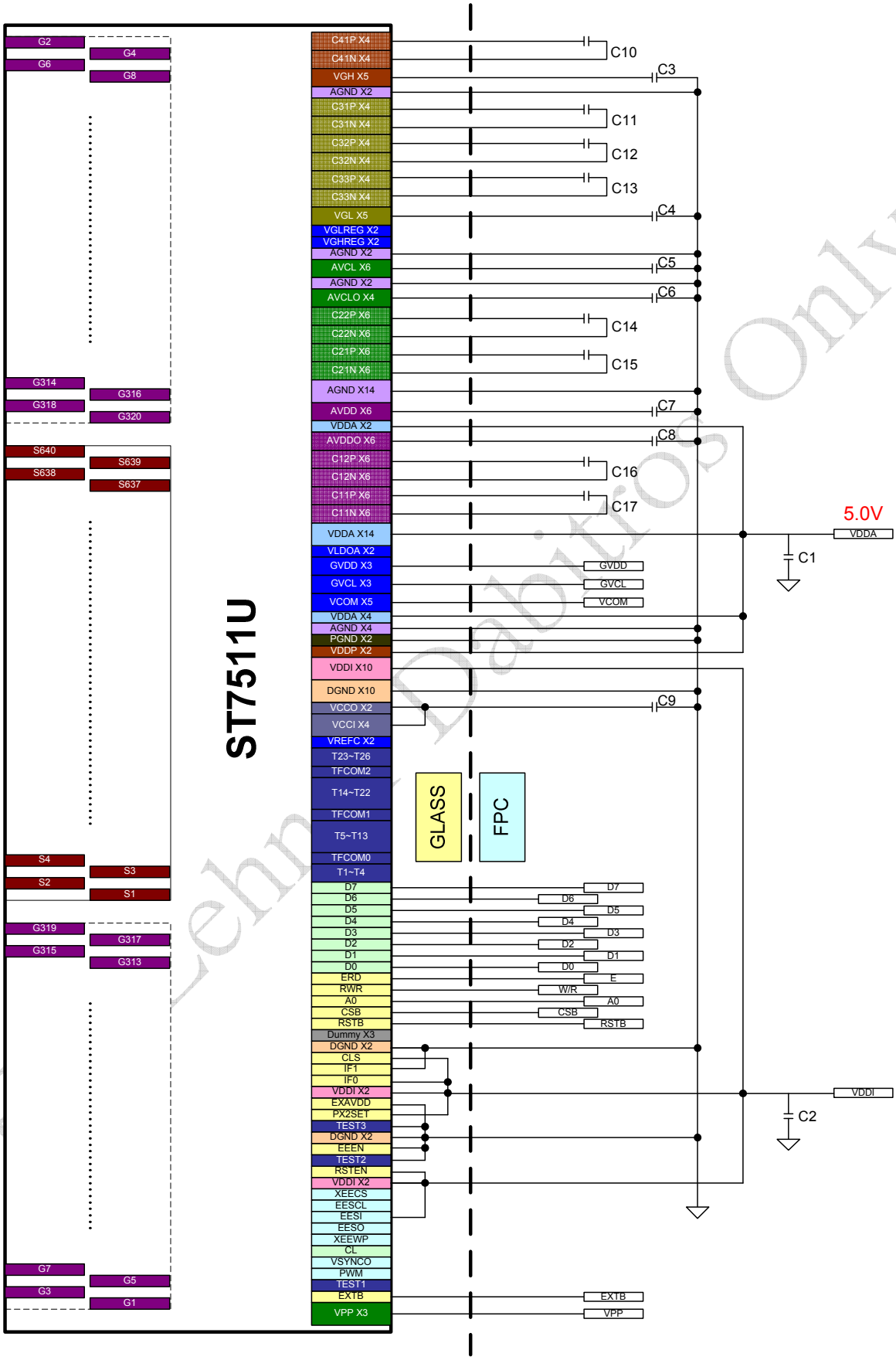
1. For PROM related operation, it takes 50ms at least for PROM Registers to load PROM contents. Do NOT use any PROM related command during this period.
2. When the system issues a RSTB LOW pulse, the reset procedure of IC will start if the LOW pulse is longer than tRW specified above. If the LOW pulse is less than tRJ specified above, the reset procedure of IC will not start. If the LOW pulse is longer than tRJ and less than tRW, the reset procedure of IC is not guaranteed.

12. APPLICATION CIRCUIT

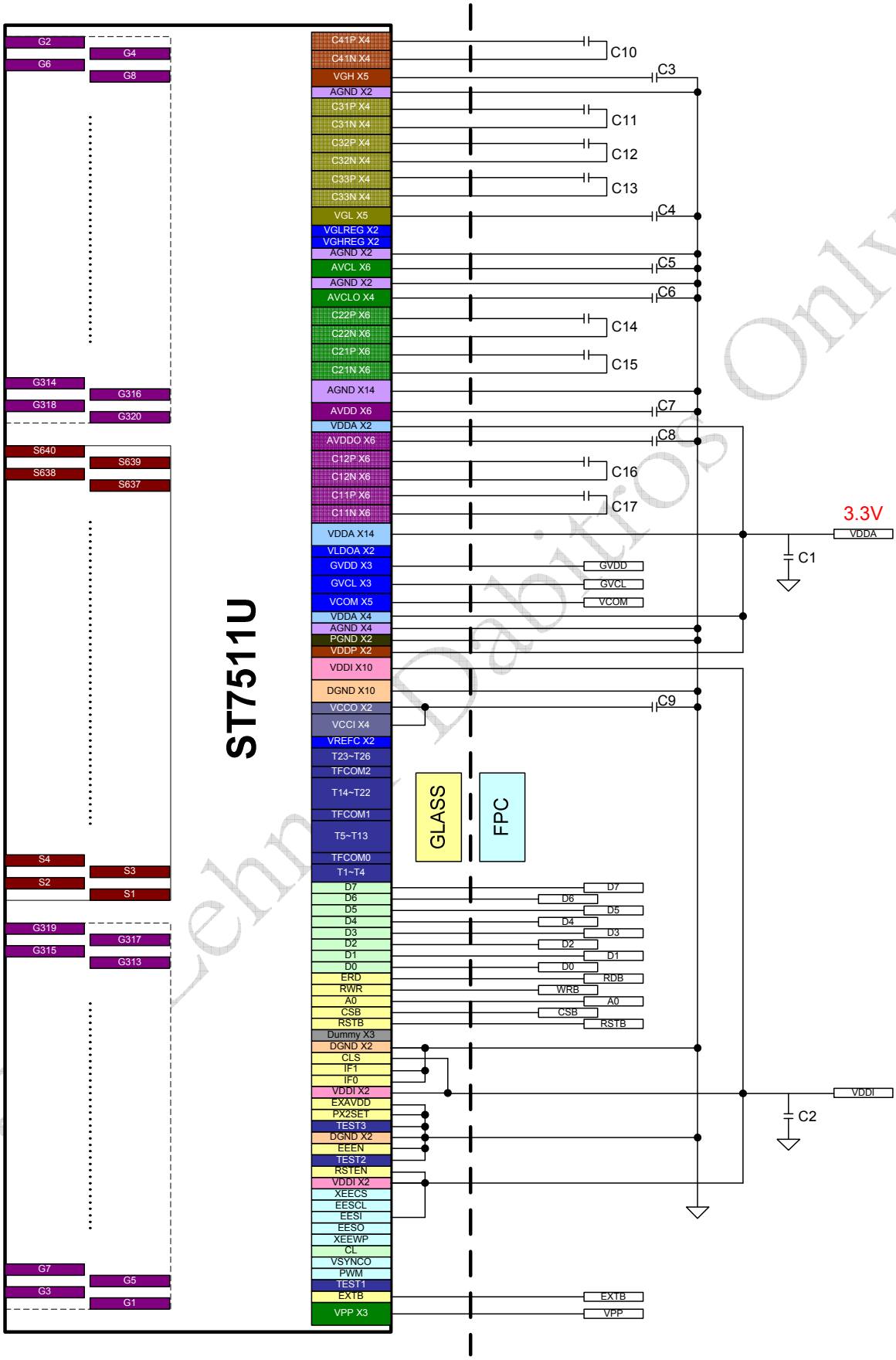
12.1 6800 Interface with VDDA=VDDP=3.3V



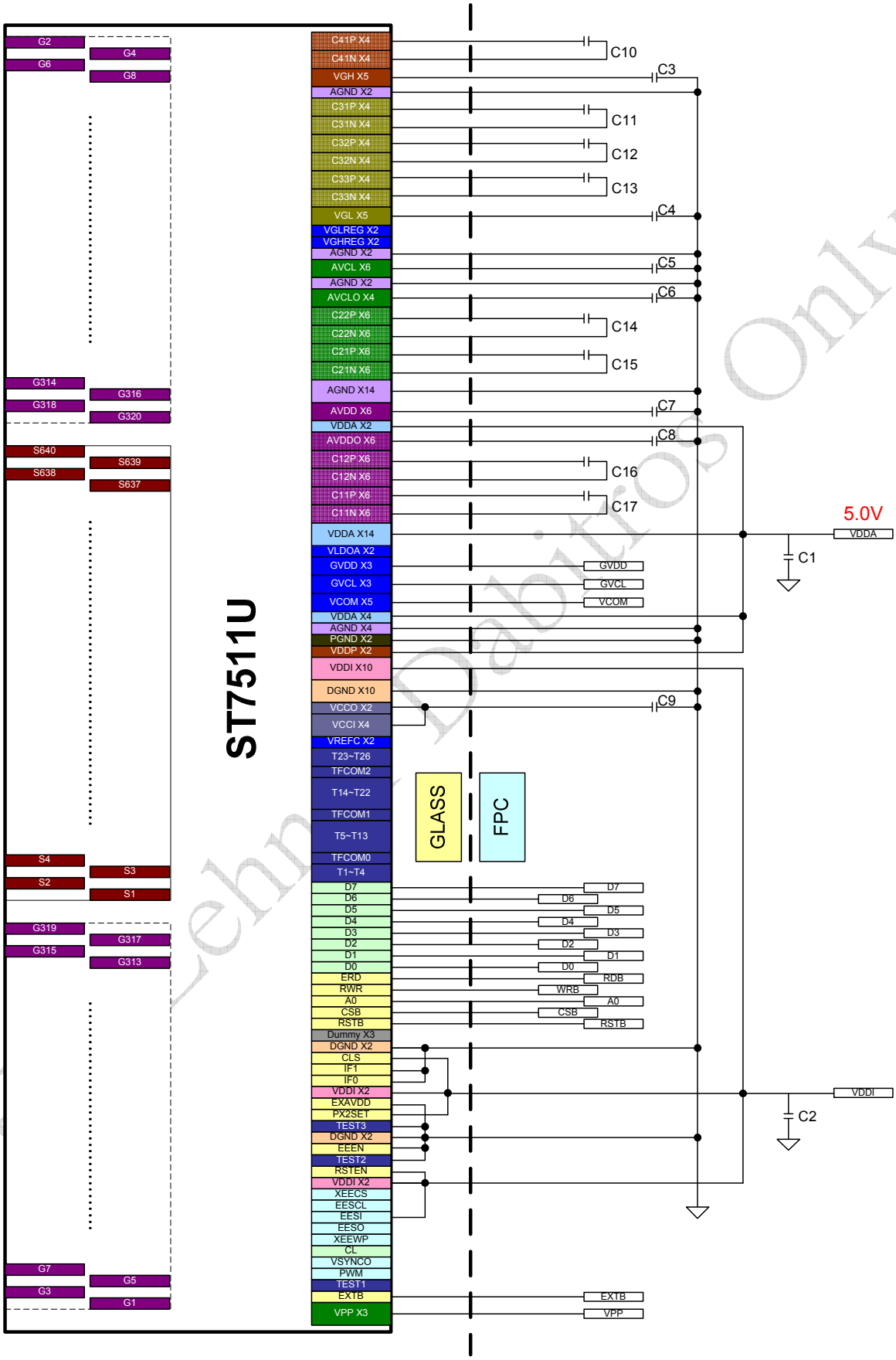
12.2 6800 Interface with VDDA=VDDP=5.0V



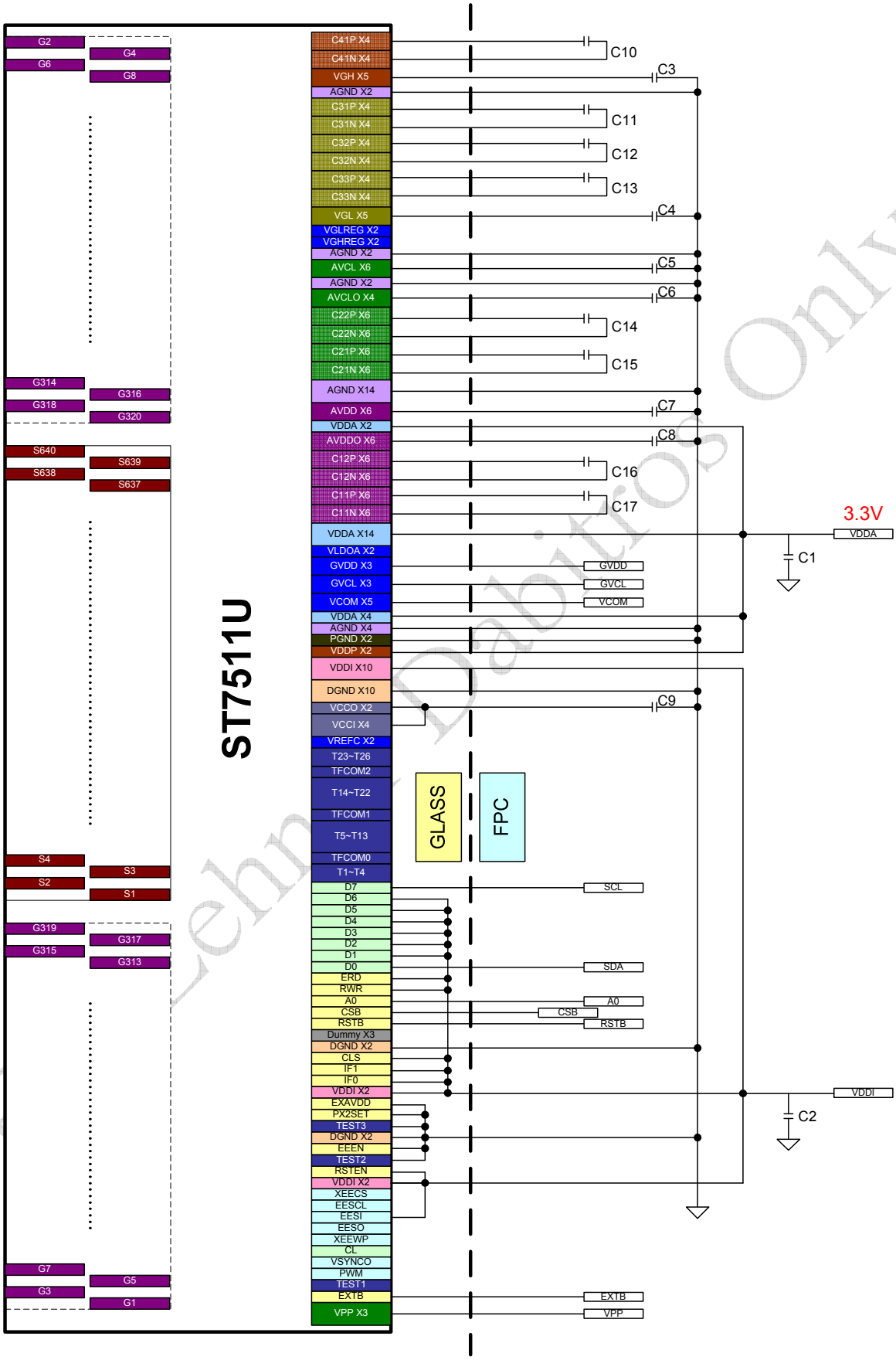
12.3 8080 Interface with VDDA=VDDP=3.3V



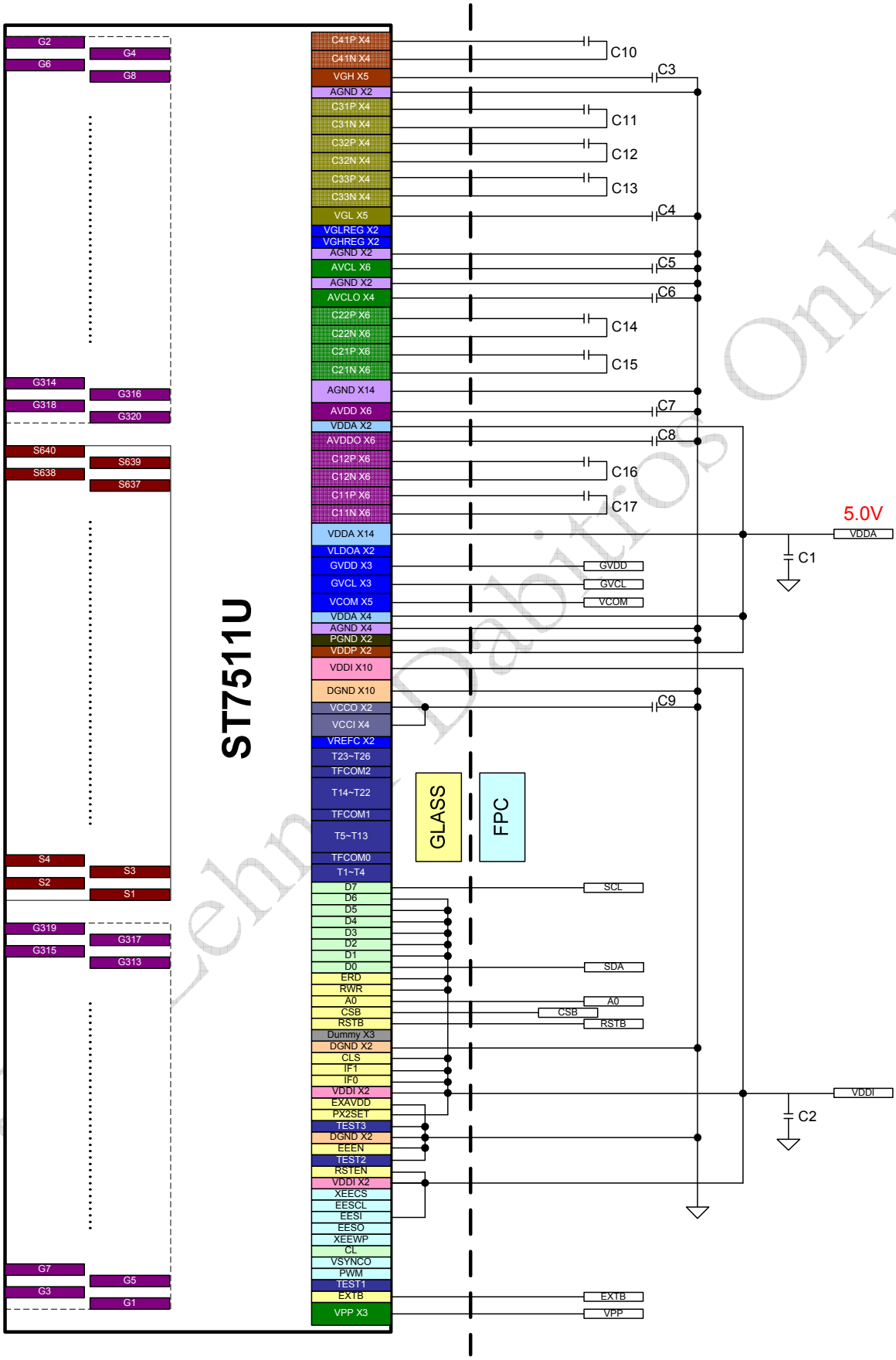
12.4 8080 Interface with VDDA=VDDP=5.0V



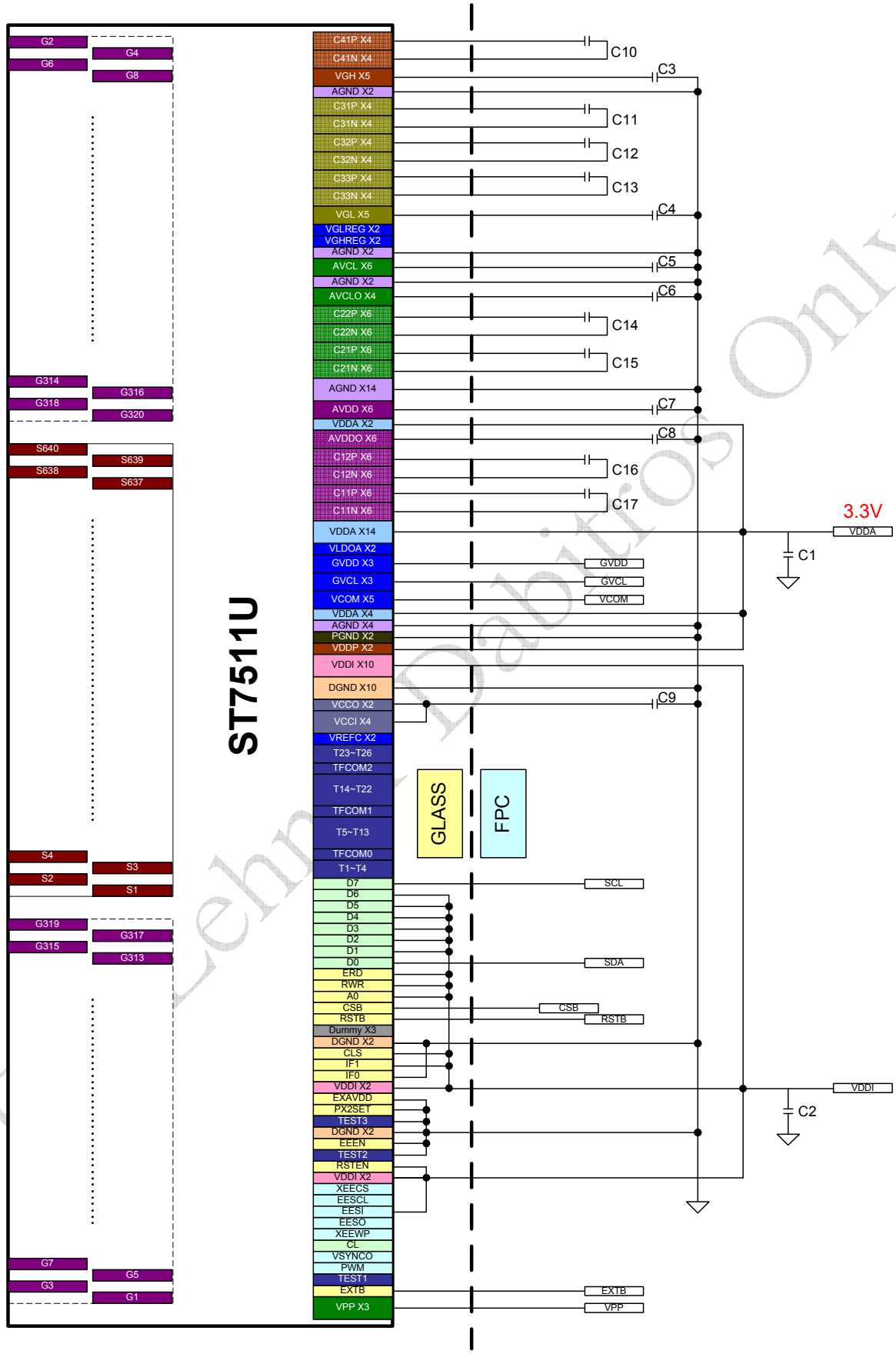
12.5 4SPI Interface with VDDA=VDDP=3.3V



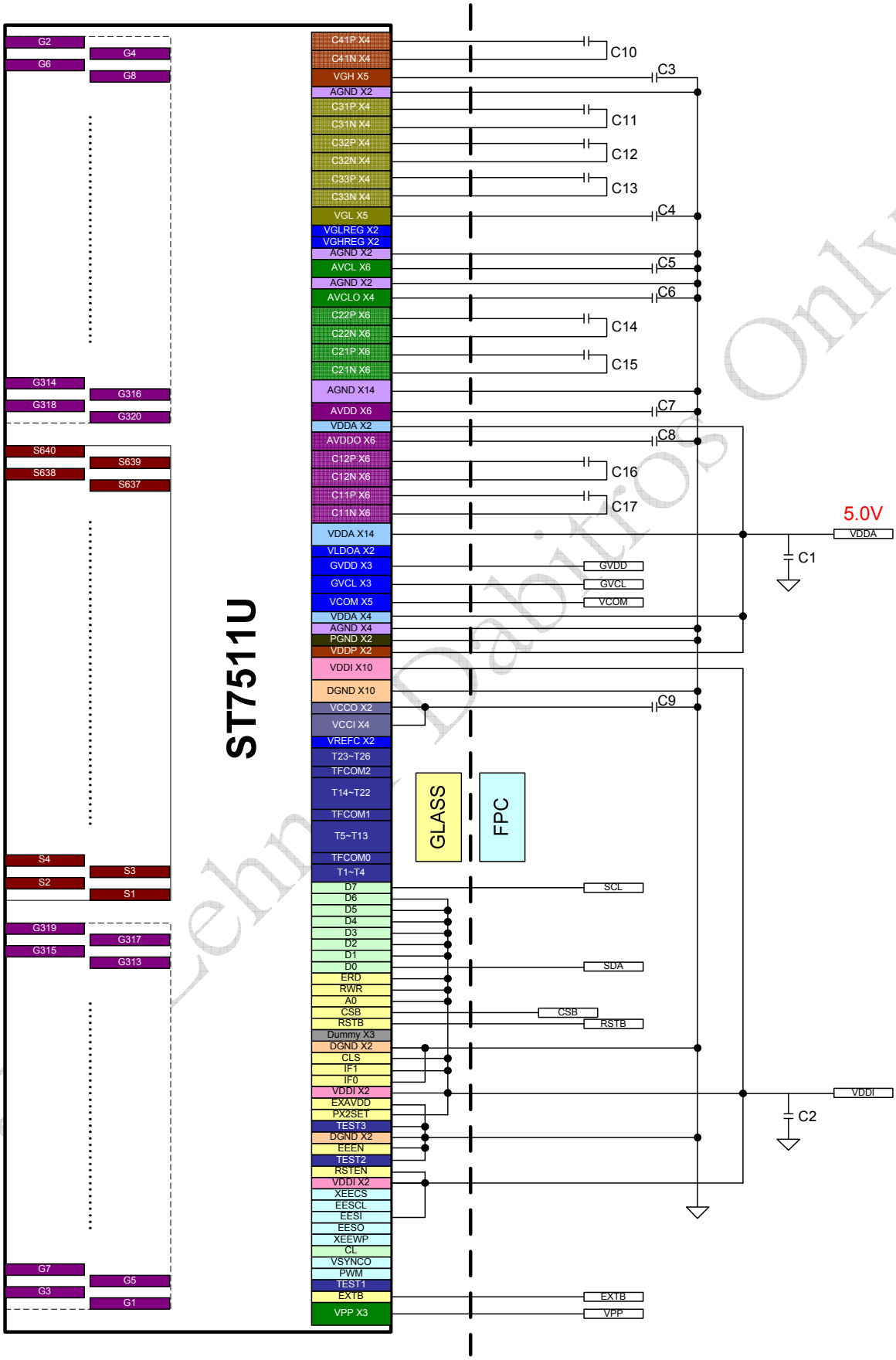
12.6 4SPI Interface with VDDA=VDDP=5.0V



12.7 3SPI Interface with VDDA=VDDP=3.3V



12.8 3SPI Interface with VDDA=VDDP=5.0V



13. REVERSION HISTORY

Version	Date	Description
0.0	2012/04	● Draft version.
0.1	2012/07/02	● Information correction ● Modify command table and descriptions
0.2	2012/07/06	● Modify pin descriptions ● Modify command table and descriptions ● Add the recommend resistance ● Add the connection diagram of external components ● Correct some typos
0.3	2012/07/23	● Change the connection of EESI from GND to VDDI
0.4	2012/07/27	● Add the linear coefficient of thermal expansion
0.5	2012/09/05	● Modify command table and descriptions ● Correct the scan mode diagrams ● Correct some typos
0.6	2012/09/21	● Modify pin descriptions ● Modify command table and descriptions ● Add the function of temperature compensation ● Add operation flow ● Add application circuits
0.7	2013/04/23	● Add the description of the partial display function ● Modify command table and descriptions ● Modify the operation flow ● Modify DC characteristics ● Modify AC characteristics
0.8	2013/04/26	● Modify the power on/off sequence
1.0	2013/07/25	● Modify DC characteristics ● Modify AC characteristics ● Correct some typos
1.1	2013/08/22	● Modify the temperature range