

ST25R3920

Datasheet - production data

Automotive high performance NFC reader for CCC digital key and car center console

VFQFPN32 (5x5 mm)

Features



- AEC-Q100 qualified
- Operating modes
 - Reader/writer
 - Card emulation
 - Active and passive peer to peer
- RF communication
 - EMVCo 3.0 analog and digital compliant
 - NFC-A / ISO14443A up to 848 kbit/s
 - NFC-B / ISO14443B up to 848 kbit/s
 - NFC-F / FeliCa[™] up to 424 kbit/s
 - NFC-V / ISO15693 up to 53 kb/s
 - NFC-A / ISO14443A and NFC-F / FeliCa™ card emulation
 - Active and passive peer to peer initiator and target modes, up to 424 kbit/s
 - Low level modes to implement MIFARE Classic[®] compliant or other custom protocols
- Key features
 - Dynamic power output (DPO) controls the field strength to stay within given limits
 - Active wave shaping (AWS) reduces overand under-shoots
 - Noise suppression receiver (NSR) allows reception in noisy environment
 - Automatic antenna tuning (AAT) via variable capacitor

- Integrated EMVCo 3.0 compliant EMD handling
- Automatic gain control and squelch feature to maximize SNR
- Low power capacitive and inductive card detection
- Low power NFC active and passive target modes
- Adjustable ASK modulation depth, from 5 to 40%
- Integrated regulators to boost system PSRR
- AM/PM and I/Q demodulator with baseband channel summation or automatic channel selection
- Possibility to drive two independent single ended antennas
- Measurement of antenna voltage amplitude and phase, RSSI, on-chip supply and regulated voltages
- External communication interfaces
 - 512-byte FIFO
 - Serial peripheral interface (SPI) up to 5 Mbit/s
 - I2C with up to 400 kbit/s in Fast-mode,
 1 Mbit/s in Fast-mode Plus, and 3.4 Mbit/s in High-speed mode
- Electrical characteristics
 - Wide supply voltage and ambient temperature range (2.6 to 5.5 V from -40 °C to +105 °C, 2.4 to 5.5 V from -20 °C to +105 °C)
 - Wide peripheral communication supply range, from 1.65 to 5.5 V
 - Quartz oscillator capable of operating with 27.12 MHz crystal with fast start-up

This is information on a product in full production.

Contents

1	Appl	ications	11
2	Desc	ription	
	2.1	System	ı diagram
	2.2	Block d	liagram
		2.2.1	Transmitter
		2.2.2	Receiver
		2.2.3	Phase and amplitude detector
		2.2.4	Automatic antenna tuning (AAT)16
		2.2.5	A/D converter
		2.2.6	Capacitive sensor
		2.2.7	External field detector17
		2.2.8	Quartz crystal oscillator
		2.2.9	Power supply regulators
		2.2.10	POR and bias
		2.2.11	RC oscillator and Wake-up timer17
		2.2.12	TX encoding
		2.2.13	RX decoding
		2.2.14	FIFO
		2.2.15	Control logic
		2.2.16	Host interface
		2.2.17	Passive target memory
		2.2.18	P2RAM
3	Pin a	Ind sign	al description
4	Appl	ication i	information
	4.1	Power-	on sequence
	4.2	Operati	ing modes
		4.2.1	Transmitter
		4.2.2	Receiver
		4.2.3	Antenna tuning
		4.2.4	Capacitive sensor
		4.2.5	Wake-up mode



	4.2.6	Quartz crystal oscillator	. 32
	4.2.7	Timers	. 32
	4.2.8	A/D converter	. 35
	4.2.9	Phase and amplitude detector	. 35
	4.2.10	External field detector	. 36
	4.2.11	Power supply system	. 37
	4.2.12	Overshoot / undershoot protection	. 40
	4.2.13	Reader operation	. 40
	4.2.14	Listen mode	. 41
4.3	Comm	unication with an external microcontroller	. 44
	4.3.1	Interrupt interface	. 44
	4.3.2	Communication interface selection	. 45
	4.3.3	Serial peripheral interface (SPI)	. 45
	4.3.4	I2C interface	. 51
4.4	Direct of	commands	. 56
	4.4.1	Set default	. 57
	4.4.2	Stop all activities	. 58
	4.4.3	Clear FIFO	. 58
	4.4.4	Transmit commands	. 58
	4.4.5	NFC field ON commands	. 59
	4.4.6	Mask receive data and Unmask receive data	. 60
	4.4.7	Change AM modulation state	. 61
	4.4.8	Measure amplitude	. 61
	4.4.9	Reset RX gain	. 61
	4.4.10	Adjust regulators	. 61
	4.4.11	Measure phase	. 61
	4.4.12	Clear RSSI	. 62
	4.4.13	Transparent mode	. 62
	4.4.14	Calibrate capacitive sensor	. 62
	4.4.15	Measure capacitance	. 62
	4.4.16	Measure power supply	. 63
	4.4.17	Test access	. 63
4.5	Registe	ers	. 65
	4.5.1	IO configuration register 1	. 68
	4.5.2	IO configuration register 2	. 69
	4.5.3	Operation control register	. 70
	4.5.4	Mode definition register	. 71



4.5.5	Bit rate definition register	72
4.5.6	ISO14443A and NFC 106kb/s settings register	73
4.5.7	ISO14443B settings register 1	74
4.5.8	ISO14443B and FeliCa settings register	75
4.5.9	NFCIP-1 passive target definition register	76
4.5.10	Stream mode definition register	77
4.5.11	Auxiliary definition register	78
4.5.12	EMD suppression configuration register	79
4.5.13	Subcarrier start timer register	80
4.5.14	Receiver configuration register 1	81
4.5.15	Receiver configuration register 2	82
4.5.16	Receiver configuration register 3	83
4.5.17	Receiver configuration register 4	83
4.5.18	P2P receiver configuration register 1	84
4.5.19	Correlator configuration register 1	85
4.5.20	Correlator configuration register 2	86
4.5.21	Mask receive timer register	87
4.5.22	No-response timer register 1	88
4.5.23	No-response timer register 2	88
4.5.24	Timer and EMV [®] control register	89
4.5.25	General purpose timer register 1	90
4.5.26	General purpose timer register 2	90
4.5.27	PPON2 field waiting register	91
4.5.28	Squelch timer register	92
4.5.29	NFC field on guard timer register	92
4.5.30	Mask main interrupt register	93
4.5.31	Mask timer and NFC interrupt register	93
4.5.32	Mask error and wake-up interrupt register	94
4.5.33	Mask passive target interrupt register	94
4.5.34	Main interrupt register	95
4.5.35	Timer and NFC interrupt register	96
4.5.36	Error and wake-up interrupt register	97
4.5.37	Passive target interrupt register	98
4.5.38	FIFO status register 1	99
4.5.39	FIFO status register 2	99
4.5.40	Collision display register1	00
4.5.41	Passive target display register1	01



4.5.42	Number of transmitted bytes register 1
4.5.43	Number of transmitted bytes register 2 102
4.5.44	Bit rate detection display register
4.5.45	A/D converter output register
4.5.46	Antenna tuning control register 1 105
4.5.47	Antenna tuning control register 2 105
4.5.48	TX driver register
4.5.49	Auxiliary modulation setting register
4.5.50	Passive target modulation register
4.5.51	TX driver timing register
4.5.52	External field detector activation threshold register
4.5.53	Resistive AM modulation register
4.5.54	External field detector deactivation threshold register
4.5.55	TX driver timing display register
4.5.56	Regulator voltage control register
4.5.57	Regulator display register
4.5.58	RSSI display register 119
4.5.59	Gain reduction state register
4.5.60	Capacitive sensor control register
4.5.61	Capacitive sensor display register
4.5.62	Auxiliary display register
4.5.63	Overshoot protection configuration register 1
4.5.64	Overshoot protection configuration register 2
4.5.65	Undershoot protection configuration register 1
4.5.66	Undershoot protection configuration register 2
4.5.67	Wake-up timer control register 125
4.5.68	Amplitude measurement configuration register
4.5.69	Amplitude measurement reference register
4.5.70	Amplitude measurement auto-averaging display register
4.5.71	Amplitude measurement display register
4.5.72	Phase measurement configuration register
4.5.73	Phase measurement reference register
4.5.74	Phase measurement auto-averaging display register
4.5.75	Phase measurement display register
4.5.76	Capacitance measurement configuration register
4.5.77	Capacitance measurement reference register
4.5.78	Capacitance measurement auto-averaging display register



8	Revi	sion hist	ory	50
7	Orde	ering info	prmation	19
	6.1	VFQFP	N32 package information 14	47
6	Pack	kage info	rmation	17
	5.6	I2C inter	rface characteristics 14	42
	5.5	SPI inte	rface characteristics	40
	5.4	Electrica	al characteristics	36
	5.3	DC/AC o	characteristics for digital inputs and outputs	35
	5.2	Operatir	ng conditions	34
	5.1	Absolute	e maximum ratings	33
5	Elec	trical cha	aracteristics	33
		4.5.80	IC identity register	32
		4.5.79	Capacitance measurement display register 1	31



List of tables

Table 1.	ST25R3920 - VFQFPN32 pin assignment	19
Table 2.	RX channel selection	24
Table 3.	Low-pass control	26
Table 4.	First and third zero setting	26
Table 5.	PT_Memory address space	43
Table 6.	NFC-212/424k SENS_RES format	43
Table 7.	IRQ output	44
Table 8.	Serial data interface (4-wire interface) signal lines	46
Table 9.	SPI operation modes	47
Table 10.	I2C interface and interrupt signal lines	52
Table 11.	List of direct commands	56
Table 12.	Timing parameters of NFC field ON commands	60
Table 13.	Analog test and observation register 1	
Table 14.	Test access register - Signal selection of CSI and CSO pins	
Table 15.	List of registers - Space A.	
Table 16.	List of registers - Space B.	
Table 17.	IO configuration register 1	
Table 18.	IO configuration register 2	
Table 19.	Operation control register	
Table 20.	Mode definition register	
Table 21.	Initiator operation modes	
Table 22.	Target operation modes	
Table 23.	Bit rate definition register	
Table 24.	Bit rate coding.	
Table 25.	ISO14443A and NFC 106kb/s settings register	
Table 26.	ISO14443A modulation pulse width	
Table 20. Table 27.	ISO14443B settings register 1	
Table 28.	ISO14443B and FeliCa settings register	
Table 20.	Minimum TR1 codings	
Table 30.	NFCIP-1 passive target definition register	
Table 30. Table 31.		
Table 31. Table 32.	Stream mode definition register	
Table 32. Table 33.	Sub-carrier frequency definition for Sub-carrier stream mode	
Table 33. Table 34.	Definition of time period for Stream mode Tx modulator control.	
	Auxiliary definition register	
Table 35.	RW receiver operation	
Table 36.	EMD suppression configuration register	
Table 37.	Subcarrier start timer register	
Table 38.	Receiver configuration register 1	
Table 39.	Receiver configuration register 2	
Table 40.	Receiver configuration register 3	
Table 41.	Receiver configuration register 4	
Table 42.	P2P receiver configuration register 1	
Table 43.	OOK threshold level settings	
Table 44.	Correlator configuration register 1	
Table 45.	Correlator configuration register 2	
Table 46.	Mask receive timer register.	
Table 47.	No-response timer register 1	
Table 48.	No-response timer register 2	88



Table 49.	Timer and EMV control register	
Table 50.	Trigger sources	
Table 51.	General purpose timer register 1	
Table 52.	General purpose timer register 2	
Table 53.	PPON2 field waiting register	91
Table 54.	Squelch timer register	92
Table 55.	NFC field on guard timer register	92
Table 56.	Mask main interrupt register	93
Table 57.	Mask timer and NFC interrupt register	93
Table 58.	Mask error and wake-up interrupt register	94
Table 59.	Mask passive target interrupt register.	94
Table 60.	Main interrupt register.	95
Table 61.	Timer and NFC interrupt register	
Table 62.	Error and wake-up interrupt register	
Table 63.	Passive target interrupt register	
Table 64.	FIFO status register 1	
Table 65.	FIFO status register 2	
Table 66.	Collision display register	
Table 67.	Passive target display register	
Table 68.	Number of transmitted bytes register 1	
Table 69.	Number of transmitted bytes register 2	
Table 70.	Bit rate detection display register	
Table 71.	A/D converter output register	
Table 72.	Antenna tuning control register 1	
Table 73.	Antenna tuning control register 2	
Table 74.	TX driver register	
Table 74.	AM modulation index	
Table 75.	RFO driver resistance	
Table 70.	Auxiliary modulation setting register	
Table 77. Table 78.	Passive target modulation register	
Table 78.	Passive target modulated and unmodulated state driver output resistance	
Table 79. Table 80.	TX driver timing register	
Table 80. Table 81.	External field detector activation threshold register	
Table 82.	Resistive AM modulation register	
Table 83.	Resistive AM modulated state driver output resistance	
Table 84.	External field detector deactivation threshold register	
Table 85.	Peer detection threshold as seen on RFI1 input.	
Table 86.	Collision avoidance threshold as seen on RFI1 input.	
Table 87.	TX driver timing display register	
Table 88.	Regulator voltage control register	
Table 89.	Regulator display register	
Table 90.	Regulated voltages	
Table 91.	RSSI display register 1	
Table 92.	RSSI	
Table 93.	Gain reduction state register	
Table 94.	Capacitive sensor control register 1	
Table 95.	Capacitive sensor display register 1	
Table 96.	Auxiliary display register	
Table 97.	Overshoot protection configuration register 11	23
Table 98.	Overshoot protection configuration register 2 1	23
Table 99.	Undershoot protection configuration register 11	24
Table 100.	Undershoot protection configuration register 2 1	



Table 101.	Wake-up timer control register
Table 102.	Typical wake-up time
Table 103.	Amplitude measurement configuration register
Table 104.	Amplitude measurement reference register
Table 105.	Amplitude measurement auto-averaging display register
Table 106.	Amplitude measurement display register
Table 107.	Phase measurement configuration register
Table 108.	Phase measurement reference register
Table 109.	Phase measurement auto-averaging display register
Table 110.	Phase measurement display register
Table 111.	Capacitance measurement configuration register
Table 112.	Capacitance measurement reference register
Table 113.	Capacitance measurement auto-averaging display register
Table 114.	Capacitance measurement display register
Table 115.	IC identity register
Table 116.	Absolute maximum ratings
Table 117.	Operating conditions
Table 118.	Characteristics of CMOS I/Os
Table 119.	ST25R3920 electrical characteristics (VDD = 3.3 V)
Table 120.	ST25R3920 electrical characteristics (VDD = 5.5 V)
Table 121.	ST25R3920 electrical characteristics (VDD = 2.4 V)
Table 122.	SPI characteristics (5 MHz) 140
Table 123.	AC measurement conditions
Table 124.	AC measurement conditions - I2C configuration
Table 125.	Input parameters
Table 126.	DC characteristics
Table 127.	100 kHz AC characteristics
Table 128.	400 kHz AC characteristics
Table 129.	1 MHz AC characteristics
Table 130.	3.4 MHz AC characteristics
Table 131.	VFQFPN32 mechanical data
Table 132.	Document revision history



List of figures

Figure 1.	Minimum system configuration - Single sided antenna driving	13
Figure 2.	Minimum system configuration - Differential antenna driving	14
Figure 3.	ST25R3920 block diagram	15
Figure 4.	ST25R3920 pinout (top view)	19
Figure 5.	Receiver block diagram	
Figure 6.	Capacitive sensor block diagram	30
Figure 7.	Phase detector inputs and output in case of 90° phase shift	36
Figure 8.	Phase detector inputs and output in case of 135° phase shift	36
Figure 9.	ST25R3920 power supply system	38
Figure 10.	Exchange of signals with a microcontroller.	46
Figure 11.	SPI communication: writing a single byte	48
Figure 12.	SPI communication: writing multiple bytes	48
Figure 13.	SPI communication: reading a single byte	49
Figure 14.	SPI communication: FIFO loading	49
Figure 15.	SPI communication: FIFO reading	50
Figure 16.	SPI communication: direct command	51
Figure 17.	SPI communication: direct command chaining	51
Figure 18.	Writing a single register	52
Figure 19.	Writing register data with auto-incrementing address	52
Figure 20.	Reading a single byte from a register	53
Figure 21.	FIFO load	53
Figure 22.	FIFO read	53
Figure 23.	Sending a direct command	
Figure 24.	Read and Write mode for register space-B access	
Figure 25.	I2C master reads slave immediately after the first byte	
Figure 26.	Direct command NFC initial field ON	
Figure 27.	Direct command NFC response field ON	
Figure 28.	SPI timing diagram - General operation 1	
Figure 29.	SPI timing diagram - Read operation 1	
Figure 30.	RPmin vs. VDD, fc = 3.4 MHz	
Figure 31.	Maximum Rbus value vs. bus parasitic capacitance, fc = 3.4 MHz 1	45
Figure 32.	I2C AC waveforms	
Figure 33.	I2C AC measurements 1	
Figure 34.	VFQFPN32 outline	
Figure 35.	VFQFPN32 footprint example	48



1 Applications

The ST25R3920 device is suitable for a wide range of NFC and HF RFID applications, among them

- CCC digital key NFC reader in locations like door handles, B-Pillars or center consoles
- NFC Forum compliant universal device for pairing applications
- Qi charging protection and NFC-based charging for in-car chargers
- EMVCo 3.0 compliant contactless payment terminal
- Original equipment, consumable and short range location detection inside a car
- ISO14443 and ISO15693 compliant general purpose NFC device
- FeliCa™ reader/writer
- Support of all five NFC Forum Tag types in reader mode
- Support of all common proprietary protocols, such as Kovio, CTS, B'.



2 Description

The ST25R3920 is an automotive grade high performance NFC universal device supporting NFC initiator, NFC target, NFC reader, and NFC card emulation modes.

Designed for CCC (car connectivity consortium) digital key applications, the ST25R3920 enables fast product development for car access/start applications in areas like door handle or center console, and enables additional functionality, like pairing or NFC card protection combined with a Qi charger. Being very robust and noise tolerant while at the same time reducing electromagnetic emission, the device works even under harsh conditions, enabling an easier certification.

The device includes an advanced analog front end (AFE) and a highly integrated data framing system for ISO18092 passive and active initiator, ISO 18092 passive and active target, NFC-A/B (ISO14443A/B) reader including higher bit rates, NFC-F (FeliCa[™]) reader, NFC-V (ISO15693) reader up to 53 kbps, and NFC-A / NFC-F card emulation.

Special stream and transparent modes of the AFE and framing system can be used to implement other custom protocols in reader or card emulation modes.

The ST25R3920 features high RF power with dynamic power output to directly drive antennas at high efficiency, achieving large interaction distance even with small antenna sizes common in door handles. The device include additional features, making it incomparable for low power applications. It offers low power card detection by performing a measurement of the amplitude or phase of the antenna signal while reducing power consumption to a minimum. Additionally, it contains a low power capacitive sensor to detect the presence of a card without switching on the reader field.

The ST25R3920 is designed to operate from a wide power supply range (2.6 to 5.5 V from -40 °C to +105 °C, 2.4 to 5.5 V from -20 °C to +105 °C), and a wide peripheral IO voltage range (from 1.65 to 5.5 V).

Due to this combination of high RF output power, low power modes, wide supply rangeand AEC-Q100 grade 2 qualification, the device is perfectly suited for automotive applications.



2.1 System diagram

Figure 1 and *Figure 2* show the minimum system configuration for, respectively, single ended and differential antenna configurations. Both include the EMC filter.

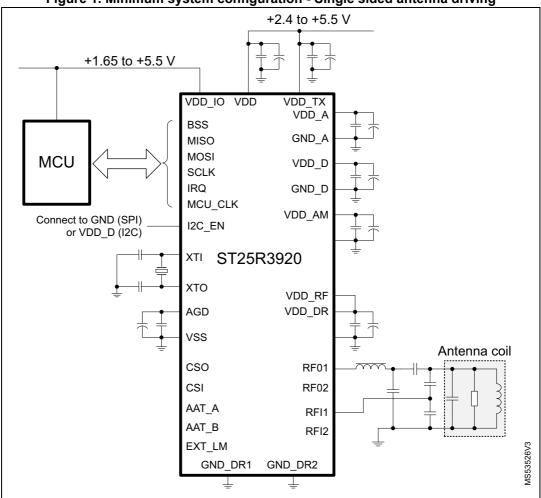


Figure 1. Minimum system configuration - Single sided antenna driving



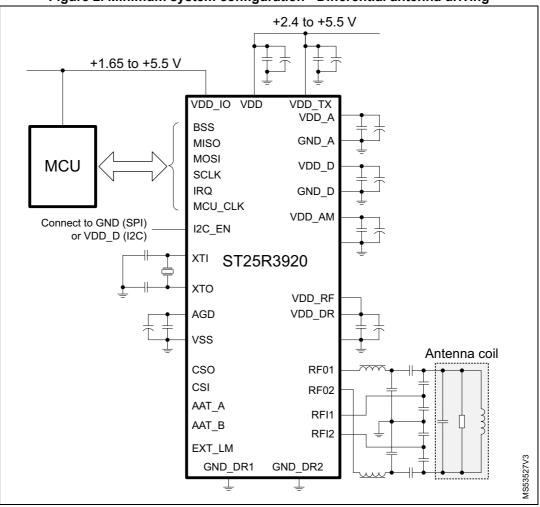
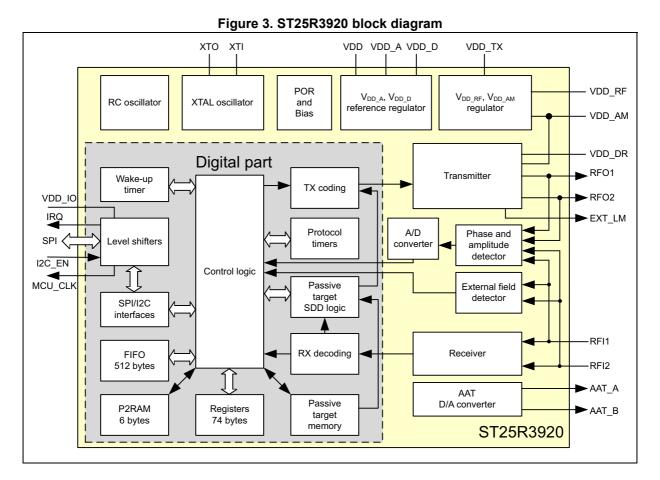


Figure 2. Minimum system configuration - Differential antenna driving



2.2 Block diagram

The ST25R3920 block diagram is shown in *Figure 3*. The main functions are described in the following subsections.



2.2.1 Transmitter

In reader mode, the transmitter drives an external antenna through pins RFO1 and RFO2 to generate the RF field. Single sided and differential antenna configurations are supported. The transmitter block also generates the OOK or AM modulation of the transmitted RF signal.

The transmitter can operate RFO1 and RFO2 independently, to drive up to two antennas in single ended configuration, or operate them together, to drive one antenna in differential configuration. The drivers are designed to drive directly one or more antennas integrated on the PCB, as well as antennas connected with 50 Ω cables. Some of the advanced features (such as antenna diagnostics) are not fully usable if the antenna is connected with a 50 Ω cable.

In card emulation mode, the transmitter generates the load modulation signal by changing the resistance of the internal antenna driver connected to the antenna via RFO1 and RFO2. To generate the load modulation signal, the transmitter can also drive an external MOS transistor via the EXT_LM pin.



DS13261 Rev 10

2.2.2 Receiver

The receiver detects card modulation superimposed on the 13.56 MHz carrier signal. The receiver consists of two chains, built from a set of demodulators, followed by two gain and filtering stages, and a final digitizer stage. The demodulators can operate as AM/PM demodulator or as I/Q demodulator. The filter characteristics can be adjusted to match the selected RF mode and bit rate, to optimize performance (subcarrier frequencies from 212 to 848 kHz are supported). Apart from the filter stage, the receiver incorporates several other features (AGC, squelch) that enable reliable operation in noisy conditions.

The receiver is connected to the antenna via the pins RFI1 and RFI2. The output of the receiver is connected to the framing block that decodes the demodulated and digitized subcarrier signal.

2.2.3 Phase and amplitude detector

The phase detector measures the phase difference between the transmitter output signals (RFO1 and RFO2) and the receiver input signals (RFI1 and RFI2).

The amplitude detector measures the amplitude of the differential RF carrier signal between the receiver inputs RFI1 and RFI2. This differential amplitude signal is directly proportional to the amplitude of the RF signal on the antenna LC tank.

The phase and amplitude detectors are used for several purposes:

- PM demodulation, by observing RFI1 and RFI2 phase variations (LF signal is fed to the receiver)
- Average phase difference between RFOx pins and RFIx pins, to check antenna tuning
- Measure amplitude of signal present on pins RFI1 and RFI2, proportional to the antenna voltage

2.2.4 Automatic antenna tuning (AAT)

The AAT block consists of two independent 8-bit D/A converters. These converters generate a programmable voltage (from 0 to 3.3 V) to control external variable capacitors.

Note: Using hardware based wake-up in combination with the automatic antenna tuning feature is not recommended. Contact your nearest ST office for further support.

2.2.5 A/D converter

A built-in A/D converter, whose input can be multiplexed from different sources, is used for the diagnostic functions and the low power card detection. The result of the A/D conversion is stored in a register that can be read through the host interface.

2.2.6 Capacitive sensor

The capacitive sensor is used to implement low power detection of card presence. It measures the capacitance between two copper patches connected to the CSI and CSO pins. This capacitance changes with the presence of an object like a card, or a hand.

During calibration the reference capacitance (representing parasitic capacitance of the environment) is stored. In the capacitive low power card detection mode the device periodically measures the capacitance and compares the measured value to the stored reference value. If the measured capacitance differs from the stored reference value by more than a register defined threshold then an interrupt is sent to the external controller.



2.2.7 External field detector

This is a low power block used in the active or passive target mode to detect the presence of an external RF field. It supports two different external field detection thresholds, namely Peer detection and Collision avoidance threshold.

The Peer detection threshold is used in the active and passive peer to peer modes to detect when the peer device turns on its RF field.

The Collision avoidance threshold is used to detect the presence of an external RF field during the RF collision avoidance procedure.

2.2.8 Quartz crystal oscillator

The quartz crystal oscillator operates with 27.12 MHz crystals. At start-up the transconductance of the oscillator is increased to achieve a fast start-up. Since the start-up time varies with crystal type, temperature and other parameters, the oscillator amplitude is observed and an interrupt is generated when stable oscillator operation is reached.

The oscillator block also provides a clock signal to the external microcontroller (MCU_CLK), according to the settings in the *IO configuration register 1*.

2.2.9 **Power supply regulators**

The integrated power supply regulators ensures a high power supply rejection ratio (PSRR) for the complete system.

Three voltage regulators, one for the analog block, one for the digital block, and one for the RF output drivers, are available to decouple noise sources from the ST25R3920. A fourth voltage regulator generates the reference voltage for the analog receivers (AGDC, analog ground).

The RF output driver voltage regulator can be configured automatically by the device, based on the systems power supply stability and RF output power (see *Section 4.4.10: Adjust regulators* for more details).

2.2.10 POR and bias

This block provides bias currents and reference voltages to all other blocks. It also incorporates a Power on Reset (POR) circuit that provides a reset at power-up and at low supply levels.

2.2.11 RC oscillator and Wake-up timer

The ST25R3920 include several possibilities for low power detection of a card presence (capacitive sensor, phase measurement, amplitude measurement). The RC oscillator and the register configurable Wake-up timer are used to periodically trigger the card presence detection in the low power card detection modes.

Note: The usage of hardware based wake-up in combination with the automatic antenna tuning feature is not recommended. Contact your nearest ST office for further support.



2.2.12 TX encoding

This block encodes the transmit frames according to the selected RF mode and bit rate. The SOF (start of frame), EOF (end of frame), CRC, and parity bits are generated automatically. The data to transmit are taken from the FIFO.

In Stream mode the framing is bypassed. The FIFO data directly define the modulation data sent to the transmitter.

In Transparent mode, the framing and FIFO are bypassed, and the MOSI pin directly drives the modulation of the transmitter.

2.2.13 RX decoding

This block decodes received frames according to the selected RF mode and bitrate. The SOF (start of frame), EOF (end of frame), CRC, and parity bits are automatically checked, all of them (except the CRC bit) are removed by this block. The received data are written to the FIFO.

In Stream mode the framing is bypassed. The digitized subcarrier signal is directly stored in the FIFO.

In Transparent mode the framing and FIFO are bypassed. The digitized subcarrier signal directly drives the MISO pin.

2.2.14 FIFO

The ST25R3920 contains a 512-byte FIFO. Depending on the direction of the data transfer, it contains either data received, or data to be transmitted.

In reader mode the ST25R3920 can transmit frames of up to 8191 bytes length and receive frames of arbitrary length.

2.2.15 Control logic

The control logic contains I/O registers that define the operation of device.

2.2.16 Host interface

A 4-wire serial peripheral interface (SPI) and a 2-wire I2C interface are available to communicate with an external microcontroller. The pins for the SPI and the I2C interface are shared, and pin I2C_EN is used to select the active interface.

2.2.17 Passive target memory

The device contains a 48-byte RAM to store configuration data for the passive target and card emulation mode.

2.2.18 P2RAM

The P2RAM stores information on wafer number, die position, device subversion, and I2C address. The P2RAM is programmed during production.



3 Pin and signal description

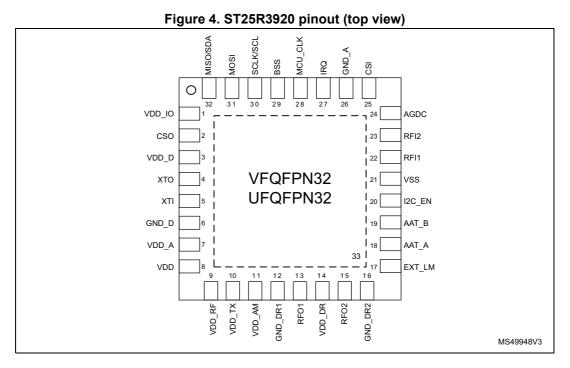


Table 1. ST25R3920 - VFQFPN32 pin assignment

VFQFPN32	Name	Type ⁽¹⁾	Description	
1	VDD_IO	Р	Positive supply for peripheral communication	
2	CSO	AO	Capacitor sensor output / Test output 2	
3	VDD_D	AO	Digital supply regulator output	
4	XTO	AO	X'tal oscillator output	
5	XTI	AI/DI	X'tal oscillator input, in test mode used as digital input (clock)	
6	GND_D	Р	Digital ground	
7	VDD_A	AO	Analog supply regulator output	
8	VDD	Р	External positive supply	
9	VDD_RF	AO	Regulated driver supply for antenna drivers	
10	VDD_TX	Р	External positive supply for the TX part	
11	VDD_AM	AO	Regulated driver supply for AM modulation	
12	GND_DR1	Р	Antenna driver ground, including driver V _{SS}	
13	RF01	AO	Antenna driver output	
14	VDD_DR	Р	Antenna driver positive supply input	
15	RFO2	AO	Antenna driver output	
16	GND_DR2	Р	Antenna driver ground, including driver V _{SS}	
17	EXT_LM	AO	External load modulation MOS gate driver	



DS13261 Rev 10

VFQFPN32 Name Type ⁽¹⁾ Description				
18	AAT_A	AO	AAT tune voltage for variable capacitor AAT_A	
19	AAT_B	AO	AAT tune voltage for variable capacitor AAT_B	
20	I2C_EN	DI	I2C interface enable (V _{DD_D} level)	
21	VSS	Р	Ground, die substrate potential	
22	RFI1	AI	Receiver input	
23	RFI2	AI	Receiver input	
24	AGDC	AIO	Analog reference voltage	
25	CSI	AIO	Capacitor sensor input / Test output 1	
26	GND_A	Р	Analog ground	
27	IRQ	DO	Interrupt request output	
28	MCU_CLK	DO	Clock output for MCU	
29	BSS	DI	SPI enable (active low)	
30	SCLK	DI	SPI clock / I2C clock	
31	MOSI	DI	SPI data input	
32	MISO	DO_T	Serial peripheral interface data output / I2C data line	
33	NA	Р	Thermal pad	

Table 1. ST25R3920 - VFQFPN32 pin assignment (continued)

1.

P: Power supply pin AIO: analog I/O, AI: analog input, AO: analog output DI: digital input, DIPD: digital input with pull-down, DO: digital output, DO_T: digital output/tri-state, DIO: digital bidirectional.



4 Application information

4.1 Power-on sequence

Once powered, the device enters the Power-down mode where the content of all registers is set to its default state.

To prevent the internal overheat protection to trigger below the junction temperature, the 3-byte frame FCh / 04h / 10h (register access / address / value) has to be sent after power-on and Set default command.

The next steps are basic configurations of the IC:

- 1. The *IO configuration register 1* and *IO configuration register 2* must be properly configured.
- 2. The internal voltage regulators have to be configured. It is recommended to use direct command Adjust regulators to improve the system PSRR.
- 3. If AAT is used the tuning procedure must be performed.

After the sequence of events mentioned above the devices are ready to operate.

4.2 Operating modes

The ST25R3920 operating mode is defined by the contents of the *Operation control register*. At power-on all its bits are set to 0, the ST25R3920 is in Power-down mode. In this mode, the AFE static power consumption is minimized, as only the POR and part of the bias are active. The regulator itself is disabled.

The SPI/I2C is still functional in this mode and all required settings on the configuration registers can be done. The PT_memory and FIFO are not accessible in this mode.

Bit en (bit 7 of the *Operation control register*) is controlling the quartz crystal oscillator, regulators and AAT control output pins. When this bit is set, the device enters in Ready mode and the quartz crystal oscillator and regulators are enabled. An interrupt is sent to inform the microcontroller when the oscillator amplitude and frequency is stable. The PT_memory and FIFO are accessible in this mode.

The enable of the receiver and the transmitter block are separated, it is possible to operate one without switching on the other (control bits rx_en and tx_en). This feature can be used when the reader field has to be maintained while no response from a tag is expected. Another example is NFCIP-1 active communication in receive mode configuration. The RF field is generated by the initiator on one side while the other side is only in receive operation.

Asserting the *Operation control register* bit wu while the other bits are set to 0 puts the ST25R3920 into the Wake-up mode, used to perform low power detection of card presence. In this mode the low power RC oscillator and register configurable wake-up timer are used to schedule periodic measurement(s). When a difference to the predefined reference is detected an interrupt is sent to wake up the MCU. Capacitive sensor, phase and amplitude measurement are available to trigger the wake-up.

4.2.1 Transmitter

The transmitter contains two identical push-pull driver blocks connected to pins RFO1 and RFO2. These drivers are differentially driving the external antenna LC tank. It is also



possible to operate only one of the two drivers by setting the *IO configuration register 1* bit single and selecting which RFO/RFI to be use on bit rfo2.

Output resistance

Each driver is composed of eight segments having binary weighted output resistance. The MSB segment typical ON resistance is 4 Ω . When all segments are turned on, the output resistance is typically 2 Ω . Usually all segments are turned on to define the normal transmission (non-modulated) level. It is also possible to switch off certain MSB segments when driving the non-modulated level to drive the circuitry with a higher impedance driver.

The bits d_res<3:0> in the *TX driver register* define the resistance during the normal transmission. The default setting is minimum available resistance.

When using the single driver mode, the number and therefore the cost of the antenna LC tank components is halved, but also the output power is reduced. In single mode it is possible to connect two antenna LC tanks to the two RFO outputs and multiplex between them by controlling the *IO configuration register 1* bit rfo2.

To transmit data, the transmitter output level must be modulated. AM and OOK modulation principles are supported. The type of modulation is defined by setting bit tr_am in the *Mode definition register*.

Driver TX modulation

During the OOK modulation (e.g. for ISO14443A) the transmitter drivers stop driving the carrier frequency. As a consequence the amplitude of the antenna LC tank oscillation decays, the time constant of the decay is defined with the LC tank Q factor.

AM modulation (for example ISO14443B) is done via an additional regulator providing the supply voltage V_{DD} _{AM}, used as the driver supply voltage during the modulation state.

The AM modulation level is set by am_mod3:0 bits in the *TX driver register*.

AM modulation has to be manually enabled and the level to be set correctly for the following protocols:

- ISO14443B
- FeliCa
- ISO15693 (if not OOK)
- NFCIP-1 212 and 424 kb/s initiator or active target.

Depending on the applicable standard the modulation index can be set in a range between 5 and 30% in the *TX driver register*.

Passive load modulation

The ST25R3920 enables passive load modulation using two different methods

- Internal driver load modulation
- Load modulation with an external MOS transistor and a diode that directly loads the antenna circuit

The driver load modulation is selected by bit Im_dri and the external MOS modulation is selected by Im_ext option bits.

Normally, the internal driver or the external load modulation should be used exclusively, but the device also allows simultaneous modulation.



The driver load modulation is based on the change of driver impedance. Typically, a high impedance during non-modulated state and a lower impedance for the modulated state is used. This yields modulation phase equal to passive tag modulation. It is also possible to reverse the polarity of the driver load modulation by using low impedance during non-modulated state and higher impedance for the modulated state.

During the non-modulated state the output impedance is defined by pt_res3:0 option bits. During modulation the output impedance is defined by ptm_res3:0 option bits.

Load modulation through an external MOS transistor and a diode is selected by the Im_ext option bit. In this case the EXT_LM pin is driven by the digital representation of the load modulation signal (848 kHz subcarrier or 424 / 212 kHz modulation signal). The EXT_LM is used to drive a gate of the external modulation MOS. The bit Im_ext_pol sets inverse polarity for the external load modulation.

The pt_res3:0 and ptm_res3:0 bits must be set prior entering passive target mode (reg 03h), because in passive target mode the resistance value propagates through the TX driver only when the extracted clock is available.

Driver load modulation is based on change of the driver impedance. Typically high impedance is used during non-modulated state, and decreased for modulated state, resulting in modulation phase equal to Passive tag modulation.

It is also possible to set inverse polarity driver load modulation by using low impedance during non-modulated state and higher impedance for the modulated state.

During non-modulated / modulated state the output impedance is defined, respectively, by pt_res3:0 / ptm_res3:0 option bits.

An external MOS transistor and a diode modulation is selected by Im_ext option bit. In this case the EXT_LM pin is driven by digital representation of the load modulation signal (848 kHz subcarrier or 424 / 212 kHz modulation signal). The EXT_LM is used to drive a gate of the external modulation MOS.

Bit Im_ext_pol sets inverse polarity for the External load modulation.

Bits pt_res<3:0> and ptm_res<3:0> must be set before entering Passive target mode (reg 03h), as in Passive target mode the resistance value propagates through the TX driver only when extracted clock is available (during PT data transmission, including FDT).

Slow transmitter ramping

When the transmitter is enabled it starts to drive the antenna LC tank with full power, the ramping of field emitted by antenna is defined by antenna LC tank Q factor.

However there are some reader systems where the reader field has to ramp up with a longer transition time when it is enabled. The STIF (Syndicat des transports d'Ile de France) specification requires a transition time from 10 to 90% of field longer than or equal to 10 μ s.

The ST25R3920 supports slow transmitter ramping by collapsing VDD_RF regulated voltage when transmitter is disabled and ramping it when transmitter is enabled. Typical transition time is 15 µs at 3 V supply and 20 µs at 5 V supply.

Procedure to implement the slow transition:

- When transmitter is disabled set *IO configuration register 2* bit slow_up to 1. Keep this state at least 2ms to allow discharge of V_{DD RF}.
- 2. Enable transmitter, its output will ramp slowly
- 3. Before sending any command set the bit slow_up back to 0.



4.2.2 Receiver

The receiver performs demodulation of the tag subcarrier modulation that is superimposed on the 13.56 MHz carrier frequency. It performs AM/PM or I/Q demodulation, amplification, band-pass filtering and digitalization of subcarrier signals. It also performs RSSI measurement, automatic gain control (AGC) and Squelch function.

The reception chain has two separate channels for AM and PM demodulation. When both channels are active the selection for reception framing is done automatically by the receiver logic. The receiver is switched on when *Operation control register* bit rx_en is set to 1.

The *Operation control register* contains bits rx_chn and rx_man, which define whether only one or both demodulation channels are active:

- bit rx_man defines the channel selection mode when both channels are active (automatic or manual)
- bit ch_sel defines which channel is used for decoding.

rx_chn	rx_man	ch_sel	Selected reception channel
0	0	х	Automatic selection
0	1	0	AM or I channel
0	1	1	PM or Q channel
1	х	0	AM or I channel
1	х	1	PM or Q channel

Table 2. RX channel selection



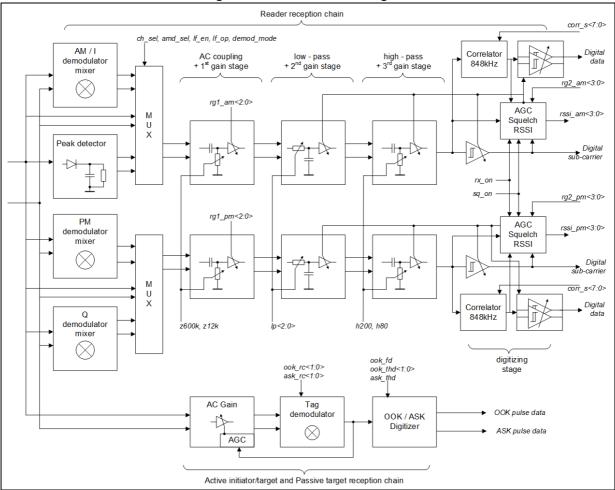


Figure 5. Receiver block diagram

Demodulation stage

The first stage performs demodulation of the tag subcarrier response signal, superimposed on the HF field carrier. Two different blocks are implemented for the AM demodulation:

- peak detector
- AM/I or PM/Q demodulator mixer.

The choice of the used demodulator is made by the *Receiver configuration register 2* bit amd_sel.

The peak detector performs AM demodulation using a peak follower. Both the positive and negative peaks are tracked to suppress any common mode signals. Its demodulation gain is G = 0.7 and the input is taken from RFI1 demodulator input only.

The AM demodulator mixer uses synchronous rectification of both receiver inputs (RFI1 and RFI2). Its gain is G = 0.55. The PM demodulation is also done by a mixer. The PM demodulator mixer has differential outputs with 60 mV differential signal for 1% phase change (16.67 mV / $^{\circ}$).

The I/Q demodulation is composed of two mixer circuits, driven with a 90° shifted local oscillator (LO) signals derived from the crystal oscillator. The outputs of the two mixers are connected to two equal base band reception chains and to the decoding logic.



Filtering and gain stages

The receiver chain has band pass filtering characteristics. The filtering is optimized to pass subcarrier frequencies while rejecting carrier frequency, low frequency noise and DC component. Filtering and gain is implemented in three stages, the first and the last stage have first order high pass characteristics while the mid stage has second order low-pass characteristic.

The gain and filtering characteristics can be optimized depending on the application by writing the *Receiver configuration register 1* (filtering), *Receiver configuration register 3* (primarily gain in first stage) and *Receiver configuration register 4* (gain in second and third stage).

The gain of first stage is around 20 dB and can be reduced in six 2.5 dB steps. There is also a special boost mode available, which increases the max gain by additional 5.5 dB. The first stage gain can only be modified by writing *Receiver configuration register 3*. The default setting of this register is the minimum gain. Default first stage zero is located at 60 kHz, it can also be lowered to 40 or 12 kHz by writing option bits in the *Receiver configuration register 1*. The first stage can be reconfigured to second order high-pass at 600 kHz by option bit z600k. The control of the first and third stage zeros is done with common control bits (see *Table 4*).

rec1<4>lp1	rec1<3>lp0	-1 dB point				
0	0	1200 kHz				
0	1	600 kHz				
1	0	300 kHz				
0	0	2 MHz				
0	1	7 MHz				
Others	Not used					
	0 0 1 0 0	0 0 0 1 1 0 0 0 0 1				

Table 3. Low-pass control

rec1<3>z600k	rec1<2>h200	rec1<1>h80	rec1<0>z12k	First stage zero	Third stage zero
0	0	0	0	60 kHz	400 kHz
0	1	0	0	00 KHZ	200 kHz
0	0	1	0	40 kHz	80 kHz
0	0	0	1	12 kHz	200 kHz
0	0	1	1		80 kHz
0	1	0	1		200 kHz
1	0	0	0	600 kHz	400 kHz
1	1	0	0		200 kHz
Others			Not used		

Table 4. First and third zero setting

The gain in the second and third stage is 23 dB and can be reduced in six 3 dB steps. Gain of these two stages is included in AGC and Squelch loops or can be manually set in



Receiver configuration register 4. Sending of direct command Reset RX Gain is necessary to initialize the AGC, Squelch and RSSI block. Sending this command clears the current Squelch setting and loads the manual gain reduction from *Receiver configuration register 4.* Second stage has a second order low-pass filtering characteristic, the pass band is adjusted according to subcarrier frequency using the bits Ip2 to Ip0 of the *Receiver configuration register 1.* See *Table 3* for -1 dB cut-off frequency for different settings.

Digitizing stage

The digitizing stage produces a digital representation of the sub-carrier signal coming from the receiver. This digital signal is then processed by the receiver framing logic. The digitizing stage consists of a window comparator with adjustable digitizing window (five possible settings, 3 dB steps, adjustment range from ± 33 to ± 120 mV). The adjustment of the digitizing window is included in the AGC and Squelch loops. The digitizing window can also be set manually in the *Receiver configuration register 4*.

AGC, Squelch and RSSI

As mentioned above, the second and third gain stage gain and the digitizing stage window are included in the AGC and Squelch loops. Eleven settings are available. The default state features minimum digitizer window and maximum gain. The first four steps increase the digitizer window in 3 dB steps, the next six steps reduce the gain in the second and third gain stage, again in 3 dB steps. The initial start setting for Squelch and AGC is defined in *Receiver configuration register 4*. The *Gain reduction state register* displays the actual state of gain resulting from Squelch, AGC and initial settings in *Receiver configuration register 4*.

Squelch

This feature is designed for operation in noisy environments. The noise can be misinterpreted as the start of tag response, resulting in decoding errors.

Automatic squelch is enabled by option bit sqm_dyn in the *Receiver configuration register 2*. It is activated automatically 18.88 µs after end of TX and is terminated at the moment the Mask receive timer (MRT) reaches the value defined in the *Squelch timer register*. This mode is primarily intended to suppress noise generated by tag processing during the time when the tag response is not expected (covered by MRT).

Squelch can operate in two modes, namely with ratios 1 and 6, selectable by pulz_61 bit in the *Receiver configuration register 2*.

Squelch ratio 1 means that system observes the subcarrier signal from the main digitizer and decrease the system gain to decrease the frequency of transitions. If there are more than two transitions on this output in a 50 μ s time period, gain is reduced by 3 dB and output is observed during the following 50 μ s. This procedure is repeated until number of transitions in 50 μ s is lower or equal to 2 or until the maximum gain reduction is reached. This mode is intended for protocols where digitized subcarrier outputs are used.

Squelch ratio 6 means the system similarly observes and decreases the frequency seen at the window comparator set to 6 times the digitizing window. This mode is intended for protocols where output from correlators are used (ISO-A, ISO-B correlated reception).

The gain setting acquired by squelch is cleared by sending direct command Reset RX gain.



AGC

The AGC (automatic gain control) can reduce the gain to keep the receiver chain and input to the digitizing stage out of saturation. The demodulation process is also less influenced by system noise when the gain is properly adjusted.

The AGC logic starts operating when the signal rx_on is asserted to high and is reset when it is reset to low. The state of the receiver gain is stored in the *Gain reduction state register* during a high to low transition of bit rx_on. Reading this register later on gives information of the gain setting used during the last reception.

The AGC system comprises a window comparator and an AGC ratio that can be set to 3 or to 6. As an example, when the AGC ratio is set to 6 the window is six times larger than the data digitalization window comparator. When the AGC function is enabled the gain is reduced until there are no transitions on its output. Such procedure assures that the input to digitalization window comparator is up to 6 times larger than its window.

If the AGC ratio is set to three, the input to the digitalization window comparator is set to be up to 3 times larger than its window.

The AGC operation is controlled by the control bits agc_en, agc_m, agc_alg, and agc6_3 in *Receiver configuration register 2*.

The bit agc_m defines the AGC mode when two AGC modes are available. The AGC can operate during the complete RX process as long as the signal rx_on is high and it can be enabled only during first eight subcarrier pulses.

There are two AGC algorithms to choose from bit agc_alg. The AGC can start either by pre-setting (maximum digitizer window and maximum gain) or by resetting (minimum digitizer window and maximum gain) it. The algorithm with preset is faster and therefore recommended for protocols with short SOF (like ISO14443A at 106 kbps).

Correlator

The correlators correlate the incoming filtered subcarrier with 848 kHz. The aim of the correlation is to maximize the system sensitivity at 848 kHz, while rejecting other frequencies. There are two correlators in the system for AM (or I) channel and PM (or Q) channel.

Correlator settings are defined in *Correlator configuration register 1* and *Correlator configuration register 2*.

RSSI

The receiver also performs the RSSI (received signal strength indicator) measurement for both channels. The RSSI measurement is started after the rising edge of rx_on. It stays active while the signal rx_on is high and frozen while rx_on is low. It is a peak hold system where the value can only increase from initial 0 value. Every time the AGC reduces the gain the RSSI measurement is reset and starts from 0. The result of RSSI measurements is a 4-bit value that can be observed by reading the *RSSI display register*. The LSB step is 2.8 dB, the maximum value is Dh (13d).

Since the RSSI measurement is of peak hold type, the result does not follow any variations in the signal strength (the highest value will be kept). To follow RSSI variation it is possible to reset RSSI bits and restart the measurement by sending direct command *Clear RSSI*.



Clock extractor

The clock extractor observes the RFI1 and RFI2 differential signal and provides a clock signal synchronous with the incoming RF field. The extracted clock is used for synchronous demodulation, for correct frame delay time and for correct data timing during passive transmission. The clock extractor is active down to 60 mV_{PP} input signal.

4.2.3 Antenna tuning

The ST25R3920 support antenna tuning through external variable capacitors. The variable capacitor is connected on its position in the matching network, and the tuning control voltage is connected to one of the control output pins (AAT_A, AAT_B).

The variable capacitors can be connected in series and parallel configurations in the matching network. Further information on the various configuration options can be found in the application note AN5322, available on *www.st.com*.

The phase and amplitude detector block is used for resonance frequency checking. The algorithm in the MCU evaluates the result and adjusts the tuning voltages at AAT_A and AAT_B output pins via the *Antenna tuning control register 1* and *Antenna tuning control register 2* according to the procedure in the MCU firmware.

The AAT_A/B pin voltages are actively set according to *Antenna tuning control register 1* and *Antenna tuning control register 2* when en and aat_en option bits are both set.

If aat_en=1 and en=0, the AAT_A/B voltages are set to a fixed value between 1.5 and 2.2 V (typically 1.9 V).

4.2.4 Capacitive sensor

The capacitive sensor enables measuring a capacitance between two pads, it can be usedfor applications with low power wakeup requirement. The capacitive sensor reacts to changes induced to the capacitive field by objects, or by a finger or a hand.

The capacitive measurement system comprises two electrodes, one is the excitation electrode emitting an electrical field of a fixed frequency in the range of a few hundred kHz (CSO), and the second one is the sensing electrode (CSI). The amount of charge generated in the sensing electrode represents the capacitance between the two electrodes. The capacitive sensor electrodes are tolerant to parasitic capacitance to ground (up to 25 pF) and to input leakage (up to 1 M Ω).

As the charge on the sensing electrode is generated with the frequency of the excitation electrode, a synchronous rectifier is used to detect it. This ensures good rejection of interference and high tolerance to parasitic capacitances (to all nodes except the excitation electrode). The synchronous rectifier output is a DC voltage linearly proportional to the capacitance between the excitation and sensing electrode. The output DC voltage is converted by the A/D converter in absolute mode. The result is stored in the A/D converter output register (see also Section 2.2.5: A/D converter).



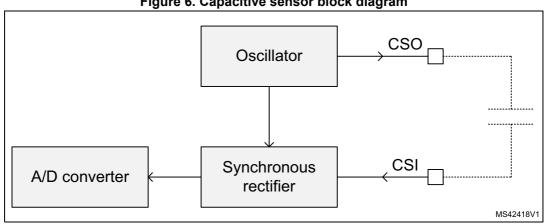


Figure 6. Capacitive sensor block diagram

Any conductive object (human hand or tag) approaching the two electrodes changes the capacitance between the excitation and sensing electrode as it 'shortens' the distance between the two by providing conductance on the part of the path between the two electrodes.

The capacitance measurement is started by sending the direct command Measure capacitance. The ST25R3920 can also be configured to automatically wake up and perform periodic capacitance measurements. The result is compared to a stored reference or to an average of previous measurements, and if the difference is greater than a predefined value an IRQ is triggered to wake up the controller (see also Section 4.2.5).

The capacitive sensor gain can be adjusted in Capacitive sensor control register. The default gain is 2.8 V / pF (typical value), the maximum gain is 6.5 V / pF (typical value). Since the LSB of the A/D converter corresponds to approximately 7.8 mV, the default gain results in a sensitivity of 2.8 fF / LSB (1.2 fF / LSB in case of maximum gain).

The duration of the capacitance measurement is 200 µs, and the current consumption during the measurement is 1.1 mA (typical value). As an example, if the capacitive measurement is performed every 100 ms in Wake-up mode, then the resulting average current consumption is 5.8 µA (3.6 µA is the standby consumption in Wake-up mode).

Capacitive sensor calibration

The capacitive sensor comprises a calibration unit that internally compensates the parasitic capacitances between CSI and CSO, thus leaving full measurement range for information about capacitance variation. Five bits are used to control the calibration. The minimum calibration step and the available calibration range are, respectively, 0.1 and 3.1 pF. The calibration can be done manually by writing to the Capacitive sensor control register or automatically by sending the direct command Calibrate capacitive sensor. The status of this command and the resulting calibration value are stored in the *Capacitive sensor display* register.

To avoid interference of the capacitive sensor with the Xtal oscillator and the reader magnetic field and to assure repetitive results it is strongly recommended to perform capacitance measurement and calibration in Power-down mode only.



4.2.5 Wake-up mode

Asserting the *Operation control register* bit wu while the other bits are set to 0 puts the ST25R3920 into the Wake-up mode, used to perform low power detection of card presence. The ST25R3920 features three possibilities, namely capacitive sensor, phase and amplitude measurement. An integrated low power 32 kHz RC oscillator and register configurable Wake-up timer are used to schedule periodic detection.

Usually the presence of a card is detected by a so-called polling. In this process the reader field is periodically turned on and the controller checks whether a card is present using RF commands. This procedure consumes a lot of energy since reader field has to be turned on for 5 ms before a command can be issued.

Low power detection of card presence is performed by detecting a change in the reader environment, produced by a card. When a change is detected, an interrupt is sent to the controller. As a result, the controller can perform a regular polling loop.

In Wake-up mode the ST25R3920 periodically performs the configured reader environment measurements, and sends an IRQ to the controller when a difference to the configured reference value is detected.

Card detection

The presence of a card close to the reader antenna coil produces a change of the antenna LC tank signal phase and amplitude. The reader field activation time needed to perform the phase or the amplitude measurement is extremely short ($\sim 20 \ \mu s$) compared to the activation time needed to send a protocol activation command.

The power level during the measurement can be lower than that during normal operation as the card does not have to be powered to produce a coupling effect. The emitted power can be reduced by changing the RFO driver resistance.

The capacitive sensor detects a change of the parasitic capacitance between the two excitation electrodes. This change in capacitance can be caused by a card antenna or a hand holding the card (see *Section 2.2.6: Capacitive sensor*).

Registers from 32h to 3Eh are dedicated to Wake-up configuration and display. The *Wake-up timer control register* is the main Wake-up mode configuration register. The timeout period between the successive detections and the measurements to be used are selected in this register. Timeouts in the range from 10 to 800 ms are available, 100 ms being the default value.

Registers from 33h to 3Dh configure the possible detection measurements and store the results, four registers are used for each method.

An IRQ is sent when the difference between a measured value and reference value is larger than configured threshold value. There are two possibilities how to define the reference value:

- The ST25R3920 can calculate the reference based on previous measurements (auto-averaging)
- The controller determines the reference and stores it in a register.

The first register in the series of four is the *Amplitude measurement configuration register*. The difference to reference, which triggers the IRQ, the method of reference value definition, and the weight of last measurement result in case of auto-averaging are defined in this register. The next register stores the reference value when the reference is defined by



the controller. The following two registers are display registers: the first one stores the auto-averaging reference, the second one stores the result of the last measurement.

Wake-up mode configuration registers must be configured before Wake-up mode is actually entered. Any modification of Wake-up mode configuration while it is active can result in unpredictable behavior.

Auto-averaging

In case of auto-averaging, the reference value is recalculated after every measurement. The last measurement value, the old reference value, and the weight are used in this calculation. The following formula is used to calculate the new reference value:

new_reference = old_reference - (old_reference - measured_value) / weight

The calculation is done on 10 bits to have sufficient precision.

The auto-averaging process is initialized when Wake-up mode is entered for the first time after initialization (power-up or using *Set default* command). The initial value is taken from the result of the first measurement, and is kept until the next power cycle or *Set default* command. During the WU period, the reference value is recalculated after each measurement.

Every measurement configuration register contains a bit defining whether the measurement that causes an interrupt is taken in account for the average value calculation (for example bit am_aam of *Amplitude measurement reference register*).

4.2.6 Quartz crystal oscillator

The quartz crystal oscillator operates with 27.12 MHz crystals; its operation is enabled when the *Operation control register* bit en is set to 1. An interrupt is sent to inform the microcontroller when the oscillator amplitude is sufficiently high, meaning that the frequency is stable (see *Main interrupt register*).

The status of oscillator can be observed by checking the *Auxiliary display register* bit osc_ok. This bit is set to 1 when the oscillator frequency is stable.

The oscillator is based on an inverter stage supplied by a controlled current source. A feedback loop controls the bias current to regulate amplitude on XTI pin to 1 V_{PP} . To enable a fast reader start-up, an interrupt is sent when the oscillator amplitude exceeds 750 mV_{PP}.

Division by two assures that the 13.56 MHz signal has a duty cycle of 50%, which is better for the transmitter performance (no PW distortion).

The oscillator output is also used to drive a clock signal output pin MCU_CLK, which can be used by the external microcontroller. The MCU_CLK pin is configured in the *IO configuration register 2*.

4.2.7 Timers

Several timers are integrated in the device, to eliminate the need to run counters in the controller, thus reducing the effort of code implementation and improve its portability to different controllers.

Every timer has one or more associated configuration registers in which the timeout duration and different operating modes are defined. These configuration registers have to be set while the corresponding timer is not running. Any modification of timer configuration while the timer is active can result in unpredictable behavior.



All timers are stopped by the direct command Stop all activities.

Mask receive timer (MRT)

In Reader mode this timer is blocking the receiver and reception process in framing logic by keeping the rx_on signal low after the end of TX during the time the tag reply is not expected. While Mask Receive timer is running the Squelch is automatically turned on when enabled. The MRT does not produce an IRQ.

The MRT timeout is configured in the *Mask receive timer register* and is automatically started at the end of data transmission (at the end of EOF).

The MRT can be triggered by direct command Start Mask-receive timer. In this case the squelch is enabled, according to the *Squelch timer register*.

In the NFCIP-1 Active Initiator, Active and Passive Target communication modes the MRT is started when the other device turns on its field and the external field detector signals I_eon.

MRT supports a longer timing needed for NFCIP1 by setting option bit mrt_step. The bit switches between fc / 64 and fc / 512 step size.

The MRT starts also in the low power Initial NFC target mode. After the initiator field has been detected the controller turns on the 27 kHz RC oscillator, regulator, crystal oscillator, receiver and MRT. After the MRT expires the receiver output starts to be observed to detect start of the initiator message.

For correct operation in the low power Initial NFC target mode the mrt_step = 1 must be used. The 27 kHz RC oscillator is used as a MRT clock source for the time before the crystal oscillator stabilises. This enables that the actual MRT time is a good approximation to the targeted time, also in case the crystal oscillator is not running yet.

No-response timer (NRT)

The purpose of this timer is intended to observe whether a response is detected during a configured time started by end of transmission. The I_nre flag in the *Timer and NFC interrupt register* is signaling interrupt events resulting from this timer timeout.

The NRT is configured by writing *No-response timer register 1* and *No-response timer register 2*). Operation options are defined by setting bits nrt_emv and nrt_step in the *Timer and EMV*[®] *control register*.

The NRT is automatically started at the end of transmission.

Bit nrt_step configures the time step of the No-response timer. Two steps are available, 64/fc (4.72 µs) and 4096/fc, covering, respectively, the range up to 309 ms and up to 19.8 s.

Bit nrt_emv controls the timer operation mode.

- When this bit is set to 0 (default mode) the IRQ is produced if the NRT expires before a start of a response is detected. The rx_on is set low to disable the receiver. In the opposite case, when the start of a tag reply is detected before timeout, the timer is stopped, and no IRQ is produced.
- When this bit is set to 1 the timer unconditionally produces an IRQ when it expires, it is
 also not stopped by direct command Stop all activities. This means that the IRQ is
 independent from whether or not a tag reply was detected. When a tag reply is being
 processed during a timeout, no other action is taken and the reply is normally received.
 In the opposite case, when no tag response is being processed, the receiver is
 disabled.



DS13261 Rev 10

The NRT can also be started using direct command Start No-response timer. The intention of this command is to extend the No-response timer timeout beyond the range defined in the No-response timer control registers. If this command is sent while the timer is running, it is reset and restarted.

The NRT can be terminated using direct command Stop No-response Timer or *Stop all activities*. The timer is terminated and no IRQ is sent. It is expected to be used in the nrt_emv mode, when the incoming reception does not stop the No-response timer.

In the NFCIP-1 active communication mode the NRT role is similar to operation in the normal Reader mode. If the NRT expires before the start of a response is detected an IRQ is produced and the receiver is disabled. There are two modes available:

- nrt_nfc = 0
 - The timer is started when the device TX field is switched off, using a general purpose timer.
 - The operation is valid for active initiator and target modes as well as for bit rate detection mode.
- nrt_nfc = 1
 - The timer is started when the peer field is turned on.
 - Operation is valid for Active initiator and Active target modes.

For Bit rate detection mode the timer is not started at peer field on as, in case of migration from Bit rate detection mode to Active target mode, the MCU has to reconfigure the device to Active target mode prior field on.

In the NFCIP-1 Passive target the No-response timer has no task and is not automatically started.

PPON2 timer

This timer is not used in Reader mode.

In NFCIP-1 mode this timer is automatically started when the transmitter is turned off after the message has been sent. If this timer expires before the peer NFC device $(T_{FADT} + n^*T_{RFW})$ field-on is detected, an I_ppon2 IRQ is sent.

If the external RF field is detected on time, the timer is stopped and no IRQ is sent.

Time is defined in the *PPON2 field waiting register*.

General purpose (GP) timer

The triggering of the this timer is configured by setting the *Timer and EMV[®] control register*. It can be used to survey the duration of reception process (triggering by start of reception, after SOF) or to time out the PCD to PICC response time (triggered by end of reception, after EOF).

In the NFCIP-1 active communication mode it is used to timeout the field switching off. In all cases an IRQ is sent when it expires.

The GP timer can also be started by sending the direct command Start General purpose timer. If this command is sent while the timer is running, it is reset and restarted.

Wake-up (WU) timer

This timer is primarily used in the Wake-up mode, it can be used by sending the direct command Start Wake-up Timer. This command is accepted in any operation mode except



Wake-up mode. When this command is sent the RC oscillator, which is used as clock source for wake-up timer is started, timeout is defined by setting the *Wake-up timer control register*. When the timer expires, an IRQ with the I_wt flag in the *Error and wake-up interrupt register* is sent.

The WU timer is used in the Power-down mode, in which other timers cannot be used because the crystal oscillator, which is the clock source for the other timers, is not running. Note that the tolerance of wake-up timer timeout is defined by tolerance of the RC oscillator.

In NFCIP-1 passive target mode the WU timer is used for time out the temporary device enable after the initial peer field on was detected.

4.2.8 A/D converter

The ST25R3920 contains an 8-bit successive approximation A/D converter. Inputs can be multiplexed from different sources to be used in several direct commands and adjustment procedures. The result of the last conversion is stored in the A/D converter output register. Typical conversion time is 224/fc (16.5 µs).

The A/D converter has two operating modes, absolute and relative.

- In absolute mode the low reference is 0 V and the high reference is 2 V. This means that A/D converter input range is from 0 to 2V, 00h code means input is 0 V or lower, FFh means that input is 2 V - 1 LSB or higher, LSB being 7.8125 mV.
- In relative mode low reference is 1/11 of V_{DD_A} and high reference is 10/11 of V_{DD_A}, so the input range is from 1/11 V_{DD_A} to 10/11 V_{DD_A}.

Relative mode is only used in phase measurement (phase detector output is proportional to power supply). In all other cases absolute mode is used.

4.2.9 Phase and amplitude detector

This block is used to provide inputs to the A/D converter to perform measurements of amplitude and phase, expected by direct commands *Measure amplitude* and *Measure phase*.

Phase detector

The phase detector observes phase difference between the transmitter output signals (RFO1 and RFO2) and the receiver input signals RFI1 and RFI2, proportional to the signal on the antenna LC tank. These signals are first passed by digitizing comparators. Digitized signals are processed by a phase detector with a strong low-pass filter characteristics to get the average phase difference. The phase detector output is inversely proportional to the phase difference between the two inputs. The 90° phase shift results in $V_{DD_A}/2$ output voltage, if both inputs are in phase the output voltage is V_{DD_A} , if they are in opposite phase the output voltage is 0 V. During execution of direct command *Measure phase* this output is multiplexed to the A/D converter input (A/D converter is in relative mode during the execution of this command). Since the A/D converter range is from 1/11 V_{DD_A} to 10/11 V_{DD_A} the actual phase detector range is from 17° to 163°. *Figure* 7 and *Figure* 8 show the two inputs and output of phase detector in case of 90° and 135° phase shift, respectively.



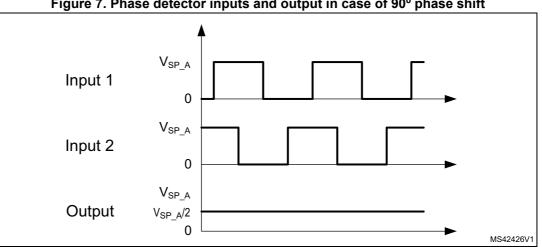
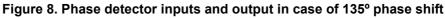
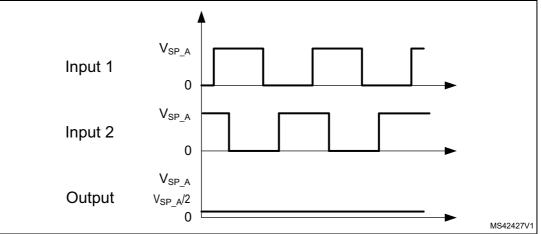


Figure 7. Phase detector inputs and output in case of 90° phase shift





Amplitude detector

Signals from pins RFI1 and RFI2 are used as inputs to the self-mixing stage. The output of this stage is a DC voltage proportional to the amplitude of signals on pins RFI1 and RFI2. During execution of direct command Measure amplitude this output is multiplexed to the A/D converter input.

4.2.10 External field detector

This block is used to detect the presence of an external device generating an RF field. It is used in NFCIP-1 Active communication and Passive target modes. It is enabled by en fd c<1:0> option bits. The external field detector supports two different detection thresholds, namely Peer detection and Collision avoidance. The two thresholds can be independently set by writing the External field detector activation threshold register. The actual state of the detector output can be checked by reading the Auxiliary display register. Input to this block is the signal from the RFI1 pin.

For both thresholds there is a possibility to separately set the activation and deactivation levels.



If the External field level is not detected yet, the Activation threshold is used. If the External field level is detected, the Deactivation threshold is used.

The Activation threshold must be set higher than or equal to the Deactivation threshold.

If the Activation is higher than the Deactivation, the hysteresis is given by the difference between the two levels.

If the Activation and Deactivation levels are equal, there is no the hysteresis in the system and multiple field-on/off events can verify if the actual field level persists in proximity of the selected threshold.

Peer detection threshold

This threshold is used to detect the field emitted by peer NFC device with whom NFC communication is going on. It can be selected in the range from 75 to 800 mV_{PP}. When this threshold is enabled the detector is in low power mode. An interrupt is generated when an external field is detected and also when it is switched off. With such implementation it can also be used to detect the moment when the external field disappears. This can be used to detect the moment when the peer NFC device (either an initiator or a target) has stopped emitting an RF field.

The External Field Detector is enabled in low power Peer Detection mode by setting bits en_fd_c,1:0> in the *Operation control register*.

Collision avoidance threshold

This threshold is used during the RF collision avoidance sequence, which is executed by sending NFC Field ON commands (see *Section 4.4.5*). It can be selected in the range from 25 to 800 mV_{PP}.

4.2.11 Power supply system

The ST25R3920 features three positive supply pins, VDD, VDD_TX and VDD_IO:

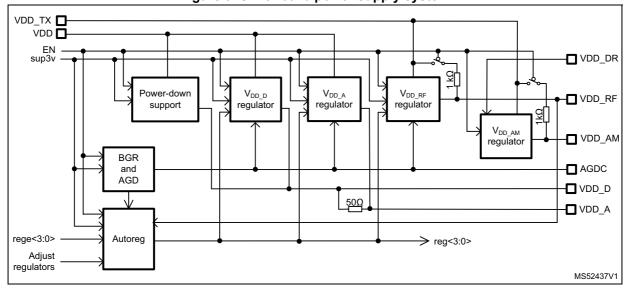
- VDD is the main power supply pin. It supplies the ST25R3920 blocks through two regulators (V_{DD A}, V_{DD D})
- VDD_TX is the transmitter supply pin. It supplies the transmitter via two regulators (V_{DD_RF}, V_{DD_AM}). V_{DD} range from 2.4 to 5.5 V is supported. VDD and VDD_TX must be connected to the same power supply.
- V_{DD_IO} is used to define supply level for digital communication pins (BSS, MISO, MOSI, SCLK, IRQ, MCU_CLK). Digital communication pins interface to the ST25R3920 logic through level shifters, therefore the internal supply voltage can be either higher or lower than V_{DD_IO}. V_{DD_IO} range from 1.65 to 5.5 V is supported.

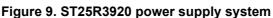
Figure 9 details the building blocks of the ST25R3920 power supply system. It contains three regulators, a power-down support block, a block generating analogue reference voltage (AGDC) and a block performing automatic power supply adjustment procedure. The three regulators are providing supply to analogue blocks (V_{DD_A}), logic (V_{DD_D}) and transmitter (V_{DD_RF}). The use of V_{DD_A} and V_{DD_D} regulators is mandatory at 5 V power supply to provide regulated voltage to analogue and logic blocks, which use only 3.3 V. The use of V_{DD_A} and V_{DD_D} regulators at 3 V supply and V_{DD_RF} regulator at any supply voltage is recommended to improve system PSRR.

Regulated voltage can be adjusted automatically to have the maximum possible regulated voltage, while still having good PSRR. All regulator pins also have corresponding negative supply pins externally connected to ground potential (V_{SS}). *Figure 1* and *Figure 2* show



typical application schematics with all regulators used. For regulators, the recommended blocking capacitors are 2.2 μ F in parallel with 10 nF, for pin AGDC 1 μ F in parallel with 10 nF is suggested.





Regulators have two basic operation modes depending on supply voltage, 3.3 V supply mode (max. 3.6 V) and 5 V supply mode (max 5.5 V). The supply mode is set by writing bit sup3V in the *IO configuration register 2*. Default setting is 5 V so this bit has to be set to 1 after power-up in case of 3.3 V supply.

In 3.3 V mode all regulators are set to the same regulated voltage in range from 2.4 to 3.4 V, while in 5 V only the V_{DD_RF} can be set in range from 3.6 to 5.1 V, while V_{DD_A} and V_{DD_D} are fixed to 3.4 V.

Figure 9 also shows the signals controlling the power supply system. The regulators are operating when signal en is high (en is configuration bit in *Operation control register*). When signal en is low the ST25R3920 is in low power Power-down mode. In this mode consumption of the power supply system is also minimized.

V_{DD RF} regulator

The purpose of this regulator is to improve the PSRR of the transmitter (the noise of the transmitter power supply is emitted and fed back to the receiver). The V_{DD_RF} regulator operation is controlled and observed by writing and reading two regulator registers:

- Regulator voltage control register controls the regulator mode and regulated voltage. Bit reg_s controls regulator mode. If it is set to 0 (default state) the regulated voltage is set using direct command Adjust regulators. When bit reg_s is asserted to 1 regulated voltage is defined by bits rege_3 to rege_0 of the same register. The regulated voltage adjustment range depends on the power supply mode. In case of 5 V supply mode the adjustment range is between 3.6 and 5.1 V in steps of 120 mV, in case of 3.3 V supply mode the adjustment range is from 2.4 to 3.6 V with 100 mV steps.
- *Regulator display register* is a read only register that displays actual regulated voltage when regulator is operating. It is especially useful in case of automatic mode, since the



actual regulated voltage, which is result of direct command *Adjust regulators*, can be observed.

The V_{DD_RF} regulator includes a current limiter that limits the regulator current to 350 mArms in normal operation. The i_lim in the *Regulator display register* is set when the V_{DD_RF} regulator is in current limiting mode.

If a transmitter output current higher than 350 mArms is required the V_{DD_RF} regulator cannot be used to supply the transmitter. VDD_RF and VDD_DR have to be externally connected to VDD_TX (connection of VDD_RF to supply voltage higher than V_{DD_TX} is not allowed).

The voltage drop of the transmitter current is the main source of the ST25R3920 power dissipation. This voltage drop is composed of a drop in the transmitter driver and of a drop in the V_{DD_RF} regulator. Due to this it is recommended to set the regulated voltage using direct command Adjust Regulators. It results in good power supply rejection ratio with relatively low dissipated power due to regulator voltage drop.

In Power-down mode the V_{DD_RF} regulator is not operating. VDD_RF pin is connected to VDD_TX through a 1 k Ω resistor. Connection through resistors assures smooth power-up of the system and a smooth transition from Power-down mode to other operating modes.

V_{DD AM} regulator

This regulator is used to support the transmitter AM modulation. Its output voltage is used as transmitter supply during modulation phase. The output is internally connected to the transmitter. It requires decoupling capacitors (2.2 μ F + 1 nF) at VDD_AM pin.

 V_{DD_DR} is used as reference voltage, resulting in correct V_{DD_AM} voltage and modulation index at supply voltage between 2.4 and 5.5 V.

The output voltage and thus modulation setting is controlled by am_mod<3:0> option bits from 5 to 30% in 16 steps.

In Power-down mode the V_{DD_AM} regulator is not operating. VDD_AM pin is connected to VDD_TX through 1 k Ω resistor, as in the V_{DD_RF} regulator.

V_{DD_A} and V_{DD_D} regulators

 V_{DD_A} and V_{DD_D} regulators are used to supply the ST25R3920 analog and digital blocks respectively. In 3.3 V mode V_{DD_A} and V_{DD_D} regulator are set to the same regulated voltage as the V_{DD_RF} regulator, in 5 V mode V_{DD_A} and V_{DD_D} regulated voltage is fixed to 3.4 V.

The use of V_{DD_A} and V_{DD_D} regulators is mandatory in 5 V mode since analog and digital blocks supplied with these two pins contain low voltage transistors which support maximum supply voltage of 3.6 V. In 3.3 V supply mode the use of regulators is strongly recommended to improve PSRR of analog processing.

For low cost applications it is possible to disable the V_{DD_D} regulator and to supply digital blocks through external short between V_{DD_A} and V_{DD_D} (configuration bit vspd_off in the *IO configuration register 2*).

Power-down support block

In the Power-down mode the regulators are disabled to save current. In this mode a low power Power-down support block that keeps V_{DD_D} and V_{DD_A} below 3.6 V is enabled. Typical regulated voltage in this mode is 3.1 V at 5 V supply and 2.2 V at 3 V supply. When



3.3 V supply mode is set this block is disabled, its output is connected to VDD through a 1 $k\Omega$ resistor.

Typical consumption of Power-down support block is 600 nA at 5 V supply.

Measurement of supply voltages

Using direct command *Measure power supply* it is possible to measure V_{DD} and regulated voltages V_{DD A}, V_{DD D} and V_{DD RF}.

4.2.12 Overshoot / undershoot protection

The overshoot / undershoot protection mechanism makes it possible to control the transmitting waveform during challenging test conditions. This is accomplished by setting bit patterns in the corresponding registers that produce additional signals during the transition phase from modulated to unmodulated state or vice versa.

The operation of this protection is explained by using the overshoot registers. The overshoot mechanism is only effective when bits are written in ov_pattern<13:0>. Setting ov_pattern<13:0> to 0 implicitly disables the overshoot protection, as the configuration from *Mode definition register* and *TX driver register* is applied for all clock cycles after the transition.

The overshoot mode has to be set in control bits $ov_tx_mode<1:0>$ and defines the drive level for the complete bit pattern. Three modes are available.

- ov_tx_mode<1:0> = 00b: the transmitter outputs are driven with V_{DD_DR} when the respective ov_pattern bit is 1.
- ov_tx_mode<1:0> = 01b: the transmitter outputs are driven with V_{DD_AM} when the respective ov_pattern bit is 1.
- ov_tx_mode<1:0> = 10b: the transmitter outputs are stopped (like Type A pause) when the respective ov_pattern bit is 1.

The overshoot protection pattern ov_pattern<13:0> is applied LSB first. For the first 14 clock cycles after the transition from modulated to unmodulated state, each of the 14 bits of the overshoot protection pattern specifies the driver configuration to apply. So ov_pattern<0> defines which driver configuration to apply for the first clock cycle after the transition from modulated to unmodulated state, and ov_pattern<9> defines which driver configuration to apply for the tenth clock cycle after the transition from modulated state. From the 15th clock cycle on the settings from *TX driver register* are used.

The undershoot protection works in a similar manner for transitions from unmodulated state of the carrier to modulated state of the carrier.

4.2.13 Reader operation

The Ready mode has to be entered by setting the bit en of the *Operation control register*. In this mode the oscillator is started and the regulators are enabled. When the oscillator operation is stable an interrupt is sent and bit osc_ok indicates it.

The operation mode and data rate must be then configured by writing the *Mode definition register* and *Bit rate definition register*. The receiver and transmitter operation options related to operation mode have to be defined too. If the selected operation mode uses AM modulation for communication reader to tag the modulation depth must be configured.

Before sending any command to a transponder the transmitter and receiver have to be enabled by setting the bits rx_en and tx_en. Several NFC standards define a guard time



(5 ms for ISO14443) requiring that the reader field must be turned on for some time before first command is sent. General purpose timer can be used to count this time or NFC Field On command with a defined time by the *NFC field on guard timer register*.

Preparation and execution of a transceive sequence:

- Execute the direct command Stop all activities
- Execute the direct command *Reset RX gain*
- Configure the timers accordingly
- Define the number of transmitted bytes in the Number of transmitted bytes register 1 and Number of transmitted bytes register 2
- Write the bytes to be transmitted in the FIFO (not in the case of direct commands REQA and WUPA)
- Send one of the commands Transmit with CRC, Transmit without CRC, Transmit REQA or Transmit WUPA
- When all the data are transmitted, an interrupt is sent to inform the microcontroller that the transmission is finished (IRQ due to end of transmission)

After the transmission is executed, the ST25R3920 receiver automatically starts to observe the RFI inputs to detect a transponder response. The RSSI and AGC (in case it is enabled) are started. The framing block processes the subcarrier signal from receiver and fills the FIFO with data. When the reception is finished and all the data are in the FIFO, an interrupt is sent to the microcontroller (IRQ due to end of receive), and the *FIFO status register 1* and *FIFO status register 1* display the number of bytes in the FIFO so the microcontroller can proceed with data download.

If an error or bit collision is detected during reception, an interrupt with appropriate flag is sent, and the microcontroller must take appropriate action.

When data packets longer than FIFO must be transmitted, the sequence detailed above changes.

The FIFO is prepared with data before the transmission starts. An interrupt is sent during the transmission to signal when the remaining number of bytes is lower than the water level (IRQ due to FIFO water level). The microcontroller then adds more data in the FIFO. When all the data are transmitted an interrupt is sent to inform the microcontroller that the transmission is finished.

The situation during reception time is similar. When the FIFO is loaded with more data than the receive water level, an interrupt is sent and the microcontroller reads the data from the FIFO. When the reception is finished an interrupt is sent to the microcontroller (IRQ due to end of receive) the *FIFO status register 1* and *FIFO status register 1* display the number of bytes in the FIFO still to be read.

4.2.14 Listen mode

The ST25R3920 listen/target mode is activated by setting to 1 bit targ in the *Mode definition register*. There are various target or listening modes implemented depending on setting of the om<3:0> bits, refer to *Table 22: Target operation modes*.

The main modes are

- NFCIP-1 active target
- Passive target used for Card mode and NFCIP-1 passive target



Fixed listen communication mode

Fixed communication mode is active when one of the target modes with om3=0 is selected. The other om bits control the type of communication.

Passive target

Communication can be performed by the host (through FIFO) or also by using automatic responses as referred in *NFCIP-1 passive target definition register*.

These automatic responses include for NFC-A the complete anti-collision including SAK. Handling of RATS and HLTA is up to the host. For NFC-F only the SENSF_REQ is handled by sending SENSF_RES.

States of NFC-A can be handled by observing *Passive target display register* and *Passive target interrupt register* bits I_wu_a, I_wu_a*. Direct commands Go to sense and Go to sleep let the host influence the passive target states.

Responses to SENSF_REQ can be observed by thanks to bit I_wu_f.

The content of the automatic responses is defined by content of PT_Memory.

NFCIP-1 active target

When operating in NFCIP-1 active target mode the following settings are relevant.

- Enable external field detector by setting bit en_fd_c in the Operation control register. Using the field detector allows the ST25R3920 to turn on a response field depending on nfc_ar setting in the Mode definition register. Bits nfc_n<1:0> of the Auxiliary definition register influence the timing of Response collision avoidance sequence.
- The General purpose timer defines the time until RF field off after data transmission. Its trigger sourcehas to be set to the end of transmit, according to *Table 50: Trigger sources* (gptc<2:0> = 011).
- After T_{ARFG} either I_cat or I_cac is flagged. T_{ARFG} is defined by NFC field on guard timer register.
- MRT starts at external field-on. NRT can be tailored by using nrt_nfc.
- After switching off its field the ST25R3920 start the PPON2 timer and observe the External field detector output to detect the response field. If no external field is detected before PPON2 timer timeout, an IRQ with I_ppon2 flag is signaled.

Bit rate detection mode

The Listen mode can also be started from the so-called Bit rate detection mode. In this mode the communication mode is not fixed. This mode is activated in case of Target mode together with bit om3 set to 1.

The other om bits define the technologies to be recognized. It is an extension of the Fixed listen communication mode.

Once the reception of the first frame starts, the Bit rate detection mode signals an IRQ I_nfct indicating that the bit rate has been identified and the host can retrieve the related information by reading nfc_rate on *Bit rate definition register*.

When the first frame has been fully received, the host can exit the Bit rate detection mode by setting the corresponding mode on om<3:0> bits in the *Mode definition register* to the corresponding fixed listen communication mode.



Bit d_ac_ap2p allows filtering of NFCIP-1 active frames.

Low power field detection

The Fixed listen communication and Bit rate detection modes can be enhanced in terms of power consumption by using the field detector in Low-power mode, putting the ST25R3920 in power-down mode (en = 0) while waiting for an external field from a peer/reader.

For this mode the Bit rate detection mode or the Fixed listen communication mode have to be selected, and bits en, rx_en and tx_en in the *Operation control register* need to be cleared to 0.

In this mode the field detector has to be configured to automatic or manual peer detection threshold.

On detection of external field (I_eon) the ST25R3920 temporarily enable the oscillator and the receiver. The host needs to confirm it by setting en and rx_en option bits in the *Operation control register* within 10 ms.

From this point on normal bit rate detection or normal target communication can be performed.

PT memory

The PT_Memory is used to store data for NFCIP-1 passive target and NFC-A card/listen mode. It is loaded via the host interface as described in *Section 4.3*.

Location	Description	Data usage			
0-9	NFCID1 (4/7/RFU bytes)	4 bytes: locations 0-3 7 bytes: locations 0-6			
10,11	SENS_RES2:1	SENS_REQ response			
12	SELR_L1	SEL Level 1 response.	NFC-A anticollision		
13	SELR_L2	SEL Level 2 response			
14	SELR_L3	RFU			
15,16	NFCF_SC	System code (SC) in SENSF_REQ ⁽¹⁾			
17-35	212/424 polling response	SENSF_RES format ⁽²⁾	NFC-F anticollision		
36-47	TSN - Random numbers	Slot selection, 24 4-bit random numbers are stored ^{(3) (4)}			

Table 5. PT_Memory address space

1. SENSF_RES is transmitted in case received SC=NFCF_SC or SC=0xFFFF.

2. NFC-212/424k SENS_RES format, see *Table 6*. The last two bytes in SENSF_RES are transmitted based on the RC bytes in the SENSF_REQ.

3. The 4-bit slot numbers are sequentially used in the NFC212/424 Polling response. When only four TSN numbers remain unused, an IRQ with I_sl_wl bit is sent.

4. Depending on the number of slots in the Polling request, appropriate number of the MSB bits in the slot number is used.

Byte 1	Bytes 2-9	Bytes 10-11 Bytes 12-1		Byte 15	Byte 16	Byte 17	Bytes 18-19	
01h	NFCID2	PAD0	PAD1	MRTICHECK	MRTIUPDATE	PAD2	[RD]	

Table 6. NFC-212/424k SENS_RES format



4.3 Communication with an external microcontroller

The ST25R3920 communicates with a microcontroller either via an SPI interface or via an I2C interface. On both interfaces the ST25R3920 acts as a slave device, relying on the microcontroller to initiate all communication. To notify the microcontroller of completed commands or external events (e.g. peer device field on) the ST25R3920 signals an interrupt on the IRQ pin. The ST25R3920 can also provide a configurable clock signal to the microcontroller on the MCU_CLK pin.

4.3.1 Interrupt interface

There are four interrupt registers implemented in the ST25R3920:

- Main interrupt register
- Timer and NFC interrupt register
- Error and wake-up interrupt register
- Passive target interrupt register

When an interrupt condition is met the source of interrupt bit is set and the IRQ pin transitions to high. The microcontroller then reads the *Main interrupt register* to distinguish between different interrupt sources. After a particular interrupt register is read, its content is reset to 0.

The IRQ pin transitions to low after the interrupt bit(s) that caused its transition to high has (have) been read.

Note: There can be more than one interrupt bit set if the microcontroller does not immediately read the interrupt registers after the IRQ signal is set and another event causing an interrupt occurs. In this case the IRQ pin transitions to low after the last bit causing interrupt is read.

If an interrupt from a certain source is not required it can be disabled by setting the corresponding bit in the Mask interrupt registers. In case of masking a certain interrupt source the IRQ line is not set high, but the interrupt status bit is still set in IRQ status registers.

Reading the IRQ status registers presents and clears also the masked interrupt bits.

If some interrupts are masked, and set to 1 because of an IRQ event, and later on one of them unmasks the IRQ status bit that is already set, the IRQ line is immediately set to high. This notifies the host system that there are some interrupt events not yet read out.

Name	Signal	Level	Description								
IRQ	Digital output	CMOS	Interrupt output pin								

Table 7. IRQ output

IRQ line and IRQ status bits are cleared at:

- Set default
- Reading the IRQ status
- Stop all activities
- Clear FIFO.



FIFO water level and FIFO status registers, FIFO reset

The ST25R3920 features a 512 byte FIFO. The control logic shifts the data during transmission, which was previously loaded by the external microcontroller to the framing block and further to the transmitter. During reception, the demodulated data are stored in the FIFO, and the external microcontroller can receive them later.

The *FIFO status register 2* also contains two bits that indicate that the FIFO was not correctly served during TX/RX process (FIFO overflow and FIFO underflow).

A FIFO overflow is set when too many data are written into the FIFO. When this bit is set during RX the external controller did not react on time on the water level IRQ and more than 512 bytes were written into the FIFO (including received CRC bytes). Consequently, the received data are corrupted. When an overflow happens during TX, it means that the controller has written more data than the FIFO size. The data to transmit are corrupted.

A FIFO underflow is set when data were read from an empty FIFO. When this bit is set during RX the external controller read more data than was actually received. When an underflow happens during TX, it means that the controller has failed to provide the quantity of data defined in the number of transmitted bytes registers on time.

FIFO pointers and FIFO status are reset at the start of each data reception (at I_rxs). They are also reset at Power-up and at commands Set Default and Clear FIFO. Reading out data from empty/cleared fifo shows data = 0.

MCU_CLK

The pin MCU_CLK can be used as clock source for the external microcontroller. Depending on the operation mode either a low frequency clock (32 kHz) from the RC oscillator or the clock signal derived from crystal oscillator is available on pin MCU_CLK. The MCU_CLK output pin is controlled by bits out_c<1:0> and If_clk_off in the *IO configuration register 1*. Bits out_c<1:0> enable the use of pin MCU_CLK as clock source and define the division when the crystal oscillator is running (13.56, 6.78 and 3.39 MHz are available). Bit If_clk_off controls the use of low frequency clock (32 kHz) when the crystal oscillator is not running. By default configuration, which is defined at power-up, the 3.39 MHz clock is selected and the low frequency clock is enabled.

If the Transparent mode (see Section 4.4.13) is used the use of MCU_CLK is mandatory since a clock synchronous with the field carrier frequency is needed to implement receive and transmit framing in the external controller. The use of MCU_CLK is recommended also when the internal framing is used. Using MCU_CLK as the microcontroller clock source generates noise, synchronous with the reader carrier frequency and therefore filtered out by the receiver, while using some other incoherent clock source can produce noise that perturbs the reception. Use of MCU_CLK is also better for EMC compliance.

4.3.2 Communication interface selection

The active communication interface is selected via the I2C_EN pin. If this pin is pulled to GND, the ST25R3920 operates in SPI mode. If this pin is pulled to V_{DD_D} , the ST25R3920 operate in I2C mode.

4.3.3 Serial peripheral interface (SPI)

The ST25R3920 has a standard serial peripheral interface with clock polarity of 0, a clock phase of 1, and an active low slave select signal. Communication starts with the MCU pulling BSS low. The MOSI pin is samples on the falling edge of SCLK, and the state of the

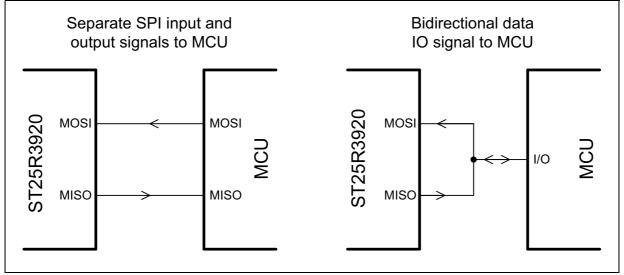


MISO pin is updated on the rising edge of the SCLK signal. Data are transferred byte-wise, most significant bit first. Read and Write commands support an address auto increment to reduce communication time. *Table 8* provides an overview of the SPI signals.

Name	Signal	Signal level	Description			
I2C_EN	Digital input		Pull to GND for SPI operation			
BSS	Digital input		Active low - Slave select			
MOSI	Digital input	CMOS	Master out - Slave in (MCU \rightarrow ST25R3920)			
MISO	Digital output with tristate	CMOS	Master in - Slave out (ST25R3920 \rightarrow MCU)			
SCLK	Digital input		Serial clock			
IRQ	Digital output		Active high - Interrupt output pin			

The MISO output is in tristate as long as no output data are available, hence MOSI and MISO can be externally shorted to create a three-wire SPI. During the time the MISO output is in tristate, it is also possible to switch on a 10 k Ω pull down, by activating option bits miso_pd1 and miso_pd2 in the *IO configuration register 2*.





The first two bits of the first byte transmitted after the BSS high to low transition define the SPI operation mode. All Read and Write modes support address auto incrementing, which means that if, after the address and first data byte some additional data bytes are sent (or read), they are written to (or read from) addresses incremented by 1.

Table 9 shows available SPI operation modes. Register read and write operations are possible in all ST25R3920 operation modes. FIFO and PT_memory operations are possible in case en (bit 7 of the *Operation control register*) is set and the crystal oscillator is stable.

Some direct commands are accepted in all operation modes, others require en (bit 7 of the *Operation control register*) to be set and the crystal oscillator to be stable (see *Table 11*).



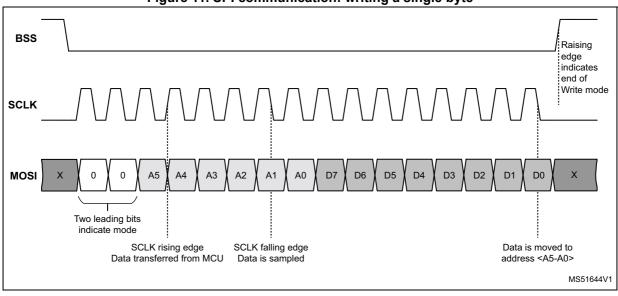
		Patte	ern (c	omm	unica	ation	bits)				
Mode	Мо	ode	Trailer						Related data		
	M1	MO	C5	C4	C3	C2	C1	C0			
Register write	0	0	A5	A4	A3	A2	A1	A0	Data byte (or more bytes in case of		
Register read	0	1	A5	A4	A3	A2	A1	A0	auto-incrementing)		
FIFO load	1	0	0	0	0	0	0	0	One or more bytes of FIFO data		
PT_memory load A-config	1	0	1	0	0	0	0	0	Passive target memory, locations from 0 on.		
PT_memory load F-config	1	0	1	0	1	0	0	0	Passive target memory, locations from 15 on.		
PT_memory load TSN data	1	0	1	0	1	1	0	0	Passive target memory, locations from 36 on. The additional address allows reload of the TSN random numbers without rewriting the whole PT_memory		
PT_memory read	1	0	1	1	1	1	1	1	Passive target memory, locations from 0 on. A 0 byte is presented to the passive target memory to support reading at all SPI speeds.		
FIFO read	1	0		1	1	1	1	1	One or more bytes of FIFO data		
Direct command	1	1	C5	C4	C3	C2	C1	C0	-		

 Table 9. SPI operation modes

Writing data to addressable registers (Write mode)

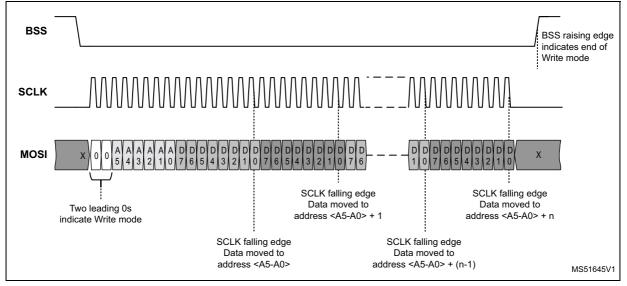
Figure 11 and *Figure 12* show cases of writing, respectively, a single byte and multiple bytes with auto-incrementing address. After the SPI operation mode bits, the address of register to be written is provided. Then one or more data bytes are transferred from the SPI, always MSB to LSB. The data byte is written in register on falling edge of its last clock. If the register on the defined address does not exist or it is a read only register no write is performed.











Reading data from addressable registers (Read register mode)

The SPI operation mode bits are followed by the address of the register to be read. Then one or more data bytes are transferred to MISO output (MSB first) for as long as SCLK is present. This mode also supports address auto-incrementing. If there is no register at a certain address, then all 0 data are sent to MISO.

Figure 13 is an example of reading a single byte.



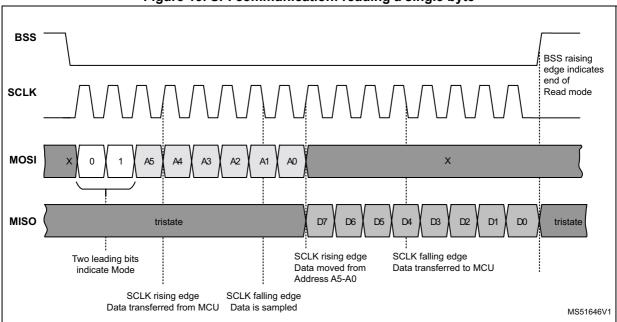


Figure 13. SPI communication: reading a single byte

Read or write access to register space-B

To access the register space-B the register read or write SPI sequence has to be prefixed with the byte FBh. Access to register space-B remains active until the rising edge of BSS.

Loading transmitting data into FIFO

Loading the transmitting data into the FIFO is similar to writing data into an addressable registers. The SPI sequence starts with SPI operation mode bits '10' to indicate a FIFO operation followed by bits <C5:C0> set to 000000b. After the FIFO mode byte at least one and up to 512 data bytes must be sent.

Figure 14 shows how to load the transmitting data into the FIFO.

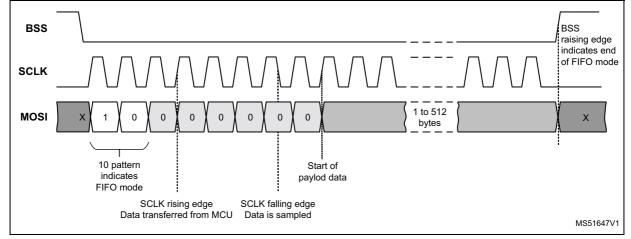
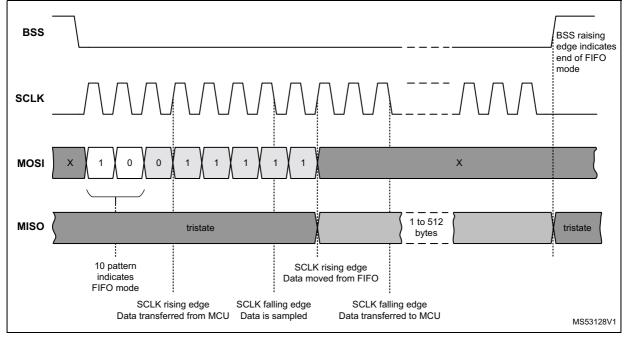


Figure 14. SPI communication: FIFO loading



Reading received data from FIFO

Reading received data from the FIFO is similar to reading data from an addressable registers. The SPI sequence starts with SPI operation mode bits '10' to indicate a FIFO operation followed by <C5:C0> set to 011111b. After the mode byte the ST25R3920 will output the data from the FIFO as long as SCLK is present and BSS is kept low.





Direct command mode

Direct command mode has no arguments, so a single byte is sent. The byte starts with the SPI operation mode bits '11' to indicate Direct Command Mode followed by the direct command code (see *Table 11*) in <C5:C0>, MSB first. Execution of the direct command starts with the rising edge of BSS (see *Figure 16*).

While the execution of some direct commands is immediate, there are others that start a process of certain duration (e.g. calibration, measurements). During the execution of such commands it is not allowed to start another activity over the SPI interface, an IRQ is sent. when the execution is terminated.



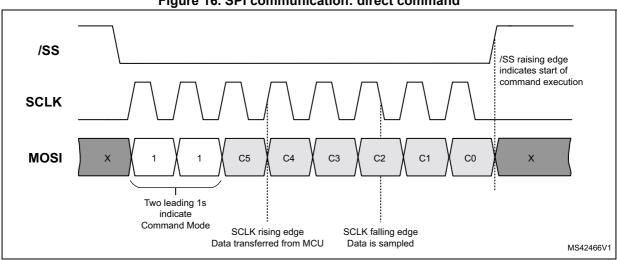
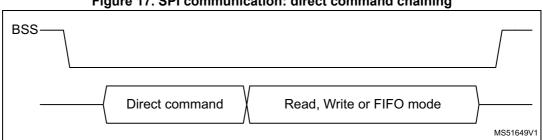
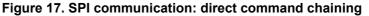


Figure 16. SPI communication: direct command

Direct command chaining

As shown in *Figure 17*, direct commands with immediate execution can be followed by another SPI mode (Read, Write or FIFO) without deactivating the BSS signal in between.





Loading data in the PT_Memory (PT_Memory load)

Loading data into the PT Memory is similar to loading data into the FIFO. There are three mode patterns available to load data into three different parts of the PT memory, as indicated in Table 9. The first byte following the mode/address pattern is stored in the location detailed in Table 9, for consecutive bytes the address is automatically incremented and data are stored to consecutive addresses.

The user must take care that the number of loaded bytes fits the size of the selected PT_memory area, not to overwrite data in the following PT_memory areas.

4.3.4 **I2C** interface

The I2C address is 50h. This interface supports:

- Standard mode (100 kHz)
- Fast mode (400 kHz)
- Fast mode Plus (1 MHz)
- High speed mode (3.4 MHz)

Table 10 summarizes the I2C interface signals.



Name	Signal	Signal level	Description							
I2C_EN	Digital input		Pull to VDD_D for I2C operation							
MISO (SDA)	Digital output	CMOS	I2C data line							
SCLK (SCL)	Digital input	CINICS	I2C clock							
IRQ	Digital output		Active high - Interrupt output pin							

Table 10. I2C interface and interrupt signal lines

Writing data to addressable registers (Register Write mode)

After the I2C slave address the address of the register to be written is sent using the same Register Write mode byte as for SPI register write access. The Register Write mode byte is then followed by one or more data bytes. If more than one data byte is sent, data are stored in subsequent registers starting form the initial register address by incrementing the target address by one for each new data byte.

Figure 18 and *Figure 19* show, respectively, how to write a single byte into a register and how to write multiple bytes into subsequent registers using address auto-incrementing.

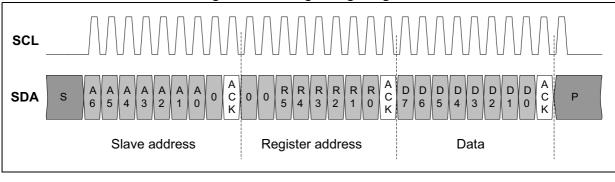
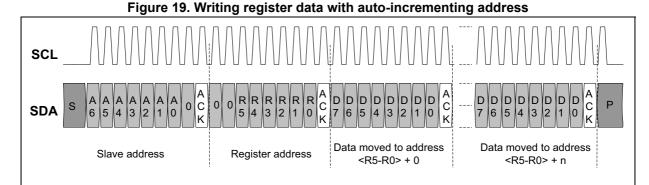


Figure 18. Writing a single register



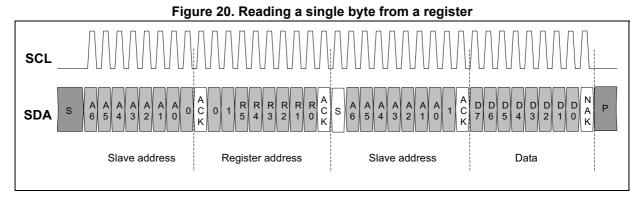
Reading data from addressable registers (Register Read mode)

After the I2C slave address the address of the register to be read is sent using the same Register Read mode byte of the SPI register read access. After the Register Read mode byte the ST25R3920 sends data bytes to the SDA output as long as the MCU keeps SCL. The Register Read mode also supports address auto-incrementing. If the addressed register does not exist, all 0 data are sent to SDA.

DS13261 Rev 10



Figure 20 shows how to read a single byte from a register.

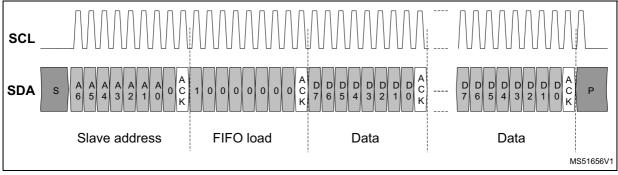


Loading data into FIFO or PT_Memory (FIFO/PT_Memory load)

Loading data into FIFO or PT_Memory is similar to writing data into addressable registers. After the I2C slave address the mode byte to trigger a load of the FIFO or selected PT_Memory area is sent (see *Table 9*) followed by the data bytes to be loaded.

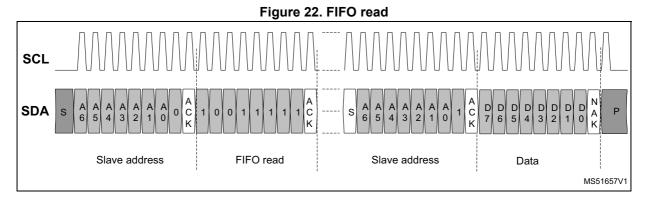
Figure 21 shows how to load data into the FIFO.





Reading data from the FIFO

Reading data from the FIFO is similar to reading data from addressable registers. After the I2C slave address the mode byte to trigger a read of the FIFO is sent. After receiving the FIFO read mode byte, the device sends data bytes from the FIFO for as long as the MCU keeps reading the bus.





DS13261 Rev 10

Direct command mode

After the I2C slave address the mode byte to trigger a direct command is sent. As for SPI some direct commands take some time to execute and no I2C access to the ST25R3920 must be performed until the execution of the direct command is completed. All such direct commands send an interrupt upon completion to notify the MCU that the I2C bus can be used again.

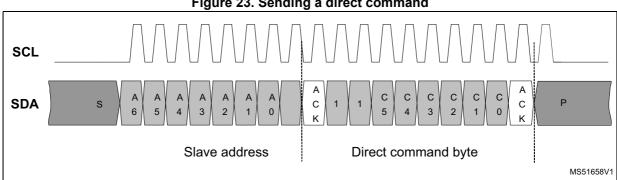


Figure 23. Sending a direct command

I2C access to register space-B

To access the register space-B, byte FBh has to be inserted between the I2C slave address and the register read or write mode byte. Access to register space-B remains active until an I2C Stop Condition is received.

Figure 24. Read and Write mode for register space-B access

٧	Write to register space B															
ę	Slave address W	A	FBh	Register address	A	Data 0	A	Data 1	A		Data N	А	Ρ			
F	Read from register space B															
S	S Slave address W A FBh Register address A Sr Slave address R A Data 0 A Data 1 A Data N N P															
L	Legend: S: Start, Sr: repeated Start, A: ACK, N: NAK, P: Stop.															

I2C: transition to and termination of the Transparent mode

When the transparent mode command is received via I2C, the chip interface lines are switched to the Analogue front end as described in Section 4.4.13: Transparent mode.

Once in transparent mode the BSS signal is used to distinguish between I2C communication and transparent mode data as follows:

- the BSS line must be set high before entering the transparent mode, and then kept high 1. during the Transparent mode
- 2. the Transparent mode is terminated when the BSS line is set to low, followed by at least one SCL clock pulse
- after the termination of the transparent mode the I2C interface can be used again. 3.



I2C: master reads slave immediately after the first byte

If the I2C master omits the mode byte and reads the ST25R3920 immediately after the slave address, then, as shown in *Figure 25*, it will first output the byte FFh, followed by a register dump starting at addres 01h.

Figure 25. I2C master reads slave immediately after the first byte

S	Slave address R	А	Data FFh	А	Data register 01h	А		Data register n	Ν	Ρ
Le	Legend: S: Start, A: ACK, N: NAK, P: Stop.									

This mode is incorporated for an easier the detection of I2C devices, but is not intended to be used in normal operation.



4.4 Direct commands

Code (hex)	Name	Comments	Chaining	Interrupt after termination	Operation mode ⁽¹⁾
C0, C1	Set default	Puts the ST25R3920 into power-up state	No	No	All
C2, C3	Stop all activities	Stops all activities: transmission, reception, direct command execution, timers	Yes	No	en
C4	Transmit with CRC	Starts a transmit sequence with automatic CRC generation	Yes	No	en
C5	Transmit without CRC	Starts a transmit sequence without automatic CRC generation	Yes	No	en
C6	Transmit REQA	Transmits REQA command (ISO14443A mode only)	Yes	No	en, tx_en
C7	Transmit WUPA	Transmits WUPA command (ISO14443A mode only)	Yes	No	en, tx_en
C8	NFC initial field ON	Performs Initial RF Collision avoidance and switches on the field	Yes	Yes	en
C9	NFC response field ON	Performs Response RF Collision avoidance and switches on the field	Yes	Yes	en
CD	Go to sense (Idle)	Puts the passive target logic into Sense (Idle) state	Yes	No	en, rx_en
CE	Go to sleep (Halt)	Puts the passive target logic into Sleep (Halt) state	Yes	No	en, rx_en
D0	Mask receive data	Stops receivers and RX decoders	Yes	No	All
D1	Unmask receive data	Starts receivers and RX decoders	Yes	No	All
D2	Change AM modulation state	Changes AM modulation state	Yes	No	en, tx_en
D3	Measure amplitude	Measures the amplitude of the signal present on RFI inputs and stores the result in the <i>A/D</i> converter output register	No	Yes	All ⁽²⁾
D5	Reset RX gain	Resets receiver gain to the value in the <i>Receiver configuration register 4</i>	No	No	en
D6	Adjust regulators	Adjusts supply regulators according to the current supply voltage level	No	Yes	en
D8	Calibrate driver timing	Starts the driver timing calibration according to the setting in the <i>TX driver timing display register</i>	No	No	en
D9	Measure phase	Measures the phase difference between the signal on RFO and RFI	No	Yes	All ⁽²⁾

Table 11.	List	of	direct	commands
144010 111		•••		



Code (hex)	Name	Comments	Chaining	Interrupt after termination	Operation mode ⁽¹⁾
DA	Clear RSSI	Clears the RSSI bits in the <i>RSSI</i> display register and restarts the measurement	Yes	No	en
DB	Clear FIFO	Clears FIFO	Yes	No	en
DC	Enter Transparent mode	Enters in Transparent mode	No	No	en
DD	Calibrate capacitive sensor	Calibrates capacitive sensor	No	Yes	All
DE	Measure capacitance	Measures capacitance between CSO and CSI pin	No	Yes	All
DF	Measure power supply	-	No	Yes	en
E0	Start General purpose timer	-	Yes	No	en
E1	Start Wake-up timer	-	Yes	No	All except wu
E2	Start Mask-receive timer	Starts the mask-receive timer and squelch operation	Yes	No	en
E3	Start No-response timer	-	Yes	No	en
E4	Start PP _{ON2} timer	-	Yes	No	en
E8	Stop No-response timer	-	Yes	No	en
FA	RFU	Not used	-	-	-
FB	Register space-B access	Enables R/W access to register Space-B	Yes	No	all
FC	Test access	Enable R/W access to Test register	Yes	No	All
Other codes	RFU	Not used	-	-	-

Table 11. List of direct con	nmands (continued)

1. Defines which *Operation control register* bits have to be set in order to accept a particular command.

2. Measure amplitude and Measure phase can be used directly from power down mode. In this case the command temporarily enables the oscillator.

4.4.1 Set default

This direct command puts the ST25R3920 in the same state as power-up initialization:

- performs Stop all activities command
- resets all registers to their default state
- clears all collision bits

Results of previous calibration and adjust commands are lost. No IRQ due to termination of direct command is produced.



4.4.2 Stop all activities

This direct command stops any ongoing activities:

- performs Clear FIFO command
- stops data transmission and reception
- stops all timers, including FDT timer
- clears IRQ line an IRQ status bits
- stops Field ON commands

If Stop All Activities is received during RF collision avoidance, the field detection is terminated and field is not set, consequently no interrupts are sent

- stops automatic field ON (same as above)
- stops automatic field OFF

If Stop All Activities is received during waiting for automatic field off via GPT, the field remains on

- nfc_ar is set to 01b, then it clears the awareness that there was a previous reception
- stops Temporary Enable

This command does not update any register apart from the FIFO status registers. Therefore it does not disable the field detector in CE mode (if it was enabled), and it does not switch off the field (if it was enabled).

4.4.3 Clear FIFO

This direct command clears the FIFO and the FIFO status registers. It does not clear the IRQ line or IRQ status bits.

To prepare a transmission send this command first before writing data into the FIFO. If a Clear FIFO command is sent during an ongoing data transmission, then the data transmission is aborted and FIFO and FIFO status registers are cleared.

4.4.4 Transmit commands

The transmit direct commands are used to start a data transmission from the ST25R3920. They switch the device to reception mode after the transmission is completed.

Before sending commands Transmit with CRC and Transmit without CRC, direct command Clear FIFO has to be sent, followed by the definition of the number of transmitted bytes and writing data to be transmitted in FIFO.

Use the direct commands Transmit REQA and Transmit WUPA to transmit ISO14443A short frame commands REQA and WUPA respectively. It is not necessary to send the direct command Clear FIFO before these two commands.

If the antcl bit is set, then the number of valid bits in the last byte must be set to 0 (nbtx<2:0> in the *Number of transmitted bytes register 2*) prior to the direct command Transmit REQA or Transmit WUPA.



The direct commands Transmit REQA and Transmit WUPA automatically disable the CRC check of the response frame. The CRC check is enabled again after any of the below conditions:

- Transmit with CRC direct command
- Mask receive data direct command
- No Response timer expires

If the direct command Transmit without CRC is used in Felica[™] mode the Length and CRC bytes are skipped. After the preamble and Sync bytes the raw FIFO content is transmitted. A transmit length nbtx<2:0> ≥1 must be used.

4.4.5 NFC field ON commands

The NFC field ON direct commands are used to perform RF collision avoidance. The external field detector must be enabled for these commands to work correctly.

Note: It is recommended to set to 01 bits en_fd_c<1:0> of Operation control register in Reader mode. In NFCIP-1 active communication (AP2P), bits en_fd must be set to 11b to automatically enable external field detector, so that the external field detector automatically exchanges its threshold between collision avoidance and peer detection level, as needed, during operation. Collision avoidance and peer detection levels must be tuned (in accordance with environmental temperature) to ensure good working conditions. A minimum collision avoidance and peer detection activation threshold of 205 mV_{PP} for bits rfe_t<3:0> and trg_l<3:0> of External field detector activation threshold register is recommended in AP2P mode.

To determine whether an external field is present the ST25R3920 compares the RF voltage level on the RFI1 pin with the collision avoidance threshold defined in the *External field detector activation threshold register*.

If no external field is detected, then the ST25R3920 transmitter is switched on automatically (bit tx_en in the *Operation control register* is set) and an I_apon IRQ is signaled. After the RF guard time defined in the *NFC field on guard timer register* has passed an I_cat IRQ is signaled. At this point the controller can initiate a data transmission using a transmit command.

If an external field is detected a I_cac IRQ is signaled, and the ST25R3920 transmitter stays off.

The direct command NFC initial field ON performs an Initial collision avoidance according to NFCIP-1 standard, and the direct command NFC response field ON performs a Response collision avoidance according to NFCIP-1 standard. See *Figure 26*, *Figure 27* and *Table 12* for details on the timing of these commands.



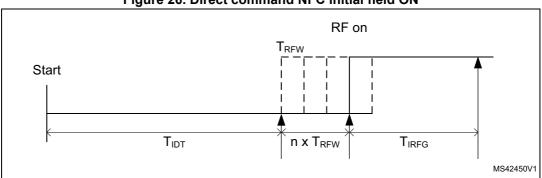




Figure 27. Direct command NFC response field ON

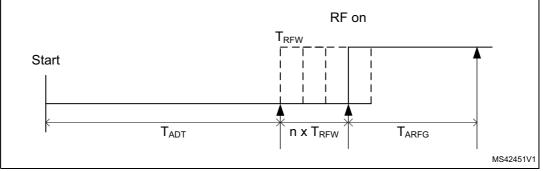


Table 12. Timing parameters of NFC field ON commands

Parameter	Symbol	Value	Unit	Notes
Initial delay time	T _{IDT}	4096	/ fc	NFC initial field ON
RF waiting time	T _{RFW}	512	/ fc	n = 03 based on nfc_n<1:0> in <i>Auxiliary</i> <i>definition register</i>
Initial guard time	T _{IRFG}	75 μs + NFC field on guard time	S	NFC field on guard time defined in the <i>NFC field</i> on guard timer register. NFCIP-1 T _{IRFG} requirement: 5 to 35 ms
Active delay time	T _{ADT}	768	/ fc	NFC response field ON
Active guard time	T _{ARFG}	75 μs + NFC field on guard time	S	NFC field ON guard time defined in the <i>NFC</i> <i>field on guard timer register</i> . NFCPIP-1 T _{ARFG} requirement: > 75 μs + NFC field ON guard times (1024 / fc)

4.4.6 Mask receive data and Unmask receive data

The direct command Mask receive data disables processing of the receiver output by the RX decoders, RSSI measurement, and AGC operation.

The direct command Unmask receive data enables processing of the received data by the RX decoders, RSSI measurement and AGC operation. A common use of this command is to re-enable the receiver operation after it was masked by the command Mask receive data. If the Mask receive timer is still running while the direct command Unmask receive data is received, reception is enabled, and the Mask receive timer is reset.



In passive target (card emulation) mode, the Unmask receive data command prepares the RX decoders for a new data reception and clears the internal FDT timer. In passive target mode, this direct command must be used only if no further transmission from the ST25R3920 is planned and the device has to wait for the next command to be received.

4.4.7 Change AM modulation state

This command changes the AM modulation state from unmodulated to modulated, and vice versa. This can be used to measure the AM modulation index with the direct command *Measure amplitude*.

4.4.8 Measure amplitude

This command measures the amplitude of the RF signal on the RFI inputs and stores the result in the *A/D converter output register*.

This command enables the transmitter and amplitude detector. The transmitter drives the antenna, and the amplitude detector converts the differential RF signal received back between RFI1 and RFI2 into a proportional DC voltage. This DC voltage is converted with the A/D converter in absolute conversion mode into an 8-bit value and stored in the A/D converter output register.

The amplitude detector conversion gain is 0.6 V_{inPP} / V_{out} referenced to the RF signal on a single RFI pin. Thus, one LSB of the A/D converter output represents 13.02 mV_{PP} on either of the RFI inputs.

Note: The maximum allowed voltage level on an RFI pin is $3 V_{PP}$. This results in 1.8 V output DC voltage of the amplitude detector and produces a value of E6h after A/D conversion.

Duration time: 25 µs max.

4.4.9 Reset RX gain

This command initializes the AGC, Squelch and RSSI block and resets the gain reduction to the value set in *Receiver configuration register 4*. Sending this command also stops any ongoing squelch process.

4.4.10 Adjust regulators

When this command is sent, then the transmitter and receiver are enabled to ensure a high current draw and the regulated voltage V_{DD_RF} is set 250 mV below the power supply level of V_{DD_TX} . Before sending the adjust regulator command it is required to toggle the bit reg_s by setting it first to 1 and then reset it to 0. After the adjustment is completed the state of the transmitter and receiver prior to the command execution is restored (either enabled or disabled).

Duration time: 5 ms max.

This command is not accepted if external definition of the regulated voltage is selected in the *Regulator voltage control register* (bit reg_s is set to 1).

4.4.11 Measure phase

This command measures the phase difference between the signals on the RFO outputs and the signals on the RFI inputs and stores the result in the *A/D converter output register*.



DS13261 Rev 10

This command enables the transmitter and phase detector, and performs an A/D conversion of the output of the phase detector with the A/D converter in relative mode. The phase measurement results can be calculated using the following formulas:

- $0 \le \Phi \le 17^{\circ}$: result = 255
- 17 < Φ < 163°: angle [°] = 17 + (1 -result / 255) * 146
- $163 \ge \Phi \ge 180^{\circ}$: result = 0

Duration time: 25 µs max.

4.4.12 Clear RSSI

The receiver automatically clears the RSSI bits in the *RSSI display register* and starts a new measurement of the RSSI when a new reception is started (e.g. after a Transmit direct command). Since the RSSI bits store the peak value (peak-hold type) eventual variation of the receiver input signal will not be followed (this can happen in case of a long message or test procedure).

The direct command Clear RSSI clears the RSSI bits in the *RSSI display register*, and restarts the RSSI measurement. This allows to obtain multiple RSSI measurements during a single reception.

4.4.13 Transparent mode

This command sets the receiver and transmitter into the transparent mode. The device enters the transparent mode on the rising edge of the BSS signal of the SPI frame used to send the direct command. The transparent mode is maintained as long as signal BSS is kept high, that is, the following SPI command sent from the microcontroller will automatically stop the transparent mode.

4.4.14 Calibrate capacitive sensor

This command calibrates the capacitive sensor.

It is strongly recommended to use this command in power-down mode only to avoid interference with the crystal oscillator or reader magnetic field. Interrupt I_dct is only generated in Ready mode. The measurement status is indicated by status bits in the *Capacitive sensor display register*.

Duration time: 3 ms max.

This command is executed only if the capacitive sensor automatic calibration mode is set (all bits cs_mcal in the *Capacitive sensor control register* are set to 0).

4.4.15 Measure capacitance

This command performs the capacitance measurement.

It is strongly recommended to use this command in power-down mode only to avoid interference with the crystal oscillator or reader magnetic field.

Duration time: 250 µs max.





4.4.16 Measure power supply

This command measures the power supply. The bits mpsv<2:0> in the *Regulator voltage control register* select which signal is measured. The result of the measurement is stored in the *A/D converter output register*.

For power supply measurements the selected supply input voltage is divided by three and measured with the A/D converter in absolute mode. This leads to a resolution of 23.4 mV per LSB for all power supply measurements.

Duration time: 25 µs max.

4.4.17 Test access

The devices do not have dedicated test pins. A direct command Test Access is used to enable RW access of test registers and entry in different test modes. Pins CSI and CSO are used as test pins.

Test mode entry and access to test registers

Test registers are not part of the normal register address space. After sending direct command Test Access, test registers can be accessed using normal Read/Write register command. Access to test registers is possible in a chained command sequence where command Test Access is sent first, followed by read/write access to test registers using auto increment feature. Test register are set to default state at power-up.

Analog test and observation register 1

Address: 01h

Type: RW

Bit	Name	Default	Function	Comments
7	tana7	0	-	Reserved
6	tana6	1	-	Reserved
5	tana5	0	-	Reserved
4	-	0	-	Reserved
5	tana3	0		
4	tana2	0	See Table 14	These test modes are also intended for observation in normal mode. Other modes of this register are
3	tana1	0	See Table 14	also available when analog test mode is not set.
0	tana0	0		

Table 13. Analog test and observation register 1



tana3:0		Pin CSI		Pin CSO	-	
(hex)	Туре	Type Functionality		Functionality	Comment	
1	A0	Analog output of AM channel (before digitizer)	D0	Digital output of AM channel (after digitizer)		
2	A0	Analog output of PM channel (before digitizer)	D0	Digital output of PM channel (after digitizer)	Normal operation	
3	A0	Analog output of AM channel (before digitizer)	A0	Analog output of PM channel (before digitizer)	(reader)	
4	A0	Analog output of AM correlation signal	A0	Analog output of PM correlation signal		
5	A0	Tag demodulator analog	D0	Tag demodulator OOK digital out	Normal operation	
6	A0		D0	Tag demodulator ASK digital out	(tag)	
7	A0	Analog voltage of phase measurement	D0	Oscillator stable	Do not set when measure amplitude command is used	
В	D0	Digital output of AM correlation data signal	D0	Digital output of AM correlation collision/start detection signal	-	
С	D0	Digital output of PM correlation data signal	D0	Digital output of PM correlation collision/start detection signal	-	
D	A0	Analog output of AM correlation signal	A0	Correlation digitizing threshold for AM channel	-	
E	A0	Analog output of PM correlation signal	A0	Correlation digitizing threshold for PM channel	-	

Table 14. Test access register - Signal selection of CSI and CSO pins



4.5 Registers

The ST25R3920 has two register spaces, each of them consists of up to 64 registers with address ranging from 00h to 3Fh:

- 1. register space A (Rs-A), see *Table 15*
- 2. register space B (Rs-B), see Table 16.

There are two types of registers implemented in the ST25R3920:

- 1. configuration registers: used to configure the device, can be written and read through the SPI or I2C interfaces
- 2. display registers: read only (RO), contain information about the state of the device.

Registers are set to their default value at power-up and after sending the direct command *Set default.* Bits set as RFU must be kept at their reset values unless otherwise specified.

Туре	Address (hex)	Register space A (Rs-A)
	00	IO configuration register 1
IO configuration	01	IO configuration register 2
	02	Operation control register
Operation control and mode definition	03	Mode definition register
	04	Bit rate definition register
	05	ISO14443A and NFC 106kb/s settings register
	06	ISO14443B settings register 1
Dratacal configuration	07	ISO14443B and FeliCa settings register
Protocol configuration	08	NFCIP-1 passive target definition register
	09	Stream mode definition register
	0A	Auxiliary definition register
	0B	Receiver configuration register 1
Dessiver configuration	0C	Receiver configuration register 2
Receiver configuration	0D	Receiver configuration register 3
	0E	Receiver configuration register 4
	0F	Mask receive timer register
	10	No-response timer register 1
	11	No-response timer register 2
Timer definition	12	Timer and EMV [®] control register
	13	General purpose timer register 1
	14	General purpose timer register 2
	15	PPON2 field waiting register

Table 15. List of registers - Space A



Туре	Address (hex)	Register space A (Rs-A)
	16	Mask main interrupt register
	17	Mask timer and NFC interrupt register
	18	Mask error and wake-up interrupt register
	19	Mask passive target interrupt register
	1A	Main interrupt register
Interrupt and	1B	Timer and NFC interrupt register
associated reporting	1C	Error and wake-up interrupt register
	1D	Passive target interrupt register
	1E	FIFO status register 1
	1F	FIFO status register 2
	20	Collision display register
	21	Passive target display register
	22	Number of transmitted bytes register 1
Definition of number of transmitted bytes	23	Number of transmitted bytes register 2
	24	Bit rate detection display register
A/D converter output	25	A/D converter output register
Antonno polibrotion	26	Antenna tuning control register 1
Antenna calibration	27	Antenna tuning control register 2
Antenna driver and	28	TX driver register
modulation	29	Passive target modulation register
External field detector	2A	External field detector activation threshold register
threshold	2B	External field detector deactivation threshold register
Regulator	2C	Regulator voltage control register
Popoivor atota dianta:	2D	RSSI display register
Receiver state display	2E	Gain reduction state register
Conceitive concer	2F	Capacitive sensor control register
Capacitive sensor	30	Capacitive sensor display register
Auxiliary display	31	Auxiliary display register

Table 15. List of registers - Space A (continued)



Туре	Address (hex)	Register space A (Rs-A)
	32	Wake-up timer control register
	33	Amplitude measurement configuration register
	34	Amplitude measurement reference register
	35	Amplitude measurement auto-averaging display register
	36	Amplitude measurement display register
	37	Phase measurement configuration register
Wake-up	38	Phase measurement reference register
Traite up	39	Phase measurement auto-averaging display register
	3A	Phase measurement display register
	3B	Capacitance measurement configuration register
	3C	Capacitance measurement reference register
	3D	Capacitance measurement auto-averaging display register
	3E	Capacitance measurement display register
IC identity	3F	IC identity register

Table 15. List of registers - Space A (continued)

Table 16. List of registers - Space B

Туре	Address (hex)	Register space B (Rs-B)
Dratagal configuration	05	EMD suppression configuration register
Protocol configuration	06	Subcarrier start timer register
	0B	P2P receiver configuration register 1
Receiver configuration	0C	Correlator configuration register 1
	0D	Correlator configuration register 2
Timer definition	0F	Squelch timer register
	15	NFC field on guard timer register
Antenna driver and modulation	28	Auxiliary modulation setting register
	29	TX driver timing register
External field detector threshold	2A	Resistive AM modulation register
	2B	TX driver timing display register
Regulator	2C	Regulator display register
	30	Overshoot protection configuration register 1
Protection	31	Overshoot protection configuration register 2
	32	Undershoot protection configuration register 1
	33	Undershoot protection configuration register 2



4.5.1 IO configuration register 1

Register space: A Address: 00h Type: RW

Bit	Name	Default		Function		Comments	
7	single	0	0: Differential antenna driving 1: Only one RFO driver will be used			Chooses between single and differential antenna driving.	
6	rfo2	0	0: RFO1, RFI1 1: RFO2, RFI2			Chooses which output driver and which input will be used in case of single driving.	
5	i2c_thd1	0	00: 380 ns /		hs-modes	-	
4	i2c_thd0	0	01: 180 ns / 160 ns 10: 180 ns / 70 ns 11: 100 ns / 70 ns			-	
3	RFU	0		-		-	
			out_cl1	out_cl0	MCU_CLK		
2	out_cl1	0	0	0	3.39 MHz	Selection of clock frequency on MCU CLK output in case Xtal	
			0	1	6.78 MHz	oscillator is running. With "11"	
1	out al0	0	1	0	13.56 MHz	MCU_CLK output is permanently low.	
	out_cl0	U	1	1	Disabled		
0	lf_clk_off	0	0: LF clock on MCU_CLK 1: No LF clock on MCU_CLK			By default the 32 kHz LF clock is present on MCU_CLK output when Xtal oscillator is not running and the MCU_CLK output is not disabled.	

Table 17. IO configuration register 1



4.5.2 IO configuration register 2

Register space: A Address: 01h Type: RW

Table 18	. IO configuratio	on register 2
14010 10		

Bit	Name	Default	Function	Comments
7	sup3V	0	0: 5 V supply 1: 3.3 V supply	Set to 0 for 3.6 V < $V_{DD} \le 5.5$ V Set to 1 for 2.4 V $\le V_{DD} \le 3.6$ V
6	vspd_off	0	0: Enable V _{DD_D} regulator 1: Disable V _{DD_D} regulator	Used for low cost applications. When this bit is set: – at 3 V or 5 V supply VDD_D and VDD_A must be shorted externally
5	aat_en	0	0: Disable AAT D/A 1: Enable AAT D/A	The AAT D/A converters are enabled if both aat_en and en are set. If only aat_en is set and en is cleared, then the AAT outputs are set to a fixed value. Note that for the fixed value to operate, en must have been set to 1 at least once, prior to having en = 0.
4	miso_pd2	0	1: Pull-down on MISO, when BSS is low and MISO is not driven by the ST25R3920.	Valid only in SPI mode.
3	miso_pd1	0	1: Pull-down on MISO when BSS is high	
2	io_drv_lvl	0	0: Normal IO driver level 1: Increase IO driving level	Increases IO driver strength of MISO, MCU_CLK an IRQ. Recommended to set to 1 for all I2C operation, and for SPI operation if $V_{DD_IO} < 3.3 V.$
1	am_ref_rf	0	0: V _{DD_AM} regulator reference from V _{DD_DR} 1: V _{DD_AM} regulator reference from V _{DD_RF}	Selects non modulated RF voltage level reference of the V _{DD_AM} voltage regulator.
0	slow_up	0	1: Slow ramp at Tx on	≥ 10 µs, 10% to 90%, for B



4.5.3 Operation control register

Address: 02h

Type: RW

Bit	Name	Default	Function	Comments
7	en	0	1: Enables oscillator and regulator (Ready mode)	-
6	rx_en	0	1: Enables Rx operation	-
5	rx_chn	0	0: Both, AM and PM, channels enabled 1: One channel enabled	If only one Rx channel is enabled, selection is done by the <i>Receiver configuration register 1</i> bit ch_sel.
4	rx_man	0	0: Automatic channel selection 1: Manual channel selection	If both Rx channels are enabled, chooses the method of channel selection, manual selection is done by the <i>Receiver configuration register 1</i> bit ch_sel.
3	tx_en	0	1: Enables Tx operation	This bit is automatically set by NFC Field ON commands and reset in NFC active communication modes after transmission is finished.
2	wu	0	1: Enables Wake-up mode	According to settings in <i>Wake-up timer control register</i> .
1	en_fd_c1	0	00: External field detector off. 01: Manually enable external field detector with collision avoidance detection threshold. 10: Manually enable external field	 01: External field detector with collision avoidance detection must be used in R/W mode when using NFC field on commands. 11: External field detector with peer detection/collision avoidance threshold activated automatically must be used in NFCIP-1 active
0	en_fd_c0	0	detector with peer detection threshold. 11: Enable external field detector automatically.	communication (AP2P) and Passive target modes. en_fd_c<1:0> \neq 0 and other bits in Operation control register set to 0 put the device in Low power initial NFC mode.

Table 19. Operation control register⁽¹⁾

1. Default setting takes place at power-up only.



4.5.4 Mode definition register

Register space: A Address: 03h Type: RW

Bit	Name	Default	Function	Comments	
7	targ	0	0: Initiator 1: Target	-	
6	om3	0			
5	om2	0	Refer to <i>Table 21</i> and <i>Table 22</i>	Selection of operation mode.	
4	om1 0			Different for initiator and target modes.	
3	om0	1			
2	tr_am	0	0: OOK 1: AM	Selects RF modulation mode.	
1	nfc_ar1	0	00: Off 01: Automatic field on after any reception (including errors)	Automatically starts the Response RF collision avoidance ⁽²⁾ .	
0	nfc_ar0	0	10: Always after peer field-off 11: RFU		

1. Register can be written only in case crystal clock is present and stable (oscok = 1).

2. Refer to note in Section 4.4.5: NFC field ON commands for handling these bits..

Table 21. Initiator operation modes⁽¹⁾

om3	om2	om1	om0	Comments
0	0	0	0	NFCIP-1 active communication
0	0	0	1	ISO14443A
0	0	1	0	ISO14443B
0	0	1	1	FeliCa [™]
0	1	0	0	NFC Forum Type 1 tag (Topaz)
1	1	1	0	Sub-carrier stream mode
1	1	1	1	BPSK stream mode
	Other con	RFU		

1. If a non supported operation mode is selected the Tx/Rx operation is disabled.

Table 22. Target operation modes⁽¹⁾⁽²⁾

om3	om2	om1	om0	Comments
0	0	0	1	ISO14443A passive target mode
0	1	0	0	FeliCa [™] passive target mode



om3	om2	om1	om0	Comments
0	1	1	1 NFCIP-1 active communication mode	
1	x	x	x	Bit rate detection mode – om2: enable FeliCa [™] bit rate detection mode – om1: RFU – om0: enable ISO14443A bit rate detection mode
	Other con	nbinations		Not allowed

Table 22. Target operation modes⁽¹⁾⁽²⁾ (continued)

1. The nfc_f0 = 1 must not be set in Bit rate detection mode (see *Table 24*).

2. When in Passive target and Bit rate detection modes, the pt_res setting is used to generate the RF field (high ohmic setting of pt_res can prevent RF field generation).

4.5.5 Bit rate definition register

Register space: A

Address: 04h

Type: RW

Table 23. Bit rate definition register

Bit	Name	Default	Function	Comments	
7	RFU	0		-	
6	RFU	0		-	
5	tx_rate1	0	Refer to <i>Table 24</i>	Selects bit rate for Tx.	
4	tx_rate0	0			
3	RFU	0		-	
2	RFU	0		-	
1	rx_rate1	0		Selects bit rate for Rx.	
0	rx_rate0	0			

Table 24. Bit rate coding⁽¹⁾

rate3	rate2	rate1	rate0	Bit rate (kbit/s)	Comments
0	0	0	0	fc / 128 (~106)	-
0	0	0	1	fc / 64 (~212)	-
0	0	1	0	fc / 32 (~424)	-
0	0	1	1	fc / 16 (~848)	-
	Other combinations			-	Not used

1. If a non supported bit rate is selected the Tx/Rx operation is disabled.



4.5.6 ISO14443A and NFC 106kb/s settings register

Register space: A Address: 05h Type: RW

Bit	Name	Default	Function	Comments	
7	no_tx_par	0	1: No parity bit is generated during Tx	Data stream is taken from FIFO, transmit to be done using command Transmit Without CRC ⁽¹⁾ .	
6	no_rx_par	0	1: Receive and put in FIFO also the parity bit	When set to 1 received bit stream is put in the FIFO, no parity and CRC detection is done ⁽¹⁾ . Supported only for 106 kbit/s data rate.	
5	nfc_f0	0	1: Support of NFCIP-1 Transport Frame format	Adds SB (F0) and LEN bytes during Tx and skip SB (F0) byte during Rx. Must not be set in bit rate detection mode.	
4	p_len3	0			
3	p_len2	0	Refer to <i>Table</i> 26	Modulation pulse width, defined in number of	
2	p_len1	0		13.56 MHz clock periods.	
1	p_len0	0			
0	antcl	0	0: Standard frame 1: ISO14443 anticollision frame	Must be set to 1 for reception of ISO14443A bit oriented anticollision frames in reader mode. Must be set to 0 for all other frames and modes.	

Table 25. ISO14443A and NFC 106kb/s settings register

1. Supported in reader modes only, not supported in card emulation modes.

		n land		Pulse width in number of 1 / fc for different bit rates			
p_len3	p_len2	p_len1	p_len0	fc / 128	fc / 64	fc / 32	fc / 16
0	1	1	1	42	-	-	-
0	1	1	0	41	24	-	-
0	1	0	1	40	23	-	-
0	1	0	0	39	22	13	-
0	0	1	1	38	21	12	8
0	0	1	0	37	20	11	7
0	0	0	1	36	19	10	6
0	0	0	0	35	18	9	5
1	1	1	1	34	17	8	4
1	1	1	0	33	16	7	3
1	1	0	1	32	15	6	2
1	1	0	0	31	14	5	-

Table 26. ISO14443A modulation pulse width



p_len3	p_len2	n lon2	n lon2	n lang	n an0			n on0	Pulse width in number of 1 / fc for different bit rates			
		p_len1	p_len0	fc / 128	fc / 64	fc / 32	fc / 16					
1	0	1	1	30	13	-	-					
1	0	1	0	29	12	-	-					
1	0	0	1	28	-	-	-					
1	0	0	0	27	-	-	-					

Table 26. ISO14443A modulation pulse width (continued)

4.5.7 ISO14443B settings register 1

Register space: A

Address: 06h

Type: RW

Table 27.	ISO14443B	settinas	reaister 1
14010 27.	10011100	ooungo	iogiotoi i

Bit	Name	Default			Functio	n	Comments
7	egt2	0	egt2	egt1	egt0	Number of etu	
	eyız	0	0	0	0	0	
			0	0	1	1	
6	egt1	0	:	÷	÷	:	EGT defined in number of etu
5	egt0	0	1	1	0	6	
5	egio	0	1	1	1	6	
4	sof_0	0	0: 10 etu 1: 11 etu				SOF, number of etu with logic 0
3	sof_1	0	0: 2 etu 1: 3 etu				SOF, number of etu with logic 1
2	eof	0	0: 10 etu 1: 11 etu	-			EOF, number of etu with logic 0
1	half	0	and eof 1: SOF	bit	ogic 0, 2.	by sof_0, sof_1, 5 etu logic 1,	Sets SOF and EOF settings in middle of specification.
0	rx_st_om	0			nust be pi mission f	resent for Rx for Rx	SOF fixed to 10 low and 2 etu high, EOF not defined, put in FIFO last full byte. CRC is not checked in this mode. Supported only in a coherent reception mode.



4.5.8 ISO14443B and FeliCa settings register

Register space: A Address: 07h Type: RW

Table 28. ISO14443B and FeliCa settings register	
--	--

Bit	Name	Default	Function	Comments
7	tr1_1	0	Refer to <i>Table 29</i>	
6	tr1_0	0		-
5	no_sof	0	1: No SOF PICC to PCD	According to ISO14443-3 chapter 7.10.3.3. Support of B'.
4	no_eof	0	1: No EOF PICC to PCD	According to ISO14443-3 chapter 7.10.3.3. Supported only in coherent reception mode.
3	RFU	0	-	-
2	RFU	0	-	-
1	f_p1	0	00: 48 01: 64	FeliCa [™] preamble length (valid also for NFCIP-1
0	f_p0	0	10: 80 11: 96	active communication bit rates 212 and 424 kb/s)

Table 29. Minimum TR1 codings

t=1 1	t=1 0	Minimum TR1 for a PICC to PCD bit rate		
tr1_1	tr1_0	fc / 128	>fc / 128	
0	0	80 / fs		
0	1	64 / fs	32 / fs	
1	0	Not u	sed	
1	1	Not used		



4.5.9 NFCIP-1 passive target definition register

Register space: A Address: 08h Type: RW

Bit	Name	Default	Function	Comments
7	fdel3	0		Valid for NFC-A CE mode
6	fdel2	0	PCD to PICC FDT compensation.	 fdel = 0: Nominal FDT time in produced in logic.
5	fdel1	0	Frame compensation defined as	 fdel > 0: Shortens the FDT provided by logic.
4	fdel0	0	fdel<3:0>*1 / fc	Due to signal processing delays fdel<3:0> = 2 is expected to be a good setting (best value dependents also on filter and antenna).
3	d_ac_ap2p	0	0: Enable AP2P frame recognition 1: Disable AP2P frame recognition	-
2	d_212/424_1r	0	0: Enable automatic SENSF_RES 1: Disable automatic SENSF_RES	
1	RFU	0	RFU	Disables the automatic responses in passive
0	d_106_ac_a	0	0: Enable automatic anti-collision in NFC-A 1: Disable automatic anti-collision in NFC-A	target mode, and completely operates via FIFO.



4.5.10 Stream mode definition register

Register space: A Address: 09h Type: RW

Bit	Name	Default	Function			Comments		
7	RFU	0			-	-		
6	scf1	0	Refer to	Table 22		Sub-carrier frequency definition for		
5	scf0	0				Sub-carrier and BPSK stream mode.		
			scp1	scp0	Number of pulses			
4	4 scp1	0	0	0	1 (BPSK only)			
			0	1	2 (BPSK only)	Number of sub-carrier pulses in report period for Sub-carrier and BPSK stream mode.		
3	scp0 0	0	1	0	4			
5				1	8			
2	stx2	0				Definition of time period for Tx modulator		
1	stx1	0	Refer to	Table 33		control (for Sub-carrier and BPSK stream		
0	stx0	0				mode).		

Table 32. Sub-carrier frequency definition for Sub-carrier stream mode

scf1	scf0	Sub-carrier mode	BPSK mode
0	0	fc / 64 (212 kHz)	fc / 16 (848 kHz)
0	1	fc / 32 (424 kHz)	
1	0	fc / 16 (848 kHz)	RFU
1	1	fc / 8 (1695 kHz)	

Table 33. Definition of time period for Stream mode Tx modulator control

stx2	stx1	stx0	Time period
0	0	0	fc / 128 (106 kHz)
0	0	1	fc / 64 (212 kHz)
0	1	0	fc / 32 (424 kHz)
0	1	1	fc / 16 (848 kHz)
1	Х	Х	RFU



4.5.11 Auxiliary definition register

Register space: A Address: 0Ah Type: RW

Bit	Name	Default	Function	Comments		
7	no_crc_rx	0	0: Receive with CRC check 1: Receive without CRC check	Valid for all protocols, for ISO14443A REQA, WUPA and anticollision receive without CRC is done automatically ⁽¹⁾ .		
6	RFU	0	-	-		
5	nfc_id1	0	00: 4 bytes NFCID1			
4	nfc_id0	0	01: 7 bytes NFCID1 1x: RFU	Selects NFCID1 size.		
3	mfaz_cl90	0	0: 0° shifted clock for phase measurement 1: 90° shifted clock for phase measurement	Affects also PM demodulation. Should be set to 0 for PM demodulation.		
2	dis_corr	0	Refer to Table 35	Selects RW receiver operation.		
1	nfc_n1	0		Value of n for direct commands NFC Initial Field		
0	nfc_n0	0	_	ON and NFC Response Field ON $(03)^{(2)}$.		

Table 34. Auxiliary definition register

1. Receive without CRC is done automatically when REQA and WUPA commands are sent using, respectively, direct commands Transmit REQA and Transmit WUPA, and in case anticollision is performed setting bit antcl.

2. The value of nfc_n<1:0> must be set prior to the NFC Initial Field ON and NFC Response Field ON operations.

Table 35. RW receiver operation

Mode	dis_corr = 0	dis_corr = 1
ISO-A (106 to 848 kHz)		NA
ISO-B (106 to 848 kHz)		Pulse reception (coherent)
Felica™ (212 to 424 kHz)	Correlator reception	Pulse reception
NFC Forum Type 1 Tag (Topaz)		NA
Stream modes (scf<1:0> = 01, scp<1:0> = 11)		Pulse reception
Stream modes - Others	NA	Pulse reception



4.5.12 EMD suppression configuration register

Register space: B Address: 05h Type: RW

Bit	Name	Default	Function	Comments
7	emd_emv	0	0: Disable EMD suppression 1: Enable EMD suppression according to EMVCo	Bits no_rx_par and no_crc_rx must be set to 0, and bit nrt_emv must be set to 1 when emd_emv is enabled
6	rx_start_emv	0	0: Reception is enabled (I_rxs) only if the first four bits of the frame are error free 1: Reception is enabled (I_rxs) also if there is an error in the first four bits of the frame	Applies to ISO-A 106k only. Must be set to 1 for EMVCo compliance.
5	RFU	0	-	-
4	RFU	0	-	-
3	emd_thld3	0	If the received frame is less than	
2	emd_thld2	0	emd_thld<3:0> bytes long then	Must be set to 4 for EMVCo compliance.
1	emd_thld1	0	EMD suppression will trigger on reception errors	
0	emd_thld0	0		

Table 36. EMD suppression configuration register



4.5.13 Subcarrier start timer register

Register space: B Address: 06h Type: RW

Table 37. Subcarrier start timer register

Bit	Name	Default	Function	Comments
7:5	RFU	0	-	-
4:0	sst<4:0>	0	Subcarrier start time Step: 0.25 etu Range: 0 etu to 7.75 etu	Applies to ISO-B, 106 kb/s. If the time from the end of the MRT timer to the detection of a subcarrier is shorter than sst<4:0>, then a soft error interrupt is generated. If emd_emv = 1 the frame will be suppressed as EMD and a restart interrupt will be generated. Note that corr_s3 defines the length of subcarrier start detection and affects the correct sst<4:0> setting.



4.5.14 Receiver configuration register 1

Register space: A Address: 0Bh Type: RW

Table 38	. Receiver	configuration	register 1
----------	------------	---------------	------------

Bit	Name	Default	Function	Comments
7	ch sel	0	0: Enable AM channel	If only one Rx channel is enabled in the <i>Operation control register</i> defines which channel is enabled.
1	51_5	0	1: Enable PM channel	If both channels are enabled and manual channel selection is active defines which channel is used for receive framing.
6	lp2	0		
5	lp1	0	Low-pass control (see Table 3)	
4	lp0	0		
3	z600k	0		-
2	h200	0	First and third stage zero setting (see <i>Table 4</i>)	
1	h80	0		
0	z12k	0		



4.5.15 Receiver configuration register 2

Register space: A Address: 0Ch Type: RW

Bit	Name	Default	Function	Comments
7	demod_mode	0	0: AM/PM demodulation 1: I/Q demodulation	Selects demodulator operation mode. I/Q demodulation requires amd_sel = 1.
6	amd_sel	0	0: peak detector 1: mixer	Selects AM demodulator.
5	sqm_dyn	1	0: Squelch disabled 1: Automatic squelch activation after end of TX	Squelch is activated 18.88 µs after end of TX, and stops when the Mask receive timer reaches the sqt<7:0> setting.
4	pulz_61	0	0: Squelch ratio 1 1: Squelch ratio 6/3	 Select squelch trigger level. Squelch triggers on signals that are 1 or 6/3 times larger than the digitizing threshold. Ratio 1: recommended for ISO-A 106k correlator, ISO-A HBR/ISO-B pulse decoder ISO-15693, and FeliCa™ Ratio 6/3: recommended for ISO-A HBR/ISO-B correlator
3	agc_en	1	0: AGC disabled 1: AGC enabled	-
2	agc_m	1	0: AGC operates on first eight sub-carrier pulses 1: AGC operates during complete receive period	-
1	agc_alg	0	0: Algorithm with preset is used 1: Algorithm with reset is used	Algorithm with preset is recommended for protocols with short SOF (like ISO14443A fc / 128).
0	agc6_3	0	0: AGC ratio 3 1: AGC ratio 6	Select AGC trigger level. AGC triggers on signals 3 or 6 times above the minimum detectable signal level.

Table 39. Receiver configuration register 2



4.5.16 Receiver configuration register 3

Register space: A Address: 0Dh Type: RW

Table 40. Receiver configuration register 3

Bit	Name	Default	Function	Comments
7	rg1_am2	1		0: Full gain
6	rg1_am1	1	Gain reduction/boost in first gain stage of AM channel.	1-6: Gain reduction 2.5 dB per step (15 dB total)
5	rg1_am0	0		7: Boost + 5.5 dB
4	rg1_pm2	1		0: Full gain
3	rg1_pm1	1	Gain reduction/boost in first gain stage of PM channel.	1-6: Gain reduction 2.5 dB per step (15 dB total)
2	rg1_pm0	0		7: Boost + 5.5 dB
1	lf_en	0	0: HF signal on receiver input 1: LF signal on receiver input	-
0	lf_op	0	0: differential LF operation 1: LF input split (RFI1 to AM channel, RFI2 to PM channel)	-

4.5.17 Receiver configuration register 4

Register space: A Address: 0Eh Type: RW

Table 41. Receiver configuration register 4⁽¹⁾

Bit	Name	Default	Function	Comments
7	rg2_am3	0		Only values from 0h to Ah are used:
6	rg2_am2	0	AM channel: gain reduction in second and third stage and digitizer	 settings 1h to 4h reduce gain by increasing the digitizer window in 3 dB steps
5	rg2_am1	0		 values from 5h to Ah additionally reduce the gain in second and third gain stage, always in 3 dB steps.
4	rg2_am0	0		
3	rg2_pm3	0		Only values from 0h to Ah are used:
2	rg2_pm2	0	PM channel: gain reduction in second and third stage and digitizer	 settings 1h to 4h reduce gain by increasing the digitizer window in 3 dB steps
1	rg2_pm1	0		 values from 5h to Ah additionally reduce the gain in second and third gain stage, always in
0	rg2_pm0	0		3 dB steps.

1. Direct command Reset RX gain is necessary to load the value of this register into AGC, Squelch, and RSSI block.



4.5.18 P2P receiver configuration register 1

Register space: B Address: 0Bh Type: RW

Bit	Name	Default	Function	Comments
7	ook_fd	0	OOK fast decay	-
6	ook_rc1	0	00 = 1.4 μs	
5	ook_rc0	0	01 = 1.0 μs 10 = 0.6 μs 11 = 0.2 μs	OOK RC time constant
4	ook_thd1	0	Refer to Table 43	OOK threshold level, depends on ook_rc<1:0>
3	ook_thd0	1		configuration.
2	ask_rc1	1	$00 = 8.4 \ \mu s$	
1	ask_rc0	0	01 = 6.8 μs 10 = 4.4 μs 11 = 2.4 μs	ASK RC time constant
0	ask_thd	0	0: 97% 1: 95%	ASK threshold level

Table 42. P2P receiver configuration register 1

Table 43. OOK threshold level settings

ook_thd<1:0>	ook_rc<1:0> = 0	ook_rc<1:0> > 0
00	55%	80%
01	45%	75%
10	35%	70%
11	25%	65%



4.5.19 Correlator configuration register 1

Register space: B Address: 0Ch Type: RW

Bit	Name	Default		Function	Comments	
7	corr_s7	1	AGC =	max AM, PM	-	
6	corr_s6	0	ISO-A 106k	0: Collision detection level defined by corr_s<1:0> 1: Collision detection level equal to data slicer level	Selecting the collision detection level with corr_s<1:0> gives better detection of weak collisions. Setting the collision detection level equal to the data slicer gives better noise immunity.	
			BPSK	0: Correlator phase correction applied during the complete reception1: No correlator phase correction after the first data bytes	No phase correction after start recommended for ISO-B 424 kb/s and 848 kb/s operation.	
5	corr_s5	0		50 mV setting, first squelch step -100 mV 100 mV setting,first squelch step -200 mV	-	
4	corr_s4	1	separat 1: AM a	nd PM correlation signals digitized ely nd PM correlation signals summed before g (summation mode)	Summation mode is recommended for all correlation operations	
3	corr_s3	0	848 kb/	it rate 106kb/s = 33, RX bit rates 212 to	BPSK start length setting (delay from the start of a tags subcarrier signal to the moment when a subcarrier start is detected). Then circuit starts observing for the first phase transition $(9/17/33 \pm$ 2 pilot pulses). At this moment the sst<4:0> check for TR0 is done.	
			ISO-A 106k	0: Normal data slicer 1: Fast data slicer		
2	corr_s2	0	BPSK ⁽	0: Normal reference time constant 1: Long reference time constant (1.5x normal)	-	
			ISO-A 106k	Collision level setting MSB		
1	corr_s1	orr_s1 1 I	corr_s1 1	BPSK ⁽	Subcarrier end detection level 0: 100% 1: 66%	Collision detection level, compared to data detection level: - 00: 16% - 01: 28%
0	corr s0	1	ISO-A 106k	Collision level setting LSB	- 10: 41% - 11: 53%	
	0 corr_s0	I	BPSK ⁽	0: Subcarrier end detector disabled 1: Subcarrier end detector enabled		

1. BPSK options apply to ISO-A HBR and ISO-B (all bit rates).



4.5.20 Correlator configuration register 2

Register space: B Address: 0Dh Type: RW

Table 45. Correlator configuration register 2

Bit	Name	Default	Function	Comments
7	RFU	0		
6	RFU	0		
5	RFU	0		
4	RFU	0	-	
3	RFU	0		
2	RFU	0		
1	corr_s9	0	0: Sleep mode disable set by timer 1: Sleep mode disable only on rx_on = 1	Correlator sleep mode option. Sleep start: 18 µs no output pulse. Stop with timer: – takes 18 µs (ISO-A/B, F424) – takes 42 µs (stream 15693, F212)
0	corr_s8	0	0: All other standards 1: 424 kHz subcarrier stream mode	Must be set to 1 for 424 kHz subcarrier stream mode.



4.5.21 Mask receive timer register

Register space: A Address: 0Fh Type: RW

Table 46.	Mask	receive	timer	register
10.010 101				

Bit	Name	Default	Function	Comments
7	mrt7	0	met atom - 0:	
6	mrt6	0	mrt_step = 0: Step: 64 / fc (4.72 μs)	
5	mrt5	0	Range: 256 / fc (~18.88 µs) to	Set time after end of TX during which the
4	mrt4	0	16320 / fc (~1.2 ms)	receiver output is ignored (masked).
3	mrt3	1	mrt step = 1:	The minimum mask receive time of 18.88 µs covers the transients in receiver after end of
2	mrt2	0	Step: 512 / fc (37.78 µs)	transmission.
1	mrt1	0	Range: 2048 / fc (151 µs) to 130560 / fc (9.62 ms)	
0	mrt0	0	100000710(0.021113)	



4.5.22 No-response timer register 1

Register space: A Address: 10h Type: RW

Table 47. No-response timer register 1

Bit	Name	Default	Function	Comments
7	nrt15	0	No-response timer definition	Defines timeout after end of Tx. If this timeout
6	nrt14	0	MSB bits	expires without detecting a response a No-response interrupt is sent.
5	nrt13	0	nrt step = 0:	In NFC mode the No-response timer is started only when external field is detected. In the
4	nrt12	0	Step: 64 / fc (4.72 µs),	NFCIP-1 active communication mode the
3	nrt11	0	Range: 309 ms	No-response timer is automatically started when the transmitter is turned off after the message has
2	nrt10	0	nrt_step = 1:	been sent.
1	nrt9	0	Step: 4096 / fc (302 µs)	All 0: No-response timer is not started. No-response timer is reset and restarted with
0	nrt8	0	Range: 19.8 s.	Start No-response timer direct command.

4.5.23 No-response timer register 2

Register space: A Address: 11h Type: RW

Table 48. No-response timer register 2

Bit	Name	Default	Function	Comments
7	nrt7	0		
6	nrt6	0		
5	nrt5	0		
4	nrt4	0	No-response timer definition	
3	nrt3	0	LSB bits	-
2	nrt2	0		
1	nrt1	0		
0	nrt0	0		



4.5.24 Timer and EMV[®] control register

Register space: A

Address: 12h

Type: RW

Table 49. Timer and EMV control register

Bit	Name	Default	Function	Comments
7	gptc2	0		
6	gptc1	0	General purpose timer trigger source. Refer to <i>Table 50</i> .	-
5	gptc0	0		
4	RFU	0	-	-
3	mrt_step	0	0: 64 / fc 1: 512 / fc	Mask receive timer step size
2	nrt_nfc	0	0: NRT starts at end of TX (own field off) 1: NRT starts at peer field-on event	No-response timer start condition in AP2P initiator and target mode.
1	nrt_emv	0	1: No-response timer EMV mode	-
0	nrt_step	0	0: 64 / fc 1: 4096 / fc	No-response timer step size.

Table 50. Trigger sources

gptc2	gptc1	gptc0	Trigger source	
Х	Х	Х	The timer starts always with direct command Start General purpose timer.	
0	0	0	No additional trigger source.	
0	0	1	Additionally starts at End of RX (after EOF).	
0	1	0	Additionally starts at Start of RX.	
0	1	1	Additionally starts at End of TX. In AP2P modes the timer is used to switch the field off. In AP2P modes enables NRT start according to nrt_nfc description.	
1	0	0		
1	0	1	DELL	
1	1	0	RFU	
1	1	1		



4.5.25 General purpose timer register 1

Register space: A Address: 13h Type: RW

Table 51. General purpose timer register 1

Bit	Name	Default	Function	Comments
7	gpt15	-		
6	gpt14	-		
5	gpt13	-	General purpose timeout	
4	gpt12	-	definition MSB bits Defined in steps of 8 / fc (590 ns) Range from 590 ns to 38,7 ms	
3	gpt11	-		-
2	gpt10	-		
1	gpt9	-		
0	gpt8	-		

4.5.26 General purpose timer register 2

Register space: A

Address: 14h

Type: RW

Table 52. General purpose timer register 2

Bit	Name	Default	Function	Comments
7	gpt7	-		
6	gpt6	-		
5	gpt5	-	General purpose timeout definition LSB bits Defined in steps of 8 / fc (590 ns)	
4	gpt4	-		
3	gpt3	-		_
2	gpt2	-	Range from 590 ns to 38,7 ms	
1	gpt1	-		
0	gpt0	-		



4.5.27 PPON2 field waiting register

Register space: A Address: 15h Type: RW

Table 53. $\ensuremath{\mathsf{PP}_{\mathsf{ON2}}}$ field waiting register

Bit	Name	Default	Function	Comments
7	ppt7	1		
6	ppt6	0		
5	ppt5	0		
4	ppt4	0	PP _{ON2} timer Step: 64 / fc (4.72 μs)	Maximum time the system waits for the peer
3	ppt3	0	Range: 1.204 ms	device field on in AP2P mode.
2	ppt2	0		
1	ppt1	0		
0	ppt0	0		



4.5.28 Squelch timer register

Register space: B Address: 0Fh Type: RW

Table 54. Squelch timer register

Bit	Name	Default	Function	Comments
7	sqt7	0		
6	sqt6	0		Squelch is enabled ~20 µs after the end of
5	sqt5	0	Squelch Timer	reader data transmission
4	sqt4	0	Step, Range: same as <i>Mask</i> receive timer register, including mrt_step selection	 sqt<7:0> > 5: Squelch stops after the time defined by sqt<7:0>. Gain reduction due to squelch is locked and used as a starting point for AGC. Sqt<7:0> ≤ 5 or sqt<7:0> ≥ mrt<7:0>:
3	sqt3	0		
2	sqt2	0		
1	sqt1	0		Squelch is enabled until the MRT expires.
0	sqt0	0		

4.5.29 NFC field on guard timer register

Register space: B

Address: 15h

Type: RW

Table 55. NFC field on guard timer register

	· · · · · · · · · · · · · · · · · · ·					
Bit	Name	Default	Function	Comments		
7	nfc_gt7	0				
6	nfc_gt6	0				
5	nfc_gt5	1		Used by NFC field on commands.		
4	nfc_gt4	1	NFC field on guard timer Step: 2048 / fc (151 µs)	The value nfc_gt<7:0> is added to the initial 75 μ s in T _{IREG} and T _{AREG} .		
3	nfc_gt3	0	Range: 38.66 ms	Set to 33 for T_{IRFG} (75 µs + 4.984 ms= 5.06 ms)		
2	nfc_gt2	0		Set to 0 for T_{ARFG} (75 µs + 0 ms = 75 µs)		
1	nfc_gt1	1				
0	nfc_gt0	1				

4.5.30 Mask main interrupt register

Register space: A Address: 16h Type: RW

Table 56. Mask main interrupt register

Bit	Name	Default	Function Comments	
7	M_osc	0	1: Mask IRQ when oscillator frequency is stable	-
6	M_wl	0	1: Mask IRQ due to FIFO water level	-
5	M_rxs	0	: Mask IRQ due to start of receive -	
4	M_rxe	0	1: Mask IRQ due to end of receive -	
3	M_txe	0	: Mask IRQ due to end of transmission -	
2	M_col	0	1: Mask IRQ due to bit collision	-
1	M_rx_rest	0	: Mask IRQ due to automatic reception restart -	
0	RFU	0	Not used	-

4.5.31 Mask timer and NFC interrupt register

Register space: A

Address: 17h

Type: RW

Table 57. Mask timer and NFC interrupt register

Bit	Name	Default	Function	Comments
7	M_dct	0	1: Mask IRQ due to termination of direct command	-
6	M_nre	0	1: Mask IRQ due to No-response timer expire	-
5	M_gpe	0	1: Mask IRQ due to general purpose timer expire	-
4	M_eon	0	1: Mask IRQ due to detection of external field higher	
3	M_eof	0	1: Mask IRQ due to detection of external field drop below Target activation level	
2	M_cac	0	1: Mask IRQ due to detection of collision during RF Collision Avoidance	-
1	M_cat	0	1: Mask IRQ after minimum guard time expire -	
0	M_nfct	0	1: Mask IRQ when in target mode the initiator bit rate has been recognized	-



4.5.32 Mask error and wake-up interrupt register

Register space: A Address: 18h Type: RW

Table 58. Mask error and wake-up interrupt register

Bit	Name	Default	Function Comments	
7	M_crc	0	1: Mask IRQ due to CRC error	-
6	M_par	0	1: Mask IRQ due to parity error	-
5	M_err2	0	1: Mask IRQ due to soft framing error -	
4	M_err1	0	1: Mask IRQ due to hard framing error -	
3	M_wt	0	1: Mask IRQ due to wake-up timer interrupt -	
2	M_wam	0	1: Mask Wake-up IRQ due to amplitude measurement -	
1	M_wph	0	1: Mask Wake-up IRQ due to phase measurement	
0	M_wcap	0	1: Mask Wake-up IRQ due to capacitance measurement	-

4.5.33 Mask passive target interrupt register

Register space: A

Address: 19h

Type: RW

Table 59. Mask passive target interrupt register

Bit	Name	Default	Function Comments	
7	M_ppon2	0	1: Mask IRQ from PPON2 field on waiting timer -	
6	M_sl_wl	0	1: Mask IRQ for Passive target slot number water level	-
5	M_apon	0	1: Mask IRQ due to Active PP Field on event -	
4	M_rxe_pta	0	1: Mask IRQ due to end of receive when the device is handling the response	
3	M_wu_f	0	1: Mask IRQ NFC 212/424 kb/s passive target active	-
2	RFU	0	-	-
1	M_wu_a*	0	1: Mask IRQ NFC 106 kb/s passive target Active* -	
0	M_wu_a	0	1: Mask IRQ NFC 106 kb/s passive target Active	-



4.5.34 Main interrupt register

Register space: A Address: 1Ah

Type: R

Table 60. Main interrupt register

Bit	Name	Default	Function	Comments
7	I_osc	-	IRQ when oscillator frequency is stable	Set after oscillator is started by setting <i>Operation control register</i> bit en.
6	I_wI	-	IRQ due to FIFO water level	Set during receive, if more than 300 bytes are in the FIFO. Set during transmit, if less than 200 bytes are in the FIFO.
5	I_rxs	-	IRQ due to start of receive	-
4	I_rxe	-	IRQ due to end of receive	-
3	I_txe	-	IRQ due to end of transmission	-
2	I_col	-	IRQ due to bit collision	-
1	I_rx_rest	-	IRQ due to automatic reception restart	Set when a frame is suppressed as EMD
0	RFU	-	-	-



4.5.35 Timer and NFC interrupt register

Register space: A Address: 1Bh

_ _

Type: R

Table 61. Timer and NFC interrupt register⁽¹⁾

Bit	Name	Default	Function	Comments
7	I_dct	-	IRQ due to termination of direct command	-
6	I_nre	-	IRQ due to No-response timer expire	-
5	I_gpe	-	IRQ due to general purpose timer expire	-
4	I_eon	-	IRQ due to detection of external field higher than Target activation level	-
3	I_eof	-	IRQ due to detection of external field drop below Target activation level	-
2	l_cac	-	IRQ due to detection of collision during RF collision avoidance	I-cac must be cleared before collision avoidance.
1	I_cat	-	IRQ after minimum guard time expire	An external field was not detected during RF collision avoidance, field was switched on, IRQ sent after minimum guard time according to NFCIP-1.
0	I_nfct	-	IRQ when in target mode the initiator bit rate was recognized	-

1. After register has been read, its content is set to 0.



4.5.36 Error and wake-up interrupt register

Register space: A Address: 1Ch Type: R

Table 62. Error and wake-up interrupt register⁽¹⁾

Bit	Name	Default	Function	Comments
7	I_crc	-	CRC error	-
6	I_par	-	Parity error	-
5	I_err2	-	Soft framing error	Framing error that does not result in corrupted Rx data.
4	I_err1	-	Hard framing error	Framing error that results in corrupted Rx data.
3	I_wt	-	Wake-up timer interrupt	Timeout after execution of Start Wake-Up Timer command in case option with IRQ at every timeout is selected.
2	I_wam	-	Wake-up interrupt due to amplitude measurement	Result of amplitude measurement Δ am larger than reference.
1	I_wph	-	Wake-up interrupt due to phase measurement.	Result of phase measurement Δpm larger than reference.
0	I_wcap	-	Wake-up interrupt due to capacitance measurement	Result of capacitance measurement Δ cm larger than reference.

1. After Main interrupt register has been read, its content is set to 0.



4.5.37 Passive target interrupt register

Register space: A Address: 1Dh Type: R

Table 63. Passive target interrupt register⁽¹⁾

Bit	Name	Default	Function	Comments
7	I_ppon2	-	PPON2 field on waiting timer interrupt	-
6	l_sl_wl	-	IRQ for passive target slot number water level	Sent if four unused slot numbers (TSN) remain in PT_memory.
5	l_apon	-	IRQ due to active P2P field on event	Sent after RF collision avoidance, if there was no collision and field was turned on.
4	I_rxe_pta	-	IRQ due to end of receive, the device is handling the response	Sent in passive target mode when NFC-A anti-collision or NFC-F SENSF_RES is automatically sent (MCU action required).
3	l_wu_f	-	NFC 212/424kb/s passive target 'Active' interrupt	Sent after NFC 212/424 kb/s automatic response to SENSF_REQ was sent.
2	RFU	-	RFU	-
1	I_wu_a*	-	Passive target Active* interrupt	Sent when Active* state is reached.
0	l_wu_a	-	Passive target Active interrupt	Sent when Active state is reached.

1. After register has been read, its content is set to 0.



4.5.38 FIFO status register 1

Register space: A Address: 1Eh Type: R

Table 64. FIFO status register 1

Bit	Name	Default	Function	Comments
7	fifo_b7	-		
6	fifo_b6	-		
5	fifo_b5	-		
4	fifo_b4	-	Number of bytes in the FIFO	Valid range is from 0 to 512.
3	fifo_b3	-	(LSB)	
2	fifo_b2	-		
1	fifo_b1	-		
0	fifo_b0	-		

4.5.39 FIFO status register 2

Register space: A Address: 1Fh Type: R

Table 65. FIFO status register 2

Bit	Name	Default	Function	Comments
7	fifo_b9	-	Number of bytes in the FIFO	-
6	fifo_b8	-	(MSB)	-
5	fifo_unf	-	1: FIFO underflow	-
4	fifo_ovr	-	1: FIFO overflow	-
3	fifo_lb2	-		The received bits are stored in the LSB part of the last byte in the FIFO. If I err1 is set then fifo Ib<2:0> dos not contain
2	fifo_lb1	-	Number of bits in the last FIFO byte if it was not complete	
1	fifo_lb0	-	byte in it was not complete	valid data.
0	np_lb	-	1: Parity bit is missing in the last byte	The bit is set if the last received byte is complete with 8 data bits but the parity bit is missing. If I_err1 is set then np_lb does not contain valid data.



4.5.40 Collision display register

Register space: A Address: 20h Type: R

Bit	Name	Default	Function	Comments
7	c_byte3	-		
6	c_byte2	-	Number of full bytes before the	The Collision display register range covers
5	c_byte1	-	bit collision happened.	ISO14443A anticollision command. If collision (or framing error interpreted as collision) happens in
4	c_byte0	-		a longer message, the Collision display register
3	c_bit2	-	Number of bits before the	is not set. If I_err1 is set then c_byte<3:0> and c_bit<2:0> do not contain valid data.
2	c_bit1	-	collision in the byte where the	
1	c_bit0	-	collision happened	
0	c_pb	-	1: Collision in parity bit 0: no collision	This error is reported if the first detected collision is in a parity bit. If I_err1 is set then c_pb dos not contain valid data.



4.5.41 Passive target display register

Register space: A Address: 21h Type: R

Table 67. Passive target display register

Bit	Name	Default	Function	Comments
7	RFU	-	-	-
6	RFU	-	-	-
5	RFU	-	-	-
4	RFU	-	-	-
3	pta_state3	-	0000: POWER OFF 0001: IDLE 0010: READY_L1	
2	pta_state2	-	0011: READY_L2 0100: RFU 0101:ACTIVE	ISO-A passive target states. In ACTIVE or ACTIVE* state, the MCU must
1	pta_state1	-	0110: RFU 1001: HALT 1010: READY_L1*	handle all commands, including SENSE/IDLE and SLEEP/HALT.
0	pta_state0	-	1011: READY_L2* 1100: RFU 1101: ACTIVE*	



4.5.42 Number of transmitted bytes register 1

Register space: A Address: 22h Type: RW

Table 68. Number of transmitted bytes register 1

Bit	Name	Default	Function	Comments
7	ntx12	0		
6	ntx11	0		
5	ntx10	0		
4	ntx9	0	Number of full bytes to be	Novimum supported number of butes is 9101
3	ntx8	0	transmitted, MSB bits first.	Maximum supported number of bytes is 8191.
2	ntx7	0		
1	ntx6	0		
0	ntx5	0		

4.5.43 Number of transmitted bytes register 2

Register space: A Address: 23h Type: RW

Table 69. Number of transmitted bytes register 2^{(1) (2)}

Bit	Name	Default	Function	Comments
7	ntx4	0		
6	ntx3	0		
5	ntx2	0	Number of full bytes to be transmitted, MSB bits first.	Maximum supported number of bytes is 8191. Bit transmission starts from LSB. Applicable for
4	ntx1	0		
3	ntx0	0		
2	nbtx2	0	Number of bits to transmit after the last full byte. Set to 000 to transmit only full	
1	nbtx1	0		 bit oriented anticollision frame when last byte is a split byte
0	nbtx0	0	bytes.	 Tx is done without parity bit generation

1. If anctl bit is set while card is in idle state and nbtx is not 000, then i_par will be triggered during REQA and WUPA direct command is issued.

2. Transmission of short or incomplete messages only works for ISO-A/B using the command Transmit without CRC.



4.5.44 Bit rate detection display register

Register space: A Address: 24h Type: R

Table 70. Bit rate detection display register

Bit	Name	Default	Function	Comments
7	RFU	-	-	-
6	RFU	-	-	-
5	nfc_rate1	-	Defende Table 04	Result of automatic bit rate detection in the bit rate detection target mode.
4	nfc_rate0	-	Refer to Table 24	
3	ppt2_on	-	1: PP _{ON2} timer is running	
2	gpt_on	-	1: General purpose timer is running	State of internal timers.
1	nrt_on	-	1: No-response timer is running	
0	mrt_on	-	1: Mask receive timer is running	



4.5.45 A/D converter output register

Register space: A Address: 25h Type: R

Table 71. A/D converter output regist	er
---------------------------------------	----

Bit	Name	Default	Function	Comments
7	ad7	-		
6	ad6	-		
5	ad5	-		
4	ad4	-	Displays the result of the last	
3	ad3	-	A/D conversion.	-
2	ad2	-		
1	ad1	-		
0	ad0	-		



4.5.46 Antenna tuning control register 1

Register space: A Address: 26h Type: RW

Table 72. Antenna tuning control register 1

Bit	Name	Default	Function	Comments
7	aat_A_7	1		
6	aat_A_6	0		
5	aat_A_5	0		
4	aat_A_4	0	AAT-A D/A converter input.	AAT-A voltage (in V) =
3	aat_A_3	0	AAT-A DIA conventer input.	(0.044 + 0.868 * aat_A<7:0> / 255) * V _{DD_A}
2	aat_A_2	0		
1	aat_A_1	0		
0	aat_A_0	0		

4.5.47 Antenna tuning control register 2

Register space: A Address: 27h Type: RW

Table 73. Antenna tuning control register 2

Bit	Name	Default	Function	Comments
7	aat_B_7	1		
6	aat_B_6	0		
5	aat_B_5	0		
4	aat_B_4	0		AAT-B voltage (in V) =
3	aat_B_3	0	AAT-B D/A converter input.	(0.044 + 0.868 * aat_B<7:0> / 255) * V _{DD_A}
2	aat_B_2	0		
1	aat_B_1	0		
0	aat_B_0	0		



4.5.48 TX driver register

Register space: A Address: 28h Type: RW

Table 74. TX driver register

Bit	Name	Default	Function	Comments
7	am_mod3	0		
6	am_mod2	1	AM modulation index	
5	am_mod1	1	(see Table 75)	-
4	am_mod0	1		
3	d_res3	0		
2	d_res2	0	RFO driver resistance	
1	d_res1	0	(see Table 76)	-
0	d_res0	0		

Table 75. AM modulation index

am_mod<3:0>	Modulation (%)		
0	5		
1	6		
2	7		
3	8		
4	9		
5	10		
6	11		
7	12		
8	13		
9	14		
10	15		
11	17		
12	19		
13	22		
14	26		
15	40		



d_res<3:0>	Driver output resistance $(\Omega)^{(1)}$	
0	1.0	
1	2.0	
2	4.1	
3-4	8.3	
5-14	17.1	
15	High Z	

Table 76. RFO driver resistance

1. The value has to be multiplied by the RFO resistance from *Section 5.4: Electrical characteristics* to obtain the driver output resistance for the corresponding d_res setting.



4.5.49 Auxiliary modulation setting register

Register space: B Address: 28h Type: RW

Table 77. Auxiliary modulation setting register

Bit	Name	Default	Function	Comments
7	dis_reg_am	0	0: Regulator AM enabled 1: Regulator AM disabled	Uses am_mod<3:0> to set the modulation index for regulator based AM modulation. Logic of this bit is inverted. Set to 0 to enable regulator AM.
6	lm_ext_pol	0	0: Normal polarity 1: Inverse polarity	Normal polarity: LM_EXT pin load modulation signal is active high. Inverse polarity: LM_EXT pin load modulation signal is active low.
5	lm_ext	0	0: External load modulation disabled 1: External load modulation enabled	Enables output of load modulation signal on LM_EXT pin.
4	lm_dri	1	0: Driver load modulation disabled 1: Driver load modulation enabled	Uses <i>Passive target modulation register</i> to set driver load modulation resistance.
3	res_am	0	0: Resistive AM modulation disabled 1: Resistive AM modulation enabled	Uses md_res<6:0> to configure resistive AM modulated driver resistance.
2	RFU	0	-	-
1	RFU	0	-	-
0	RFU	0	-	-



4.5.50 Passive target modulation register

Register space: A Address: 29h Type: RW

Table 78. Passive target modulation register

Bit	Name	Default	Function	Comments
7	ptm_res3	0		RFO resistance during passive load modulation,
6	ptm_res2	1		modulated state.
5	ptm_res1	1		ptm_res<3:0> must be set before the <i>Mode</i>
4	ptm_res0	1	- Refer to <i>Table 79</i>	<i>definition register</i> is set to passive target mode.
3	pt_res3	0		RFO resistance during passive load modulation,
2	pt_res2	0		unmodulated state.
1	pt_res1	0		pt_res<3:0> must be set before the <i>Mode</i>
0	pt_res0	0		<i>definition register</i> is set to passive target mode.

Table 79. Passive target modulated and unmodulated state driver output resistance

ptm_res<3:0> pt_res<3:0>	Driver output resistance R _{RFO} (normalized) ⁽¹⁾
0	1.0
1	2.0
2	4.1
3	8.3
4	12.2
5	17.1
6	25.6
7	32.0
8	36.6
9	42.7
10	51.2
11	64.0
12	85.3
13	128.0
14	256.0
15	High Z

1. The value has to be multiplied by the RFO resistance from *Section 5.4: Electrical characteristics* to obtain the driver output resistance for the corresponding ptm/pt_res setting.



4.5.51 TX driver timing register

Register space: B Address: 29h Type: RW

Table 80. TX driver timing register

Bit	Name	Default	Function	Comments	
7	d_rat_t3	0		The value presents the target ratio between one RF	
6	d_rat_t2	1		period and whole non-overlap time (both sides L to H and H to L).	
5	d_rat_t1	1	Driver transient ratio target	The system starts with the slowest available	
4	d_rat_t0	1	(in number of non-overlap times in one RF period)	transient and measures the ratio. If this is lower than targeted the system switches to faster transient. The procedure is repeated until the target ratio is reached (or exceeded for the first time). There are five steps available, procedure can take up to ten RF periods.	
3	d_tim_man	1	0: Use automatically acquired timing setting 1: Use manual timing setting	-	
2	d_tim_m2	1	000: Slow		
1	d_tim_m1	0	001: Medium slow 010: Nominal	Manual driver timing used if d, tim, man is set to 1	
0	d_tim_m0	0	010. Nominal 011: Medium fast 1xx: Fast	Manual driver timing, used if d_tim_man is set to 1.	



4.5.52 External field detector activation threshold register

Register space: A

Address: 2Ah

Type: RW

Table 81. External field detector activation threshold register⁽¹⁾

Bit	Name	Default	Function	Comments
7	RFU	0	Not used	-
6	trg_l2	0		
5	trg_l1	1	Peer detection threshold. Refer to <i>Table 85</i> .	-
4	trg_10	1		
3	rfe_t3	0		
2	rfe_t2	0	Collision avoidance threshold.	
1	rfe_t1	1	Refer to Table 86.	-
0	rfe_t0	1		

1. The value of rfe_3 (see *Table 86*) must be the same for the activation and deactivation thresholds.



4.5.53 Resistive AM modulation register

Register space: B Address: 2Ah Type: RW

Table 82. Resistive AM modulation register

Bit	Name	Default	Function	Comments
7	fa3_f	0	0: Use normal non-overlap	_
		•	1: Use minimum non-overlap	
6	md_res6	0		
5	md_res5	0		
4	md_res4	0		
3	md_res3	0	Refer to Table 83.	Resistive AM modulated state driver output resistance.
2	md_res2	0		
1	md_res1	0		
0	md_res0	0		

Table 83. Resistive AM modulated state driver output resistance

md_res<6:0>	Driver output resistance R _{RFO} (normalized) ⁽¹⁾	md_res<6:0>	Driver output resistance R _{RFO} (normalized) ⁽¹⁾
0	1.004	64	4.063
1	1.020	65	4.129
2	1.036	66	4.197
3	1.053	67	4.267
4	1.071	68	4.339
5	1.089	69	4.414
6	1.108	70	4.491
7	1.128	71	4.571
8	1.148	72	4.655
9	1.169	73	4.741
10	10 1.191		4.830
11	11 1.213		4.923
12	1.237	76	5.020
13	1.261	77	5.120
14	1.286	78	5.224
15	1.313	79	5.333
16	1.340	80	5.447



md_res<6:0>	Driver output resistance R _{RFO} (normalized) ⁽¹⁾	md_res<6:0>	Driver output resistance R _{RFO} (normalized) ⁽¹⁾	
17	1.369	81	5.565	
18	1.399	82	5.689	
19	1.430	83	5.818	
20	1.463	84	5.953	
21	1.497	85	6.095	
22	1.533	86	6.244	
23	1.571	87	6.400	
24	1.610	88	6.564	
25	1.652	89	6.737	
26	1.695	90	6.919	
27	1.741	91	7.111	
28	1.790	92	7.314	
29	1.842	93	7.529	
30	1.896	94	7.758	
31	1.954	95	8.000	
32	2.016	96	8.258	
33	2.081	97	8.533	
34	2.151	98	8.828	
35	2.226	99	9.143	
36	2.306	100	9.481	
37	2.349	101	9.846	
38	2.393	102	10.24	
39	2.438	103	10.67	
40	2.485	104	11.13	
41	2.535	105	11.64	
42	2.586	106	12.19	
43	2.639	107	12.80	
44	2.695	108	13.47	
45	2.753	109	14.22	
46	2.813	110	15.06	
47	2.876	111	16.00	
48	2.943	112	17.07	
49	3.012	113	18.29	
50	3.084	114	19.69	

Table 83. Resistive AM modulated state driver output resistance (continued)



md_res<6:0>	Driver output resistance R _{RFO} (normalized) ⁽¹⁾	md_res<6:0>	Driver output resistance R _{RFO} (normalized) ⁽¹⁾
51	3.160	115	21.3
52	3.241	116	23.3
53	3.325	117	25.6
54	3.413	118	28.4
55	3.507	119	32.0
56	56 3.606		36.6
57	3.657	121	42.7
58	3.710	122	51.2
59	59 3.765		64.0
60	60 3.821		85.3
61	61 3.879		128
62	62 3.938		256
63	4.000	127	High Z

Table 83. Resistive AM modulated state driver out	put resistance (continued)

1. The value has to be multiplied by the RFO resistance from Section 5.4: Electrical characteristics to obtain the driver output resistance for the corresponding md_res setting.

4.5.54 External field detector deactivation threshold register

Register space: A Address: 2Bh

Type: RW

Table 84. External field detector deactivation threshold register⁽¹⁾

Bit	Name	Default	Function	Comments
7	RFU	0	Not used	-
6	trg_ld2	0		
5	trg_ld1	1	Deactivation peer detection threshold (see <i>Table 85</i>).	-
4	trg_ld0	1		
3	rfe_td3	0		
2	rfe_td2	0	Deactivation collision avoidance	
1	rfe_td1	1	threshold (see Table 86).	-
0	rfe_td0	1		

1. The value of rfe_3 (see *Table 86*) must be the same for the activation and deactivation thresholds.



trg_l2	trg_l1	trg_I0	Peer detection threshold voltage (mV _{pp}) on RFI1
ti <u>g_</u> 12	" <u>"</u> "		reer detection tilleshold voltage (inv _{pp}) on Rinn
0	0	0	75
0	0	1	105
0	1	0	150
0	1	1	205
1	0	0	290
1	0	1	400
1	1	0	560
1	1	1	800

Table 85. Peer detection threshold as seen on RFI1 input

Table 86. Collision avoidance threshold as seen on RFI1 input

rfe_3	rfe_2	rfe_1	rfe_0	Collision avoidance threshold voltage (mV $_{\rm pp}$) on RFI1
0	0	0	0	75
0	0	0	1	105
0	0	1	0	150
0	0	1	1	205
0	1	0	0	290
0	1	0	1	400
0	1	1	0	560
0	1	1	1	800
1	0	0	0	25
1	0	0	1	33
1	0	1	0	47
1	0	1	1	64
1	1	0	0	90
1	1	0	1	125
1	1	1	0	175
1	1	1	1	250



4.5.55 TX driver timing display register

Register space: B Address: 2Bh

Type: R

Bit	Name	Default	Function	Comments
7	d_rat_r3	-		
6	d_rat_r2	-	Driver Transient ratio readout (in number of non-overlap	Driver transient ratio readout
5	d_rat_r1	-	times in one RF period)	
4	d_rat_r0	-		
3	RFU	-	-	-
2	d_tim_r2	-	000: Slow	
1	d_tim_1	-	001: Medium slow 010: Nominal	Driver timing readout
0	d_tim_0	-	011: Medium fast 1xx: Fast	Driver timing readout



4.5.56 Regulator voltage control register

Register space: A

Address: 2Ch

Type: RW

Table 88. Regulator voltage control register

Bit	Name	Default	Function	Comments	
7	reg_s	0	0: Regulated voltages are defined by result of Adjust Regulators command 1: Regulated voltages are defined by rege_x bits written in this register	Defines mode of regulator voltage setting.	
6	rege_3	0	External definition of regulated values	In 5 \/ mode \/ and \/ regulators	
5	rege_2	0	External definition of regulated voltage (see <i>Table 90</i>).	In 5 V mode V_{DD_D} and V_{DD_A} regulators are set to 3.4 V.	
4	rege_1	0	In 5 V mode V_{DD_D} and V_{DD_A}	In 3.3 V mode $V_{DD_{D}}$ and $V_{DD_{A}}$ regulators	
3	rege_0	0	regulators are set to 3.4 V	are set to the same value as V _{DD_RF} .	
2	mpsv2	0	000: V _{DD} 001: V _{DD_A} 010: V		
1	mpsv1	0	010: V _{DD_D} 011: V _{DD_RF} 100: V _{DD_AM}	Defines source of direct command <i>Measure</i> power supply.	
0	mpsv0	0	101: RFU 110: RFU 111: RFU		



4.5.57 Regulator display register

Register space: B Address: 2Ch Type: R

Table 89. Regulator display register

Bit	Name	Default	Function	Comments
7	reg_3	-		
6	reg_2	-	Voltage regulator setting after Adjust regulators command.	
5	reg_1	-	Refer to <i>Table 90</i> for definition.	-
4	reg_0	-		
3	RFU	-	-	-
2	RFU	-	-	-
1	RFU	-	-	-
0	i_lim	-	1: V _{DD_RF} regulator in current limit mode	-

Table 90. Regulated voltages

reg_3	reg_2	reg_1	reg_0	Typical regula	ted voltage (V)
rege_3	rege_2	rege_1	rege_0	5 V mode	3.3 V mode
1	1	1	1	5.1	3.4
1	1	1	0	5.0	3.3
1	1	0	1	4.9	3.2
1	1	0	0	4.8	3.1
1	0	1	1	4.7	3.0
1	0	1	0	4.6	2.9
1	0	0	1	4.5	2.8
1	0	0	0	4.4	2.7
0	1	1	1	4.3	2.6
0	1	1	0	4.2	2.5
0	1	0	1	4.1	2.4
0	1	0	0	4.0	-
0	0	1	1	3.9	-
0	0	1	0	3.8	-
0	0	0	1	3.7	-
0	0	0	0	3.6	-



4.5.58 RSSI display register

Register space: A

Address: 2Dh

Type: R

Table 91. RSSI display register

Bit	Name	Default	Function	Comments
7	rssi_am_3	-		
6	rssi_am_2	-	AM channel RSSI peak value.	Stores the AM channel RSSI peak value until the start of the next reception, or until the <i>Clear RSSI</i>
5	rssi_am_1	-	Refer to <i>Table 92</i> for definition.	command is sent.
4	rssi_am_0	-		
3	rssi_pm_3	-		
2	rssi_pm_2	-	PM channel RSSI peak value.	Stores the PM channel RSSI peak value until the start of the next reception, or until the <i>Clear RSSI</i>
1	rssi_pm_1	-	Refer to <i>Table 92</i> for definition.	command is sent.
0	rssi_pm_0	-		

rssi_3	rssi_2	rssi_1	rssi_0	Typical signal on RFI1 (mV _{rms})
0	0	0	0	≤20
0	0	0	1	>20
0	0	1	0	>27
0	0	1	1	>37
0	1	0	0	>52
0	1	0	1	>72
0	1	1	0	>99
0	1	1	1	>136
1	0	0	0	>190
1	0	0	1	>262
1	0	1	0	>357
1	0	1	1	>500
1	1	0	0	>686
1	1	0	1	>950
1	1	1	0	>1150
1	1	1	1	- 1150

Table 92. RSSI



4.5.59 Gain reduction state register

Register space: A Address: 2Eh Type: R

Table 93. Gain reduction state register

Bit	Name	Default	Function	Comments
7	gs_am_3	-		
6	gs_am_2	-	Refer to rg2_am<3:0> for value	Overall AM channel second and third stage gain reduction (includes register gain reduction,
5	gs_am_1	-	explanation.	squelch and AGC).
4	gs_am_0	-		
3	gs_pm_3	-		
2	gs_pm_2	-	Refer to rg2_pm<3:0> for value	Overall PM channel second and third stage gain reduction (includes register gain reduction,
1	gs_pm_1	-	explanation.	squelch and AGC).
0	gs_pm_0	-		



4.5.60 Capacitive sensor control register

Register space: A Address: 2Fh Type: RW

Table 94. Capacitive sensor control register

Bit	Name	Default	Function	Comments
7	cs_mcal4	0	1.6 pF	
6	cs_mcal3	0	0.8 pF	Manual capacitive sensor calibration value
5	cs_mcal2	0	0.4 pF	(binary weighted). Sets cs mcal<4:0> to 0 to enable automatic
4	cs_mcal1	0	0.2 pF	calibration mode.
3	cs_mcal0	0	0.1 pF	
2	cs_g2	0	000: 2.8 V / pF 001: 6.5 V / pF	
1	cs_g1	0	010: 1.1 V / pF 100: 0.5 V / pF	Capacitor sensor gain.
0	cs_g0	0	110: 0.35 V / pF Others: Not used	

4.5.61 Capacitive sensor display register

Register space: A

Address: 30h

Type: R

Table 95. Capacitive sensor display register

Bit	Name	Default	Function	Comments
7	cs_cal4	-	1.6 pF	
6	cs_cal3	-	0.8 pF	
5	cs_cal2	-	0.4 pF	Capacitive sensor calibration value (binary weighted).
4	cs_cal1	-	0.2 pF	
3	cs_cal0	-	0.1 pF	
2	cs_cal_end	-	1: Calibration ended	-
1	cs_cal_err	-	1: Calibration error	-
0	RFU	-	-	-



4.5.62 Auxiliary display register

Register space: A Address: 31h Type: R

Table 96. Auxiliary display register

Bit	Name	Default	Function	Comments
7	a_cha	-	0: AM 1: PM	Receiver channel used in ongoing/last reception.
6	efd_o	-	1: External field detected	External field detector output.
5	tx_on	-	1: Transmission is active	Data transmission due to automatic handling of CE mode collision avoidance are not indicated.
4	osc_ok	-	1: Xtal oscillation is stable	Indication that Xtal oscillator is active and its output is stable.
3	rx_on	-	1: Receive decoder is enabled	-
2	rx_act	-	1: Receive decoder is receiving a message	-
1	en_peer	-	1: External field detector is active in Peer detection mode	-
0	en_ac	-	1: External field detector is active in RF collision avoidance mode	-



4.5.63 Overshoot protection configuration register 1

Register space: B Address: 30h Type: RW

Table 97. Overshoot protection configuration register 1

Bit	Name	Default	Function	Comments
7	ov_tx_mode1	0	00: Drive with V _{DD_DR} 01: Drive with V _{DD_AM}	Selects RF drive level to apply when
6	ov_tx_mode0	0	10: Driver stop (at GND / V _{DD_DR}) 11: RFU	ov_patternX is set to 1.
5	ov_pattern13	0	-	-
4	ov_pattern12	0	-	-
3	ov_pattern11	0	-	-
2	ov_pattern10	0	-	-
1	ov_pattern9	0	-	-
0	ov_pattern8	0	-	-

4.5.64 Overshoot protection configuration register 2

Register space: B

Address: 31h

Type: RW

Table 98. Overshoot protection configuration register 2

Bit	Name	Default	Function	Comments
7	ov_pattern7	0	-	-
6	ov_pattern6	0	-	-
5	ov_pattern5	0	-	-
4	ov_pattern4	0	-	-
3	ov_pattern3	0	-	-
2	ov_pattern2	0	-	-
1	ov_pattern1	0	-	-
0	ov_pattern0	0	-	-



4.5.65 Undershoot protection configuration register 1

Register space: B Address: 32h

Type: RW

Table 99. Undershoot protection configuration register 1

Bit	Name	Default	Function	Comments
7	un_tx_mode1	0	00: Drive with V _{DD_DR} 01: Drive with V _{DD_AM}	Selects RF drive level to apply when
6	un_tx_mode0	0	10: Driver stop (at GND / V _{DD_DR}) 11: RFU	un_patternX is set to 1.
5	un_pattern13	0	-	-
4	un_pattern12	0	-	-
3	un_pattern11	0	-	-
2	un_pattern10	0	-	-
1	un_pattern9	0	-	-
0	un_pattern8	0	-	-

4.5.66 Undershoot protection configuration register 2

Register space: B

Address: 33h

Type: RW

Table 100. Undershoot protection configuration register 2

Bit	Name	Default	Function	Comments
7	un_pattern7	0	-	-
6	un_pattern6	0	-	-
5	un_pattern5	0	-	-
4	un_pattern4	0	-	-
3	un_pattern3	0	-	-
2	un_pattern2	0	-	-
1	un_pattern1	0	-	-
0	un_pattern0	0	-	-



4.5.67 Wake-up timer control register

Register space: A Address: 32h Type: RW

Table 101. Wake-up timer control register

Bit	Name	Default	Function	Comments
7	wur	0	0: 100 ms 1: 10 ms	Wake-up timer range
6	wut2	0		
5	wut1	0	Refer to Table 102	Wake-up timer timeout value
4	wut0	0		
3	wto	0	1: IRQ at every timeout	-
2	wam	0	1: At timeout perform amplitude measurement	Generates I_wam interrupt if amplitude difference is larger than ∆am.
1	wph	0	1: At timeout perform phase measurement	Generates I_wph interrupt if phase difference is larger than Δpm .
0	wcap	0	1: At timeout perform capacitance measurement	Generates I_wcap interrupt if capacitance difference is larger than Δ cm.

Table 102. Typical wake-up time

wut2	wut1	wut0	100 ms range (wur = 0)	10 ms range (wur = 1)
0	0	0	100 ms	10 ms
0	0	1	200 ms	20 ms
0	1	0	300 ms	30 ms
0	1	1	400 ms	40 ms
1	0	0	500 ms	50 ms
1	0	1	600 ms	60 ms
1	1	0	700 ms	70 ms
1	1	1	800 ms	80 ms



4.5.68 Amplitude measurement configuration register

Register space: A

Address: 33h

Type: RW

Table 103. Amplitude measurement configuration register

Bit	Name	Default	Function	Comments
7	am_d3	0		
6	am_d2	0	Definition of Δam (difference vs.	
5	am_d1	0	reference that triggers interrupt)	-
4	am_d0	0		
3	am_aam	0	0: Exclude the IRQ measurement 1: Include the IRQ measurement	Includes/excludes the measurement that causes IRQ (having difference > Δ am to reference) in auto-averaging.
2	am_aew1	0	00: 4 01: 8	Weight of last measurement result for
1	am_aew2	0	10: 16 11: 32	auto-averaging.
0	am_ae	0	0: Use Amplitude measurement reference register	Selects reference value for amplitude measurement Wake-up mode.

4.5.69 Amplitude measurement reference register

Register space: A

Address: 34h

Type: RW

Table 104. Amplitude measurement reference register

Bit	Name	Default	Function	Comments
7	am_ref7	0	-	-
6	am_ref6	0	-	-
5	am_ref5	0	-	-
4	am_ref4	0	-	-
3	am_ref3	0	-	-
2	am_ref2	0	-	-
1	am_ref1	0	-	-
0	am_ref0	0	-	-



4.5.70 Amplitude measurement auto-averaging display register

Register space: A

Address: 35h

Type: R

Table 105. Amplitude measurement auto-averaging display register

Bit	Name	Default	Function	Comments
7	amd_aad7	0	-	-
6	amd_aad6	0	-	-
5	amd_aad5	0	-	-
4	amd_aad4	0	-	-
3	amd_aad3	0	-	-
2	amd_aad2	0	-	-
1	amd_aad1	0	-	-
0	amd_aad0	0	-	-

4.5.71 Amplitude measurement display register

Register space: A

Address: 36h

Type: R

Table 106. Amplitude measurement display register

Bit	Name	Default	Function	Comments
7	am_amd7	0	-	-
6	am_amd6	0	-	-
5	am_amd5	0	-	-
4	am_amd4	0	-	-
3	am_amd3	0	-	-
2	am_amd2	0	-	-
1	am_amd1	0	-	-
0	am_amd0	0	-	-



4.5.72 Phase measurement configuration register

Register space: A Address: 37h

Type: RW

Table 107. Phase measurement configuration register

Bit	Name	Default	Function	Comments
7	pm_d3	0		
6	pm_d2	0	Definition of Δpm (difference to	
5	pm_d1	0	reference that triggers interrupt)	-
4	pm_d0	0		
3	pm_aam	0	0: Exclude the IRQ measurement 1: Include the IRQ measurement	Includes/excludes the measurement value that triggered the I_wph interrupt in the auto-averaging.
2	pm_aew1	0	00: 4 01: 8	Weight of last measurement result for
1	pm_aew0	0	10: 16 11: 32	auto-averaging.
0	pm_ae	0	0: Use <i>Phase measurement</i> <i>reference register</i> 1: Use phase measurement auto-averaging as reference	Selects reference value for phase measurement Wake-up mode.

4.5.73 Phase measurement reference register

Register space: A

Address: 38h

Type: RW

Table 108. Phase measurement reference register

Bit	Name	Default	Function	Comments
7	pm_ref7	0	-	-
6	pm_ref6	0	-	-
5	pm_ref5	0	-	-
4	pm_ref4	0	-	-
3	pm_ref3	0	-	-
2	pm_ref2	0	-	-
1	pm_ref1	0	-	-
0	pm_ref0	0	-	-



4.5.74 Phase measurement auto-averaging display register

Register space: A

Address: 39h

Type: R

Table 109. Phase measurement auto-averaging display register

Bit	Name	Default	Function	Comments
7	pm_aad7	0	-	-
6	pm_aad6	0	-	-
5	pm_aad5	0	-	-
4	pm_aad4	0	-	-
3	pm_aad3	0	-	-
2	pm_aad2	0	-	-
1	pm_aad1	0	-	-
0	pm_aad0	0	-	-

4.5.75 Phase measurement display register

Register space: A

Address: 3Ah

Type: R

Table 110. Phase measurement display register

Bit	Name	Default	Function	Comments
7	pm_amd7	0	0	-
6	pm_amd6	0	0	-
5	pm_amd5	0	0	-
4	pm_amd4	0	0	-
3	pm_amd3	0	0	-
2	pm_amd2	0	0	-
1	pm_amd1	0	0	-
0	pm_amd0	0	0	-



4.5.76 Capacitance measurement configuration register

Register space: A

Address: 3Bh

Type: RW

Table 111. Capacitance measurement configuration register

Bit	Name	Default	Function	Comments
7	cm_d3	0		
6	cm_d2	0	Definition of Δcm (difference to	
5	cm_d1	0	reference that triggers interrupt)	-
4	cm_d0	0		
3	cm_aam	0	0: Exclude the IRQ measurement 1: Include the IRQ measurement	Includes/excludes the measurement that causes IRQ (having difference > Δ cm to reference) in auto-averaging.
2	cm_aew1	0	00: 4	
1	cm_aew0	0	01: 8 10: 16 11: 32	Weight of last measurement result for auto-averaging.
0	cm_ae	0	0: Use Capacitance measurement reference register 1: Use capacitance measurement auto-averaging as reference	Selects reference value for capacitance measurement Wake-up mode.

4.5.77 Capacitance measurement reference register

Register space: A

Address: 3Ch

Type: RW

Table 112. Capacitance measurement reference register

Bit	Name	Default	Function	Comments
7	cm_ref7	0	-	-
6	cm_ref6	0	-	-
5	cm_ref5	0	-	-
4	cm_ref4	0	-	-
3	cm_ref3	0	-	-
2	cm_ref2	0	-	-
1	cm_ref1	0	-	-
0	cm_ref0	0	-	-



4.5.78 Capacitance measurement auto-averaging display register

Register space: A

Address: 3Dh

Type: R

Table 113. Capacitance measurement auto-averaging display register

Bit	Name	Default	Function	Comments
7	cm_aad7	0	-	-
6	cm_aad6	0	-	-
5	cm_aad5	0	-	-
4	cm_aad4	0	-	-
3	cm_aad3	0	-	-
2	cm_aad2	0	-	-
1	cm_aad1	0	-	-
0	cm_aad0	0	-	-

4.5.79 Capacitance measurement display register

Register space: A

Address: 3Eh

Type: R

Table 114. Capacitance measurement display register

Bit	Name	Default	Function	Comments
7	cm_amd7	0	-	-
6	cm_amd6	0	-	-
5	cm_amd_	0	-	-
4	cm_amd_	0	-	-
3	cm_amd3	0	-	-
2	cm_amd2	0	-	-
1	cm_amd1	0	-	-
0	cm_amd0	0	-	-



4.5.80 IC identity register

Register space: A Address: 3Fh Type: R

Table 115. IC identity register

Bit	Name	Default	Function	Comments		
7	ic_type4	0				
6	ic_type3	0	C tupo codo			
5	ic_type2	1	IC type code 00101: ST25R3920	5-bit IC type code		
4	ic_type1	0	00101.012010320			
3	ic_type0	1				
2	ic_rev2	0				
1	ic_rev1	1	IC revision code 010: rev 3.1	3-bit IC revision code		
0	ic_rev0	0				



5 Electrical characteristics

5.1 Absolute maximum ratings

Any stress beyond the limits listed in *Table 116* can cause permanent damage to the device. These are stress ratings only.

Functional operation of the device at these or any other conditions beyond those indicated in *Table 116* is not implied. Exposure to absolute maximum rating conditions for extended periods can affect device reliability.

Symbol	Parameter	Min	Мах	Unit
$V_{DD}, V_{DD_TX}^{(1)}$	Positive supply voltage	-0.3	6.0	
$V_{DD}, V_{DD_TX}^{(1)(2)}$	Positive supply voltage when option bit sup3V is set	-0.3	5	
$\Delta_{VDD-VDD_TX}^{(1)}$	Difference between V_{DD} and V_{DD_TX}	-0.3	0.3	
V _{DD_IO} ⁽¹⁾	Peripheral communication supply voltage	-0.3	6	
V _{GND} ⁽¹⁾	Negative supply voltage	-0.3	0.3	V
V _{plO} ⁽¹⁾	Voltage for peripheral IO communication pins (27 to 32)	-0.3	6	
V _{p5V} ⁽¹⁾	Voltage for other pins (9, 11, 13, 14, 15, and 17) in the 5 V domain	-0.3	6	
V _{p3V} ⁽¹⁾	Voltage for other pins (2 to 5, 7, 18, 19, 20 and 22 to 25) in the 3 V domain	-0.3	5	
I _{scr}	Input current (latch-up immunity) according to JESD78	-100	100	mA
I _{VDD_LDO}	Maximum driver current using internal voltage regulator	-	350 ⁽³⁾	
I _{VDD_EXT} ⁽⁴⁾	Peak current supplied from an external source, internal voltage regulator bypassed		500 ⁽⁵⁾	mA
ESD voltage	Electrostatic discharge voltage according to JS-001, human body model	-	2000	V
Pt	Total power dissipation (all supplies and outputs)	-	300	mW
T _{strg}	Storage temperature	-65	150	
T _{body}	Package body temperature according to IPC/JEDEC J-STD-020 ⁽⁶⁾	-	260	°C
T _{Jun}	Junction temperature	-40	125	
-	Humidity non-condensing	5	85	%

Table 116. Absolute maximum ratings

1. Referenced to V_{SS} .

2. Bit sup3V set to 1 in *IO configuration register 2*.

- 3. Provide good thermal management to ensure that junction temperature remains below the specified value.
- 4. VDD_RF is connected to VDD_TX to bypass the internal voltage regulator.
- 5. Peak current with RF driver externally supplied. Provide good thermal management to ensure that junction temperature remains below the specified value.
- Reflow peak soldering temperature (body temperature) is specified according to IPC/JEDEC J-STD-020 "Moisture/Reflow Sensitivity Classification for Non-hermetic Solid State Surface Mount Devices".



5.2 Operating conditions

All defined tolerances for external components in this specification need to be ensured over the whole operation conditions range and also over lifetime.

Symbol	Parameter	Min	Max	Unit
	Positive supply voltage (pins 8 and 10), $T_{amb} = -40$ to 105 °C, rege <3:0> \ge 07h	2.6	5.5	
V _{DD} , V _{DD_TX} ^{(1) (2)}	Positive supply voltage (pins 8 and 10), T _{amb} = -20 to 105 °C	2.4	5.5	V
TX: ***	Positive supply voltage when option bit sup3V is set ⁽³⁾ , T _{amb} = -40 to 105 °C, rege <3:0> \ge 07h	2.6	3.6	v
	Positive supply voltage when option bit sup3V is set ⁽³⁾ , T_{amb} = -20 to 105 °C	2.4	3.6	
$V_{DD_DR}^{(1)}$	Driver positive supply voltage when driver is directly supplied (pin 14) Mandatory condition: V _{DD_DR} ≤ V _{DD} , V _{DD_TX}	2.4	5.5	
$\Delta_{VDD-VDD_TX}^{(1)}$	Difference between V_{DD} and V_{DD_TX}	-0.2	0.2	
V _{DD_IO} ⁽¹⁾	Peripheral communication supply voltage (pin 1)	1.65	5.5	
V _{GND} ⁽¹⁾	Negative supply voltage (pins 6, 12, 16 and 26)	0	0	v
V _{plO} ⁽¹⁾	Voltage for peripheral IO communication pins (27 to 32)	0	5.5	
V _{p5V} ⁽¹⁾	Voltage for other pins (9, 11, 13, 14, 15 and 17) in the 5 V domain	0	5.5	
V _{p3V} ⁽¹⁾	Voltage for other pins (2 to 5, 7, 18 to 20 and 22 to 25) in the 3 V domain	0	3.6	
T _(amb, VFQFPN32) ⁽⁴⁾	Ambient temperature range for VFQFPN32 package	-40	105	°C
V _{RFI_A}	RFI input amplitude ⁽⁵⁾	0.15	3	V_{PP}

Table	117.	Operating	conditions
-------	------	-----------	------------

1. Referenced to V_{SS} .

2. If power supply is lower than 2.6 V, PSSR cannot be improved using internal regulators (minimum regulated voltage is 2.4 V).

3. Bit sup3V set to 1 in *IO configuration register* 2.

4. The device must be mounted on a PCB with sufficient heat dissipation.

5. The minimum RFI input signal definition is meant for NFC active P2P reception and NFC passive target reception. In HF reader mode and NFC transmit mode the recommended signal level is 2.5 V_{PP} .



5.3 DC/AC characteristics for digital inputs and outputs

Туре	Symbol	Parameter	Conditions	Min	Тур	Мах	Unit
	V _{IH}	High level input voltage	-	0.8 * V _{DD_IO}	-	-	V
Inputs ⁽²⁾	V _{IL}	Low level input voltage	-	-	-	0.2 * V _{DD_IO}	v
	I _{LEAK}	Input leakage current	V _{DD_IO} = 5.5 V	-1	-	1	μA
	V _{OH}	High level output voltage	I _{source} = 1 mA V _{DD_IO} = 3.3 to5.5 V, io_drv_IvI=0	0.9 * V _{DD_IO}	-	-	
			I _{source} = 0.5 mA V _{DD_IO} < 3.3 V io_drv_IvI = 1		-	-	V
Output	N/		$\begin{array}{c c c c c c c c c c c c c c c c c c c $	0.1 * V _{DD_IO}			
	V _{OL}	Low level output voltage	I _{source} = 0.5 mA V _{DD_IO} < 3.3 V io_drv_IvI = 1	-	-	0.1 * V _{DD_IO}	
	CL	Capacitive load	-	-	-	50	pF
	R _O	Output resistance	V _{DD_IO} = 3.3 V	-	250	500	Ω
	R _{PD}	Pull-down resistance pin MISO ⁽³⁾	V _{DD_IO} = 3.3 V	-	10	13	kΩ

Table 118. Characteristics of CMOS I/Os⁽¹⁾

1. Tested in production at 25 $^\circ\text{C}$ and 125 $^\circ\text{C},$ evaluated by characterization at -40 $^\circ\text{C}.$

2. Pins BSS, MOSI and SCLK.

3. Use bits miso_pd1 and miso_pd2 in the IO configuration register 2 to control the optional pull down on the MISO pin.



5.4 Electrical characteristics

Symbol	Parameter	Conditions	Min	Тур	Мах	Unit
		T_{Jun} = -40 °C to 25 °C ⁽³⁾	-	0.8	2.5	
I _{PD}	Supply current in Power-down mode	T _{Jun} = 85 °C ⁽³⁾	-	2	20	μA
		T _{Jun} = 125 °C ⁽³⁾	-	12	60	
		T_{Jun} = -40 °C to 25 °C ⁽⁴⁾	-	3.5	7.0	
I _{NFCT}	Supply current in Initial NFC target mode	T _{Jun} = 85 °C ⁽⁴⁾	-	5	20	μA
		T _{Jun} = 125 °C ⁽⁴⁾	-	14	60	
		T_{Jun} = -40 °C to 25 °C ⁽⁵⁾	-	3.0	6.3	
I _{WU}	Supply current in Wake-up mode (logic and RC oscillator)	T _{Jun} = 85 °C ⁽⁵⁾		2.8	20	μA
		T _{Jun} = 125 °C ⁽⁵⁾		15	60	
I _{CS}	Capacitive sensor supply current	(6)	-	1.1	2.0	mA
I _{RD}	Supply current in Ready mode	(7)	-	4.5	7.5	
I _{AL}	Supply current all active	(8)	-	16	23	m۸
I _{AL-AM}	Supply current all active, AM	(9)	-	17	26	mA
I _{AL1}	Supply current all active single RX channel	(10)	-	11	16	
R _{RFO}	RFO1 and RFO2 driver output resistance	I _{RFO} = 10 mA	-	1.7	4	Ω
V _{RFI}	RFI input sensitivity	(11) (12)	-	0.5	-	mV _{rms}
R _{RFI}	RFI input resistance	-	-	12	16	kΩ
V _{POR}	Power on reset voltage	-	1.0	1.45	2.0	
V _{AGDC}	AGDC voltage	(7)	1.4	1.5	1.6	V
V _{REG}	Regulated voltage	(13)	2.65	3.00	3.20	

Table 119. ST25R3920 electrical characteristics (V_{DD} = 3.3 V) ⁽¹⁾⁽²⁾

1. 3.3 V supply mode with V_{DD} = 3.3 V, unless specified otherwise. Regulated voltages are set at 3.0 V, 27.12 MHz Xtal connected to XTO and XTI.

2. Minimum and maximum values tested in production at 25 °C and 125 °C, other temperature values evaluated by characterization.

- 3. Registers 00h to 07h (no clock on MCU_CLK), 01h to 80h (3 V supply mode), other registers in default state.
- 4. Registers 00h to 07h (no clock on MCU_CLK), 01h to 80h (3 V supply mode), 02h to 03h (external field detector enable), 03h to E8h (enable NFC Target mode), other registers in default state.
- Registers 00h to 07h (no clock on MCU_CLK), 01h to 80h (3 V supply mode), 02h to 04h (enable Wake-up mode), 32h to 08h (100 ms timeout, IRQ at every timeout), other registers in default state.
- Registers 00h to 07h (no clock on MCU_CLK), 01h to 80h (3 V supply mode), Test register 02h to 0Eh (tdana<3:0>=0Eh; CS analog test mode 14), other registers in default state.
- Registers 00h to 07h (no clock on MCU_CLK), 01h to C0h (3 V supply mode, disable VDD_D), 02h to 80h (en = 1), 2Ch to D8h (3.0 V regulator), other registers in default state, short VDD_A and VDD_D.
- Registers 00h to 07h (no clock on MCU_CLK), 01h to C0h (3 V supply mode, disable VDD_D), 02h to C8h (enable RX, enable TX), 28h to 7Fh (RFO segments disabled), 2Ch to D8h (3.0 V regulator), other registers in default state, short VDD_A and VDD_D.
- Registers 00h to 07h (no clock on MCU_CLK), 01h to C0h (3 V supply mode, disable VDD_D), 02h to C8h (enable RX, enable TX), 03h to 14h (AM modulation), 28h to 7Fh (RFO segments disabled), 2Ch to D8h (3.0 V regulator), other registers in default state, short VDD_A and VDD_D.



- Registers 00h to 07h (no clock on MCU_CLK), 01h to C0h (3 V supply mode, disable VDD_D), 02h to E8h (enable RX, 1 RX channel, enable TX), 28h to 7Fh (RFO segments disabled), 2Ch to D8h (3.0 V regulator), other registers in default state, short VDD_A and VDD_D.
- 11. f_{SUB} = 848 kHz, AM channel with peak detector input stage selected.
- 12. Specified by design, not tested in production.
- 13. Manual regulator mode, V_{DD} = 3.6 V, regulated voltage set to 3.0 V, measured on pin VDD_RF: register 00h set to 0Fh, register 01h set to 80h (3 V supply mode), register 02h set to E8h (one channel RX, enable TX), 2Ch to D8h (3.0 V regulator), other registers in default state.

Symbol	Parameter	Conditions	Min	Тур	Мах	Unit
		T _{Jun} = -40 to 25 °C $^{(3)}$	-	1	3	
I _{PD}	Supply current in Power-down mode	T _{Jun} = 125 °C ⁽³⁾	-	-	90	
		T _{Jun} = 85 °C	-	2.5	25	
		T_{Jun} = -40 to 25 °C ⁽⁴⁾	-	3.4	8	
INFCT	Supply current in initial NFC target mode	T _{Jun} = 125 °C ⁽⁴⁾	-	35	90	μA
		T _{Jun} = 85 °C	-	5	25	
		T_{Jun} = -40 to 25 °C ⁽⁵⁾	-	3	8	
I _{WU}	Supply current in Wake-up mode (logic and RC oscillator)	T _{Jun} = 125 °C ⁽⁵⁾	-	15	90	
	(T _{Jun} = 85 °C		5	_	
I _{CS}	Capacitive sensor supply current	(6)	-	1.1	2.0	mA
I _{RD}	Supply current in Ready mode	(7)	-	5.6	7.5	
I _{AL}	Supply current all active	(8)	-	15.0	23.0	
I _{AL-AM}	Supply current all active, AM	(9)	-	16.0	26.0	mA
I _{AL1}	Supply current all active single RX channel	(10)	-	11.0	16.0	
R _{RFO}	RFO1 and RFO2 driver output resistance	I _{RFO} = 10 mA ⁽¹¹⁾	-	1.7	4	Ω
R _{RFI}	RFI input resistance	(12)	-	12	16	kΩ
V _{POR}	Power on reset voltage	-	1.00	1.45	2.00	
V _{AGDC}	AGDC voltage	(8)	1.40	1.50	1.60	V
V _{REG}	Regulated voltage	(8)	4.3	5.0	5.3	

Table 120. ST25R3920 electrical characteristi	ics (V_{DD} = 5.5 V) ⁽¹⁾ ⁽²⁾
---	---

1. Minimum and maximum values tested in production at 25 °C and 125 °C, other temperature values evaluated by characterization.

 5.0 V supply mode with V_{DD} = 5.5 V unless specified otherwise. Regulated voltages set to 5.1 V, 27.12 MHz Xtal connected to XTO and XTI.

- 3. Registers 00h to 07h (no clock on MCU_CLK), 01h to 00h (5 V supply mode), other registers in default state.
- Registers 00h to 07h (no clock on MCU_CLK), 01h to 00h (5 V supply mode), 02h to 03h (external field detector enable), 03h to E8h (enable NFC Target mode), other registers in default state.
- Registers 00h to 07h (no clock on MCU_CLK), 01h to 00h (5 V supply mode), 02h to 04h (enable Wake-up mode), 32h to 08h (100 ms timeout, IRQ at every timeout), other registers in default state.
- Registers 00h to 07h (no clock on MCU_CLK), 01h to 00h (5 V supply mode), Test register 02h to 0Eh (tdana<3:0>=0Eh; CS analog test mode 14), other registers in default state.
- Registers 00h to 07h (no clock on MCU_CLK), 01h to 40h (5 V supply mode, disable VDD_D), 02h to 80h (en = 1), 2Ch to F8h (5.1 V regulator), other registers in default state, short VDD_A and VDD_D.



- Registers 00h to 07h (no clock on MCU_CLK), 01h to 40h (5 V supply mode, disable VDD_D), 02h to C8h (enable RX, enable TX), 28h to 7Fh (RFO segments disabled), 2Ch to F8h (5.1 V regulator), other registers in default state, short VDD_A and VDD_D.
- Registers 00h to 07h (no clock on MCU_CLK), 01h to 40h (5 V supply mode, disable VDD_D), 02h to C8h (enable RX, enable TX), 03h to 14h (AM modulation), 28h to 7Fh (RFO segments disabled), 2Ch to F8h (5.1 V regulator), other registers in default state, short VDD_A and VDD_D.
- Registers 00h to 07h (no clock on MCU_CLK), 01h to 40h (5 V supply mode, disable VDD_D), 02h to E8h (enable RX, 1 RX channel, enable TX), 28h to 7Fh (RFO segments disabled), 2Ch to F8h (5.1 V regulator), other registers in default state, short VDD_A and VDD_D.
- 11. Evaluated by characterization, not tested in production.
- 12. f_{SUB} = 848 kHz, AM channel with peak detector input stage selected.

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
		T _{Jun} = -40 to 25 °C $^{(3)}$	-	0.5	2.2	
I _{PD}	Supply current in Power-down mode	T _{Jun} = 85 °C ⁽³⁾	-	1.5	15	
		T _{Jun} = 125 °C ⁽³⁾		7.0	50	
		T_{Jun} = -40 to 25 °C ⁽⁴⁾	-	1.5	5	
I _{NFCT}	Supply current in initial NFC target mode	$T_{Jun} = 85 \ ^{\circ}C \ ^{(4)}$	-	2	15	μA
		T _{Jun} = 125 °C ⁽⁴⁾		8	50	
		T_{Jun} = -40 to 25 °C ⁽⁵⁾	-	1.8	5	
I _{WU}	Supply current in Wake-up mode (logic and RC oscillator)	T _{Jun} = 85 °C ⁽⁵⁾	-	2.7	15	
	(T _{Jun} = 125 °C ⁽⁵⁾		9	50	
I _{CS}	Capacitive sensor supply current	(6)	-	0.7	2.0	mA
I _{RD}	Supply current in Ready mode	(7)	-	3.4	7.5	
I _{AL}	Supply current all active	(8)	-	11	23	
I _{AL-AM}	Supply current all active, AM	(9)	-	12.5	26	mA
I _{AL1}	Supply current all active single RX channel	(10)	-	10	16	
R _{RFO}	RFO1 and RFO2 driver output resistance	I _{RFO} = 10 mA ⁽¹¹⁾	-	1.7	4	Ω
R _{RFI}	RFI input resistance	(11)(12)	-	12	16	kΩ
V _{POR}	Power on reset voltage	-	1.00	1.45	2.00	
V _{AGDC}	AGDC voltage	(8)	1.40	1.50	1.60	V
V _{REG}	Regulated voltage	(8)	2.20	2.40	2.45	

Table 121. ST25R3920 electrical characteristics	$s (V_{DD} = 2.4 \text{ V})^{(1) (2)}$
---	--

1. Minimum and maximum values tested in production at 25 °C and 125 °C, other temperature values evaluated by characterization.

 3.3 V supply mode with V_{DD} = 2.4 V unless specified otherwise. Regulated voltages set to 2.4 V, 27.12 MHz Xtal connected to XTO and XTI.

3. Registers 00h to 07h (no clock on MCU_CLK), 01h to 80h (3 V supply mode), other registers in default state.

- Registers 00h to 07h (no clock on MCU_CLK), 01h to 80h (3 V supply mode), 02h to 03h (external field detector enable), 03h to E8h (enable NFC Target mode), other registers in default state.
- Registers 00h to 07h (no clock on MCU_CLK), 01h to 80h (3 V supply mode), 02h to 04h (enable Wake-up mode), 32h to 08h (100 ms timeout, IRQ at every timeout), other registers in default state.



- Registers 00h to 07h (no clock on MCU_CLK), 01h to 80h (3 V supply mode), Test register 02h to 0Eh (tdana<3:0>=0Eh; CS analog test mode 14), other registers in default state.
- Registers 00h to 07h (no clock on MCU_CLK), 01h to C0h (3 V supply mode, disable VDD_D), 02h to 80h (en = 1), 2Ch to A8h (2.4 V regulator), other registers in default state, short VDD_A and VDD_D.
- Registers 00h to 07h (no clock on MCU_CLK), 01h to C0h (3 V supply mode, disable VDD_D), 02h to C8h (enable RX, enable TX), 28h to 7Fh (RFO segments disabled), 2Ch to A8h (2.4 V regulator), other registers in default state, short VDD_A and VDD_D.
- Registers 00h to 07h (no clock on MCU_CLK), 01h to C0h (3 V supply mode, disable VDD_D), 02h to C8h (enable RX, enable TX), 03h to 14h (AM modulation), 28h to 7Fh (RFO segments disabled), 2Ch to A8h (2.4 V regulator), other registers in default state, short VDD_A and VDD_D.
- Registers 00h to 07h (no clock on MCU_CLK), 01h to C0h (3 V supply mode, disable VDD_D), 02h to E8h (enable RX, 1 RX channel, enable TX), 28h to 7Fh (RFO segments disabled), 2Ch to A8h (2.4 V regulator), other registers in default state, short VDD_A and VDD_D.
- 11. Evaluated by characterization, not tested in production.
- 12. f_{SUB} = 848 kHz, AM channel with peak detector input stage selected.



5.5 SPI interface characteristics

Operation	Symbol	Parameter	Conditions	Min	Тур	Max	Unit
	T _{SCLK}	SCLK period	$T_{SCLK} = T_{SCLKL} + T_{SCLKH}$	-	200	-	
	T _{SCLKL}	SCLK low	-	95	-	-	
	T _{SCLKH}	SCLK high	-	95	-	-	
Conoral	T _{SSH}	SPI reset (BSS high)	-	100	-	-	
	T _{NCSL}	BSS falling to SCLK rising	First SCLK pulse	25	-	-	
	T _{NCSH}	SCLK falling to BSS rising	Last SCLK pulse	25	-	-	
	T _{DIS}	Data in setup time	-	10	-	-	ns
	T _{DIH}	Data in hold time	-	10	-	-	
	T District		C _{load} ≤ 50 pF, V _{DD_IO} = 1.65 to 3.0 V	-	80	95	
Read	T _{DOD}	Data out delay	C _{load} ≤ 50 pF, V _{DD_IO} = 3.0 to 5.5 V	-	-	70	
	T _{DOHZ}	Data out to high impedance delay	$C_{load} \le 50 \text{ pF}$	-	20	-	

Table 122. SPI characteristics (5 MHz) ⁽¹⁾

1. Evaluated by characterization, not tested in production.

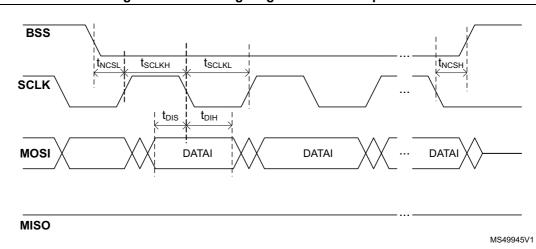


Figure 28. SPI timing diagram - General operation



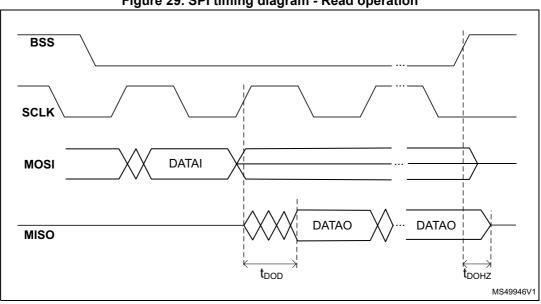


Figure 29. SPI timing diagram - Read operation



5.6 I2C interface characteristics

Transition from 100 kHz / 400 kHz / 1 MHz mode to 3.4 MHz mode (High speed mode) is done via Master code 00001XXX, as described in the I2C specification.

Symbol	Parameter		Min Max	
C _{BUS}	Load capacitance	100		pF
-	SCL input rise/fall time, SDA input fall time	- 50		ns

 Table 123. AC measurement conditions

Mode	Rate	Setting
S	100 kHz	i2c_thd = 00b, io_drv_lvl = 1b
F	400 kHz	i2c_thd = 01b, io_drvl_lvl = 1b
F+	1000 kHz	i2c_thd = 11b, lo_drv_lvl = 1b
HS	3400 kHz	i2c_thd = 11b, io_drv_lvl = 1b

Table 124. AC measurement conditions - I2C configuration

Table 125. Input parameters⁽¹⁾

Symbol	Parameter	Conditions	Min	Max	Unit
C	Input capacitance (SDA)	-	-	15	ъĘ
C _{IN}	Input capacitance (SCL)	-	-	15	pF

1. Evaluated by characterization, not tested in production.

Table 126. DC characteristics⁽¹⁾

Symbol	Parameter	Conditions (in addition to those in <i>Table 123</i> and <i>Table 124</i>)	Min	Мах	Unit
ILI	Input leakage current (SCL, SDA)	V _{IN} = V _{SS} or V _{CC} , device in Standby mode	-	± 10	μA
I _{LO}	Output leakage current	SDA in Hi-Z, external voltage applied on SDA: V _{SS} or V _{CC}	-	± 10	μΛ
V _{IL}	Input low voltage (SCL, SDA)	-	-0.4	0.2 V _{DD_IO}	
V _{IH}	Input high voltage (SCL, SDA)	-	0.8 V _{DD_IO}	V _{DD_IO} + 0.4	
		V _{DD_IO} = 1.65 V, I _{OL} = 2.5 mA	-	0.1 V _{DD_IO}	V
V	Output low voltage	V _{DD_IO} = 2.4 V, I _{OL} = 3.0 mA	-	0.1 V _{DD_IO}	
V _{OL}	Output low voltage	V _{DD_IO} = 3.3 V, I _{OL} = 8 mA	-	0.1 V _{DD_IO}	
		V _{DD_IO} = 5.5 V, I _{OL} = 8 mA	-	0.1 V _{DD_IO}	

1. Evaluated by characterization, not tested in production.



Symbol	Alt.	Parameter	Min	Max	Unit
f _C	f _{SCL}	Clock frequency	-	100	kHz
t _{CHCL}	t _{HIGH}	Clock pulse width high	4000	-	
t _{CLCH}	t _{LOW}	Clock pulse width low	4700	-	
t _{QL1QL2}	t _F	SDA (out) fall time	-	300	
t _{DXCH}	t _{SU:DAT}	Data in set up time	250	-	
t _{CLDX} X	t _{HD:DAT}	Data in hold time	5000	-	
t _{CLQX}	t _{DH}	Data out hold time	50	-	
t _{CLQV}	t _{AA}	Clock low to next data valid (access time)	-	3450	ns
t _{CHDL}	t _{SU:STA}	Start condition setup time	4700	-	
t _{DLCL}	t _{HD:STA}	Start condition hold time	4000	-	
t _{CHDH}	t _{SU:STO}	Stop condition set up time	4000	-	
t _{DHDL}	t _{BUF}	Time between Stop condition and next Start condition	4700	-	
t _{NS} ⁽²⁾	-	Pulse width ignored (input filter on SCL and SDA), single glitch	-	40	

Table 127. 100 kHz AC characteristics⁽¹⁾

1. Conditions in addition to those specified in *Table 123* and *Table 124*.

2. Evaluated by characterization, not tested in production.

Symbol	Alt.	Parameter	Min	Мах	Unit
f _C	f _{SCL}	Clock frequency	-	400	kHz
t _{CHCL}	t _{HIGH}	Clock pulse width high	600	-	
t _{CLCH}	t _{LOW}	Clock pulse width low	1300	-	
t _{QL1QL2}	t _F	SDA (out) fall time	-	300	
t _{DXCH}	t _{SU:DAT}	Data in set up time	100	-	
t _{CLDX} X	t _{HD:DAT}	Data in hold time	0	-	
t _{CLQX}	t _{DH}	Data out hold time	50	-	
t _{CLQV}	t _{AA}	Clock low to next data valid (access time)	-	900	ns
t _{CHDL}	t _{SU:STA}	Start condition setup time	600	-	
t _{DLCL}	t _{HD:STA}	Start condition hold time	600	-	
t _{CHDH}	t _{SU:STO}	Stop condition set up time	600	-	
t _{DHDL}	t _{BUF}	Time between Stop condition and next Start condition	1300	-	
t _{NS}	-	Pulse width ignored (input filter on SCL and SDA), single glitch	-	40	

1. Conditions in addition to those specified in *Table 123* and *Table 124*.

2. Evaluated by characterization, not tested in production.



Symbol	Alt.	Parameter	Min	Max	Unit
f _C	f _{SCL}	Clock frequency	-	1	MHz
t _{CHCL}	t _{HIGH}	Clock pulse width high	260	-	
t _{CLCH}	t _{LOW}	Clock pulse width low	500	-	
t _{QL1QL2}	t _F	SDA (out) fall time	-	120	
t _{DXCH}	t _{SU:DAT}	Data in set up time	50	-	
t _{CLDX} X	t _{HD:DAT}	Data in hold time	0	-	
t _{CLQX}	t _{DH}	Data out hold time	50	-	
t _{CLQV}	t _{AA}	Clock low to next data valid (access time)	-	450	ns
t _{CHDL}	t _{SU:STA}	Start condition setup time	250	-	
t _{DLCL}	t _{HD:STA}	Start condition hold time	250	-	
t _{CHDH}	t _{SU:STO}	Stop condition set up time	250	-	
t _{DHDL}	t _{BUF}	Time between Stop condition and next Start condition	500	-	
t _{NS}	-	Pulse width ignored (input filter on SCL and SDA), single glitch	-	40	

Table 129.	1 MHz AC characteristics	(1)(2)
------------	--------------------------	--------

1. Conditions in addition to those specified in *Table 123* and *Table 124*.

2. Evaluated by characterization, not tested in production.

Table 130. 3.4 MHz AC characteristics	Table 130	. 3.4 MHz AC characteristics ⁽¹⁾⁽²⁾	(3)
---------------------------------------	-----------	--	-----

Symbol	Alt.	Parameter		Max	Unit
f _C	f _{SCL}	Clock frequency		3.4	MHz
t _{CHCL}	t _{HIGH}	Clock pulse width high	80	-	
t _{CLCH}	t _{LOW}	Clock pulse width low	160	-	
t _{QL1QL2}	t _F	SDA (out) fall time (10-100 pF)	-	41	
t _{DXCH}	t _{SU:DAT}	Data in set up time	25	-	
t _{CLDX} X	t _{HD:DAT}	Data in hold time	0	-	
t _{CLQX}	t _{DH}	Data out hold time	20	-	ns
t _{CLQV}	t _{AA}	Clock low to next data valid	-	150	
t _{CHDL}	t _{SU:STA}	Start condition setup time	160	-	
t _{DLCL}	t _{HD:STA}	Start condition hold time	160	-	
t _{CHDH}	t _{SU:STO}	Stop condition set up time	160	-	
t _{NS}	-	Pulse width ignored (input filter on SCL and SDA), single glitch		10	

1. Conditions in addition to those specified in *Table 123* and *Table 124*.

2. Evaluated by characterization, not tested in production.

3. $V_{DD_{-}IO}$ supply must not exceed V_{DD} .



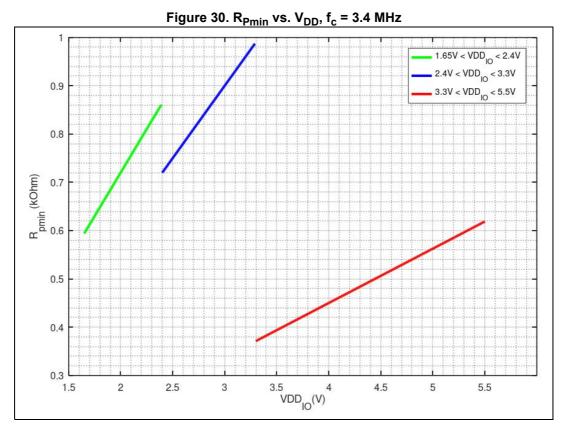
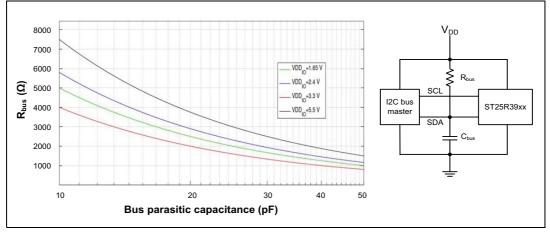
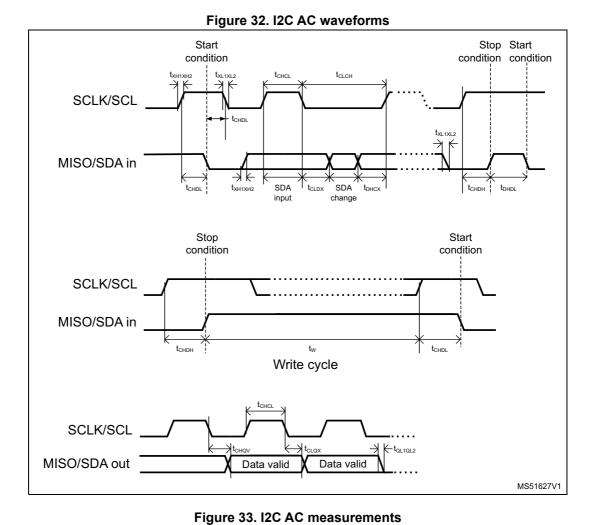


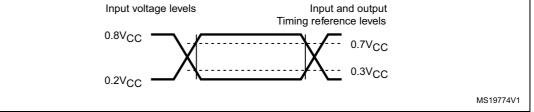
Figure 31. Maximum R_{bus} value vs. bus parasitic capacitance, $f_c = 3.4$ MHz







.





6 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at *www.st.com*.

ECOPACK is an ST trademark.

6.1 VFQFPN32 package information

VFQFPN32 is a 32-pin, 5x5 mm, 0.5 mm pitch, very thin fine pitch quad flat no lead package.

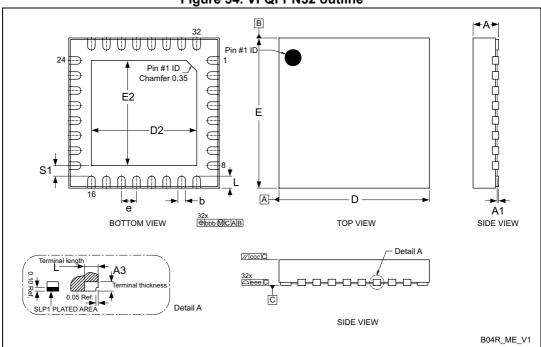


Figure 34. VFQFPN32 outline

- 1. Drawing is not to scale.
- 2. Coplanarity applies to the exposed pad as well as to the terminal.

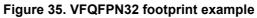
Table 131. VFQFPN32 mechanical data

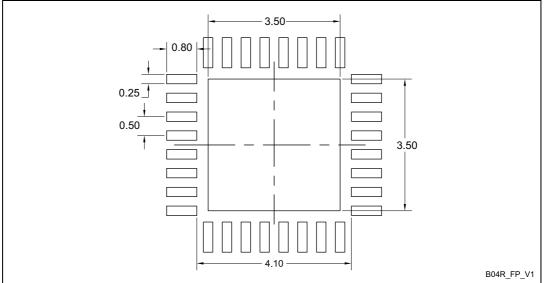
Symbol	millimeters			inches ⁽¹⁾		
Symbol	Min	Тур	Мах	Min	Тур	Max
A	0.800	0.900	1.000	0.0315	0.0354	0.0394
A1	0	-	0.050	0	-	0.0020
A3	0.200		0.0079			
L	0.300	0.400	0.500	0.0118	0.0157	0.0197
b	0.180	0.250	0.300	0.0071	0.0098	0.0118



Symbol	millimeters			inches ⁽¹⁾		
	Min	Тур	Мах	Min	Тур	Max
D	5.000 0.19			0.1969		
D2	3.400	3.500	3.600	0.1339	0.1378	0.1417
E		5.000			0.1969	
E2	3.400	3.500	3.600	0.1339	0.1378	0.1417
е		0.500			0.0197	
S1		0.350			0.0138	
bbb	-	0.100	-	-	0.0039	-
CCC	-	0.100	-	-	0.0039	-
eee	-	0.080	-	-	0.0031	-

1. Values in inches are converted from mm and rounded to four decimal digits.

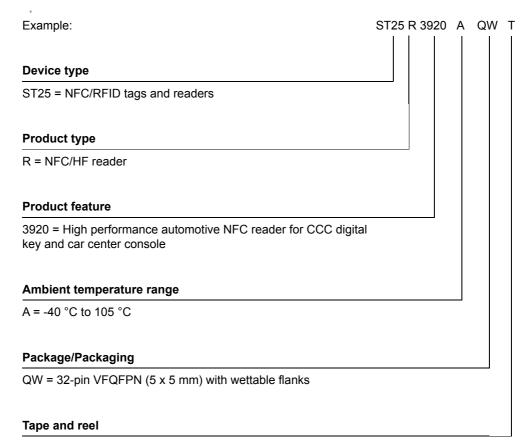




1. Dimensions are expressed in millimeters.



7 Ordering information



T = 4000 pcs/reel

Note: Parts marked as "ES", "E" or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not approved for use in production. ST is not responsible for any consequences resulting from such use. In no event will ST be liable for the customer using any of these engineering samples in production. ST's Quality department must be contacted prior to any decision to use these engineering samples to run a qualification activity.

For a list of available options (speed, package, etc.) or for further information on any aspect of this device contact your nearest ST sales office.



8 Revision history

Date	Revision	Changes			
17-Apr-2020	1	Initial release.			
29-Apr-2020	2	Updated Features and Section 2: Description. Updated Table 79: Passive target modulated and unmodulated state driver output resistance, Table 83: Resistive AM modulated state driver output resistance and Table 117: Operating conditions. Added footnote 2 to Table 34: Auxiliary definition register.			
20-May-2020	3	Updated footnote 3 of Table 130: 3.4 MHz AC characteristics.			
28-May-2020	4	Updated Section 2.2.13: RX decoding. Updated Table 4: First and third zero setting and Table 25: ISO14443A and NFC 106kb/s settings register. Added footnote 1 to Table 118: Characteristics of CMOS I/Os. Updated Figure 5: Receiver block diagram and Figure 31: Maximum Rbus value vs. bus parasitic capacitance, fc = 3.4 MHz.			
27-Apr-2021	5	Updated Section 2: Description . Updated Table 11: List of direct commands. Updated wording of table footnotes in Section 5: Electrical characteristics. Minor text edits across the whole document.			
09-Aug-2021	6	Updated Section 4.4.17: Test access. Updated Figure 1: Minimum system configuration - Single sided antenna driving and Figure 2: Minimum system configuration - Differential antenna driving. Updated Table 1: ST25R3920 - VFQFPN32 pin assignment, Table 10: I2C interface and interrupt signal lines, Table 116: Absolute maximum ratings, Table 117: Operating conditions, footnote 1 of Table 118: Characteristics of CMOS I/Os and footnote 1 of Table 121: ST25R3920 electrical characteristics (VDD = 2.4 V). Added footnotes to tables 22, 76, 79, 83, 119, 120 and 121.			
11-Apr-2022	7	Added note in Section 4.4.5: NFC field ON commands. Updated Section 4.5: Registers. Updated Table 14: Test access register - Signal selection of CSI and CSO pins, Table 19: Operation control register, Table 31: Stream mod definition register, and Table 61: Timer and NFC interrupt register. Added footnotes to Table 20: Mode definition register, Table 81: Extending the detector activation threshold register, and to Table 84: External field detector deactivation threshold register.			
03-May-2022	8	Updated <i>Table 69: Number of transmitted bytes register 2.</i> Minor text edits across the whole document.			

Table 132	Document	revision	history
-----------	----------	----------	---------



Date	Revision	Changes		
07-Nov-2022	9	Updated Figure 1: Minimum system configuration - Single sided antenna driving, Figure 2: Minimum system configuration - Differential antenna driving, and Figure 4: ST25R3920 pinout (top view). Updated Table 1: ST25R3920 - VFQFPN32 pin assignment and Table 8: Serial data interface (4-wire interface) signal lines. Minor text edits across the whole document.		
06-Jun-2023	10	Updated <i>Auto-averaging</i> . Minor text edits across the whole document.		

Table 132. Document revision history (continued)



IMPORTANT NOTICE – READ CAREFULLY

STMicroelectronics NV and its subsidiaries ("ST") reserve the right to make changes, corrections, enhancements, modifications, and improvements to ST products and/or to this document at any time without notice. Purchasers should obtain the latest relevant information on ST products before placing orders. ST products are sold pursuant to ST's terms and conditions of sale in place at the time of order acknowledgment.

Purchasers are solely responsible for the choice, selection, and use of ST products and ST assumes no liability for application assistance or the design of purchasers' products.

No license, express or implied, to any intellectual property right is granted by ST herein.

Resale of ST products with provisions different from the information set forth herein shall void any warranty granted by ST for such product.

ST and the ST logo are trademarks of ST. For additional information about ST trademarks, refer to www.st.com/trademarks. All other product or service names are the property of their respective owners.

Information in this document supersedes and replaces information previously supplied in any prior versions of this document.

© 2023 STMicroelectronics – All rights reserved

DS13261 Rev 10

