Elektronische Bauelemente

SSPR60N03

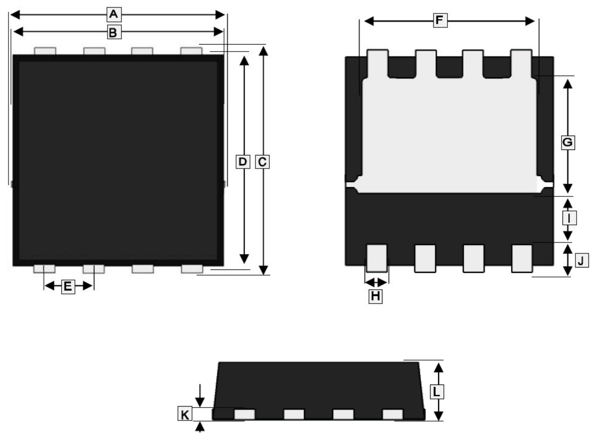
60A , 30V , $R_{DS(ON)}$ 6 mΩ
N-Channel Enhancement Mode Power MOSFET

RoHS Compliant Product
A suffix of "-C" specifies halogen & lead-free

DESCRIPTION

The SSPR60N03 provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness. The SPR-8PP package is universally preferred for all commercial-industrial surface mount applications and suited for low voltage applications such as DC/DC converters.

SPR-8PP

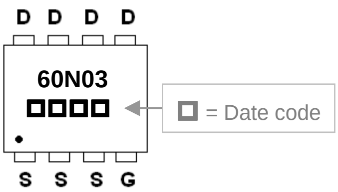


REF.	Millimeter Min.	Millimeter Max.	REF.	Millimeter Min.	Millimeter Max.
A	3.25	3.40	G	1.35	1.55
B	3.05	3.25	H	0.24	0.35
C	3.20	3.40	I	1.13 REF.	
D	3.00	3.20	J	0.30	0.50
E	0.65 BSC.		K	0.10	0.20
F	2.40	2.60	L	0.70	0.90

FEATURES

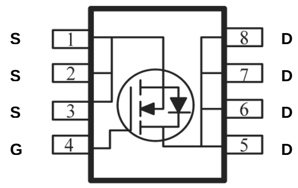
- Lower Gate Charge
- Simple Drive Requirement
- Fast Switching Characteristic

MARKING



PACKAGE INFORMATION

Package	MPQ	Leader Size
SPR-8PP	3K	13 inch



ABSOLUTE MAXIMUM RATINGS (T_A=25℃ unless otherwise specified)

Parameter		Symbol	Rating	Unit
Drain-Source Voltage		V_{DS}	30	V
Gate-Source Voltage		V_{GS}	±20	V
Continuous Drain Current [1]@V_{GS}=10V	T_C=25℃	I_D	60	A
	T_C=100℃		38	
Pulsed Drain Current [2]		I_{DM}	180	A
Single Pulse Avalanche Energy [3]		EAS	252	mJ
Avalanche Current		I_{AS}	48	A
Power Dissipation [4]	T_C=25℃	P_D	37	W
Operating Junction & Storage Temperature		T_J, T_{STG}	-55~150	℃
Thermal Resistance Rating				
Thermal Resistance Junction-Ambient[1](Max).		$R_{\theta JA}$	75	℃ / W
Thermal Resistance Junction-Case[1](Max).		$R_{\theta JC}$	3.38	℃ / W

ELECTRICAL CHARACTERISTICS (T_J = 25℃ unless otherwise specified)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Teat Conditions
Static						
Drain-Source Breakdown Voltage	BV_{DSS}	30	-	-	V	V_{GS}=0, I_D= 250uA
Gate-Threshold Voltage	$V_{GS(th)}$	1	-	2.5	V	V_{DS}=V_{GS}, I_D=250uA
Gate-Source Leakage Current	I_{GSS}	-	-	±100	nA	V_{GS}= ±20V
Drain-Source Leakage Current	I_{DSS}	-	-	1	uA	V_{DS}=24V, V_{GS}=0, T_J=25℃
		-	-	5		V_{DS}=24V, V_{GS}=0, T_J=55℃
Static Drain-Source On-Resistance [2]	$R_{DS(ON)}$	-	-	6	mΩ	V_{GS}=10V, I_D=30A
		-	-	8		V_{GS}=4.5V, I_D=15A
Gate Resistance	R_g	-	1.6	2.8	Ω	f =1.0MHz
Total Gate Charge(10V)	Q_g	-	20	-	nC	I_D=15A V_{DS}=15V V_{GS}=4.5V
Gate-Source Charge	Q_{gs}	-	7.6	-		
Gate-Drain Change	Q_{gd}	-	7.2	-		
Turn-on Delay Time [2]	$T_{d(on)}$	-	7.8	-	nS	V_{DD}=15V I_D=15A V_{GS}=10V R_G=3.3Ω
Rise Time	T_r	-	15	-		
Turn-off Delay Time	$T_{d(off)}$	-	37.3	-		
Fall Time	T_f	-	10.6	-		
Input Capacitance	C_{iss}	-	2295	-	pF	V_{GS} =0 V_{DS}=15V f =1.0MHz
Output Capacitance	C_{oss}	-	267	-		
Reverse Transfer Capacitance	C_{rss}	-	210	-		
Guaranteed Avalanche Characteristics						
Single Pulse Avalanche Energy [3]	EAS	63	-	-	mJ	V_D=25V, L=0.1mH, I_{AS}=24A
Source-Drain Diode						
Diode Forward Voltage [2]	V_{SD}	-	-	1	V	I_S=1A, V_{GS}=0, T_J=25℃
Continuous Source Current [1,4]	I_S	-	-	60	A	V_D=V_G=0, Force Current
Pulsed Source Current [2,4]	I_{SM}	-	-	180	A	
Reverse Recovery Time	T_{rr}	-	14	-	nS	I_F=30A, dI/dt=100A/μS, T_J=25℃
Reverse Recovery Charge	Q_{rr}	-	5	-	nC	

Note:
1. The data tested by surface mounted on a 1 inch2 FR-4 board with 2OZ copper , ≦10sec , 125℃/W at steady state
2. The data tested by pulsed , pulse width ≦ 300us , duty cycle ≦ 2%
3. The EAS data shows Max. rating . The test condition is V_{DD}=25V,V_{GS}=10V,L=0.1mH,I_{AS}=48A
4. The power dissipation is limited by 150℃ juncti on temperature
5. The Min. value is 100% EAS tested guarantee.
6. The data is theoretically the same as ID and IDM , in real applications , should be limited by total power dissipation.

CHARACTERISTIC CURVES

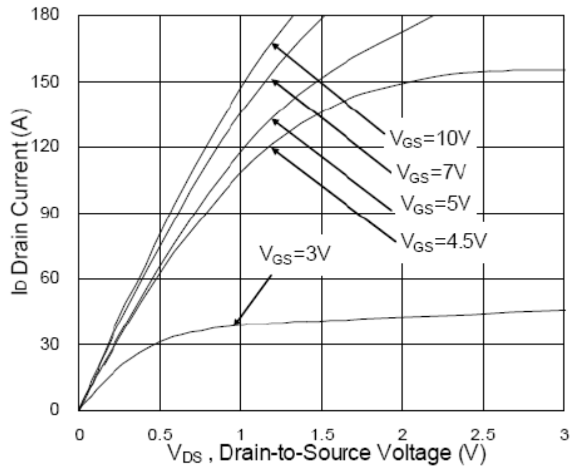


Fig.1 Typical Output Characteristics

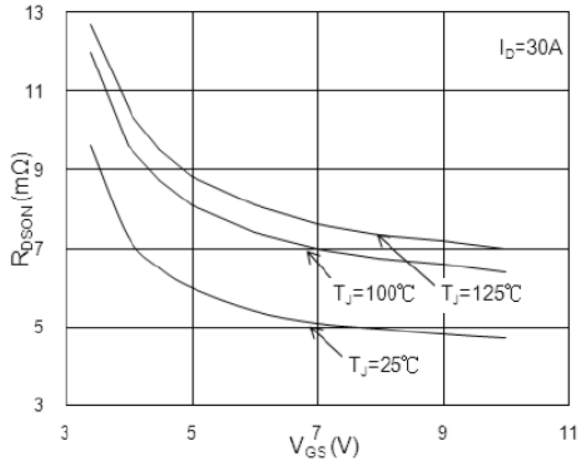


Fig.2 On-Resistance vs. G-S Voltage

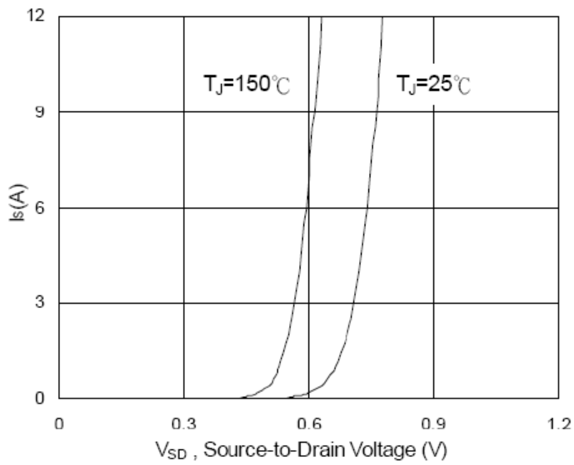


Fig.3 Forward Characteristics of Reverse

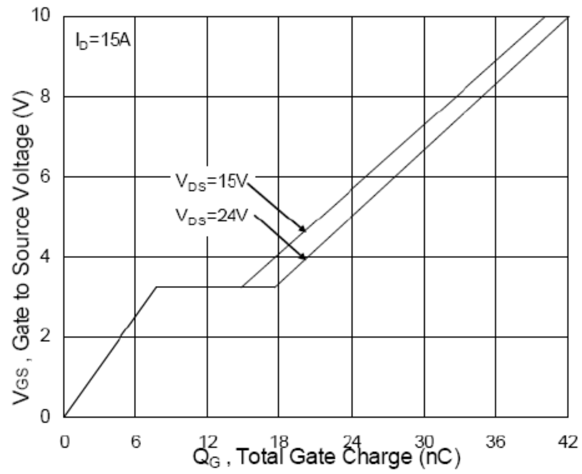


Fig.4 Gate-Charge Characteristics

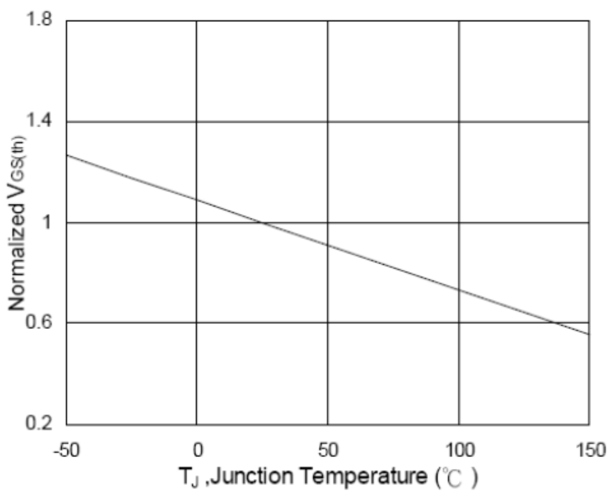


Fig.5 Normalized $V_{GS(th)}$ vs. T_J

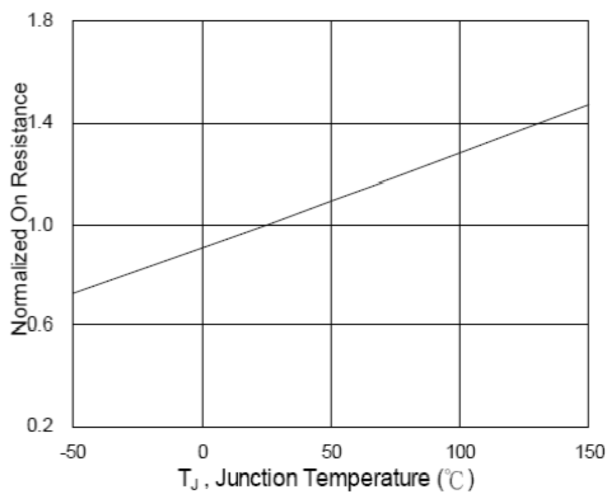


Fig.6 Normalized R_{DSON} vs. T_J

Elektronische Bauelemente

SSPR60N03

60A , 30V , $R_{DS(ON)}$ 6 mΩ

N-Channel Enhancement Mode Power MOSFET

CHARACTERISTIC CURVES

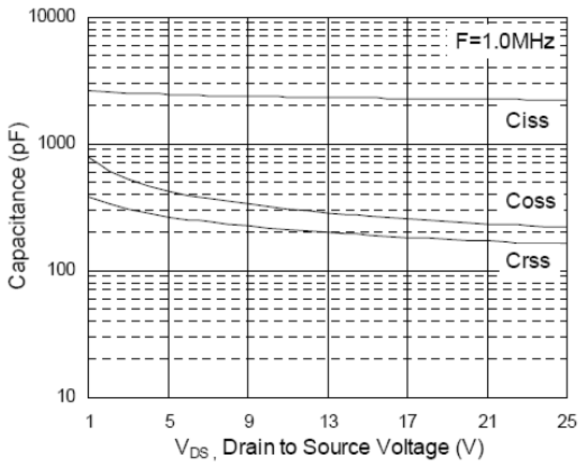


Fig.7 Capacitance

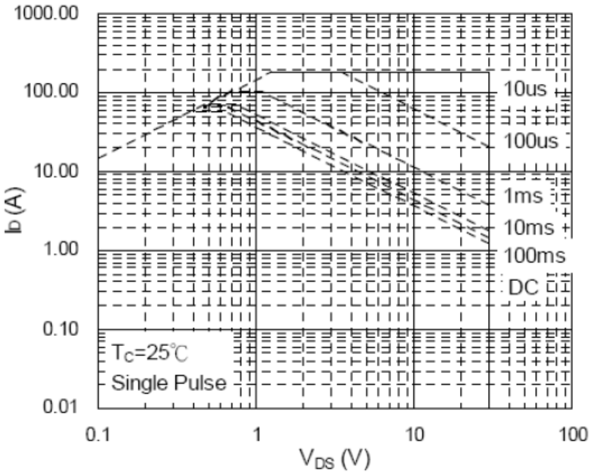


Fig.8 Safe Operating Area

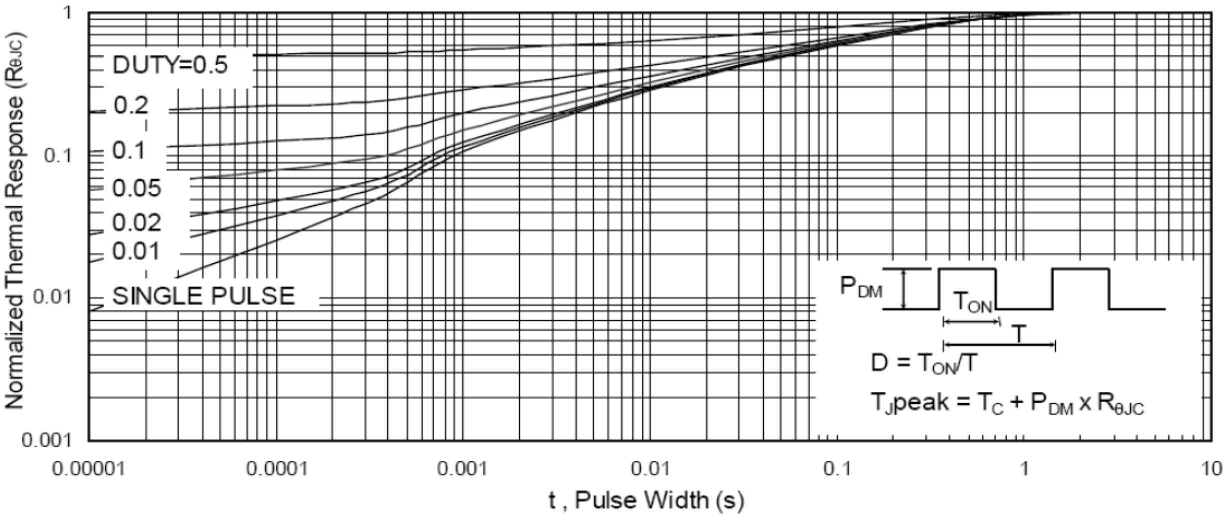


Fig.9 Normalized Maximum Transient Thermal Impedance

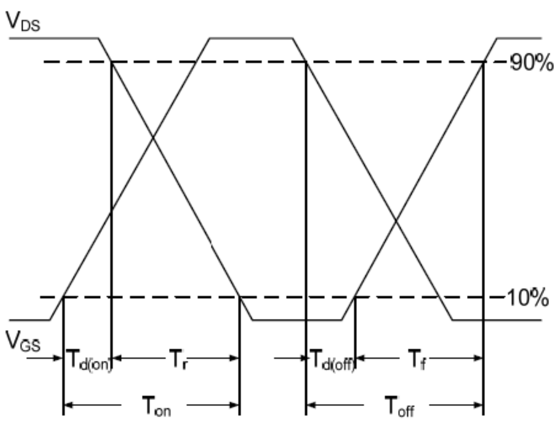


Fig.10 Switching Time Waveform

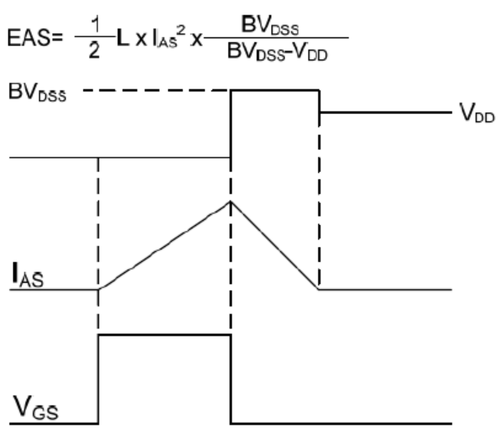


Fig.11 Unclamped Inductive Switching Wave