

SRM20100LC_{70/85/10}

CMOS 1M-BIT STATIC RAM

- Low Supply Current
- Access Time 70ns/85ns/100ns
- 131,072 Words × 8-Bit Asynchronous

DESCRIPTION

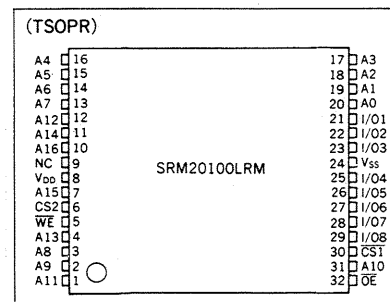
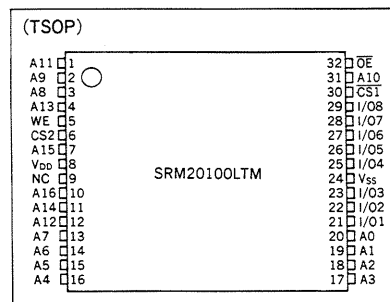
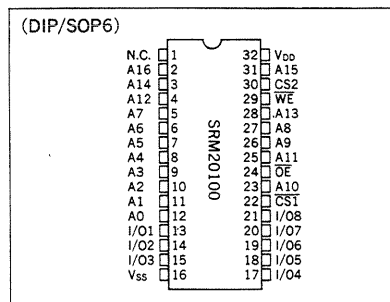
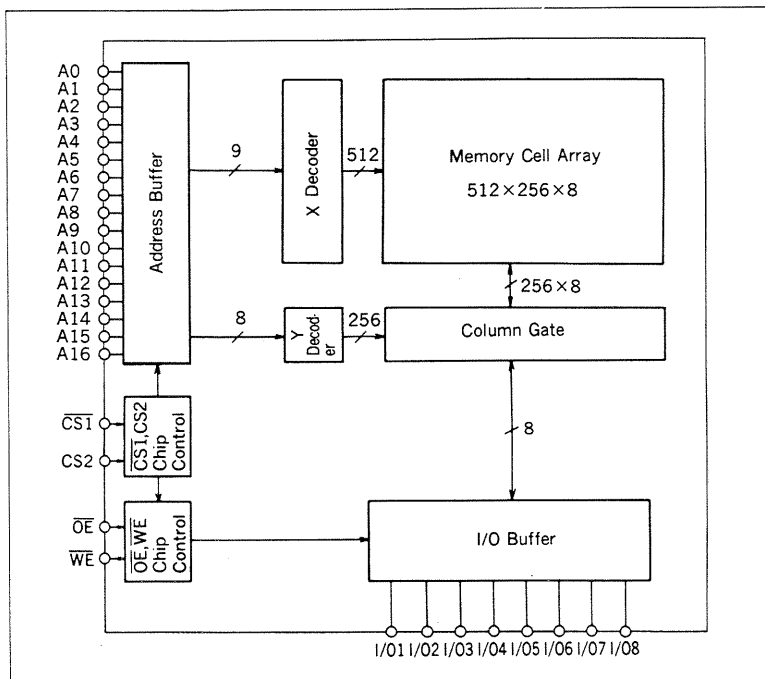
The SRM20100LC_{70/85/10} is an 131,072 words × 8-bit asynchronous, static, random access memory on a monolithic CMOS chip. Its very low standby power requirement makes it ideal for applications requiring non-volatile storage with back-up batteries. The asynchronous and static nature of the memory requires no external clock or refreshing circuit. Both the input and output ports are TTL compatible and the 3-state output allows easy expansion of memory capacity.

FEATURES

- Fast Access time..... SRM20100LC₇₀ 70ns (Max)*
SRM20100LC₈₅ 85ns (Max)
SRM20100LC₁₀ 100ns (Max)
- Low supply current..... standby : 2μA (Typ)
operation: 15mA/MHz (Typ)
- Completely static..... No clock required
- Single power supply..... 5V ± 10%
- TTL compatible inputs and outputs
- 3-state output with wired-OR capability
- Non-volatile storage with back-up batteries
- Package..... SRM20100LC_{70/85/10} DIP-32pin (plastic)
SRM20100LM_{70/85/10} SOP6-32pin (plastic)
SRM20100LTM_{70/85/10} TSOP-32pin (plastic)*
SRM20100LRM_{70/85/10} TSOPR-32pin (plastic)*

* : Under development

BLOCK DIAGRAM



PIN DESCRIPTION

A0 to A16	Address Input
WE	Write Enable
OE	Output Enable
CS1, CS2	Chip Select
I/O1 to I/O8	Data I/O
VDD	Power Supply(+5V)
VSS	Power Supply(0V)
NC	No connection

■ ABSOLUTE MAXIMUM RATINGS

(V_{SS}=0V)

Parameter	Symbol	Ratings	Unit
Supply voltage	V _{DD}	-0.5 to 7.0	V
Input voltage*	V _I	-0.5 to 7.0	V
Input/Output voltage*	V _{I/O}	-0.5 to V _{DD} + 0.3	V
Power dissipation	P _D	1.0	W
Operating temperature	T _{opr}	0 to 70	°C
Storage temperature	T _{stg}	-65 to 150	°C
Soldering temperature and time	T _{sol}	260°C, 10s (at lead)	—

* V_I, V_{I/O} (Min) = -3.0V (Pulse width is 50ns)

■ DC RECOMMENDED OPERATING CONDITIONS

(V_{SS}=0V, Ta=0 to 70°C)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Supply voltage	V _{DD}	—	4.5	5.0	5.5	V
	V _{SS}	—	0	0	0	V
Input voltage	V _{IH}	—	2.2	3.5	V _{DD} + 0.3	V
	V _{IL}	—	-0.3*	0	0.8	V

* If pulse width is less than 50ns, it is -3.0V

■ ELECTRICAL CHARACTERISTICS

● DC Electrical Characteristics

(V_{DD}=5V±10%, V_{SS}=0V, Ta=0 to 70°C)

Parameter	Symbol	Conditions	SRM20100LC70			SRM20100LC85			SRM20100LC10			Unit
			Min	Typ*	Max	Min	Typ*	Max	Min	Typ*	Max	
Input leakage	I _{LI}	V _I =0 to V _{DD}	-1	—	1	-1	—	1	-1	—	1	μA
Standby supply current	I _{DDs}	CS1=V _{IH} or CS2=V _{IL}	—	1.0	3.0	—	1.0	3.0	—	1.0	3.0	mA
	I _{DDs1}	CS1=CS2≥V _{DD} -0.2V or CS2≤0.2V	—	2	100	—	2	100	—	2	100	μA
Average operating current	I _{DDA}	V _I =V _{IL} , V _{IH} I _{I/O} =0mA t _{cyc} =Min	—	45	70	—	45	70	—	45	70	mA
Operating supply current	I _{DDO}	V _I =V _{IL} , V _{IH} I _{I/O} =0mA	—	15	35	—	15	35	—	15	35	mA
Output leakage	I _{LO}	CS1=V _{IH} or CS2=V _{IL} or WE=V _{IL} or OE=V _{IH} V _{I/O} =0 to V _{DD}	-1	—	1	-1	—	1	-1	—	1	μA
High level output voltage	V _{OH}	I _{OH} =-1.0mA	2.4	—	—	2.4	—	—	2.4	—	—	V
Low level output voltage	V _{OL}	I _{OL} =2.1mA	—	—	0.4	—	—	0.4	—	—	0.4	V

* Typical values are measured at Ta=25°C and V_{DD}=5.0V

● Terminal Capacitance

(f=1MHz, Ta=25°C)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Address Capacitance	C _{ADD}	V _{ADD} =0V	—	—	8	pF
Input Capacitance	C _I	V _I =0V	—	—	10	pF
I/O Capacitance	C _{I/O}	V _{I/O} =0V	—	—	10	pF

● AC Electrical Characteristics

○ Read Cycle

(V_{DD}=5V±10%, V_{SS}=0V, Ta=0 to 70°C)

Parameter	Symbol	Conditions	SRM20100LC70		SRM20100LC85		SRM20100LC10		Unit
			Min	Max	Min	Max	Min	Max	
Read cycle time	t _{RC}	* 1	70	—	85	—	100	—	ns
Address access time	t _{ACC}		—	70	—	85	—	100	ns
Chip select 1 access time	t _{ACS1}		—	70	—	85	—	100	ns
Chip select 2 access time	t _{ACS2}		—	70	—	85	—	100	ns
Output enable access time	t _{OE}		—	40	—	45	—	50	ns
Chip select 1 output set time	t _{CLZ1}	* 2	10	—	10	—	10	—	ns
Chip select 1 output floating	t _{CHZ1}		—	30	—	30	—	35	ns
Chip select 2 output set time	t _{CLZ2}		10	—	10	—	10	—	ns
Chip select 2 output floating	t _{CHZ2}		—	30	—	30	—	35	ns
Output enable output set time	t _{OLZ}		5	—	5	—	5	—	ns
Output enable output floating	t _{OHZ}	* 1	—	30	—	30	—	35	ns
Output hold time	t _{OH}		10	—	10	—	10	—	ns

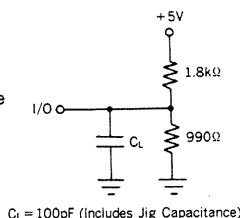
○ Write Cycle

(V_{DD} = 5V ± 10%, V_{SS} = 0V, Ta = 0 to 70°C)

Parameter	Symbol	Conditions	SRM20100LC ₇₀		SRM20100LC ₈₅		SRM20100LC ₁₀		Unit
			Min	Max	Min	Max	Min	Max	
Write cycle time	t _{wc}	* 1	70	—	85	—	100	—	ns
Chip select time 1	t _{cw1}		60	—	70	—	80	—	ns
Chip select time 2	t _{cw2}		60	—	70	—	80	—	ns
Address enable time	t _{AW}		60	—	70	—	80	—	ns
Address setup time	t _{AS}		0	—	0	—	0	—	ns
Write pulse width	t _{WP}		55	—	65	—	75	—	ns
Address hold time	t _{WR}		0	—	0	—	0	—	ns
Input data setup time	t _{DW}		30	—	35	—	40	—	ns
Input data hold time	t _{DH}		0	—	0	—	0	—	ns
$\overline{\text{WE}}$ Output floating	t _{WHZ}	* 2	—	30	—	30	—	35	ns
$\overline{\text{WE}}$ Output setup time	t _{OW}		5	—	5	—	5	—	ns

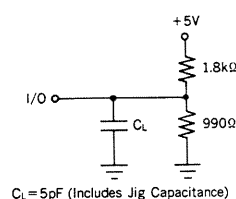
* 1 Test Conditions

1. Input pulse level : 0.6V to 2.4V
2. $t_r = t_f = 5\text{ns}$
3. Input and output timing reference levels : 1.5V
4. Output load $C_L = 100\text{pF}$



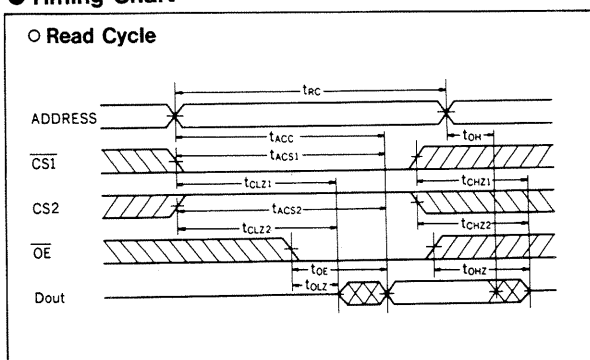
* 2 Test Conditions

1. Input pulse level : 0.6V to 2.4V
2. $t_r = t_f = 5\text{ns}$
3. Input timing reference levels : 1.5V
4. Output timing reference levels : ±200mV (the level displaced from stable output voltage level)
5. Output load $C_L = 5\text{pF}$

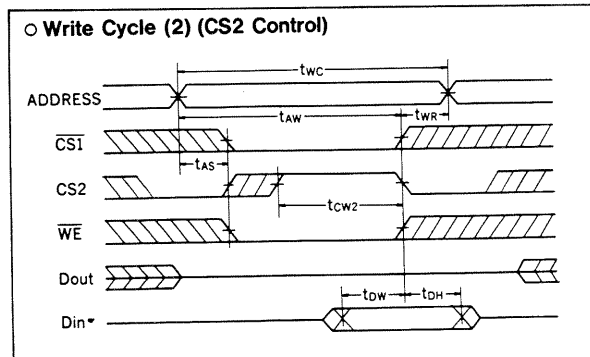


● Timing Chart

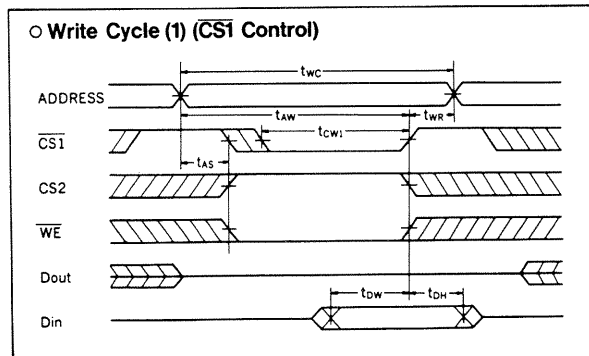
○ Read Cycle



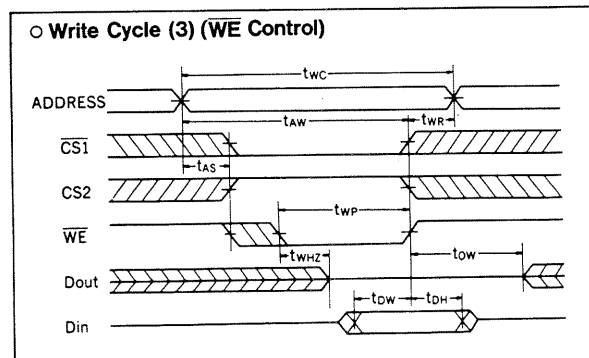
○ Write Cycle (2) (CS2 Control)



○ Write Cycle (1) (CS1 Control)



○ Write Cycle (3) (WE Control)

Note : 1. During read cycle time, $\overline{\text{WE}}$ is to be "H" level.2. During write cycle time that is controlled by CS1 or CS2, Output Buffer is in high impedance state whether $\overline{\text{OE}}$ level is "H" or "L".3. During write cycle time that is controlled by $\overline{\text{WE}}$, Output Buffer is high impedance state if $\overline{\text{OE}}$ is "H" level.

4. When I/O terminals are output mode, be careful that do not give the opposite signals to the I/O terminals.

DATA RETENTION CHARACTERISTIC WITH LOW VOLTAGE POWER SUPPLY

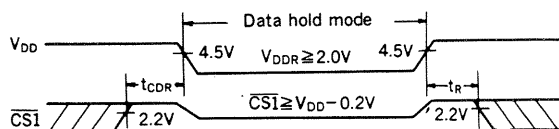
(Ta = 0 to 70°C)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Data retention supply voltage	V_{DDR}		2.0	—	5.5	V
Data retention current	I_{DDR}	$V_{DD} = 3V$ $\overline{CS1} = CS2 \geq V_{DD} - 0.2V$ or $CS2 \leq 0.2V$	—	1 *1	50	μA
Chip select·data hold time	t_{CDR}		0	—	—	ns
Operation recovery time	t_R		t_{RC} *2	—	—	ns

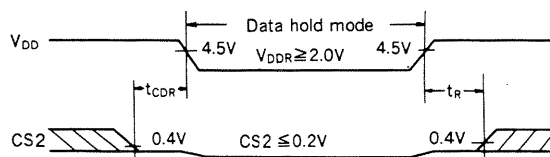
*1 Ta = 25°C

*2 t_{RC} = Read cycle time

Data retention timing ($\overline{CS1}$ Control)



Data retention timing (CS2 Control)



FUNCTIONS

● Truth Table

$\overline{CS1}$	CS2	$\overline{OE}$	$\overline{WE}$	DATA I/O	Mode	I_{DD}
H	X	—	—	Hi-Z	Unselected	I_{DDs}, I_{DDs1}
—	L	—	—	Hi-Z	Unselected	I_{DDs}, I_{DDs1}
L	H	X	L	Input data	Write	I_{DDO}
L	H	L	H	Output data	Read	I_{DDO}
L	H	H	H	Hi-Z	Output disable	I_{DDO}

X: "H" or "L", — : "H", "L" or "Hi-Z"

● Reading data

Data is able to be read when the address is setted while holding $\overline{CS1} = "L"$, $CS2 = "H"$, $\overline{OE} = "L"$ and $\overline{WE} = "H"$. Since Data I/O terminals are in high impedance state when $\overline{OE} = "H"$, the data bus line can be used for any other objective, then access time apparently is able to be cut down.

● Writing data

There are the following four ways of writing data into the memory.

- (1) Hold $CS2 = "H"$, $\overline{WE} = "L"$ set addresses and give "L" pulse to $\overline{CS1}$.
- (2) Hold $\overline{CS1} = "L"$, $\overline{WE} = "L"$, set addresses and give "H" pulse to $CS2$.
- (3) Hold $\overline{CS1} = "L"$, $CS2 = "H"$, set addresses and give "L" pulse to $\overline{WE}$.
- (4) After setting addresses, give "L" pulse to $\overline{CS1}$, $\overline{WE}$ and give "H" pulse to $CS2$.

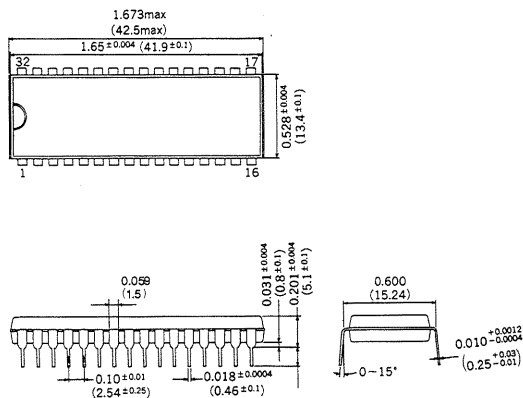
Anyway, data on the Data I/O terminals are latched up into the SRM20100LC70/85/10 at the end of the period that $\overline{CS1}$, $\overline{WE}$ are "L" level, and $CS2$ is "H" level. As Data I/O terminals are in high impedance state when any of $\overline{CS1}$, $\overline{OE} = "H"$, or $CS2 = "L"$, the contention on the data bus can be avoided.

● Standby mode

When $\overline{CS1}$ is "H" or CS2 is "L" level, the SRM20100LC_{70/85/10} is in the standby mode which has retaning date operation. In this case Data I/O terminals are Hi-Z, and all inputs of addresses, $\overline{WE}$ and data can be any "H" or "L". When $\overline{CS1}$ and CS2 level are in the range over $V_{DD}-0.2V$, or CS2 level is in the range under 0.2V, in the SRM20100LC_{70/85/10} there is almost no current flow except through the high resistance parts of the memory.

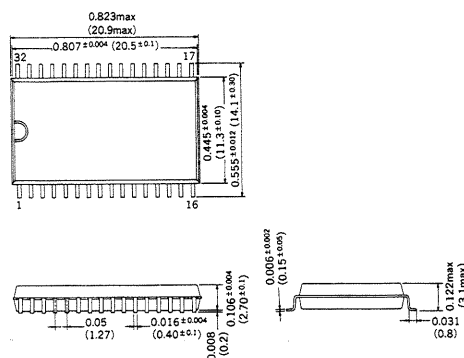
■ PACKAGE DIMENSIONS

Plastic DIP-32pin



unit : inch
(mm)

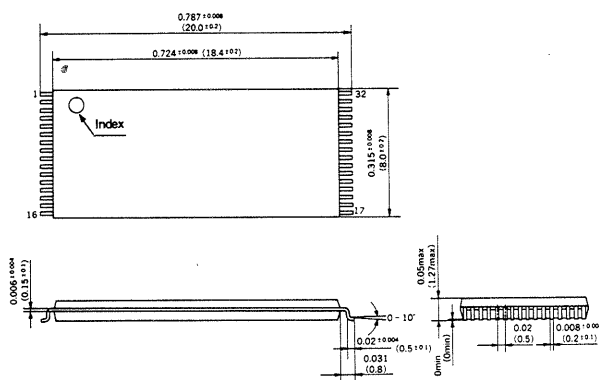
Plastic SOP6-32pin*1



unit : inch
(mm)

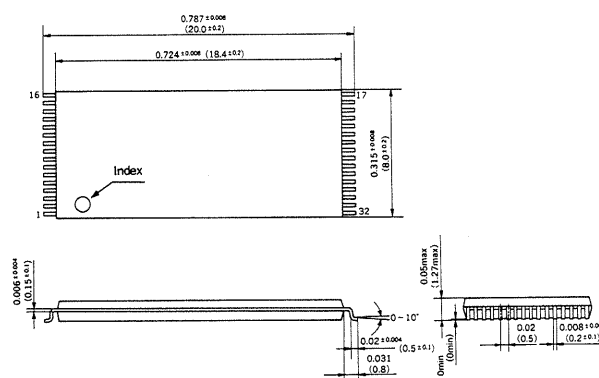
*1 SRM20100LM_{70/85/10} has the same characteristics as SRM20100LC_{70/85/10}.

Plastic TSOP-32pin*1 (Under development)

unit : inch
(mm)

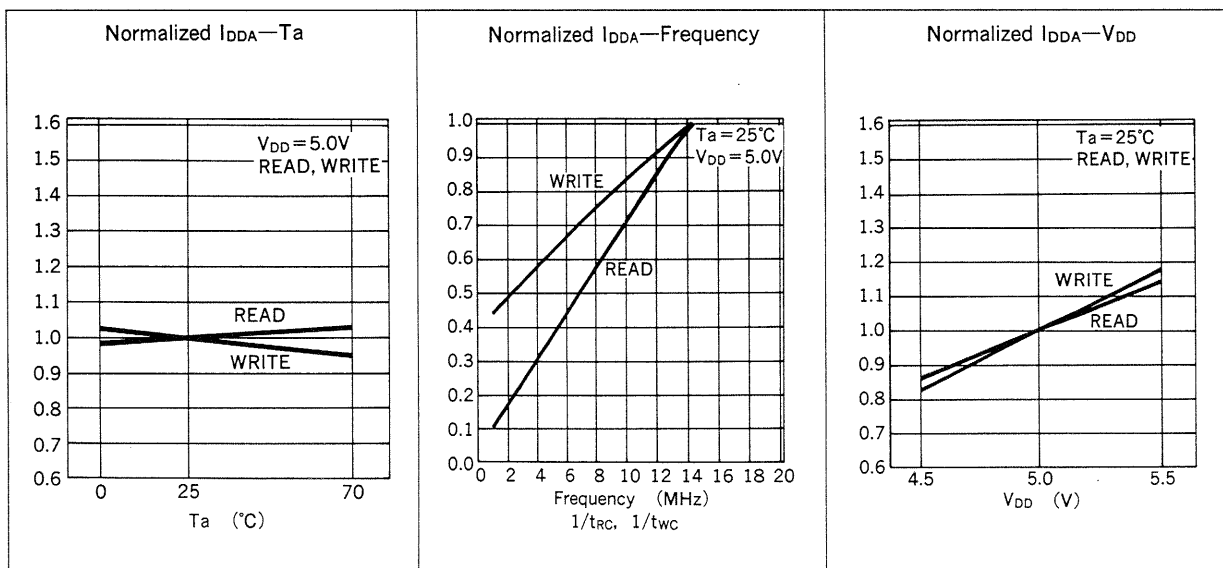
*1 SRM20100LTM70/85/100 has the same characteristics as SRM20100LC70/85/10.

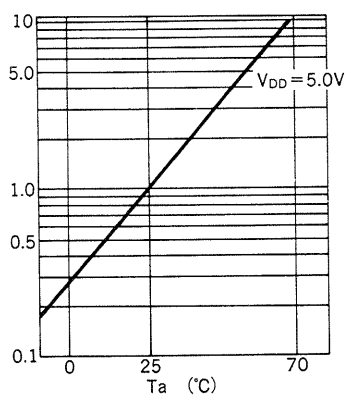
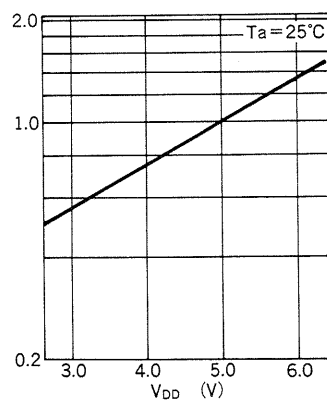
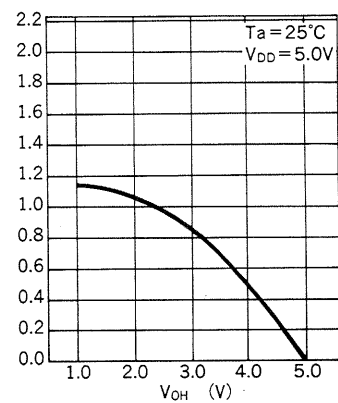
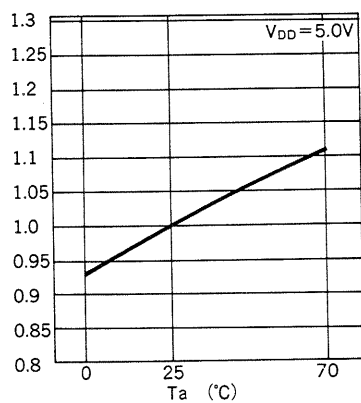
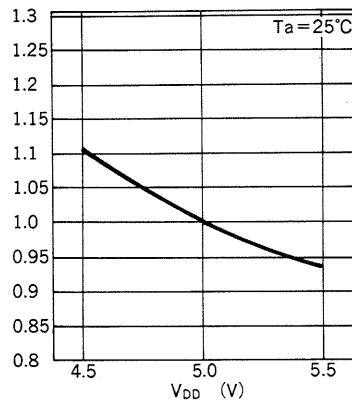
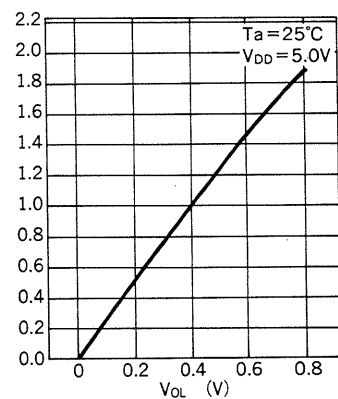
Plastic TSOPR-32pin*2 (Under development)

unit : inch
(mm)

*2 SRM20100LRM70/85/100 has the same characteristics as SRM20100LC70/85/10.

■ CHARACTERISTICS CURVES



Normalized I_{DD1} — T_a Normalized I_{DD1} — V_{DD} Normalized I_{OH} — V_{OH} Normalized t_{ACC}
 t_{ACS1}
 t_{ACS2} — T_a Normalized t_{ACC}
 t_{ACS1}
 t_{ACS2} — V_{DD} Normalized I_{OL} — V_{OL} Normalized t_{ACC}
 t_{ACS1}
 t_{ACS2} — C_L 