超低功耗USB 2.0转10/100M 快速以太网控制电路

概述

SR9900A是一个高集成度、超低功耗、单芯片USB 2.0转10/100M以太网控制电路。为各类应用增加低成本、小型封装、即插即用的快速以太网功能，可用于台式电脑、笔计本电脑、超便携式电脑、平板电脑、托架/端口复制器/扩展坞、游戏机、智能家居及任何有USB接口的嵌入式设备。

SR9900A内部集成USB 2.0收发器、基于IEEE802.3和IEEE802.3az-2010的10/100M以太网模块、以及高效的内存控制模块。

SR9900A完全兼容Microsoft 的NDIS5、NDIS6（IPv4、IPv6、TCP、UDP）Checksum特性。并支持IEEE802 IP2层优先编码，以及IEEE802.1Q虚拟本地网（VLAN）。

主要特点

- 单芯片USB2.0转10/100M快速以太网控制器
- USB设备接口
  - 集成USB2.0收发器，符合USB2.0 协议
  - 支持USB全速及高速模式
- 快速10/100M以太网接口
  - 集成10/100M快速以太网MAC和PHY模块
  - 兼容IEEE 802.3 10Base-T/100Base-TX
  - 兼容IEEE 802.3 100Base-FX
  - 自动协商功能
  - 支持双绞线交换、极性、相位偏移校正
  - 网线交叉检测及自动校正
  - 支持无振荡的网络唤醒
  - 内置TX/RX 封包缓存
  - 内置IPv4/IPv6封包校验和承载引擎，支持IPv4 TCP/IP/UDP/ICMP/IGMP、IPv6 TCP/UDP/ICMPv6封包校验的生成和检查
  - 支持全双工IEEE 802.3x流量控制及半双工冲突压力回退流量控制
  - 支持IEEE 802.1Q VLAN 标记
  - 支持IEEE 802.3az-2010（EEE）
- 支持网络远程唤醒功能
  - 支持休眠模式
  - 支持通过网络链接状态改变、魔术包、Microsoft唤醒包等事件进行远程唤醒
  - 支持Protocol Offloads（ARP和NS）
  - 休眠模式下可选择网络低功耗或关闭PHY供电
- 先进的电源管理功能
  - 支持动态电源管理以节省在空载或轻负载状态下的功耗
  - 支持IEEE 802.3az-2010（EEE）节能模式
  - 支持休眠模式时的极低功耗睡眠模式
- 支持通过GPIO管脚禁用网络功能
- 支持SPI Flash及串行EEPROM
- 支持CDC-ECM驱动
- MacOS/IOS免驱
- 内置OTP存储器，可在线更新USB设备描述符等设置
- 单个25MHz 时钟输入，支持晶体及钟振
- 5.0V单电源供电，内部集成电压转换电路
- 支持LED闪烁频率及占空比可设置
- 采用符合RoHS规范的小型QFN24-04x04封装
- SR9900A网卡芯片内置随即MAC地址（Efuse烧录完成）

应用范围

- USB以太网适配器
- 网络打印机
- 支付终端读卡器
- 移动互联网装置
- 上网本、个人平板电脑
- 移动终端
- 多媒体网关
- 游戏机、移动媒体播放器
- IP机顶盒、IPTV、DVD、DVR等

内部框图

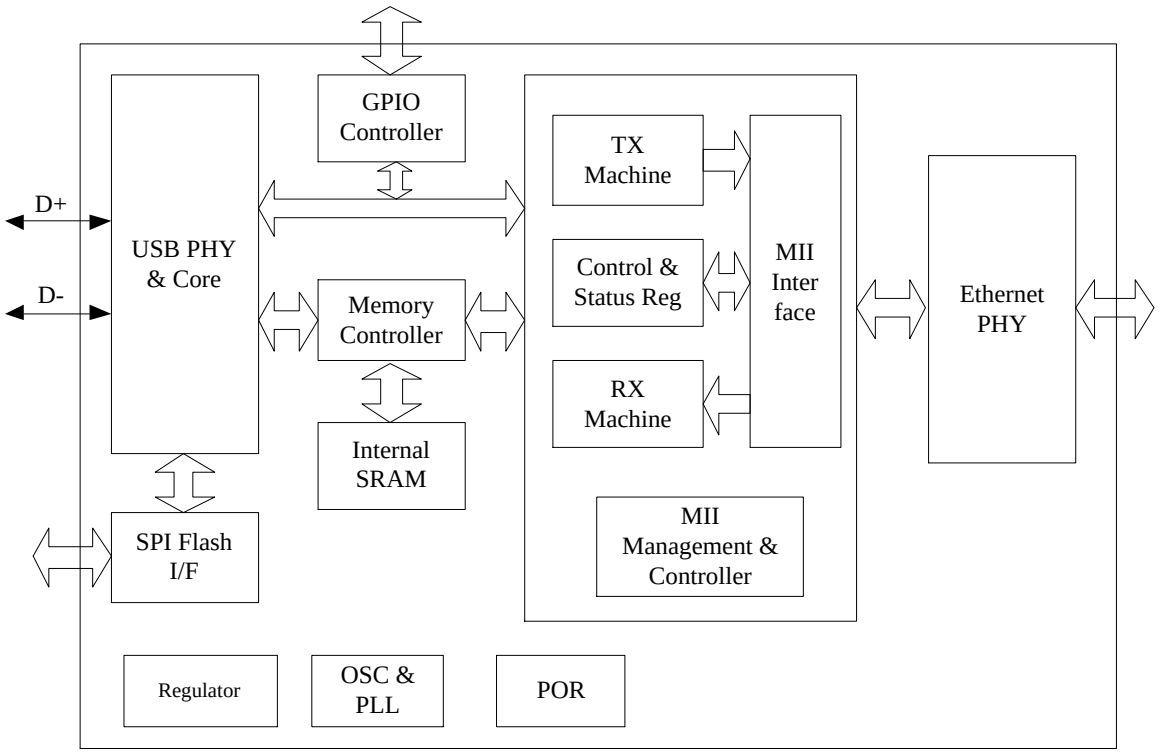

GPIO Controller
D+
D-
USB PHY & Core
Memory Controller
Internal SRAM
SPI Flash I/F
TX Machine
Control & Status Reg
RX Machine
MII Inter face
MII Management & Controller
Ethernet PHY
Regulator
OSC & PLL
POR

图1 内部框图

管脚排列图

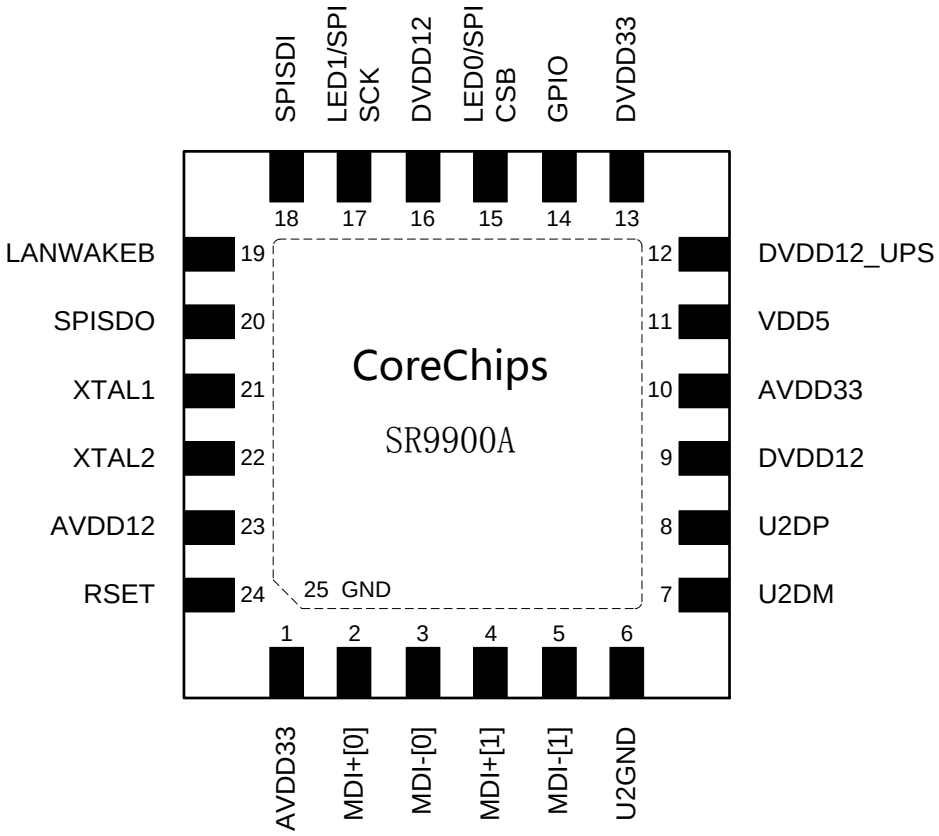


图2 QFN24 封装管脚

管脚定义

管脚名称	符 号	I/O	描　　述
2、3	MDI+[0]、MDI-[0]	I/O	在 MDI 模式下为网络接收端；在 MDIX 模式下为网络发送端
4、5	MDI+[1]、MDI-[1]	I/O	在MDI模式下为网络发送端；在MDIX模式下为网络接收端
24	RSET	I	参考电阻脚，外接2.49K欧姆电阻
22	XTAL2	O	25MHz 振荡输出脚
21	XTAL1	I	25MHz 振荡输入脚
8	U2DP	I/O	USB2.0/USB1.1 数据线 DP
7	U2DM	I/O	USB2.0/USB1.1 数据线 DM
19	LANWAKEB	O	电源管理事件输出脚，低电平有效
15	LED0	O	LED 指示灯驱动管脚
17	LED1	O	
15	SPICSB	O	SPI Flash 芯片选择脚
20	SPISDO	I	输入从 SPI Flash 串行数据输出脚
18	SPISDI	O	输出到 SPI Flash 串行数据输入脚。
17	SPISCK	O	SPI Flash 串行时钟
14	GPIO	I/O	通用 IO 接口
6	U2GND	P	USB模块地
25	GND	P	模拟地
11	VDD5	P	LDO1稳压电路5V电源输入
10	AVDD33	P	LDO1稳压电路3.3V电源输出
12	DVDD12_UPS	P	LDO1 稳压电路 1.2V 电源输出，备用
1	AVDD33	P	3.3V 模拟电源输入
13	DVDD33	P	3.3V 数字电源输入
23	AVDD12	P	LDO2 稳压线路 1.2V 输出及 1.2V 模拟电源输入
16	DVDD12	P	1.2V 数字电源输入
9	DVDD12	P	USB 模块 1.2V 电源输入

I=输入，O=输出，I/O=输入/输出，I/PU=输入带上拉，P=电源

电气特性

极限参数

参　　数	符 号	参 数 范 围	单位
5V工作电压	V_{DD5}	-0.3 ~ 5.5	V
3.3V工作电压	DV_{DD33} AV_{DD33}	-0.3 ~ 3.63	V
1.2V工作电压	AV_{DD12} V_{DD12} DV_{DD12_UPS}	-0.3 ~ 1.35	V
输入/输出电压	V_{I33}/V_{O33}	-0.3 ~ DV_{DD33}+0.3	V
贮存温度	T_{stg}	-55 ~ 125	^{o}C

推荐工作条件

参　　数	符 号	参 数 范 围	单位
5V工作电压	V_{DD5}	4.75 ~ 5.25	V
3.3V工作电压	DV_{DD33} AV_{DD33}	3.14 ~ 3.46	V
1.2V工作电压	AV_{DD12} V_{DD12} DV_{DD12_UPS}	1.15 ~ 1.25	V
输入/输出电压	V_{I33}/V_{O33}	0 ~ DV_{DD33}	V
工作温度	T_{opr}	0 ~ 70	^{o}C

工作电气特性 (除非特别说明，T_{opr}=25°C, V_{DD5}=5.0V, V_{DD33}=3.3V, V_{DD12}=1.2V, V_{GND}=0V)

参　　数	符 号	测 试 条 件	最小值	典型值	最大值	单位
5V工作电压	V_{DD5}		4.2	5.0	5.5	V
3.3V工作电压	DV_{DD33} AV_{DD33}		3.14	3.3	3.46	V
1.2V工作电压	AV_{DD12} V_{DD12} DV_{DD12_UPS}		1.08	1.2	1.32	V
电源电流1	I_{DD1}	100Base-T 重负载		75		mA
电源电流2	I_{DD1}	100Base-T 空闲 (EEE未使能)		65		mA
电源电流3	I_{DD1}	100Base-T 空闲带 EEE		34		mA
电源电流4	I_{DD1}	10Base-T 重负载		50		mA

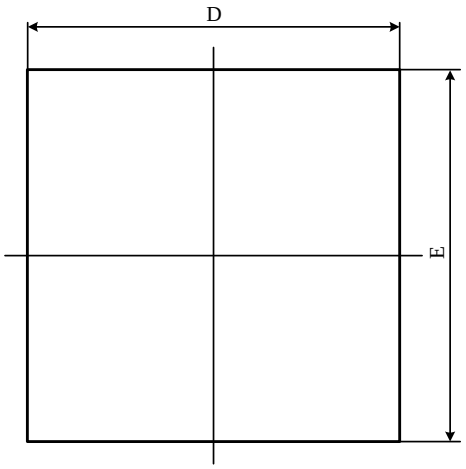
电源电流5	I_{DD1}	10Base-T 空闲		30		mA
电源电流6	I_{DD1}	链接断开省电模式		28		mA
AVDD33稳压输出	AV_{DD33}		3.14	3.3	3.46	V
AVDD12稳压输出	AV_{DD12}		1.08	1.2	1.32	V
DVDD12_UPS稳压输出	DV_{DD12_UPS}		1.08	1.2	1.32	V
USB 2.0 收发器（高速模式）						
高速差分输入电压	V_{HSDIFF}	|VI(DP)-VI(DM)|	300			mV
高速共模电压范围	V_{HSCM}		-50		500	mV
高速抑制检测阈值	V_{HSSQ}	抑制检测			100	mV
		非抑制检测	200			mV
高速空闲状态输出电压	V_{HSQI}		-10		10	mV
高速低电平输出电压	V_{HSOL}		-10		10	mV
高速高电平输出电压	V_{HSOH}		-360		400	mV
高速J电平输出电压	V_{CHIPJ}		700		1100	mV
高速K电平输出电压	V_{CHIPK}		-900		-500	mV
输出阻抗	R_{DRV}		40.5	45	49.5	Ω
USB 1.1 收发器（全速模式）						
DP/DM低电平输出电压	V_{OL}	1.5K to V_{DD33}	0		0.3	V
DP/DM高电平输出电压	V_{OH}	15K to GND	2.8		3.6	V
DP/DM 差分输入电压	V_{DI}		0.2			V
DP/DM 差分共模范围	V_{CM}		0.8		2.5	V
单端接收阈值	V_{SE}		0.8		2.0	V
DP/DM 收发器电容	C_{IN}				20	pF
DP/DM 高阻态输入漏电流	I_{LO}		-10		+10	A
网络端口						
输出端电压峰峰值	V_{PP1}	10BASE-T模式		3.2		V
输出端电压峰峰值	V_{PP2}	100BASE-TX模式	1.9	2.0	2.1	V
上升沿/下降沿时间	T_R/T_F	100BASE-TX模式	3	4	5	ns
输出端信号抖动	T_{JT}	100BASE-TX模式，空闲状态			1.2	ns
输出过冲电压	V_{OS}	100BASE-TX模式			5	%
输入阻抗	R_I			10		KΩ
共模输入电压	V_{CM}		1.7	2.0	2.3	V
无差错接收最长线缆	L_{RCV}		120			m
通用IO端口						
低电平输入电压	V_{IL}				0.9	V
高电平输入电压	V_{IH}		2.0			V

低电平输出电压	V_{OL}	IOL=8mA			0.4	V
高电平输出电压	V_{OH}	IOH=8mA	2.4			V
输入上拉电阻	R_{PU}		40	75	150	KΩ
输入下拉电阻	R_{PD}		40	75	150	KΩ
输入漏电流	I_{LEAK}	VIN=0 或 DV_{DD33}			1	μA

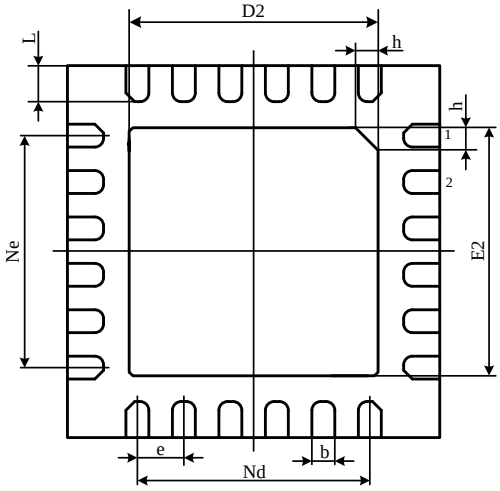
封装外形图

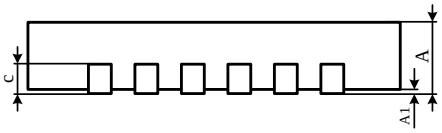
QFN24-4x4-0.50　　单位: mm

TOP VIEW



BOTTOM VIEW





符 号	单位（毫米）		
	最小	典型	最大
A	0.70	0.75	0.80
A1		0.01	0.05
b		0.25	
c		0.20	
e	0.50BSC		
Ne	2.50BSC		
Nd	2.50BSC		
D	3.90	4.00	4.10
D2			2.70
E	3.90	4.00	4.10
E2			2.70
L		0.40	
h		0.30	

Ultra-Low Power Single-Chip USB 2.0 to 10/100M Ethernet Controller

General Description

The CoreChips SR9900A 10/100M Ethernet controller combines an IEEE 802.3u compliant Media Access Controller (MAC), USB bus controller, and embedded memory. A linear regulator (LDO) is incorporated for reduced BOM cost.

With state-of-the-art DSP technology and mixed-mode signal technology, the SR9900A offers high-speed transmission over CAT 5 UTP cable or CAT 3 UTP (10Mbps only) cable. Functions such as Crossover Detection and Auto-Correction, polarity correction, adaptive equalization, cross-talk cancellation, echo cancellation, timing recovery, and error correction are implemented to provide robust transmission and reception capabilities. The SR9900A features embedded One-Time-Programmable (OTP) memory.

Advanced Configuration Power management Interface (ACPI)—power management for modern operating systems that are capable of Operating System-directed Power Management (OSPM)—is supported to achieve the most efficient power management possible. In addition to the ACPI feature, remote wake-up (including AMD Magic Packet and Microsoft Wake-Up Frame) is supported in both ACPI and APM (Advanced Power Management) environments.

The SR9900A supports Microsoft Wake Packet Detection (WPD) to provide Wake-Up Frame information to the OS, e.g., PatternID, OriginalPacketSize, SavedPacketSize, SavedPacketOffset, etc. WPD helps prevent unwanted/ unauthorized wake-up of a sleeping computer.

The SR9900A is fully compliant with Microsoft NDIS5, NDIS6 (IPv4, IPv6, TCP, UDP) Checksum features, and supports IEEE 802 IP Layer 2 priority encoding and IEEE 802.1Q Virtual bridged Local Area Network (VLAN). The above features contribute to lowering CPU utilization, especially benefiting performance when in operation on a network server.

The SR9900A supports Protocol offload. It offloads some of the most common protocols to NIC hardware in order to prevent spurious wake-up and further reduce power consumption. The SR9900A can offload ARP (IPv4) and NS (IPv6) protocols while in the D3 power saving state.

The SR9900A supports IEEE 802.3az-2010, also known as Energy Efficient Ethernet (EEE). IEEE 802.3az operates with the IEEE 802.3 Media Access Control (MAC) Sublayer to support operation in Low Power Idle mode. When the Ethernet network is in low link utilization, EEE allows systems on both sides of the link to save power.

The SR9900A also features USB 2.0 technology. It provides higher bandwidth and improved protocols for data exchange between the host and the device. In addition, USB 2.0 offers a more aggressive power management feature that enables selective suspend to save energy.

The SR9900A is suitable for multiple market segments and emerging applications, such as desktop, mobile, workstation, server, communications platforms, docking station, and embedded applications.

Features

- Supports USB 2.0 and 1.1
- Integrated 10/100M transceiver
  - Supports Full Duplex flow control (IEEE 802.3x)
  - Fully compliant with IEEE 802.3, IEEE 802.3u
  - Supports IEEE 802.1P Layer 2 Priority Encoding
  - Supports IEEE 802.1Q VLAN tagging
  - Supports IEEE 802.3az-2010 (EEE)
  - Auto-Negotiation with Next Page capability
- Microsoft AOAC (Always On Always Connected)
  - Supports Wake-Up Frame pattern exact matching
  - Supports link change wake up
  - Supports Microsoft WPD (Wake Packet
  - Detection)
  - Supports Protocol Offload (ARP & NS)
- Microsoft NDIS5, NDIS6 Checksum Offload (IPv4, IPv6, TCP, UDP) and Segmentation Task-offload (Large send v1 and Large send v2) support
- Supports pair swap/polarity/skew correction
- Crossover Detection & Auto-Correction
- Standard for sleeping hosts (see note 1)
- XTAL-Less Wake-On-LAN
- Supports 25MHz external clock (from oscillator or system clock source)
- Supports power down/link down power saving
- Transmit/Receive on-chip buffer support
- Embedded OTP memory
- Low power supply 1.2V 3.3V and 5.0V; 1.2V and 3.3V are generated by internal linear regulator (LDO)
- Supports Customizable LEDs
- Controllable LED Blinking Frequency and Duty Cycle
- Supports hardware CRC (Cyclic Redundancy Check) function
- LAN disable with GPIO pin
- Supports LPM (Link Power Management)
- SPI Flash Interface
- Supports CDC-ECM
- 24-pin QFN ‘Green’ package
- 0.11μm CMOS process
- Built in random MAC address （Eufse）

Application

- USB Dongle
- Network Printer
- Card Reader for payment
- Docking Station
- Port Replicator for Mobile Computer
- Internet Security USB Key
- Media Gateway
- Pocketable Computer
- Portable Media Player
- TiVo Box
- Game Console
- IP STB
- DVD-Recorder/DVR
- IPTV

Block Diagram

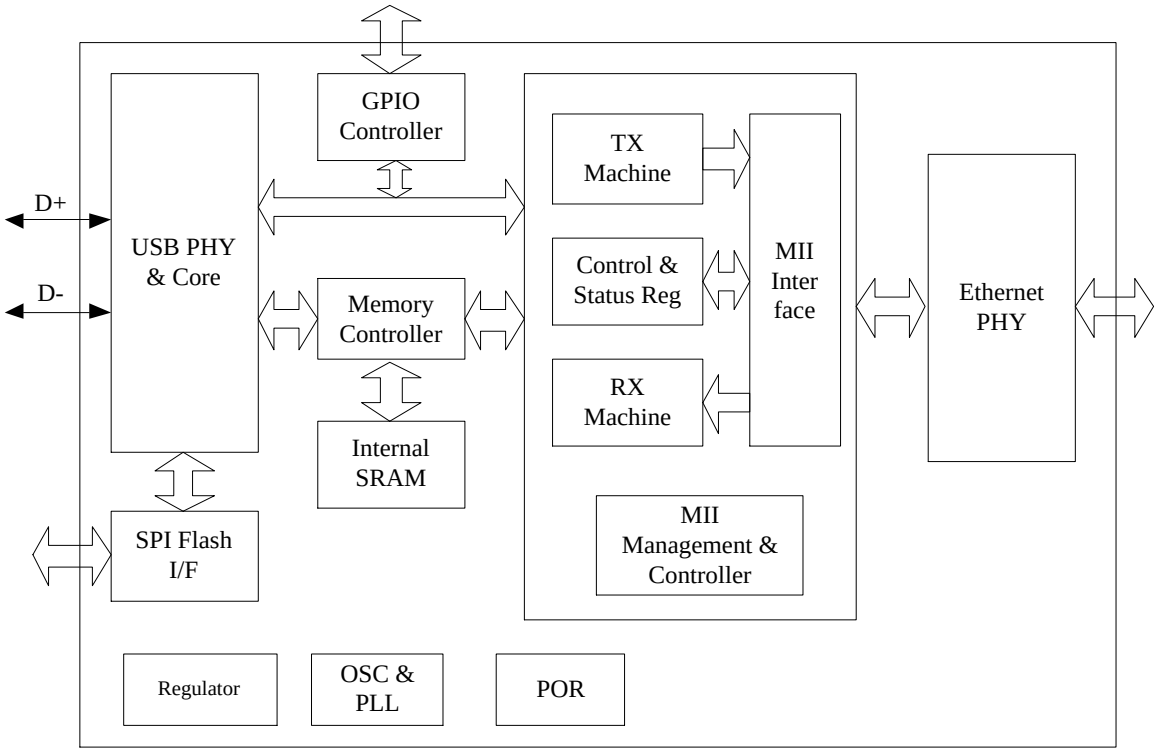


Figure 1. Block Diagram

Pin Assignment

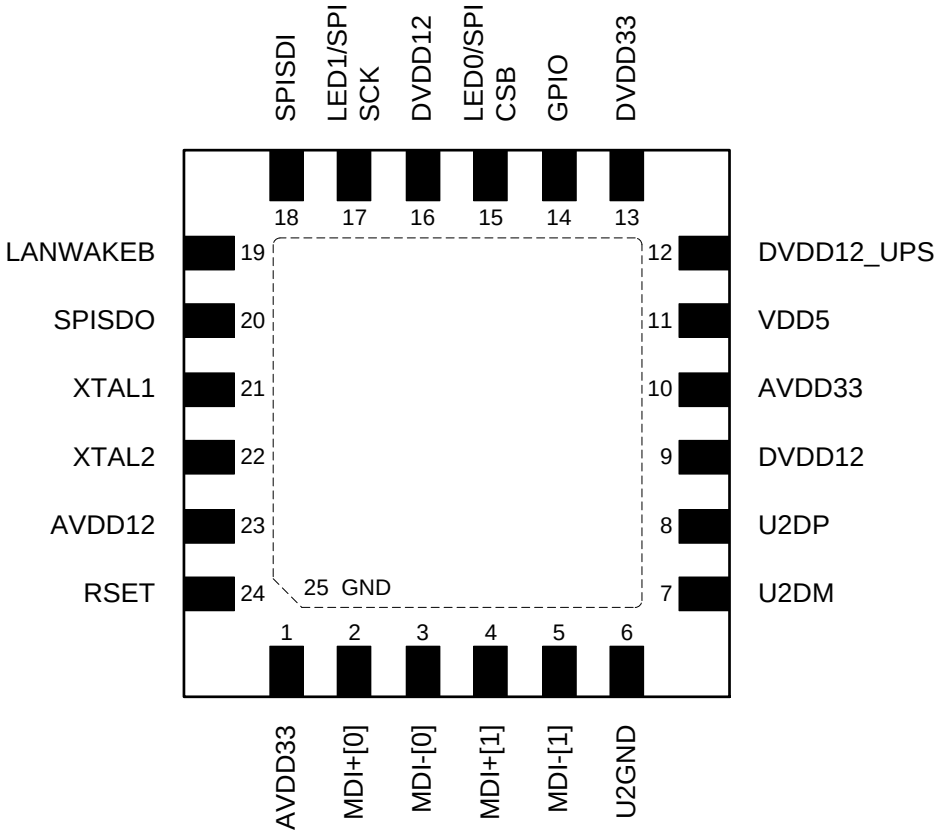


Figure2. Pin Assignments

Pin Descriptions

Pin No	Symbol	Type	Description
2,3	MDI+[0]、MDI-[0]	I/O	In MDI mode, this pair acts as the BI_DA+/- pair, and is the transmit pair in 10Base-T and 100Base-TX. In MDI crossover mode, this pair acts as the BI_DB+/- pair, and is the receive pair in 10Base-T and 100Base-TX.
4,5	MDI+[1]、MDI-[1]	I/O	In MDI mode, this pair acts as the BI_DB+/- pair, and is the receive pair in 10Base-T and 100Base-TX. In MDI crossover mode, this pair acts as the BI_DA+/- pair, and is the transmit pair in 10Base-T and 100Base-TX.
24	RSET	I	Reference input. For external resistor reference
22	XTAL2	O	Output of 25MHz Clock Reference
21	XTAL1	I	Input of 25MHz Clock Reference
8	U2DP	I/O	USB 2.0/USB 1.1 Differential Signal Pair
7	U2DM	I/O	
19	LANWAKEB	O	Power Management Event Output Pin (Active Low)
15	LED0	O	Customizable LED0
17	LED1	O	Customizable LED1
15	SPICSB	O	SPI Flash Chip Select
20	SPISDO	I	Input from SPI Flash Serial Data Output Pin
18	SPISDI	O	Output to SPI Flash Serial Data Input Pin
17	SPISCK	O	SPI Flash Serial Data Clock
14	GPIO	I/O	General Purpose Input/Output Pin
6	U2GND	P	USB Ground
25	GND	P	Ground (Exposed Pad)
11	VDD5	P	LDO 5.0V Power Supply
10	AVDD33	P	Analog 3.3V Power Supply
12	DVDD12_UPS	P	Digital 1.2V Uninterruptible Power Supply
1	AVDD33	P	Analog 3.3V Power Supply
13	DVDD33	P	Digital 3.3V Power Supply
23	AVDD12	P	Analog 1.2V Power Supply
16	DVDD12	P	Digital 1.2V Power Supply
9	DVDD12	P	USB Digital 1.2V Power Supply

I=Input, O=Output, IO= Bi-directional input and output, P=Power

Electrical Characteristics

Absolute Maximum Ratings

Parameter	Symbol	Range	Units
5.0V Supply Voltage	V_{DD5}	-0.3 ~ 5.5	V
3.3V Supply Voltage	DV_{DD33} AV_{DD33}	-0.3 ~ 3.63	V
1.2V Supply Voltage	AV_{DD12} V_{DD12} DV_{DD12_UPS}	-0.3 ~ 1.35	V
Input/ Output Voltage	V_{I33}/V_{O33}	-0.3 ~ DV_{DD33}+0.3	V
Storage Temperature Range	Tstg	-55 ~ 125	^{o}C

Recommend Operation Conditions

Parameter	Symbol	Range	Units
5.0V Supply Voltage	V_{DD5}	4.75 ~ 5.25	V
3.3V Supply Voltage	DV_{DD33} AV_{DD33}	3.14 ~ 3.46	V
1.2V Supply Voltage	AV_{DD12} DV_{DD12} DV_{DD12_UPS}	1.15 ~ 1.25	V
Input/output Voltage	V_{I33}/V_{O33}	0 ~ DV_{DD33}	V
Operating Temperature Range	Topr	0 ~ 70	^{o}C

DC Characteristics (unless otherwise specified T_{opr}=25°C, V_{DD5}=5.0V, V_{DD33}=3.3V, V_{DD12}=1.2V, V_{GND}=0V)

Parameter	Symbol	Condition	MIN	TYP	MAX	Units
5.0V Supply Voltage	V_{DD5}		4.2	5.0	5.5	V
3.3V Supply Voltage	DV_{DD33} AV_{DD33}		3.14	3.3	3.46	V
1.2V Supply Voltage	AV_{DD12} DV_{DD12} DV_{DD12_UPS}		1.08	1.2	1.32	V
Supply Current 1	I_{DD1}	100Base-T with heavy network traffic		75		mA

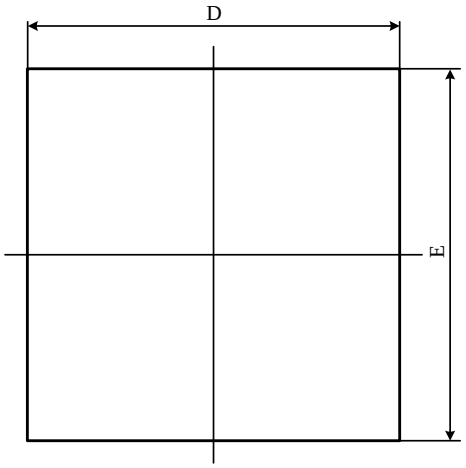
Supply Current 2	I_{DD2}	100Base-T Idle (EEE not Enable)		65		mA
Supply Current 3	I_{DD3}	100Base-T Idle with EEE		34		mA
Supply Current 4	I_{DD4}	10Base-T Full Duplex		50		mA
Supply Current 5	I_{DD5}	10Base-T Idle		30		mA
Supply Current 6	I_{DD6}	Link Down Power Saving		28		mA
AVDD33 regulator output	AV_{DD33}		3.14	3.3	3.46	V
AVDD12 regulator output	AV_{DD12}		1.08	1.2	1.32	V
DVDD12_UPS regulator output	DV_{DD12_UPS}		1.08	1.2	1.32	V
USB 2.0 Transceiver (HS)						
High speed differential input sensitivity	V_{HSDIFF}	$\|V_{I(DP)}-V_{I(DM)}\|$	300			mV
High speed data signaling common mode voltage range	V_{HSCM}		-50		500	mV
High speed squelch detection threshold	V_{HSSQ}	Squelch detected			100	mV
		No squelch detected	200			mV
High speed idle level output voltage	V_{HSQI}		-10		10	mV
High speed low level output Voltage	V_{HSOL}		-10		10	mV
High speed high level output voltage	V_{HSOH}		-360		400	mV
Chirp-J output voltage	V_{CHIPJ}		700		1100	mV
Chirp-K output voltage	V_{CHIPK}		-900		-500	mV
Driver output impedance	R_{DRV}		40.5	45	49.5	Ω
USB 1.1 Transceiver (FS/LS)						
Low-level output voltage	V_{OL}	1.5K to V_{DD33}	0		0.3	V
High-level output voltage	V_{OH}	15K to GND	2.8		3.6	V
Differential input sensitivity	V_{DI}		0.2			V
Differential common mode voltage	V_{CM}		0.8		2.5	V
Single ended receiver threshold	V_{SE}		0.8		2.0	V
Receiver capacity	C_{IN}				20	pF
Leakage current	I_{LO}		-10		+10	A
10/100M Ethernet PHY Transmitter						
Peak-to-peak differential output voltage 1	V_{PP1}	10BASE-T		3.2		V
Peak-to-peak differential output voltage 2	V_{PP2}	100BASE-TX	1.9	2.0	2.1	V
Signal rise / fall time	T_R/T_F	100BASE-TX	3	4	5	ns
Output jitter	T_{JT}	100BASE-TX Idle			1.2	ns
Overshoot	V_{OS}	100BASE-TX			5	%

Receiver input impedance	R_I			10		KΩ
Common mode input voltage	V_{CM}		1.7	2.0	2.3	V
Maximum error-free cable length	L_{RCV}		120			m
GPIO Port						
Input Voltage Low	V_{IL}				0.9	V
Input Voltage High	V_{IH}		2.0			V
Output Voltage low	V_{OL}	I_{OL}=8mA			0.4	V
Output Voltage High	V_{OH}	I_{OH}=8mA	2.4			V
Input pull-up resistance	R_{PU}		40	75	150	KΩ
Input Pull-down resistance	R_{PD}		40	75	150	KΩ
Leakage current	I_{LEAK}	V_{IN}=0 or DV_{DD33}			1	μA

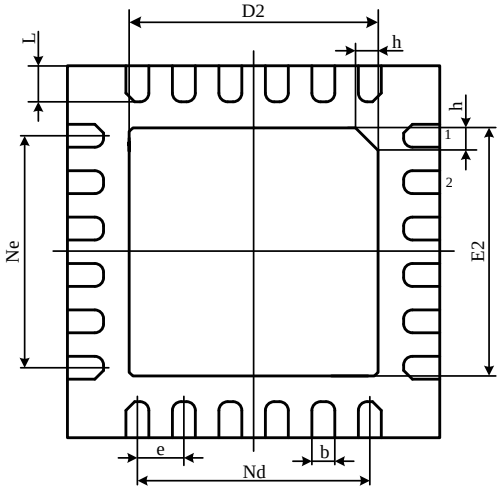
PACKAGE DIAGRAM

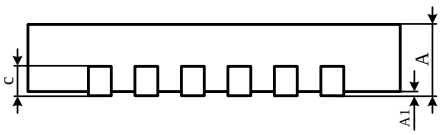
QFN24-4x4-0.50 Unit: mm

TOP VIEW



BOTTOM VIEW





Symbol	Unit (mm)		
	Min	Typ	Max
A	0.70	0.75	0.80
A1		0.01	0.05
b		0.25	
c		0.20	
e	0.50BSC		
Ne	2.50BSC		
Nd	2.50BSC		
D	3.90	4.00	4.10
D2			2.70
E	3.90	4.00	4.10
E2			2.70
L		0.40	
h		0.30	