SPEEDPIXEL TECHNOLOGY

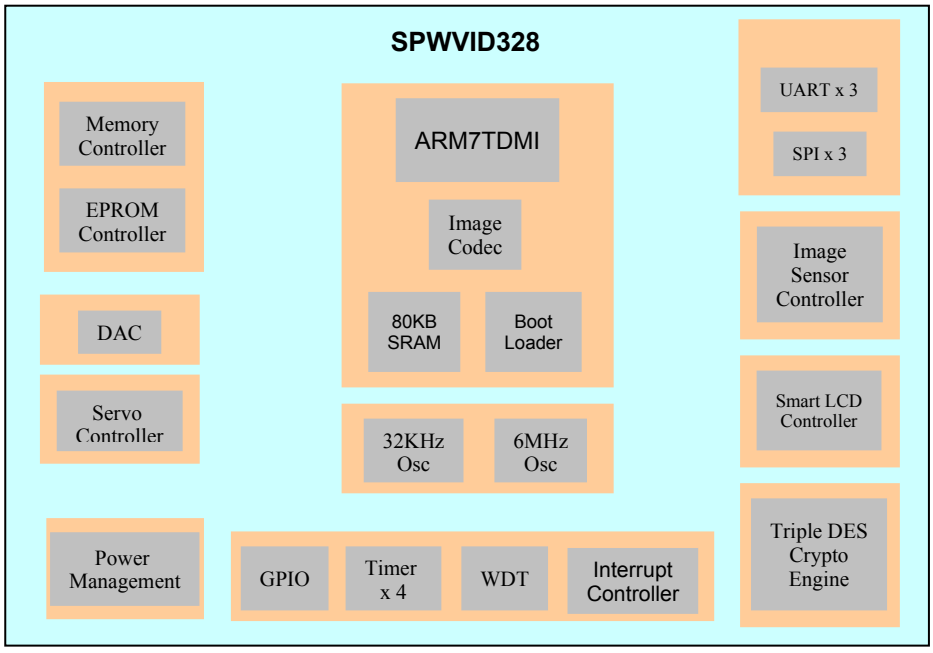
SPWVID328 Technical Data **Rev. 2.5/2008**

Package Information: LQFP-100 (RoHS)

SPWVID328
SPIC Wireless Portable System Processor

Introduction

The SPWVID328 is a system on chip integrated circuit optimized for power-efficient and cost-effective portable electronic products. The device has peripheral cluster embedded including CMOS sensor interface, smart LCD controller, image codec and servo controller etc. The rich peripheral set and broad-user based ARM7TDMI will enable fast product development cycle for applications such as digital wireless video transmission, advance remote controller, imaging and robotic application etc.



Features

Hardware Video Compression Decompression Engine

- Supports JPEG Baseline format
- Supports up to 1024x1024 pixels per frame
- Direct data streaming for enhanced traffic throughput
- Controllable compression rate for different application requirement
- Stallable processing pipeline to manage real-time processing requirement

Smart LCD Controller

- Supports 8-bit and 16-bit controller type panel
- Supports small memory-less AV delta panel in RGB mode, ITU-R BT.601 and 656 format
- Supports one layer true colour overlay
- Supports direct image data streaming from image decoder

Image Sensor Controller

- Supports ITU-R BT.601 format
- Supports direct image data streaming to image encoder
- Support resolution up to 1024x1024 pixels

Triple DES Crypto Engine

- Encryption and decryption with 3 unique 64-bit keys
- Supports data block operation to minimize CPU control
- Supports data block size up to 64KBytes
- Served as DMA for memory to memory move

Host Processor System

- 64MHz ARM7TDMI
- 80KByte embedded single cycle SRAM
- 16KByte embedded single cycle ROM with pre-installed RTOS
- Embedded boot-loader for flexible program upload from external serial ROM
- Vectored interrupt controller

Clock and Power Management

- 6MHz master clock crystal oscillator with programmable frequency synthesizer PLL
- 64MHz internal clock
- 32KHz crystal oscillator for timer served as real-time clock and wake up time base in deep sleep mode
- Nominal 1.8V core VDD and 3.3V IO VDD
- PLL and master clock crystal oscillator can be selectively turned off
- GPIO pins can be programmed to sense the external activity to wake up system from deep sleep mode

UART

- 3 UARTs with 16550 compatible programming model
- Independent 16-Byte transmit and receive FIFO

SPI

- 3 SPIs with configurable master or slave
- Configurable to emulate x32 I^2S master or slave
- Serial clock frequency up to 20MHz
- Independent 16-Byte transmit and receive FIFO

TIMER

- 4 timers with selectable 64MHz or 32KHz clock source

Memory Controller

- Selectable boot source from embedded ROM or external ROM
- Support auto detection of external SPI or I^2C type serial ROM
- Serial ROM encryption protection for software IP protection

Servo Controller for Robotic Application

- 32 independent channels for 20ms periodic pulse width servo control protocol
- Power noise reduction logic for power noise reduction in simultaneous servo activation

1-bit DAC

- 10-bit accuracy with good linearity
- Queue buffer for audio streaming
- Pop-reduction circuit for audio output
- Programmable watermark interrupt

GPIO

- Maximum 59 GPIO
- Almost all unused pin can be mapped as GPIO

Packaging

- 100 Pins LQFP Package (14x14x1.4mm)

Pin Function

NOTE: Most of the pins on the device has selectable function governed by the programmable system register. The IO type suffixed PU means the pin has hard-wired pull up resistor on the device. The IO type suffixed PUE means the pin has programmable (enable/disable) pull up resistor on the device.

	Normal Input	Schmitt Input	Output	Fix Pull up	Programmable Pull up Enable/Disable
O			√		
IPU	√			√	
IOPU	√		√	√	
IOPUE	√		√		√
IS		√			
IOS		√	√		
ISPU		√		√	
IOSPUE		√	√		√

Table 1: IO Type Combinations

Pin #	*Pin Name*	*Type*	*Default State*[1]	*Functional Description*
1	VDD33OSC	Power		3.3V supply for oscillator
2	VSSOSC_1	Power		GND for 32KHz oscillator
3	OSC32_PI	OSC XIN		32KHz crystal reference oscillator input; Tie to GND when 32KHz crystal is not mounted;
4	OSC32_PO	OSC XOUT		32KHz crystal reference oscillator output
5	VDD18OSC32	Power		1.8V supply for 32KHz oscillator
6	VSSOSC_2	Power		GND for 32KHz oscillator
7	TDO	O(4mA)	Hiz	JTAG TDO function
8	NTRST	IS		JTAG NTRST function
9	TCK	ISPU		JTAG TCK function
10	TMS	ISPU		JTAG TMS function
11	TDI	ISPU		JTAG TDI function
12	NRESET	ISPU		System power on reset for the whole device
13	NC	ISPU		Tie to VDDIO for normal operation

1 IO state during reset (i.e. NRESET pin forced low).

Pin #	Pin Name	Type	Default State	Functional Description
14	SRCK_SPICK0_PA1	IOSPUE	Input: pull up enabled	When {BOOT1,BOOT0}=11, it is external serial SPI boot ROM serial clock(output); SPI #0 serial clock(master output slave input); GPIO port A1(input/output);
15	SRSI_SPIMOSI0_PA3	IOSPUE	Input: pull up enabled	When {BOOT1,BOOT0}=11, it is external serial SPI boot ROM SI data(output); SPI #0 MOSI data(master output slave input); GPIO port A3(input/output);
16	SRSO_SPIMISO0_PA2	IOSPUE	Input: pull up enabled	When {BOOT1,BOOT0}=11, it is external serial SPI boot ROM SO data. It is the channel to upload application code from boot ROM to embedded memory(input); SPI #0 MOSI data(master input slave output); GPIO port A3(input/output);
17	SPICS0_PA0	IOSPUE	Input: pull up enabled	SPI #0 slave CS. When it is configured as SPI slave, it is SPI #0 chip select input. When it is configured as SPI master, it is GPIO port A0 (input/output); GPIO port A0(input/output);
18	VDDIO_5	Power		3.3V for IO supply
19	VSSIO_5	Power		GND for IO
20	VDDC_2	power		1.8V for core supply
21	PR2	IOPUE	Input	GPIO port R2 (input/output);
22	PR1	IOPUE	Input	GPIO port R1 (input/output);
23	PR0	IOPUE	Input	GPIO port R0 (input/output);
24	RC22_PM0	IOSPUE	Input	Servo channel #22 (output); GPIO port M0 (input/output);
25	R23_PM1	IOSPUE	Input	Servo channel #23 (output); GPIO port M1 (input/output);
26	CKCFG1	ISPU		Clock configuration pin: Do not connect when 1. Tie to GND when 0. {CKCFG1,CKCFG0} 00=bypass PLL and feed clock directly in XIN; 01=RESERVED 10=64MHz 11=54MHz

Pin #	Pin Name	Type	Default State	Functional Description
27	CKCFG0	ISPU		
28	BOOT1	ISPU		Boot configuration pin: Do not connect when 1. Tie to GND when 0. {BOOT1,BOOT0} 00=8-bit external parallel ROM 01=16-bit external parallel ROM 10=software external serial ROM boot loader (auto sensing) 11=hardware external SPI serial ROM boot loader
29	BOOT0	ISPU		
30	NC	ISPU		Tie to 3.3V VDDIO for normal operation
31	NC	ISPU		Tie to 3.3V VDDIO for normal operation
32	CTS2_PB4	IOSPUE	Input: pull up enabled	UART #2 CTS (input); GPIO port B4 (input/output);
33	RTS2_PN3	IOSPUE	Input: pull up enabled	UART #2 RTS (output); GPIO port N3 (input/output);
34	RX2_PB7	IOSPUE	Input: pull up enabled	UART #2 RX (input); GPIO port B7 (input/output);
35	TX2_PB6	IOSPUE	Input: pull up enabled	UART #2 TX (output); GPIO port B6 (input/output);
36	VDDIO_4	Power		3.3V for IO supply
37	VSSIO_4	Power		GND for IO
38	NC	IO	Output	Must be kept unconnected;
39	PS3	IOSPUE	Input: pull up enabled	GPIO port S3 (input/output);
40	PP4	IOPUE	Input	GPIO port P4 (input/output);
41	PP5	IOPUE	Input	GPIO port P5 (input/output);
42	PP6	IOPUE	Input	GPIO port P6 (input/output);
43	PP7	IOPUE	Input	GPIO port P7 (input/output);
44	RTS0_PG3	IOSPUE	Input:	UART #0 RTS (output);

Pin #	Pin Name	Type	Default State	Functional Description
			pull up enabled	GPIO port G3 (input/output);
45	CTS0_PG2	IOSPUE	Input: pull up enabled	UART #0 CTS (input); GPIO port G2 (input/output);
46	TX0_PG1	IOSPUE	Input: pull up enabled	UART #0 TX (output); GPIO port G1 (input/output);
47	RX0_PG0	IOSPUE	Input: pull up enabled	UART #0 RX (input); GPIO port G0 (input/output);
48	VSSIO_3	Power		GND for IO
49	VDDIO_3	Power		3.3V for IO supply
50	PN2	IOSPUE(4mA)[2]	Output	GPIO port N2 (input/output);
51	DA0_PB5	IOSPUE	Input: pull up enabled	DAC channel #0 PWM data (output); GPIO port B5 (input/output);
52	SRCS	OPU		Dedicated CS for external serial SPI boot ROM. When {BOOT1,BOOT0}=11, it will be active during power on reset. It negate after the content upload of boot ROM.
53	SPIMOSI2_DA3_RC11_PB3	IOSPUE	Input: pull up enabled	SPI #2 MOSI data(master output slave input); DAC channel #3 PWM data (output); Servo channel #11 (output); GPIO port B3 (input/output);
54	SPIMISO2_DA2_RC10_PB2	IOSPUE	Input: pull up enabled	SPI #2 MISO data (master input slave output); DAC channel #2 PWM data (output); Servo channel #10 (output); GPIO port B2 (input/output);
55	SPICK2_DA1_RC9_PB1	IOSPUE	Input: pull up enabled	SPI #2 serial clock(output);; DAC channel #1 PWM data (output); Servo channel #9 (output); GPIO port B1 (input/output);
56	SPICS2_RC8_PB0	IOSPUE	Input: pull up enabled	SPI #2 slave CS. When it is configured as SPI slave, it is SPI #2 chip select input. When it is configured as SPI master, it is GPIO port B0 (input/output);

2 IO type suffix (4) has output drive capability of 4mA. Otherwise all other output capability is 2mA.

Pin #	Pin Name	Type	Default State	Functional Description
				Servo channel #8 (output); GPIO port B0 (input/output);
57	VSSIO_2	Power		GND for IO
58	VDDIO_2	Power		3.3V for IO supply
59	CTS1_PD2	IOPUE	Input: pull up enabled	UART #1 CTS (input); GPIO port D2 (input/output);
60	RTS1_PD3	IOPUE	Input: pull up enabled	UART #1 RTS (output); GPIO port D3 (input/output);
61	DSR1_PD4	IOPUE	Input: pull up enabled	UART #1 DSR (input); GPIO port D4 (input/output);
62	DTR1_PD5	IOPUE	Input: pull up enabled	UART #1 DTR (output); GPIO port D5 (input/output);
63	VDDC_1	power		1.8V core supply
64	VSSC_1	power		GND for core supply
65	VDDIO_6	Power		3.3V for IO supply
66	LCLK_LCS_CPCLK_PE0	IOPUE	Input: pull up enabled	Scan type LCD pixel data clock (output); Controller type LCD chip select (output); Secondary camera data clock (input); GPIO port E0 (input/output);
67	LDRDY_LRS_CMCLK_PE3	IOSPUE	Input: pull up enabled	Scan type LCD data ready (output); Controller type LCD RS select (output); Secondary camera master clock (output); GPIO port E3 (input/output);
68	LHS_LWE_CVS_PE1	IOSPUE	Input: pull up enabled	Scan type LCD HSYNC (output); Controller type LCD write enable (output); Secondary camera VSYNC (input); GPIO port E1 (input/output);
69	LVS_LRD_CHS_PE2	IOSPUE	Input: pull up enabled	Scan type LCD VSYNC (output); Controller type LCD read enable (output); Secondary camera HSYNC (input); GPIO port E2 (input/output);
70	LD0_CD0_PE4	IOPUE	Input: pull up enabled	LCD data line D0 (output); Secondary camera data line D0 (input); GPIO port E4 (input/output);

Pin #	Pin Name	Type	Default State	Functional Description
71	LD1_CD1_PE5	IOPUE	Input: pull up enabled	LCD data line D1 (output); Secondary camera data line D1 (input); GPIO port E5 (input/output);
72	LD2_CD2_PE6	IOPUE	Input: pull up enabled	LCD data line D2 (output); Secondary camera data line D2 (input); GPIO port E6 (input/output);
73	LD3_CD3_PE7	IOPUE	Input: pull up enabled	LCD data line D3 (output); Secondary camera data line D3 (input); GPIO port E7 (input/output);
74	LD4_CD4_PF0	IOPUE	Input: pull up enabled	LCD data line D4 (output); Secondary camera data line D4 (input); GPIO port F0 (input/output);
75	LD5_CD5_PF1	IOPUE	Input: pull up enabled	LCD data line D5 (output); Secondary camera data line D5 (input); GPIO port F1 (input/output);
76	LD6_CD6_PF2	IOPUE	Input: pull up enabled	LCD data line D6 (output); Secondary camera data line D6 (input); GPIO port F2 (input/output);
77	LD7_CD7_PF3	IOPUE	Input: pull up enabled	LCD data line D7 (output); Secondary camera data line D7 (input); GPIO port F3 (input/output);
78	LD8_PF4	IOSPUE	Input: pull up enabled	LCD data line D8 (output); GPIO port F4 (input/output);
79	LD9_PF5	IOSPUE	Input: pull up enabled	LCD data line D9 (output); GPIO port F5 (input/output);
80	LD10_PF6	IOSPUE	Input: pull up enabled	LCD data line D10 (output); GPIO port F6 (input/output);
81	LD11_PF7	IOSPUE	Input: pull up enabled	LCD data line D11 (output); GPIO port F7 (input/output);
82	LD12_SPICS2_PG5	IOSPUE	Input: pull up enabled	LCD data line D12 (output); Secondary SPI #2 slave CS. When it is configured as SPI slave, it is SPI #2 chip select input. When it is configured as SPI master, it is GPIO port B0 (input/output); GPIO port G5 (input/output);

Pin #	Pin Name	Type	Default State	Functional Description
83	LD13_SPICK2_PG6	IOSPUE	Input: pull up enabled	LCD data line D13 (output); Secondary SPI #2 serial clock (master output slave input); GPIO port G6 (input/output);
84	VSSIO_1	Power		GND for IO
85	VDDIO_1	Power		3.3V for IO supply
86	LD14_SPIMISO2_PG7	IOSPUE	Input: pull up enabled	LCD data line D14 (output); Secondary SPI #2 MISO data (master input slave output); GPIO port G7 (input/output);
87	LD15_SPIMOSI2_PJ0	IOSPUE	Input: pull up enabled	LCD data line D15 (output); Secondary SPI #2 MOSI data (master output slave input); GPIO port J0 (input/output);
88	RX1_PD0	IOPUE	Input: pull up enabled	UART #1 RX (input); GPIO port D0 (input/output);
89	TX1_PD1	IOPUE	Input: pull up enabled	UART #1 TX (output); GPIO port D0 (input/output);
90	SPICK1_PA5	IOSPUE	Input: pull up enabled	SPI #1 serial clock (master output slave input); GPIO port A5 (input/output);
91	SPIMOSI1_PA7	IOSPUE	Input: pull up enabled	SPI #1 MOSI data (master output slave input); GPIO port A7 (input/output);
92	SPIMISO1_PA6	IOSPUE	Input: pull up enabled	SPI #1 MISO data (master input slave output); GPIO port A6 (input/output);
93	SPICS1_PA4	IOSPUE	Input: pull up enabled	SPI #1 slave CS. When it is configured as SPI slave, it is SPI #1 chip select input. When it is configured as SPI master, it is GPIO port A4 (input/output); Internal SYS_CLK output; GPIO port A4 (input/output);
94	RC7_PC7	IOSPUE	Input: pull up enabled	Servo channel #7 (output); GPIO port C7 (input/output);
95	VDDA	power		1.8V for Analog supply (keep this away from noisy supply)
96	VSSA	power		GND for Analog supply (keep this away

Pin #	Pin Name	Type	Default State	Functional Description
				from noisy ground)
97	VDD18OSC	Power		1.8V supply for 6MHz oscillator
98	OSC_PI	OSC XIN		6MHz crystal reference oscillator input
99	OSC_PO	OSC XOUT		6MHz crystal reference oscillator output
100	VSS33OSC	Power		GND for 6MHz oscillator

Electrical Characteristics

1 Recommend Operating Conditions

Description	*Symbol*	*Min*	*Typ*	*Max*	*Unit*
Core Power Supply	VDD_{CORE}	1.62	1.80	1.98	V
IO Power Supply	VDD_{IO}	3.0	3.3	3.6	V
Operating Temperature	T_{op}	-40	25	+85	°C

2 Recommend Crystal Frequency

Description	*Symbol*	*Min*	*Typ*	*Max*	*Unit*
Main Oscillator Crystal frequency	f_{OSC}	4	6	7	MHz
Real Time Clock Crystal frequency	$f32_{OSC}$		32.768		KHz

3 DC Electrical Characteristics for IO

Symbol	*Parameter*	*Condition*	*Min*	*Max*
V_{IL}	Input Low Voltage	CMOS input, LVTTL input	-0.3V	0.8V
V_{IH}	Input High Voltage		2.0V	5.5V
V_{IL}	Input Low Voltage	CMOS Schmitt input, LVTTL Schmitt input	-0.3V	0.8V
V_{IH}	Input High Voltage		2.0V	5.5V
⎍	Hysteresis		346mV	464mV
I_{IL}	Input Low Current	V_{in} = VSS	-10uA	10uA
I_{IH}	Input High Current	V_{in} = VDDIO	-10uA	10uA
V_{OL}	Output Low Voltage	I_{OL} = -2, -4 mA	0.0V	0.4V
V_{OH}	Output High Voltage	I_{OH} = 2, 4 mA	2.4V	3.6V
	Pull Up Resistor		68kΩ	119kΩ
	Pull Down Resistor		30kΩ	81kΩ

4 Absolute Maximum Ratings

Description	Value	Unit	Note
Power Supply Voltage for group VDD1 and VDD2	-0.3 to 4.9	V	1
Power Supply Voltage for group VDD3,VDD4,VDD5, and VDD6	-0.3 to 2.7	V	2
Storage Temperature	-50 to +125	°C	
ESD: HBM	2K	V	3
ESD: CDM	150	V	

Note:

1. Refer to power supply voltage group VDD1 and VDD2 in section “Power Supply Group”.
2. Refer to power supply voltage group VDD3, VDD4, VDD5, and VDD6 in in section “Power Supply Group”.
3. All pins has ESD protection that meet ESD 2KV HBM (Human Body Model) requirement except oscillator pins (pin 3,4,96,97,98,99,).

This Device can be damaged by ESD. SPEEDPIXEL recommends that all integrated circuits be handled with appropriate precautions.

5 Power Consumption

(VDD_{CORE} = 1.8V, VDD_{IO} = 3.3V, TA = 25°C, System Clock Frequency = 64MHz, unless otherwise specified)

Description	*Symbol*	*Min*	*Typ*	*Max*	*Unit*
Static Power	p_{STATIC}		80		uW
Dynamic Power[3]	$p_{DYNAMIC}$		39		mW

3 Benchmark condition: Video Stream Encoding in 15FPS color QVGA. The actual figure subject to change due to system parasitics

6 Power Supply Groups

Table below is grouping of power supply on the IC assembly. The VDD pins or GND pins that connected internally to the IC assembly are grouped together. Pins that having the same voltage level can be connected at system board level.

Group	Pin Number	Pin Name	Description
VDD1	18,36,49,58,65,85	VDD*	3.3V **VDD** supply for IO
VDD2	1	VDD33OSC	3.3V **VDD** supply for oscillators
VDD3	20, 63	VDDC_1, VDDC2	1.8V **VDD** supply for core logic
VDD4	5	VDD18OSC32	1.8V **VDD** supply for 32K oscillators
VDD5	97	VDD18OSC	1.8V **VDD** supply for 6M oscillators
VDD6	95	VDDA	1.8V **VDD** supply for PLL
GND1	6, 19, 37, 48, 57, 64, 84	VSS*	**VSS** for IO, core, and 32K oscillator
GND2	2	VSS33OSC32	**VSS** for 32K oscillator (3.3V part)
GND3	96	VSSA	**VSS** for PLL and 6M oscillator (1.8V part)
GND4	100	VSS33OSC	**VSS** for 6M oscillator (3.3V part)

Table 2: IC Assembly Power Supply Groups

4 AC Electrical Characteristics

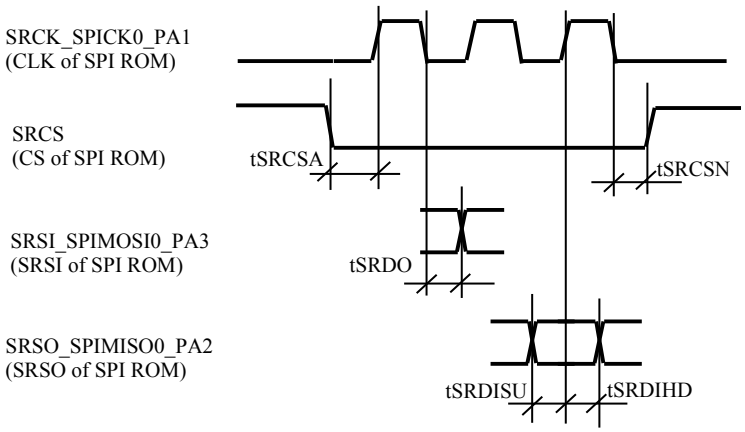
(Measurement taken at operating range in table 3, unless otherwise specified)

Description	*Symbol*	*Min*	*Typ*	*Max*	*Unit*
Core Power Supply	VDD_{CORE}	1.62	1.80	1.98	V
IO Power Supply	VDD_{IO}	3.0	3.3	3.6	V
Operating Temperature	T_{op}	-40	25	+85	°C

Table 3: Operating Condition Range for AC Parameters

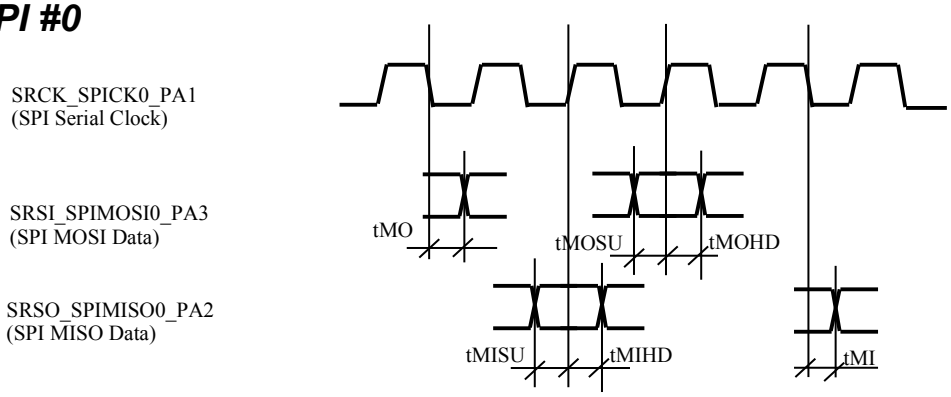
6.1 Hardware Serial SPI PROM code Loader

Application program can be kept in the external SPI programmable ROM. Pins {BOOT1,BOOT0} has to be 11 in order to use this feature.The chip select of the SPI ROM is connected to pin SRCS. The other SPI signal will be shared with the SPI #0. During power up reset the embedded loader will upload the 64KByte content from the external SPI ROM into the embedded SRAM.



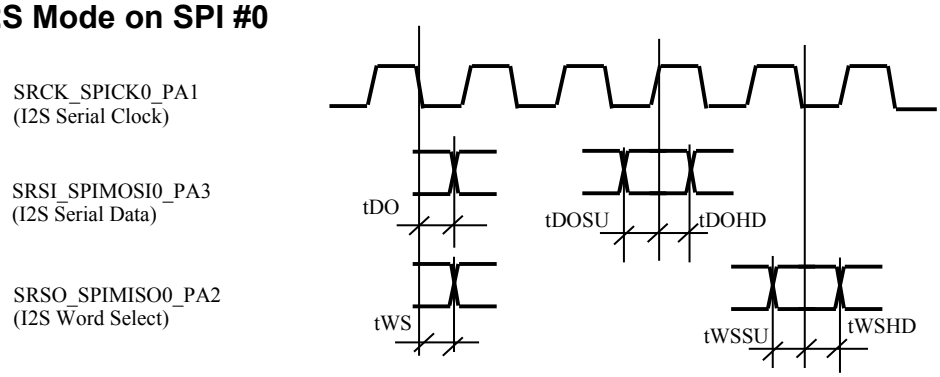
Timing Symbol	*Parameters*	*Min*	*Typ*	*Max*	*Unit*
tSRCSA	Chip select assertion before first serial clock positive edge	30.0	-	-	ns
tSRCSN	Chip select negation after last serial clock negative edge	30.0	-	-	ns
tSRDO	Clock to output data	-	-	7.5	ns
tSRDISU	Input data setup	10.0	-	-	ns
tSRDIHD	Input data hold	3.0	-	-	ns

6.2 SPI #0



Mode	*Timin Symbol*	*Parameters*	*Min*	*Typ*	*Max*	*Unit*
Master	tMO	Clock to MOSI Output Data	0	-	7.0	ns
	tMISU	MISO Input Data Setup	9.0	-	-	ns
	tMIHD	MISO Input Data Hold	0	-	-	ns
Slave	tMI	Clock to MISO Output Data	0	-	14.5	ns
	tMOSU	MOSI Input Data Setup	4.0	-	-	ns
	tMOHD	MOSI Input Data Hold	0	-	-	ns

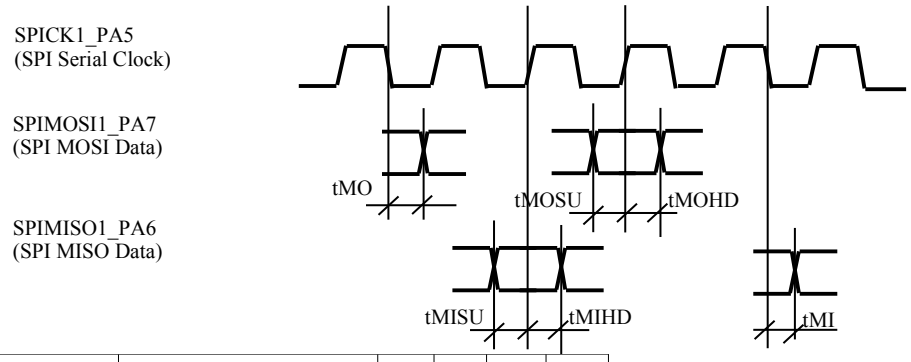
6.3 I2S Mode on SPI #0



Note: Register SPICR_0.ICK is cleared to make data change at serial clock falling edge

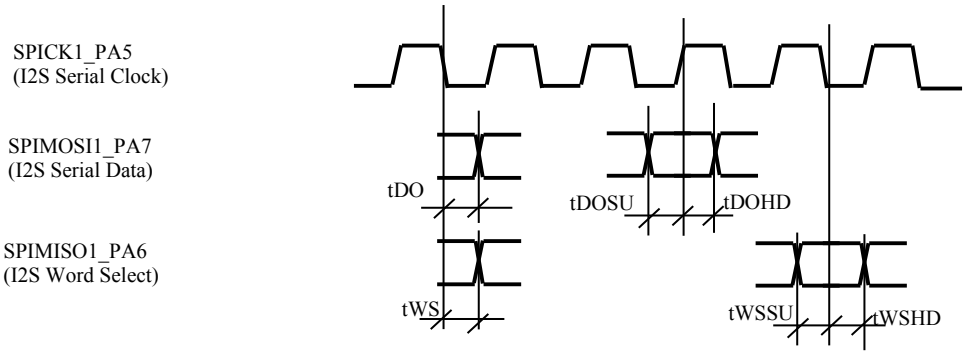
Mode	*Timing Symbol*	*Parameters*	*Min*	*Typ*	*Max*	*Unit*
Master	tDO	Clock to Serial Data	0	-	8.0	ns
	tWS	Clock to Word Select	0	-	8.0	ns
Slave	tDOSU	Serial Data Setup	0	-	-	ns
	tDOHD	Serial Data Hold	3.0	-	-	ns
	tWSSU	WS Setup	0	-	-	ns
	tWSHD	WS Hold	4.3	-	-	ns

6.4 SPI #1



Mode	*Timin Symbol*	*Parameters*	*Min*	*Typ*	*Max*	*Unit*
Master	tMO	Clock to MOSI Output Data	0	-	7.0	ns
	tMISU	MISO Input Data Setup	9.0	-	-	ns
	tMIHD	MISO Input Data Hold	0	-	-	ns
Slave	tMI	Clock to MISO Output Data	-	-	14.5	ns
	tMOSU	MOSI Input Data Setup	4.0	-	-	ns
	tMOHD	MOSI Input Data Hold	0	-	-	ns

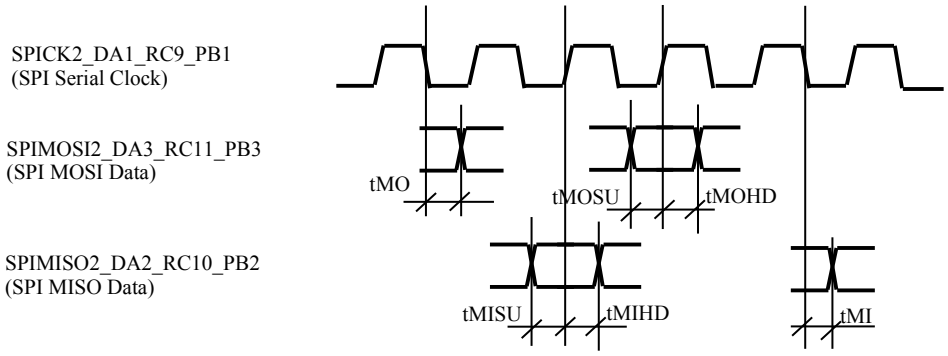
6.5 I2S Mode on SPI #1



Note: SPICR_1.ICK is cleared to make data change at serial clock falling edge

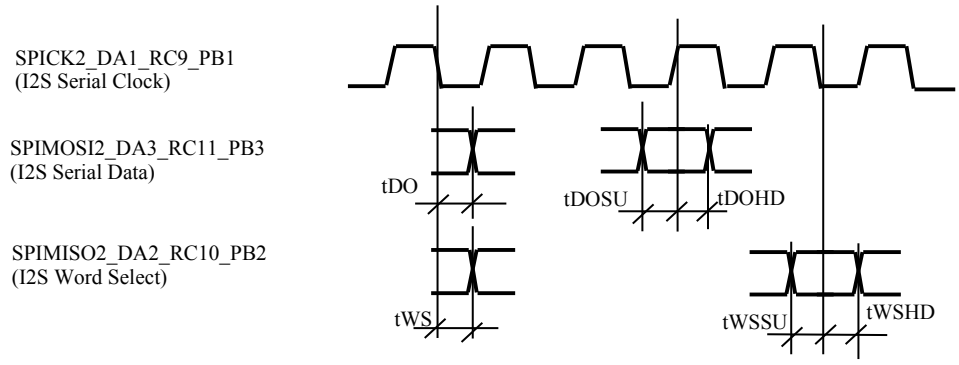
Mode	*Timing Symbol*	*Parameters*	*Min*	*Typ*	*Max*	*Unit*
Master	tDO	Clock to Serial Data	0	-	7.8	ns
	tWS	Clock to Word Select	0	-	6.8	ns
Slave	tDOSU	Serial Data Setup	0	-	-	ns
	tDOHD	Serial Data Hold	3.0	-	-	ns
	tWSSU	WS Setup	0	-	-	ns
	tWSHD	WS Hold	4.0	-	-	ns

6.6 SPI #2



Mode	*Timin Symbol*	*Parameters*	*Min*	*Typ*	*Max*	*Unit*
Master	tMO	Clock to MOSI Output Data	0	-	7.74	ns
	tMISU	MISO Input Data Setup	9.0	-	-	ns
	tMIHD	MISO Input Data Hold	0	-	-	ns
Slave	tMI	Clock to MISO Output Data	-	-	14.5	ns
	tMOSU	MOSI Input Data Setup	4.0	-	-	ns
	tMOHD	MOSI Input Data Hold	0	-	-	ns

6.7 I2S Mode on SPI #2

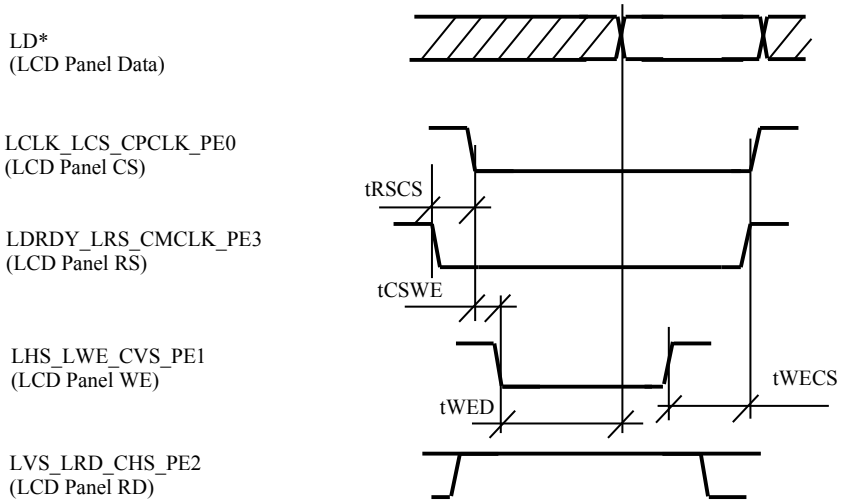


Note: SPICR_2.ICK=0 to output data and WS at serial clock falling edge

Mode	*Timing Symbol*	*Parameters*	*Min*	*Typ*	*Max*	*unit*
Master	tDO	Clock to Serial Data	0	-	8.0	ns
	tWS	Clock to Word Select	0	-	6.4	ns
Slave	tDOSU	Serial Data Setup	0	-	-	ns
	tDOHD	Serial Data Hold	3.0	-	-	ns
	tWSSU	WS Setup	0	-	-	ns
	tWSHD	WS Hold	4.0	-	-	ns

6.8 Controller Type LCM 8080 Parellel Interface

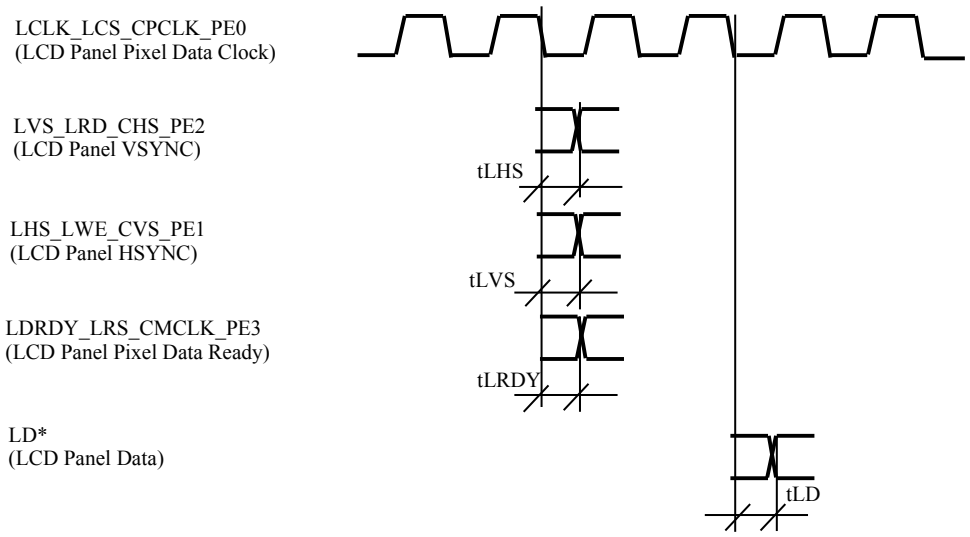
6.8.1 LCM Write



Timing Symbol	*Parameters*	*Min*	*Typ*	*Max*	*Unit*
tRSCS	RS assert (fall) to CS assert (fall)	-	1T[4]	-	ns
tCSWE	CS assert (fall) to WE assert (fall)	-	-	0.7	ns
tWED	WE assert (fall) to data ready	-	-	8.7	ns
tWECS	WE negate (rise) to CS negate (rise)	-	1T	-	ns

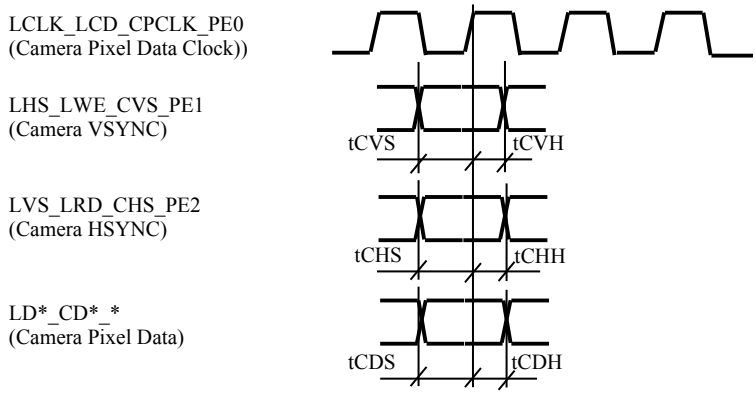
4 T=1 system clock cycle

6.9 Scan Type LCM Interface



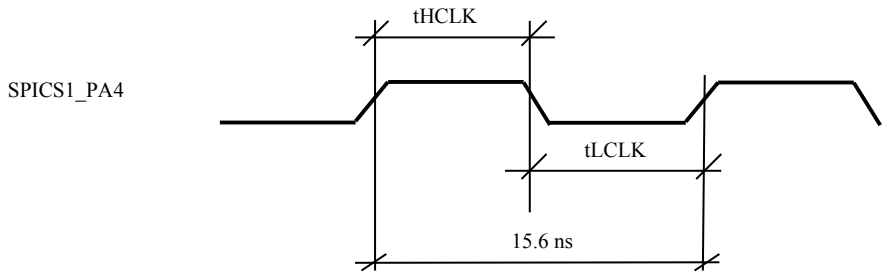
Timing Symbol	*Parameters*	*Min*	*Typ*	*Max*	*unit*
tLHS	Pixel Data Clock fall to HSYNC	0	-	3.8	ns
tLVS	Pixel Data Clock fall to VSYNC	0	-	3.6	ns
tLRDY	Pixel Data Clock fall to Data Ready	-0.2	-	1.9	ns
tLD	Pixel Data Clock fall to Pixel Data	0	-	7.4	ns

6.10 CMOS Image Sensor Interface



Timing Symbol	*Description*	*Min*	*Typ*	*Max*	*unit*
tCDS	Data Setup	9.0	-	-	
tCDH	Data Hold	1.0	-	-	
tCHS	HSYNC Setup	9.0	-	-	ns
tCHH	HSYNC Hold	1.0	-	-	ns
tCVS	VSYNC Setup	9.0	-	-	ns
tCVH	VSYNC Hold	1.0	-	-	ns

6.11 SYS_CLK output at pin SPICS1_PA4

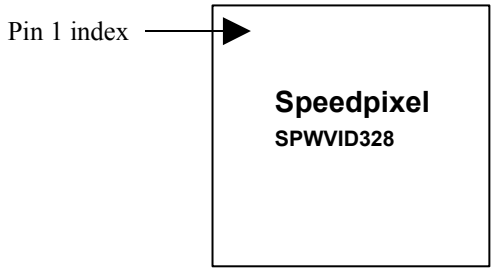


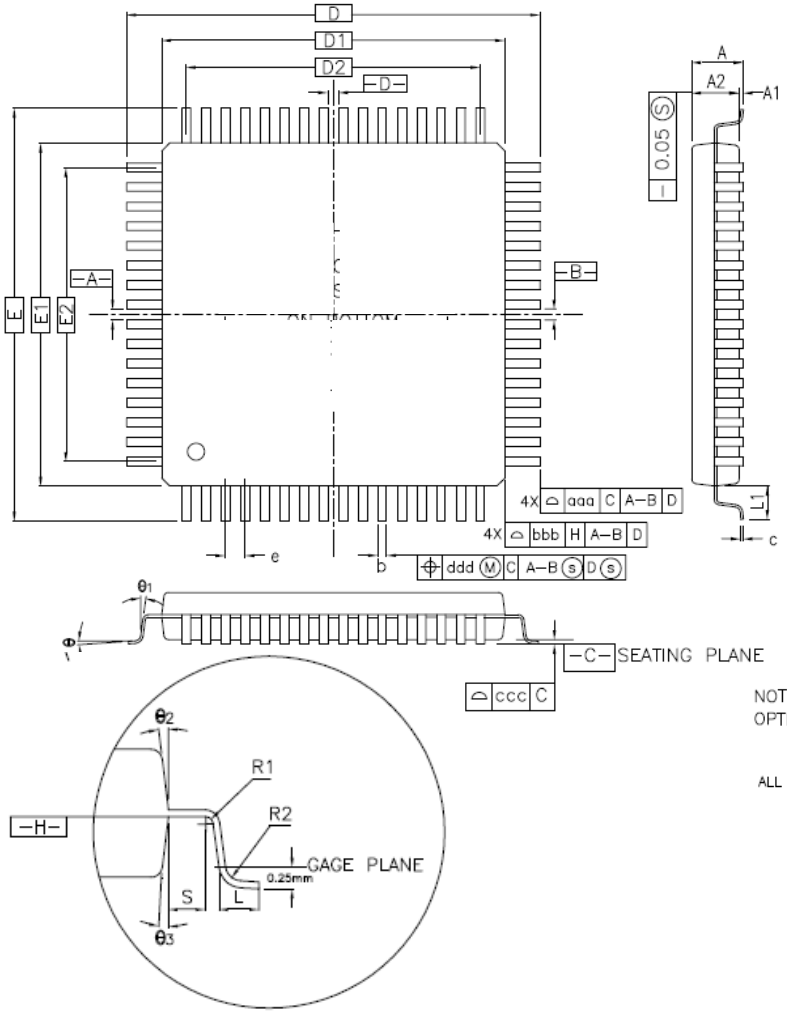
Note: SYS_CLK frequency at 64MHz

Timing Symbol	*Description*	*Min*	*Typ*	*Max*	*unit*
tHCLK	Clock High Pulse Wdith	5.1	7.0	7.0	ns
tLCLK	Clock Low Pulse Wdith	8.6	8.6	10.5	ns

Packaging Information

package type: LQFP 100L
body size: 14 x 14 x 1.4 mm





CONTROL DIMENSIONS ARE IN MM.

SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	—	—	1.60	—	—	0.063
A_1	0.05	—	0.15	0.002	—	0.006
A_2	1.35	1.40	1.45	0.053	0.055	0.057
D	16.00 BSC.			0.630 BSC.		
D_1	14.00 BSC.			0.551 BSC.		
E	16.00 BSC.			0.630 BSC.		
E_1	14.00 BSC.			0.551 BSC.		
R_2	0.08	—	0.20	0.003	—	0.008
R_1	0.08	—	—	0.003	—	—
θ	0°	3.5°	7°	0°	3.5°	7°
θ_1	0°	—	—	0°	—	—
θ_2	11°	12°	13°	11°	12°	13°
θ_3	11°	12°	13°	11°	12°	13°
c	0.09	—	0.20	0.004	—	0.008
L	0.45	0.60	0.75	0.018	0.024	0.030
L_1	1.00 REF			0.039 REF		
S	0.20	—	—	0.008	—	—

NOTE:
OPTION: SQUARE DOTTED LINE IS E-PAD OUTLINE SIZE DEPENDENT ON DIE ATTACH PAD

ALL DIMENSION IN MM

SYMBOL	100L					
	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
b	0.17	0.20	0.27	0.007	0.008	0.011
e	0.50 BSC.			0.020 BSC.		
D2	12.00			0.472		
E2	12.00			0.472		
)RM AND POSITION						
aaa	0.20			0.008		
bbb	0.20			0.008		
ccc	—	0.08	—	—	0.003	—
ddd	—	0.08	—	—	0.003	—

Revision History

Revision	*Remarks*
1.2	-First Release
2.0	-Revise test pins assignment
2.1	-Add more information on IO default state, IO DC characteristics
2.2	-Add Reliability Qualification: Operating Temperature Characteristic -Add Reliability Qualification: ESD class
2.3	-Re-arrange absolute maximum rating table -Rename some VSS and IO -Add ESD warning
2.4	-Add description of SYS_CLK output at pin SPICS1_PA4
2.5	-Revise max number of GPIO -Revise ESD sensitive pins

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