Elektronische Bauelemente

SPW3842S

High Performance Current Mode Controlers

RoHS Compliant Product
A suffix of "-C" specifies halogen and lead-free

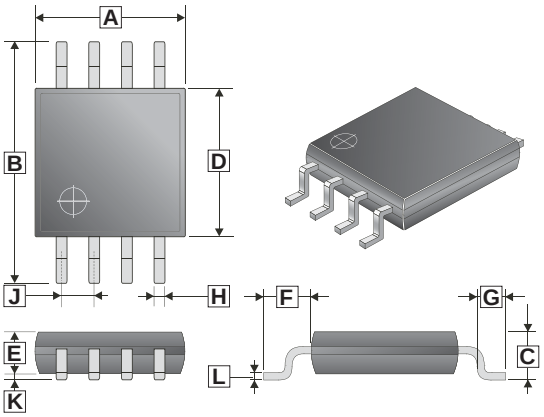
DESCRIPTION

The SPW3842S is high performance fixed frequency current mode controllers.
This is specifically designed for Off-Line and DC-DC converter applications offering the designer a cost-effective solution with minimal external components.
These intergrater circuits feature a trimmed oscillator for precise duty cycle control.
A temperature compensated reference, high gain Error amplifier, current sensing comparator, and a high current totem pole output ideally suited for driving a power MOSFET. Also included are protective features consisting of input and reference undervoltage lockouts each with hysteresis, cycle-by-cycle current limiting, programmable output deadtime, and latch for single pulse metering.

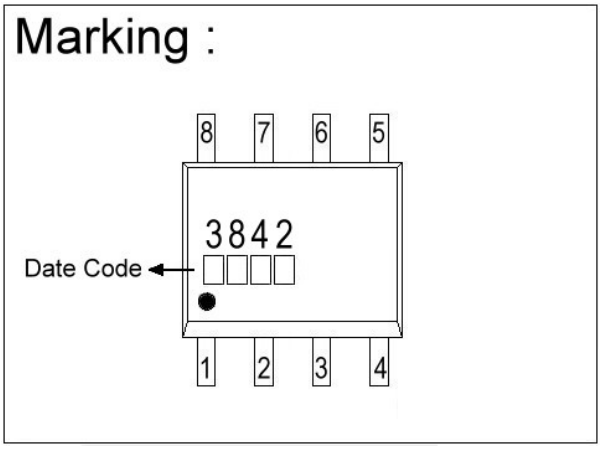
SOP-8

FEATURES

- Trimmed Oscillator for Precise Frequency Control
- Oscillator Frequency Guaranteed at 250 KHz
- Current Mode Operation to 500 KHz
- Automatic Feed Forward Compensation
- Latching PWM for Cycle-By-Cycle Current Limiting
- Internally Trimmed Reference with Undervoltage Lockout
- High Current Totem Pole Output
- Undervoltage Lockout with Hysteresis
- Low Startup and Operating Current



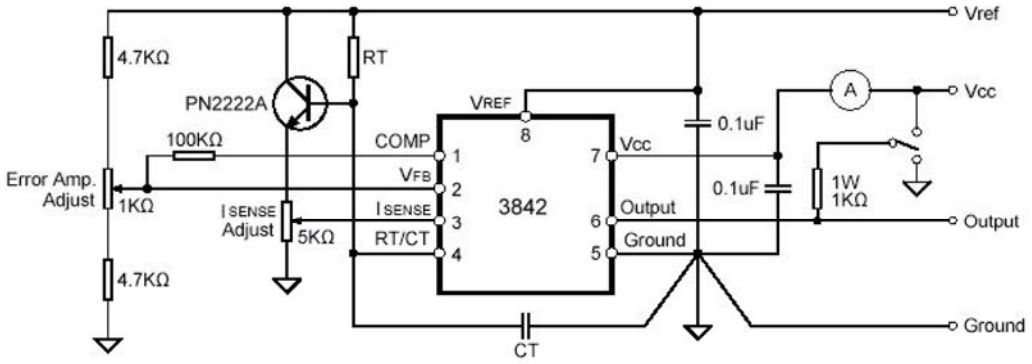
MARKING :



REF.	Millimeter		REF.	Millimeter	
	Min.	Max.		Min.	Max.
A	4.80	5.00	G	0.40	0.90
B	5.80	6.20	H	0.35	0.49
C	1.35	1.75	J	1.27 TYP.	
D	3.80	4.00	K	0.10	0.25
E	1.25	1.50	L	0.19	0.25

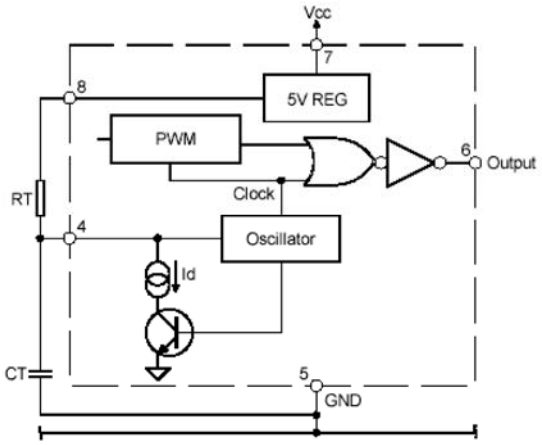
APPLICATION INFORMATION

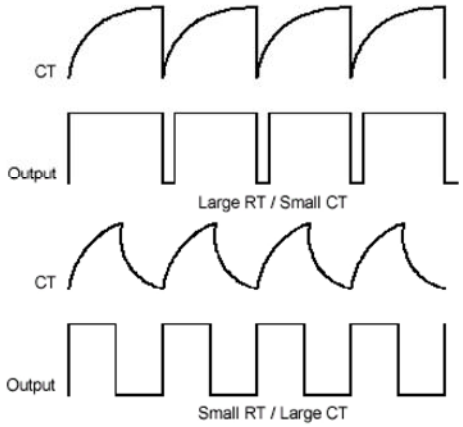
Open Loop Test Circuit



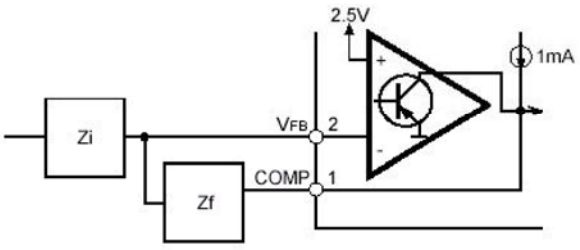
High peak currents associated with capacitive loads necessitate careful grounding techniques. Timing and bypass capacitors should be connected close to pin5 in a single point ground. The transistor and 5KΩ potentiometerare used to samplethe oscillator waveform and apply an adjustable ramp to pin3.

Oscillator and Output Waveforms

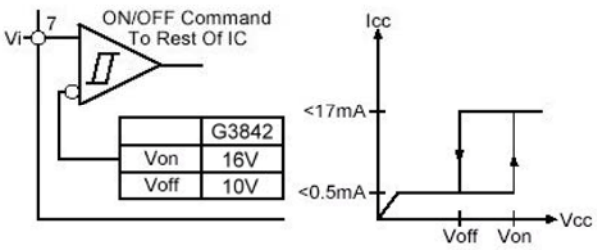




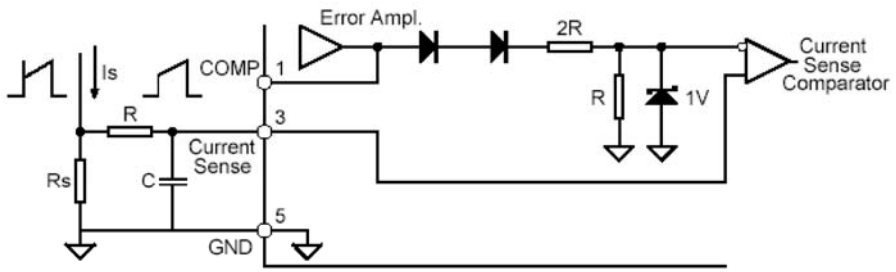
Error Amp Configuration



Under Voltage Lockout

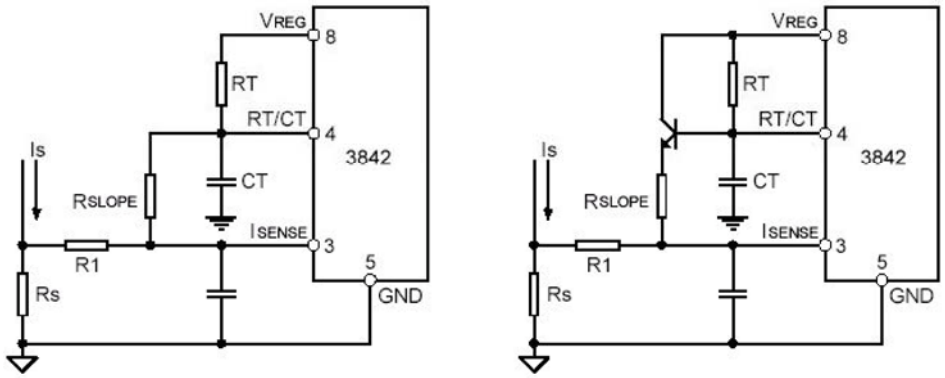


Current Sense Circuit

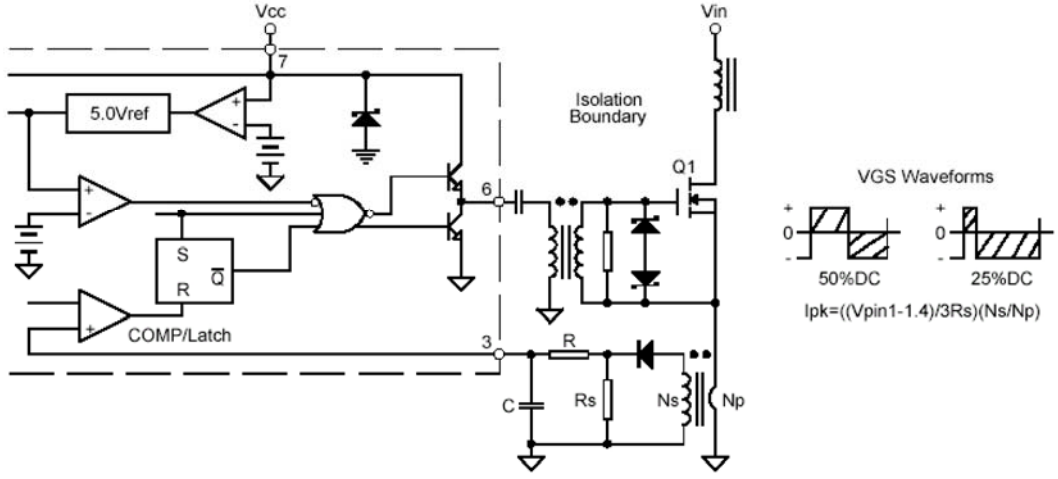


Peak current (Is) is determined by the formula
Is(max.) ≈ 1V/Rs
A small RC filter may be required to suppress switch transients.

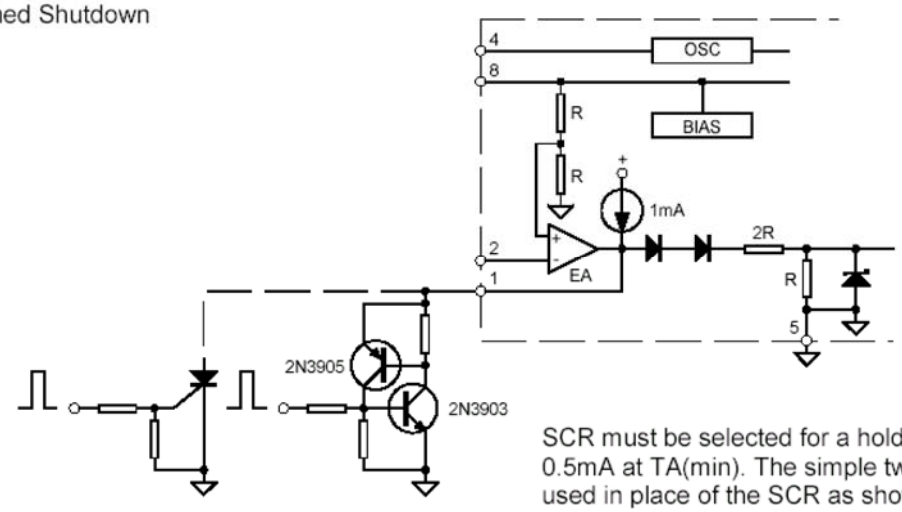
Slope Compensation Techniques



Isolated MOSFET Drive and Current Transformer Sensing

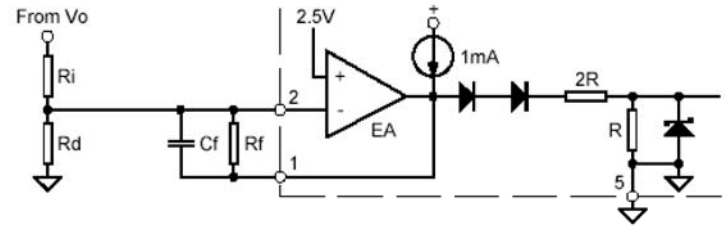


Latched Shutdown

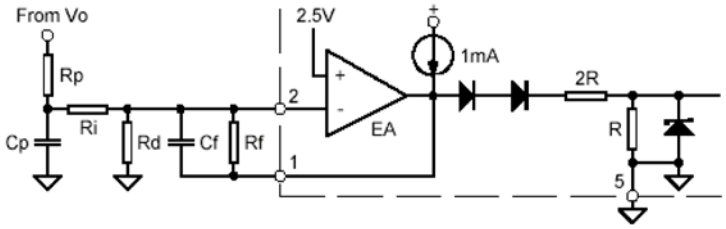


SCR must be selected for a holding current of less than 0.5mA at TA(min). The simple two transistor circuit can be used in place of the SCR as shown. All resistors are 10K.

Error Amplifier Compensation

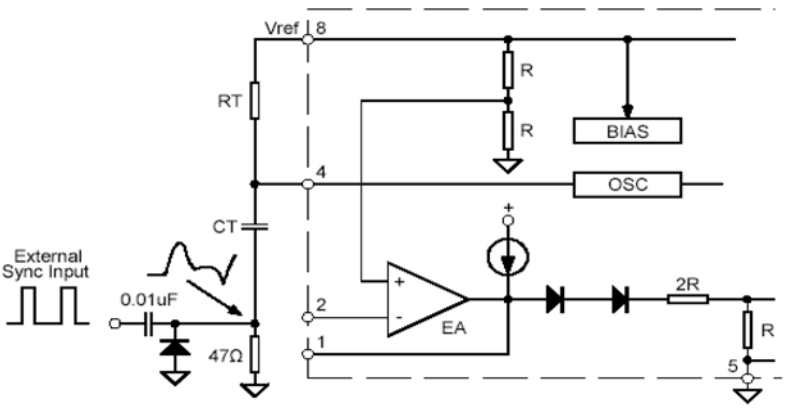


Error Amp compensation circuit for stabilizing any current-mode topology except for boost and flyback converters operating with continuous inductor current



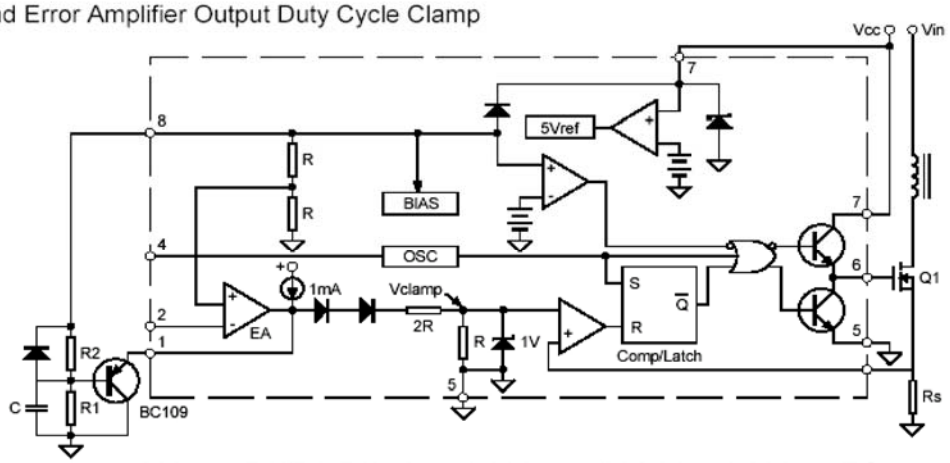
Error Amp compensation circuit for stabilizing current-mode boost and flyback topologies operating with continuous inductor current.

External Clock Synchronization



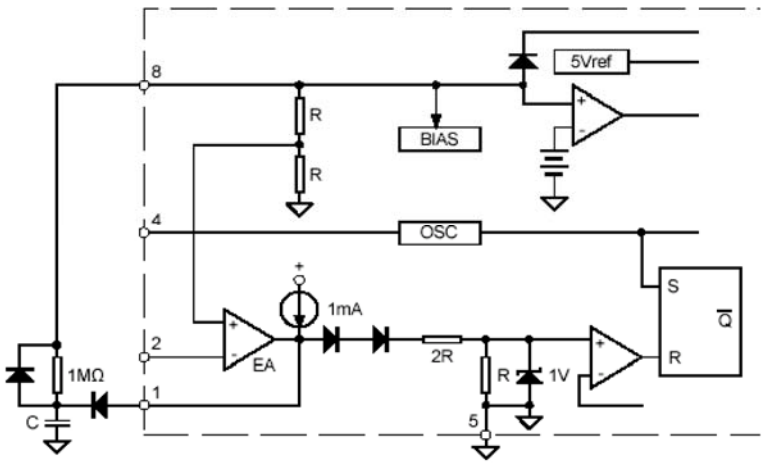
The diode clamp is required if the Sync amplitude is large enough to cause the bottom side of CT to go more than 300mV below ground

Soft-Start and Error Amplifier Output Duty Cycle Clamp

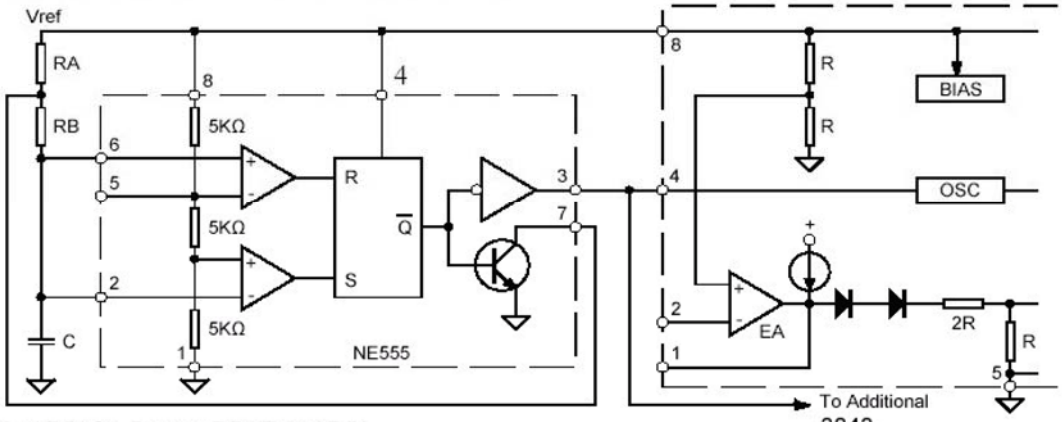


Vclamp=R1/(R1+R2) where 0<Vclamp<1V, Ipk(max)=Vclamp/RS

Soft-Start Circuit



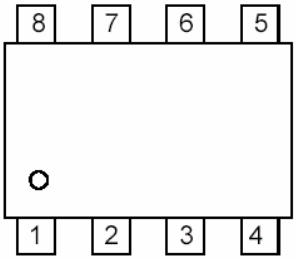
External Duty Cycle Clamp and Multi Unit Synchronization



f=1.44/((RA+2RB)C), Dmax=RB/(RA+2RB)

PIN FUNCTION DESCRIPTION

FUNCTION	PIN	DESCRIPTION
Compensation	1	This pin is the Error Amplifier output and is made available for loop compensation.
Voltage Feedback	2	This is the inverting input of the Error Amplifier. It's normally connected to the Switching power supply output through a resistor divider.
Current Sense	3	A voltage proportional to inductor current is connected to this input. The PWN uses this information to terminate the output switch conduction.
RT / CT	4	The oscillator frequency and maximum output duty cycle are programmed by connecting resistor RT to Vref and capacitor CT to ground. Operation 500 KHz is possible.
Ground	5	This pin is the combined control circuitry and power ground.
Output	6	This output directly drives the gate of a power MOSFET. Peak currents up to 1 A are sourced and sunk by this pin.
Vcc	7	This pin is the positive supply of the control IC.
Vref	8	This is the reference output. It provides charging current for capacitor CT through resistor RT.



ABSOLUTE MAXIMUM RATINGS (T_A=25 °C, unless otherwise specified)

PARAMETER	SYMBOL	VALUE	UNIT
Total power Supply and Zener current	(ICC+Iz)	30	mA
Output current, source or sink (note1)	Io	1.0	A
Output energy (capacitive load per cycle)	W	5.0	μJ
Current sense and voltage feedback inputs	Vin	-0.3 ~ 5.5	V
Error Amplifier Output Sink Current	Io	10	mA
Power Dissipation at Thermal characteristics	PD PθJA	702 178	mW °C / W
Storage Temperature Range	T_{STG}	-65 ~ 150	°C
Operating Junction Temperature	T_J	150	°C
Operating ambient Temperature	T_A	0 ~ 70	°C

ELECTRICAL CHARACTERISTICS

(0°C ≦ T_A ≦ 70 °C, V_{CC}= 15V[note 2], R_T= 10k, C_T= 3.3nF, unless otherwise specified)

CHARACTERISTICS	SYMBOL	MIN	TYP	MAX	UNIT	TEST CONDITIONS
REFERENCE SECTION						
Output Voltage	V_{REF}	4.90	5	5.1	V	T_J= 25°C, Io= 1mA
Line Regulation	Regline	-	2.0	20	mV	Vcc= 12V ~ 25V
Load Regulation	Regload	-	3.0	25	mV	Io= 1mA ~ 20mA
Temperature. Stability	T_S	-	0.2	-	mV / °C	-
Total Output Variation	V_{REF}	4.82	-	5.18	V	Line, Load, Temperature
Output Noise Voltage	Vn	-	50	-	μV	F= 10KHz ~ 10Hz, T_J= 25°C
Long Term Stability	S	-	5	-	mV	T_A=125°C, 1000Hrs
Output Short Circuit Current	ISC	-30	-85	-180	mA	-

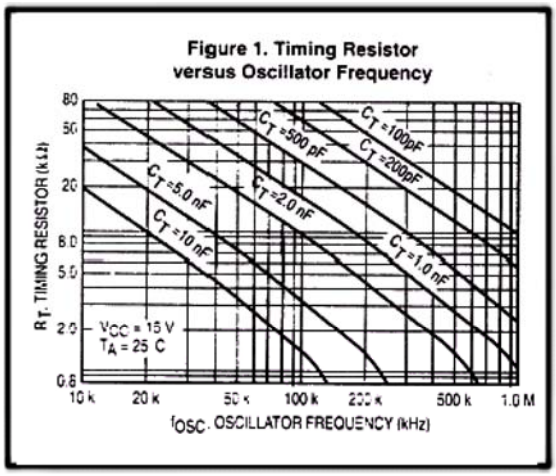
OSCILLATOR SECTION						
Frequency		49	52	55	KHz	T_J= 25°C
		48	-	56		T_A= 0°C ~ 70°C
		225	250	275		T_J= 25°C(RT= 6.2K,CT= 1.0nF)
Frequency Change with Voltage	△fosc / △V	-	0.2	1.0	%	V_{CC}=12V ~ 25V
Frequency Change with Temperature	△fosc / △T	-	0.5	-	%	T_A= 0°C ~ 70°C
Oscillator Voltage Swing (Peak to Peak)	VOSC	-	1.6	-	V	-
Discharge Current	Idischg	7.8	8.3	8.8	mA	T_J= 25°C
		7.6	-	8.8		T_A= 0°C ~ 70°C
ERROR AMPLIFIER SECTION						
Voltage Feedback Input	V_{FB}	2.42	2.50	2.58	V	V_O= 2.5V
Input Bias Current	I_{IB}	-	-0.1	-2.0	μA	V_{FB}= 5.0V
Open Loop Voltage Gain	AVOL	65	90	-	dB	V_O= 2V ~ 4V
Unity Gain Bandwidth	BW	0.7	1.0	-	MHz	T_J= 25°C
Power Supply Rejection Ratio	PSRR	60	70	-	dB	V_{CC}=12V ~ 25V
Output Sink Current	Isink	2.0	12	-	mA	V_O= 1.1V, V_{FB}= 2.7V
Output Source Current	Isource	-0.5	-1.0	-	mA	V_O= 5.0V, V_{FB}= 2.3V
Output Voltage Swing High State	V_{OH}	5.0	6.2	-	V	V_{FB}= 2.3V, R_L=15K to GND
Output Voltage Swing Low State	V_{OL}	-	0.8	1.1	V	V_{FB}= 2.7V, R_L=15K to Vref
CURRENT SENSE SECTION						
Current Sense Input Voltage gain	A_V	2.85	3.0	3.15	V / V	(Note 3, 4)
Maximum Current Sense Input Threshold	Vth	0.9	1.0	1.1	V	(Note 3)
Power Supply Rejection Ratio	PSRR	-	70	-	dB	V_{CC}= 12 ~ 25V(Note 3)
Input Bias Current	I_{IB}	-	-2	-10	μA	-
Propagation Delay	Tplh(in/out)	-	150	300	ns	Current Sense Input to Output
Output Low Voltage	V_{OL}	-	0.1	0.4	V	Isink= 20mA
		-	1.6	2.2		Isink= 200mA
Output High Level	V_{OH}	13	13.5	-	V	Isource= 20mA
		12	13.4	-		Isource= 200mA
Output Voltage with UVLO Activated	V_{OL} (UVLO)	-	0.1	1.1	V	V_{CC}= 6.0V, Isink=1.0mA
Output Voltage Rise Time	T_R	-	50	150	ns	T_J= 25°C, C_L= 1nF
Output Voltage Fall Time	T_R	-	50	150	ns	T_J= 25°C, C_L= 1nF
UNDER-VOLTAGE LOCKOUT SECTION						
Startup Threshold	Vth	14.5	16	17.5	V	-
Min. Operating Voltage After Turn-on(VCC)	Vcc(min)	8.5	10	11.5	V	-
PWM SECTION						
Maximum Duty Cycle	$DC_{(MAX)}$	94	96	-	%	-
Minimum Duty Cycle	$DC_{(MIN)}$	-	-	0	%	-
TOTAL DEVICE						
Power Startup Supply Current	I_{CC}+I_C	-	0.3	0.5	mA	V_{CC}= 14V
Power Operating Supply Current	I_{CC}+I_C	-	12	17	mA	(Note 2)
Power Supply Zener Voltage	Vz	30	36	-	V	I_{CC}= 25mA

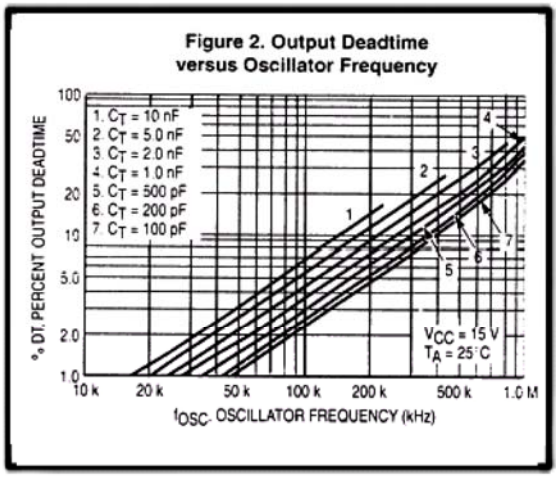
Note:

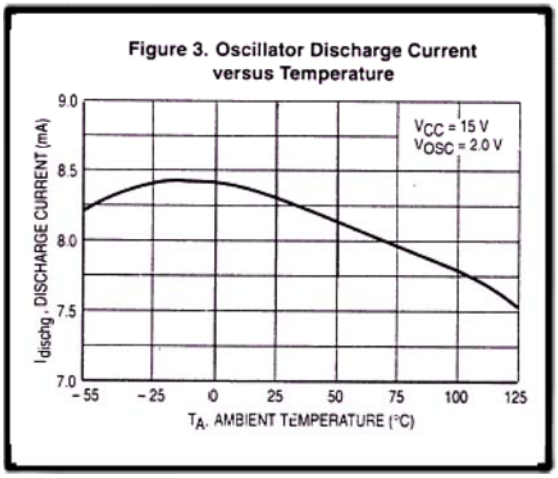
1. **Maximum Package power dissipation limits must be observed.**
2. **Adject V_{CC} above the Startup threshold before setting to 15V.**
3. **This parameter is measured at the latch trip point with V_{FB}= 0V.**
4. **Comparator gain is defined as：：**

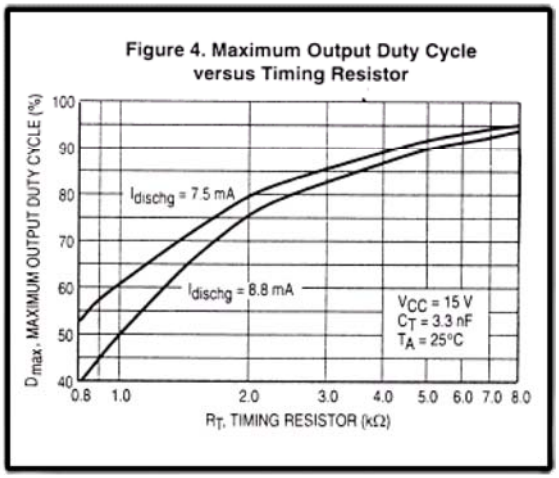
$$AV = \frac{\triangle V \text{ Output Compensation}}{\triangle V \text{ Current Sense Input}}$$

CHARACTERISTICS CURVE









CHARACTERISTICS CURVE

Figure 5. Error Amp Small Signal Transient Response

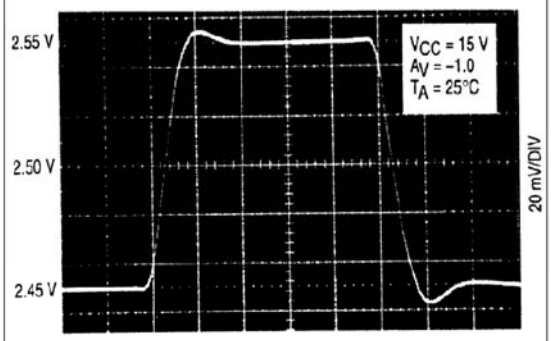


Figure 6. Error Amp Large Signal Transient Response

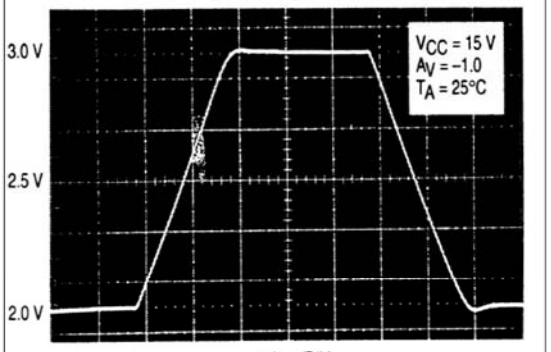


Figure 7. Error Amp Open Loop Gain and Phase versus Frequency

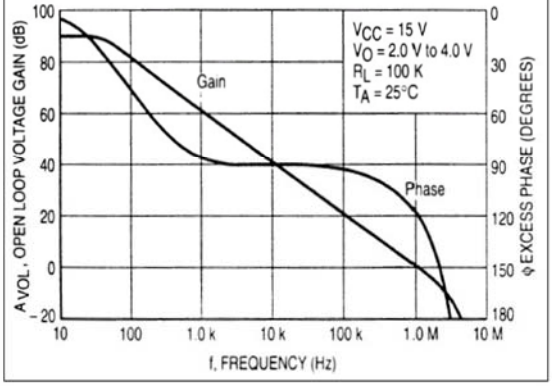


Figure 8. Current Sense Input Threshold versus Error Amp Output Voltage

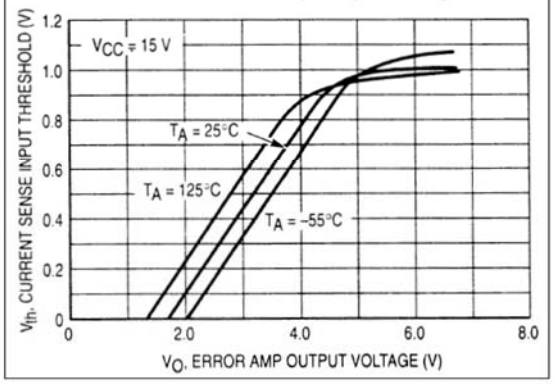


Figure 9. Reference Voltage Change versus Source Current

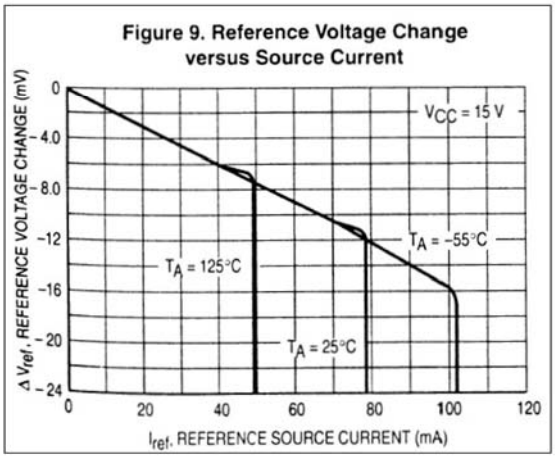
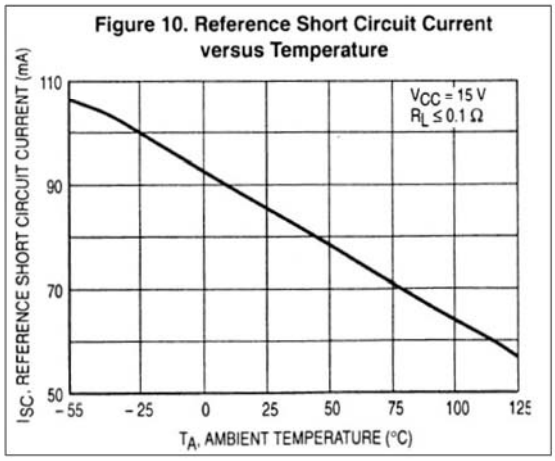


Figure 10. Reference Short Circuit Current versus Temperature



CHARACTERISTICS CURVE

Figure 11. Reference Load Regulation

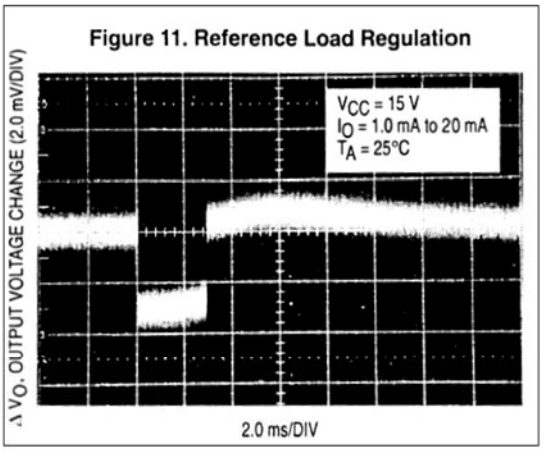


Figure 12. Reference Line Regulation

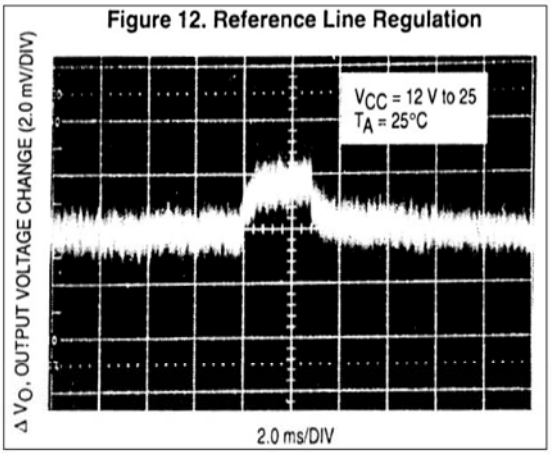


Figure 13. Output Saturation Voltage versus Load Current

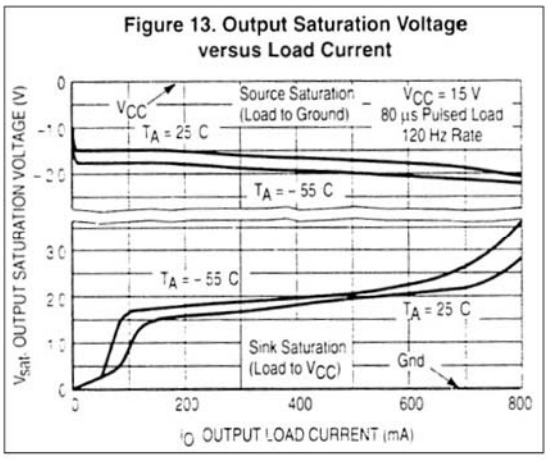


Figure 14. Output Waveform

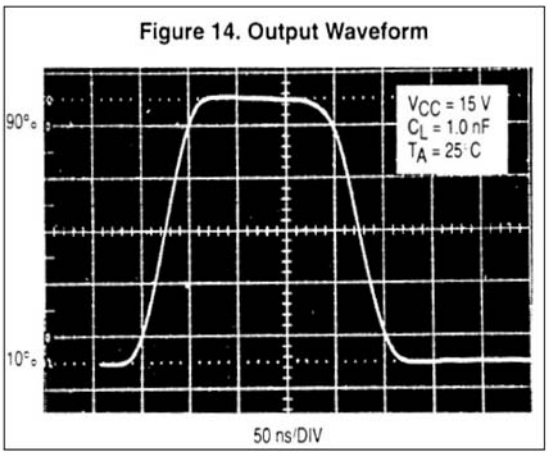


Figure 15. Output Cross Conduction

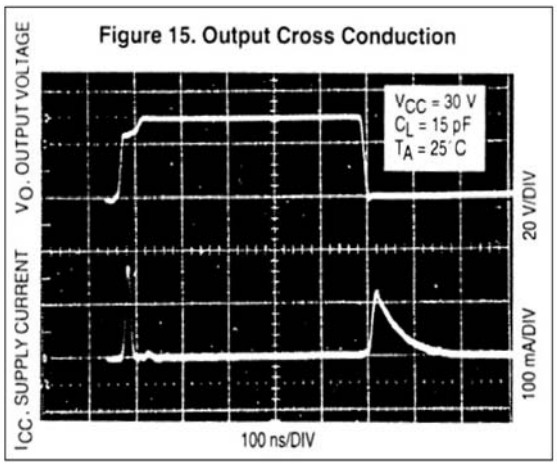


Figure 16. Supply Current versus Supply Voltage