650V N-ch Super-Junction MOSFET

Lead Free Package and Finish

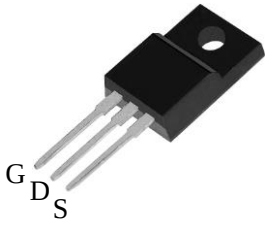
BV_{DSS}	$R_{DS(ON),typ.}$	I_D
650V	0.24Ω	14A

General Features

- New technology for high voltage device
- $R_{DS(ON),typ.}$=0.24 Ω@V_{GS}=10V
- Ultra Low Gate Charge cause lower driving requirements

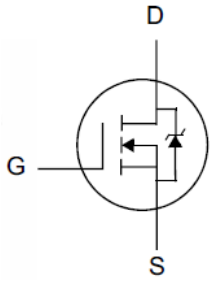
Applications

- Power factor correction（PFC）
- Uninterruptible Power Supply（UPS）
- Switched mode power supplies(SMPS)



TO-220F

Package Not to Scale



Ordering Information

Part Number	Package	Brand
SPTA65R280	TO-220F	

Absolute Maximum Ratings

T_C=25℃ unless otherwise specified

Symbol	Parameter	Value	Unit
		SPTA65R280	
V_{DSS}	Drain-to-Source Voltage	650	V
V_{GSS}	Gate-to-Source Voltage	±30	
I_D	Continuous Drain Current	14	A
I_{DM}	Pulsed Drain Current at V_{GS}=10V[1]	56	
E_{AS}	Single Pulse Avalanche Energy[2]	307	mJ
P_D	Power Dissipation	25	W
dv/dt	Drain Source voltage slope, VDS≤480V	50	V/ns
dv/dt	Reverse diode dv/dt，VDS≤480 V,ISD<ID	15	V/ns
T_L	Soldering Temperature Distance of 1.6mm from case for 10 seconds	300	℃
T_J& T_{STG}	Operating and Storage Temperature Range	-55 to 150	

Caution: Stresses greater than those listed in the "Absolute Maximum Ratings" may cause permanent damage to the device.

Thermal Characteristics

Symbol	Parameter	Max. Value	Unit
		SPTA65R280	
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	5.0	℃/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	100	

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Electrical Characteristics

OFF Characteristics

T_J =25℃ unless otherwise specified

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	650	--	--	V	V_{GS}=0V, I_D=250uA
I_{DSS}	Drain-to-Source Leakage Current	--	--	1	uA	V_{DS}=650V, V_{GS}=0V
		--	--	100		V_{DS}=650V, V_{GS}=0V, T_J =125℃
I_{GSS}	Gate-to-Source Leakage Current	--	--	+100	nA	V_{GS}=+20V, V_{DS}=0V
		--	--	-100		V_{GS}=-20V, V_{DS}=0V

ON Characteristics

T_J =25℃ unless otherwise specified

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
$R_{DS(ON)}$	Static Drain-to-Source On-Resistance[3]	--	0.24	0.28	Ω	V_{GS}=10V, I_D=7.0A
$V_{GS(TH)}$	Gate Threshold Voltage	2.0	--	4.0	V	V_{DS}=V_{GS}, I_D=250uA

Dynamic Characteristics

Essentially independent of operating temperature

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
C_{iss}	Input Capacitance	--	920	--	pF	V_{GS}=0V, V_{DS}=100V, f=1.0MH_Z
C_{rss}	Reverse Transfer Capacitance	--	1.0	--		
C_{oss}	Output Capacitance	--	41	--		
Q_g	Total Gate Charge	--	26	--	nC	V_{DD}=520V, I_D=14A, V_{GS}=0 to 10V
Q_{gs}	Gate-to-Source Charge	--	7.2	--		
Q_{gd}	Gate-to-Drain (Miller) Charge	--	12	--		

Resistive Switching Characteristics

Essentially independent of operating temperature

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
$t_{d(ON)}$	Turn-on Delay Time	--	19	--	ns	V_{DD}=325V, I_D=14A, V_{GS}=10V Rg=24Ω
t_{rise}	Rise Time	--	44	--		
$t_{d(OFF)}$	Turn-Off Delay Time	--	68	--		
t_{fall}	Fall Time	--	36	--		

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Source-Drain Body Diode Characteristics

T_J=25℃ unless otherwise specified

Symbol	Parameter	Min	Typ.	Max.	Unit	Test Conditions
I_{SD}	Continuous Source Current	--	--	14	A	Maximum Ratings
I_{SM}	Pulsed Source Current	--	--	56		
V_{SD}	Diode Forward Voltage	--	--	1.4	V	I_S=14A, V_{GS}=0V
t_{rr}	Reverse Recovery Time	--	266	--	ns	I_F= 14A, di/dt =100A/μs
Q_{rr}	Reverse Recovery Charge	--	3.4	--	uC	

Note:

[1] Repetitive Rating: Pulse width limited by maximum junction temperature
[2] Tj=25℃,VDD=100V, RG=25Ω, L=79mH
[3] Pulse Test: Pulse width ≤ 300us, Duty Cycle≤ 2%

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Typical Characteristics

图 1. 输出特性

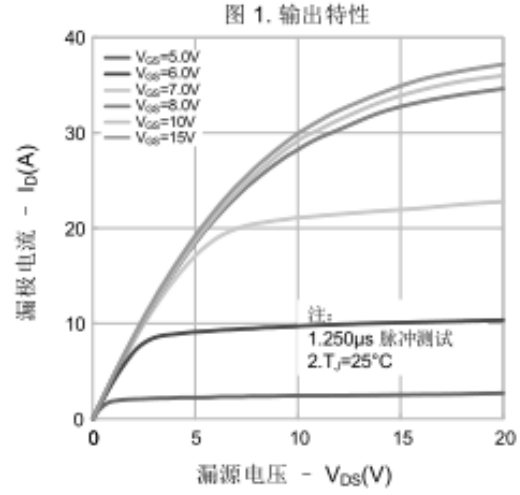

图 2. 输出特性

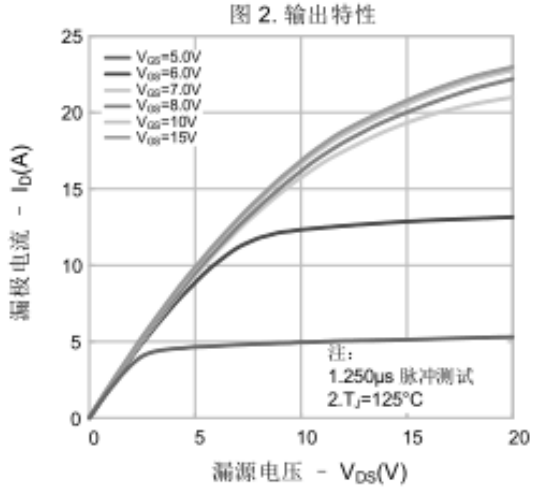

图 3. 传输特性

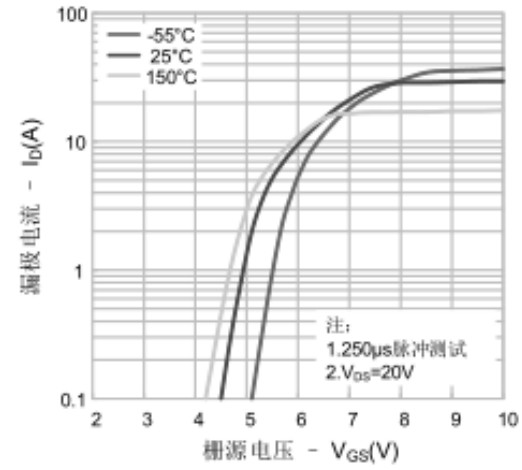

图 4. 导通电阻 vs. 漏极电流

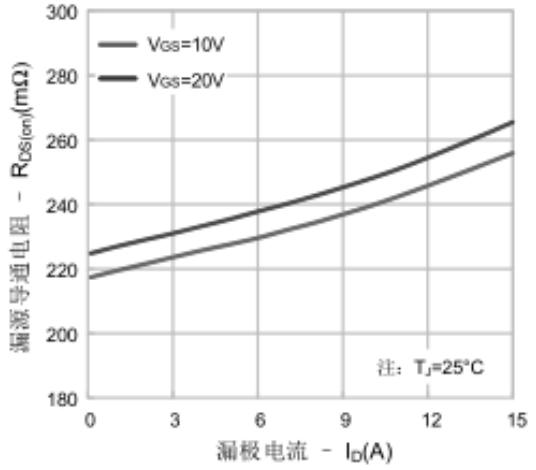

图 5. 导通电阻 vs. 漏极电流

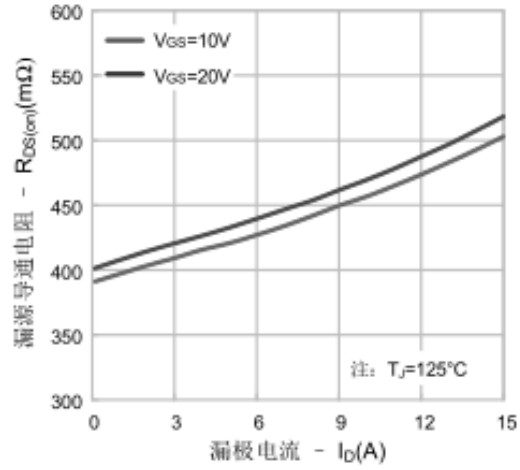

图 6. 导通电阻 vs. 栅源电压

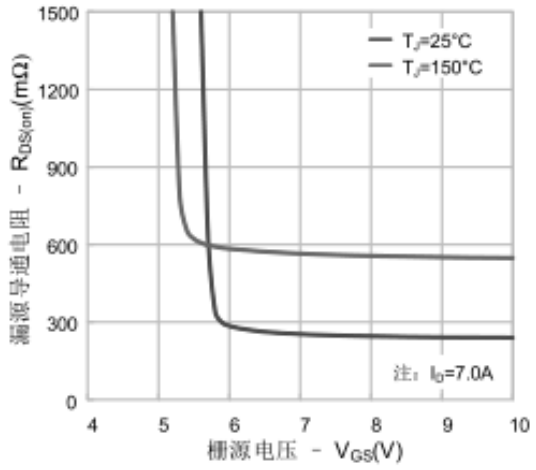

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图 7. 开启电压 vs. 温度特性

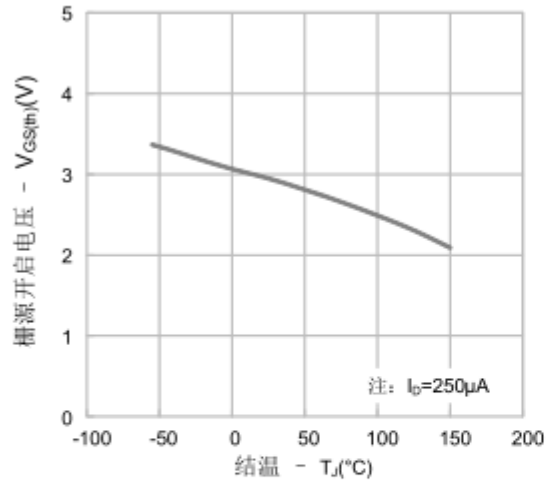

图 8. 体二极管正向压降 vs. 源极电流、温度

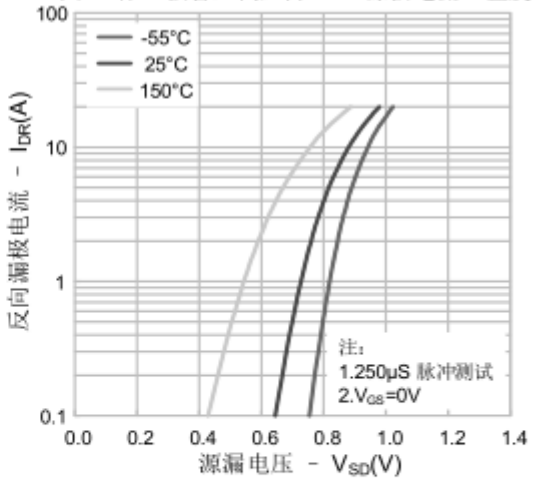

图9. 电容特性

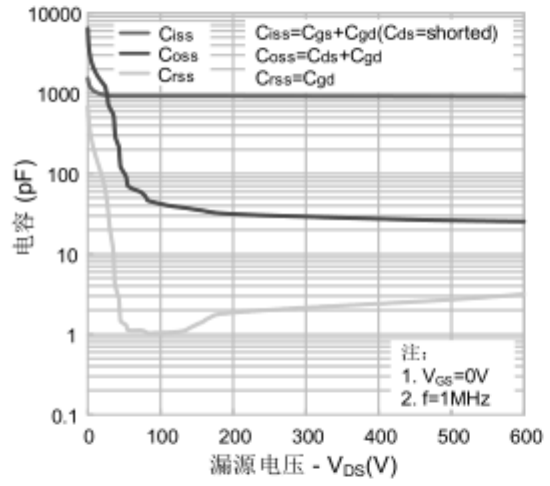

图 10. 电荷量特性

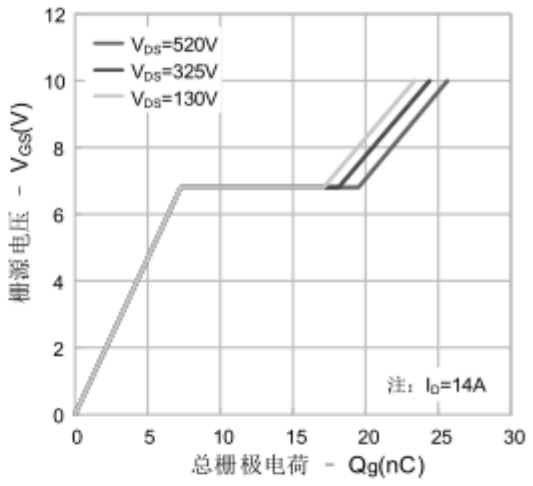

图 11. 击穿电压 vs. 温度特性

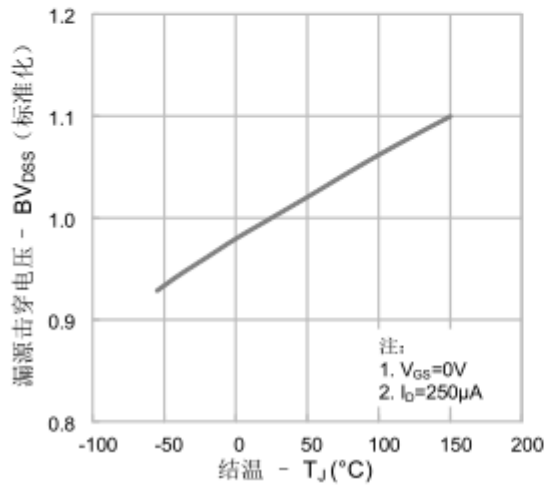

图 12. 导通电阻 vs. 温度特性

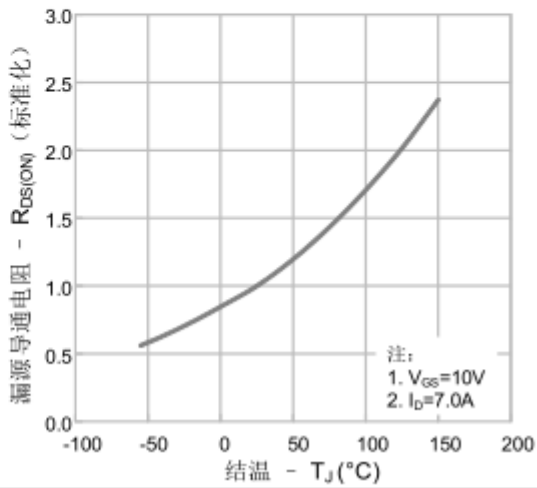

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图 13-1. 最大安全工作区域

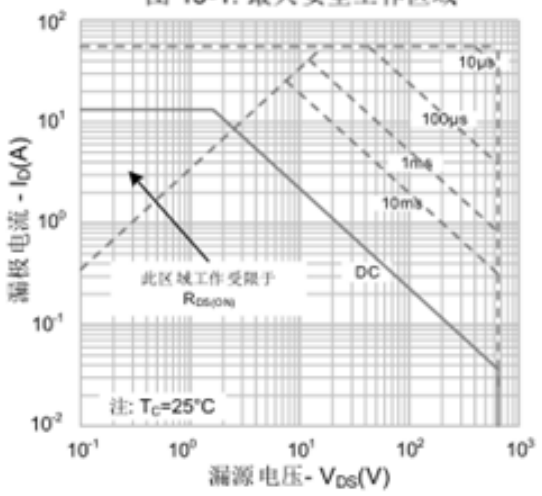


图14-1. 耗散功率 vs. 温度

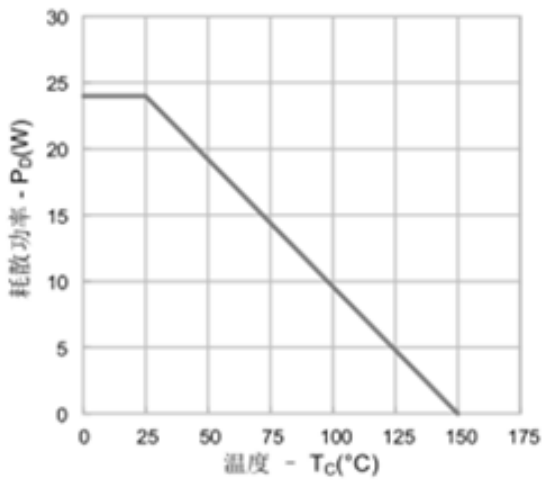


图15. 漏极电流 vs. 壳温

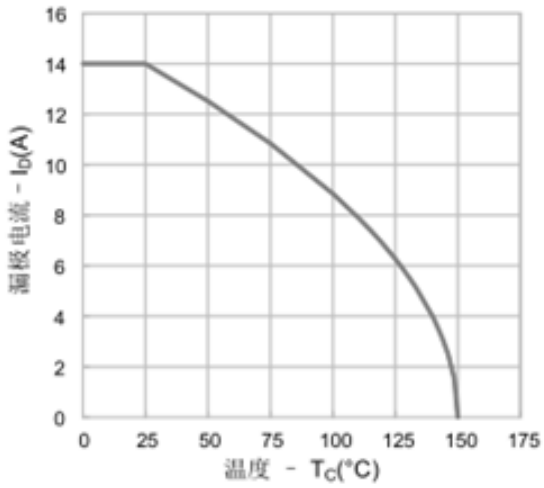
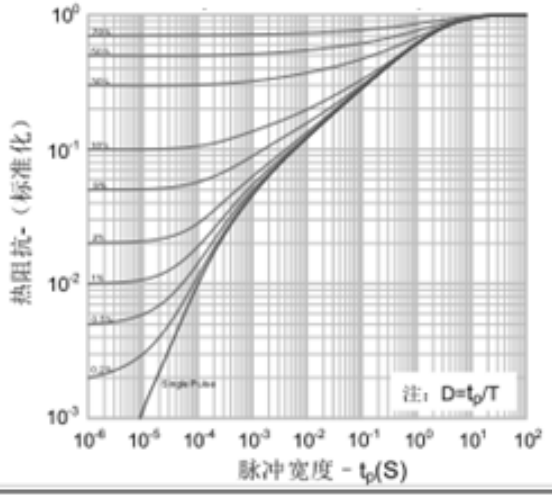


图16-1.瞬态热阻抗 vs. 脉冲宽度



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Test Circuits and Waveforms

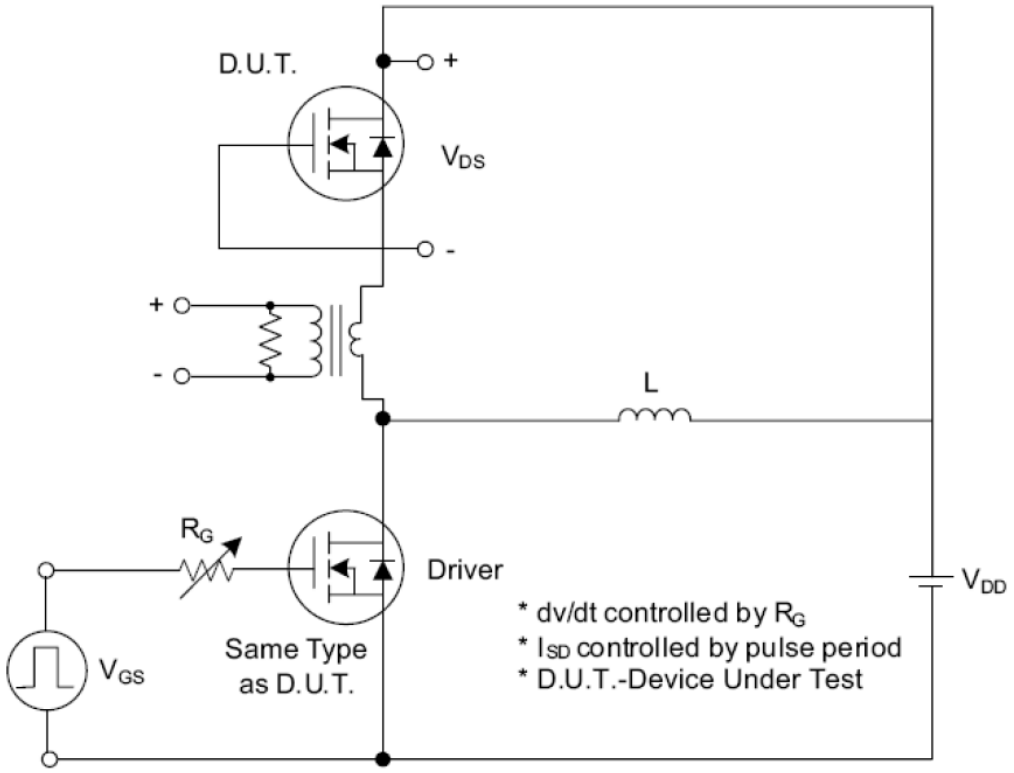

Fig. 1.1 Peak Diode Recovery dv/dt Test Circuit

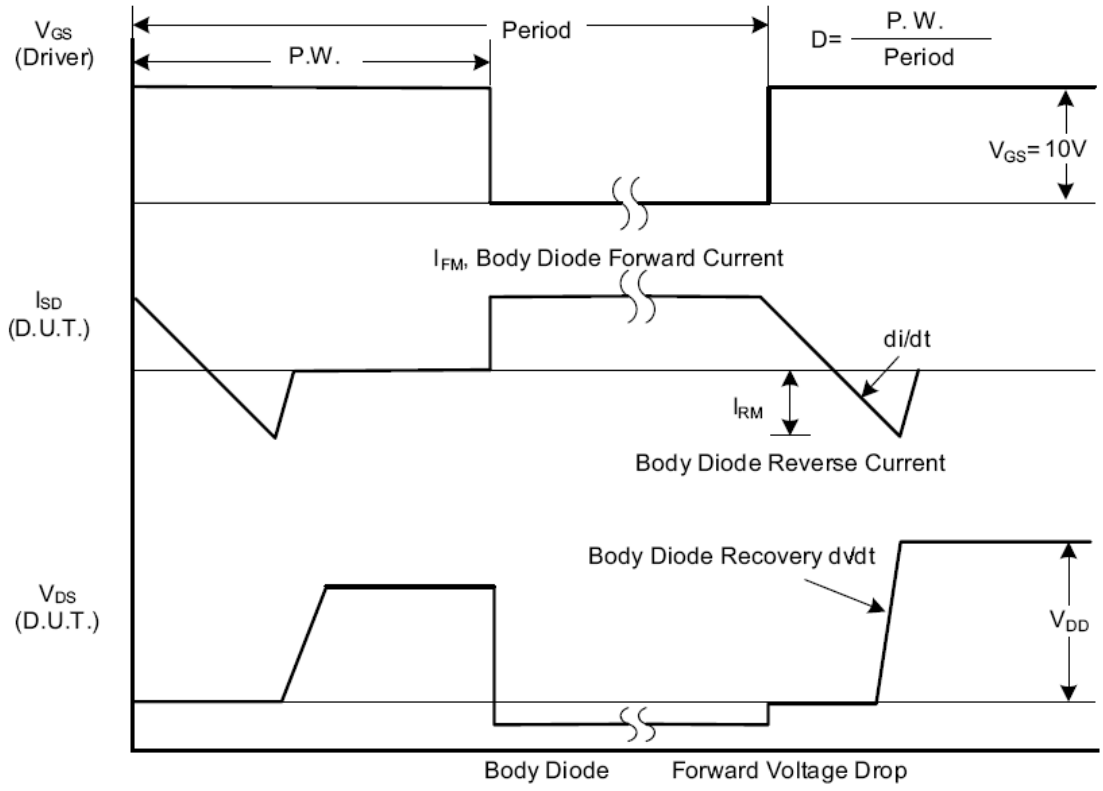

Fig. 1.2 Peak Diode Recovery dv/dt Waveforms

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Test Circuits and Waveforms (Cont.)

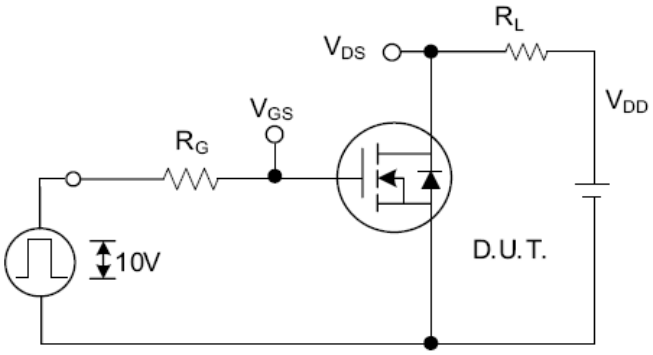

Fig. 2.1 Switching Test Circuit

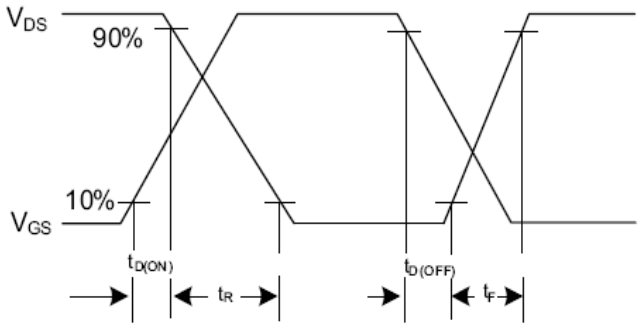

Fig. 2.2 Switching Waveforms

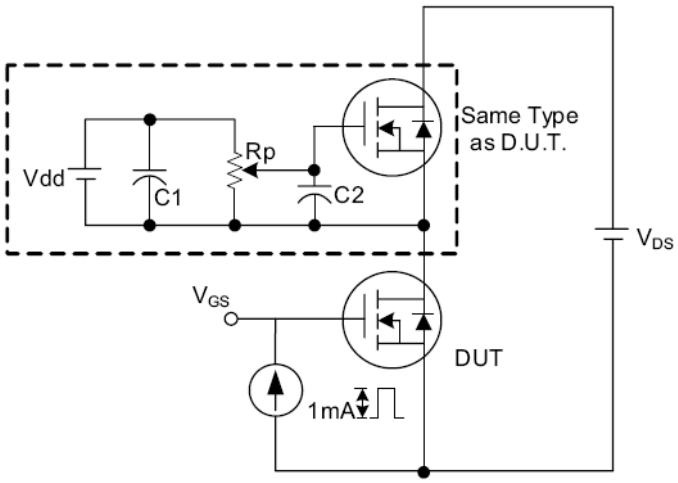

Fig. 3 . 1 Gate Charge Test Circuit

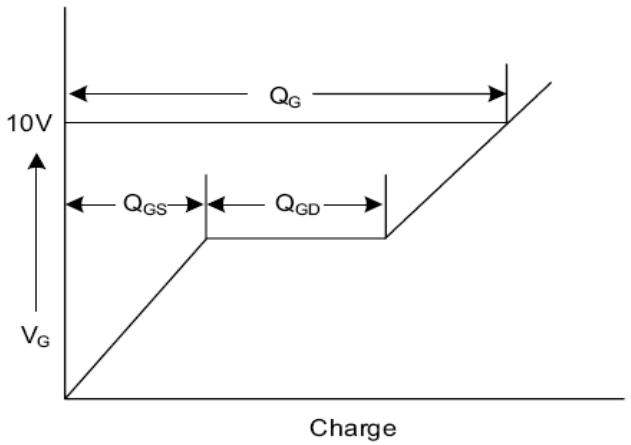

Fig. 3 . 2 Gate Charge Waveform

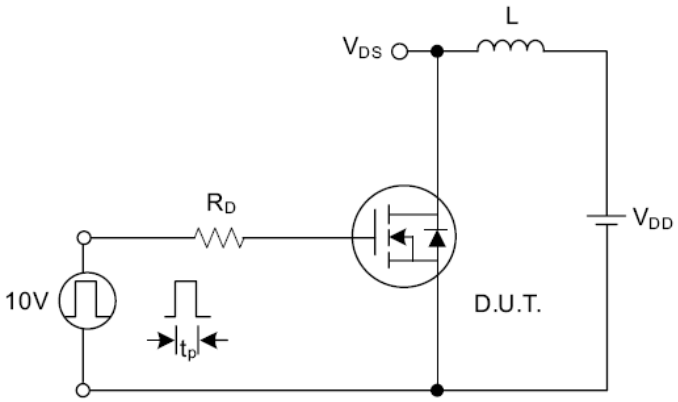

Fig. 4.1 Unclamped Inductive Switching Test Circuit

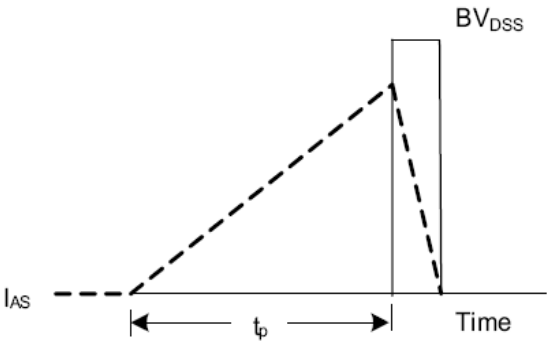

Fig. 4.2 Unclamped Inductive Switching Waveforms

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   b. support or sustain life,
   c. whose failure to perform when properly used in accordance with instructions for used provided in the labeling, can be reasonably expected to result in significant injury to the user.
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