Elektronische Bauelemente

SPR40N06

40A , 60V , $R_{DS(ON)}$ 12 mΩ

N-Channel Enhancement Mode Power MOSFET

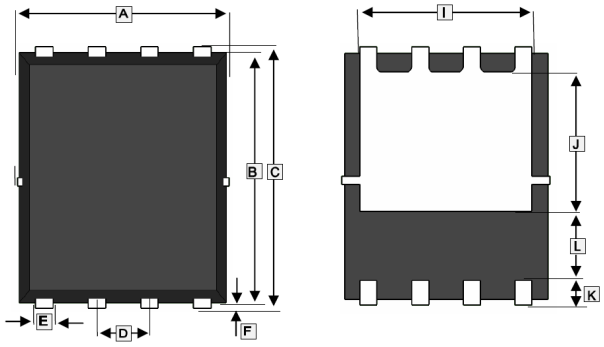
RoHS Compliant Product

A suffix of "-C" specifies halogen & lead-free

DESCRIPTION

The SPR40N06 provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness. The PR-8PP package is universally preferred for all commercial-industrial surface mount applications and suited for low voltage applications such as DC/DC converters.

PR-8PP

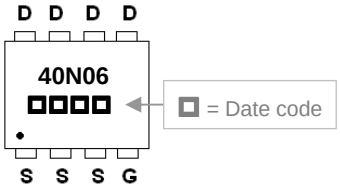


REF.	Millimeter		REF.	Millimeter	
	Min.	Max.		Min.	Max.
A	4.9	5.1	G	0.8	1.0
B	5.7	5.9	H	0.254 Ref.	
C	5.95	6.2	I	4.0 Ref.	
D	1.27 BSC.		J	3.4 Ref.	
E	0.35	0.49	K	0.6 Ref.	
F	0.1	0.2	L	1.4 Ref.	

FEATURES

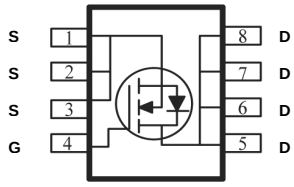
- Lower Gate Charge
- Simple Drive Requirement
- Fast Switching Characteristic

MARKING



PACKAGE INFORMATION

Package	MPQ	Leader Size
PR-8PP	3K	13 inch



ABSOLUTE MAXIMUM RATINGS (T_A=25℃ unless otherwise specified)

Parameter		Symbol	Rating	Unit
Drain-Source Voltage		V_{DS}	60	V
Gate-Source Voltage		V_{GS}	±20	V
Continuous Drain Current [1]@V_{GS}=10V	T_C=25℃	I_D	40	A
	T_C=100℃		28	
Pulsed Drain Current [2]	T_C=25℃	I_{DM}	110	A
Single Pulse Avalanche Energy [3]		EAS	50	mJ
Avalanche Current		I_{AS}	30	A
Total Power Dissipation [4]	T_C=25℃	P_D	69	W
Operating Junction & Storage Temperature		T_J, T_{STG}	-55~150	℃
Thermal Resistance Rating				
Thermal Resistance Junction-Ambient[1](Max).		$R_{\theta JA}$	36	℃ / W
Thermal Resistance Junction-Case[1](Max).		$R_{\theta JC}$	1.8	℃ / W

ELECTRICAL CHARACTERISTICS (T_J = 25℃ unless otherwise specified)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Teat Conditions
Static						
Drain-Source Breakdown Voltage	BV_{DSS}	60	-	-	V	V_{GS}=0, I_D= 250uA
Gate-Threshold Voltage	$V_{GS(th)}$	2	-	4	V	V_{DS}=V_{GS}, I_D=250uA
Gate-Source Leakage Current	I_{GSS}	-	-	±100	nA	V_{GS}= ±20V
Drain-Source Leakage Current	I_{DSS}	-	-	1	uA	V_{DS}=60V, V_{GS}=0, T_J=25℃
		-	-	5		V_{DS}=60V, V_{GS}=0, T_J=55℃
Static Drain-Source On-Resistance [2]	$R_{DS(ON)}$	-	-	12	mΩ	V_{GS}=10V, I_D=20A
Gate Resistance	R_g	-	-	3.5	Ω	f =1.0MHz
Total Gate Charge	Q_g	-	20	-	nC	I_D=20A V_{DS}=30V V_{GS}=10V
Gate-Source Charge	Q_{gs}	-	5	-		
Gate-Drain Change	Q_{gd}	-	1.8	-		
Turn-on Delay Time [2]	$T_{d(on)}$	-	6	-	nS	V_{DD}=30V V_{GS}=10V R_L=1.5Ω R_G=3Ω
Rise Time	T_r	-	2.5	-		
Turn-off Delay Time	$T_{d(off)}$	-	25	-		
Fall Time	T_f	-	2.5	-		
Input Capacitance	C_{iss}	-	1543	-	pF	V_{GS} =0 V_{DS}=30V f =1.0MHz
Output Capacitance	C_{oss}	-	165	-		
Reverse Transfer Capacitance	C_{rss}	-	9	-		
Guaranteed Avalanche Characteristics						
Single Pulse Avalanche Energy [5]	EAS	22	-	-	mJ	V_D=25V, L=0.1mH, I_{AS}=20A
Source-Drain Diode						
Diode Forward Voltage [2]	V_{SD}	-	-	1.3	V	I_S=20A, V_{GS}=0
Continuous Source Current [1,6]	I_S	-	-	40	A	V_D=V_G=0, Force Current
Pulsed Source Current [2,6]	I_{SM}	-	-	110	A	
Reverse Recovery Time	T_{rr}	-	18	-	nS	I_F=20A, dI/dt=100A/μS, T_J=25℃
Reverse Recovery Charge	Q_{rr}	-	65	-	nC	

Note:

1. The data tested by surface mounted on a 1 inch2 FR-4 board with 2OZ copper , ≦10sec , 125℃/W at steady state
2. The data tested by pulsed , pulse width ≦ 300us , duty cycle ≦ 2%
3. The EAS data shows Max. rating . The test condition is V_{DD}=25V,V_{GS}=10V,L=0.1mH,I_{AS}=30A
4. The power dissipation is limited by 150℃ juncti on temperature
5. The Min. value is 100% EAS tested guarantee.
6. The data is theoretically the same as ID and IDM , in real applications , should be limited by total power dissipation.

CHARACTERISTIC CURVES

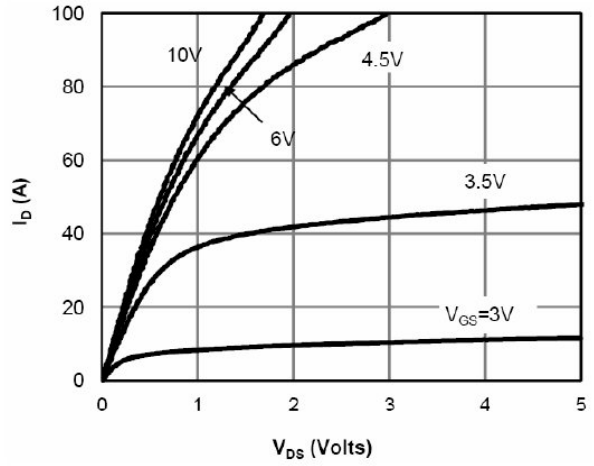


Fig 1. Typical Output Characteristics

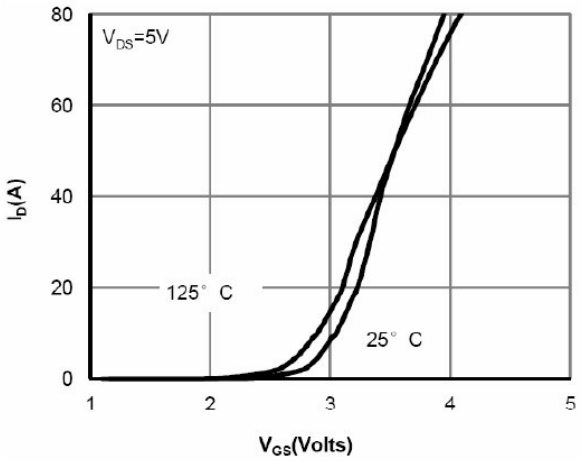


Fig 2. Transfer Characteristics

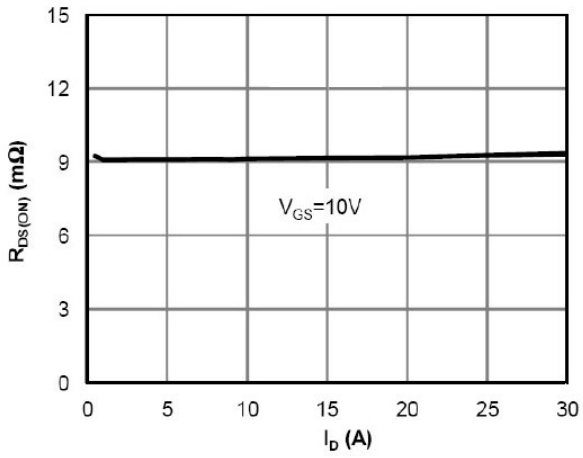


Fig 3. On-Resistance vs. Drain Current

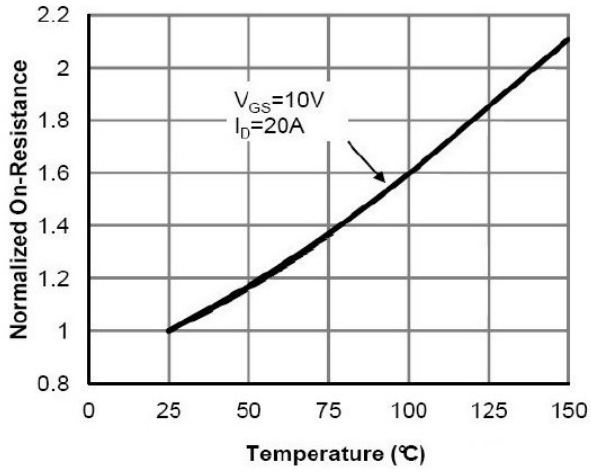


Fig 4. On-Resistance vs. Junction Temperature

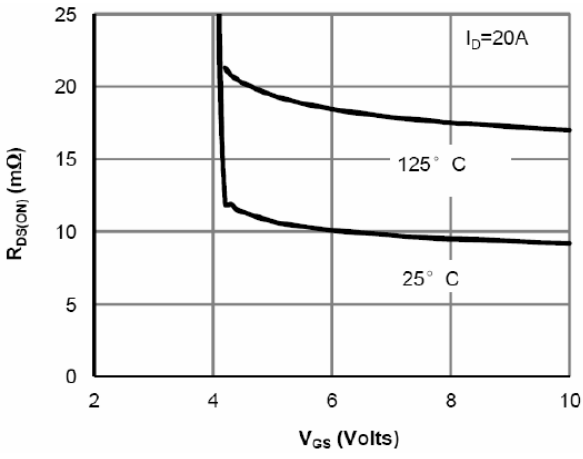


Fig 5. On-Resistance vs. Gate-Source Voltage

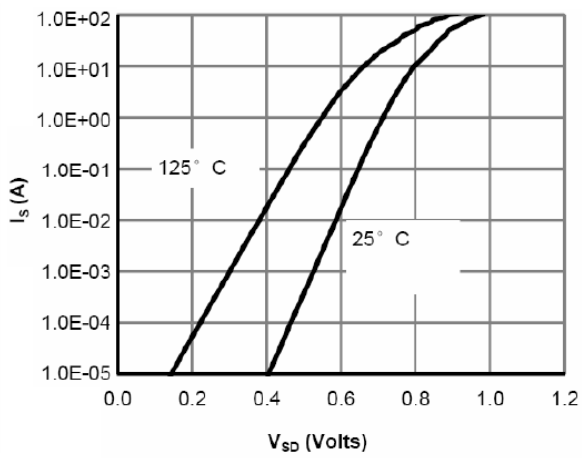


Fig 6. Body Diode Characteristics

CHARACTERISTIC CURVES

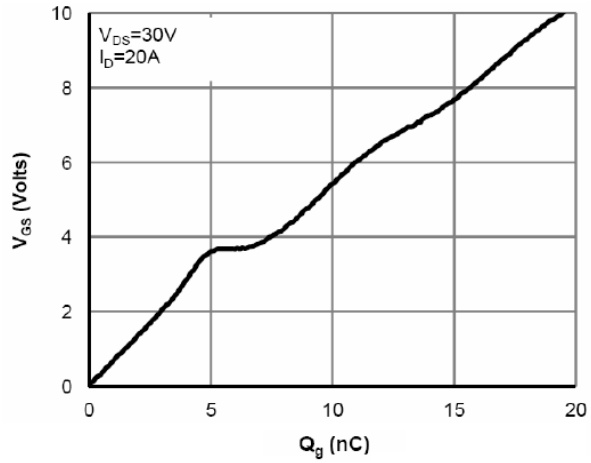


Fig 7. Gate Charge Characteristics

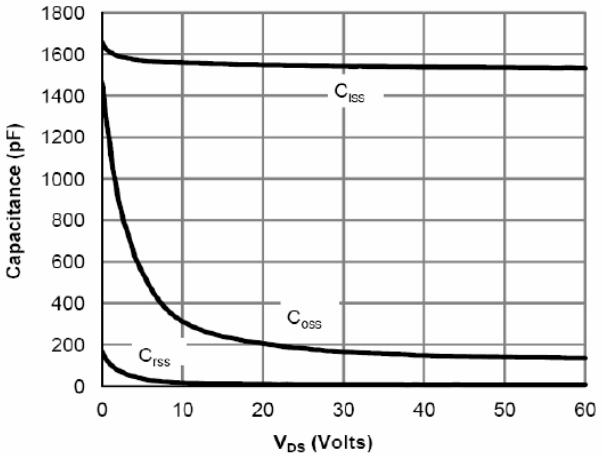


Fig 8. Typical Capacitance Characteristics

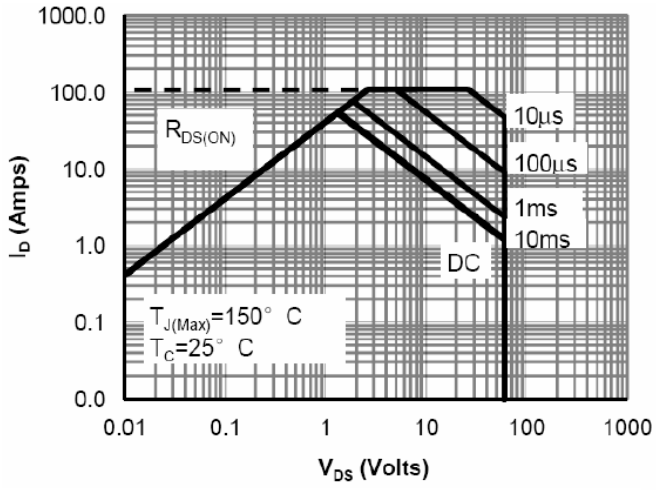


Fig 9. Safe Operating Area

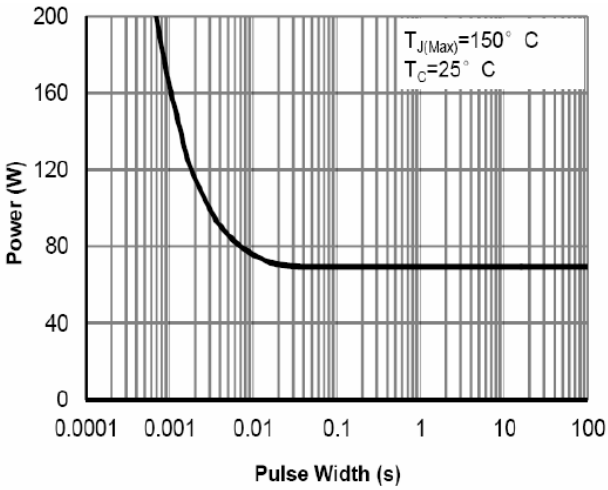


Fig 10. Single Pulse Power

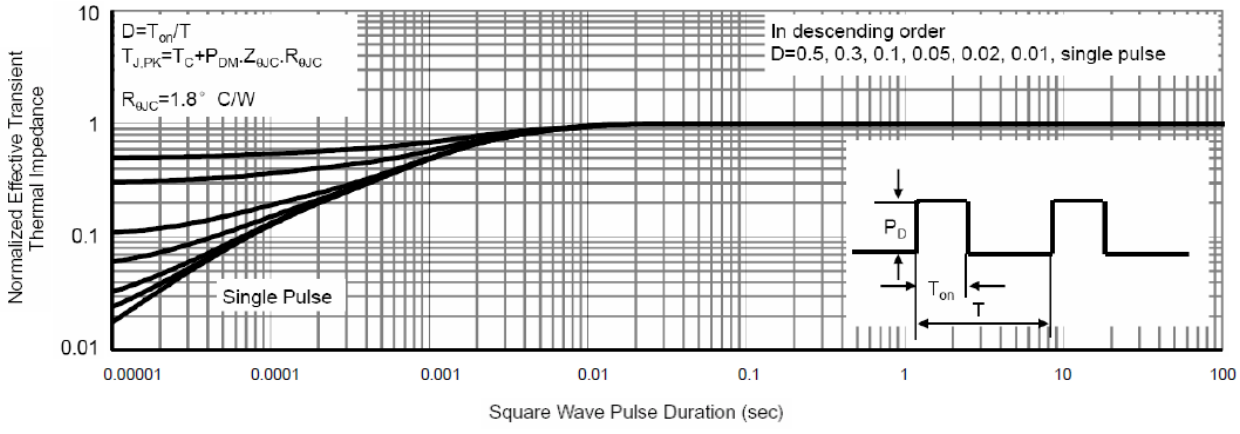


Fig 11. Normalized Maximum Transient Thermal Impedance