



SPP3401W

P-Channel Enhancement Mode MOSFET

DESCRIPTION

The SPP3401W is the P-Channel logic enhancement mode power field effect transistors are produced using high cell density , DMOS trench technology.

This high density process is especially tailored to minimize on-state resistance.

These devices are particularly suited for low voltage application such as cellular phone and notebook computer power management and other battery powered circuits, and low in-line power loss are needed in a very small outline surface mount package.

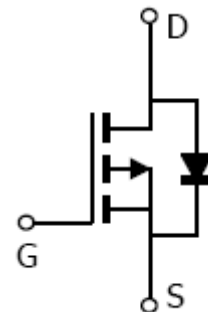
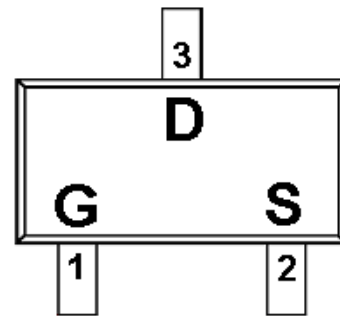
FEATURES

- ◆ $-30\text{V}/-4.0\text{A}, R_{\text{DS(ON)}}=70\text{m}\Omega @ V_{\text{GS}}=-10\text{V}$
- ◆ $-30\text{V}/-3.2\text{A}, R_{\text{DS(ON)}}=90\text{m}\Omega @ V_{\text{GS}}=-4.5\text{V}$
- ◆ $-30\text{V}/-1.2\text{A}, R_{\text{DS(ON)}}=115\text{m}\Omega @ V_{\text{GS}}=-2.5\text{V}$
- ◆ Super high density cell design for extremely low $R_{\text{DS(ON)}}$
- ◆ Exceptional on-resistance and maximum DC current capability
- ◆ SOT-23 package design

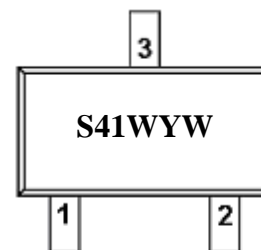
APPLICATIONS

- Power Management in Note book
- Portable Equipment
- Battery Powered System
- DC/DC Converter
- Load Switch
- DSC
- LCD Display inverter

PIN CONFIGURATION(SOT-23)



PART MARKING



Y : Year Code
W : Week Code



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PIN DESCRIPTION

Pin	Symbol	Description
1	G	Gate
2	S	Source
3	D	Drain

ORDERING INFORMATION

Part Number	Package	Part Marking
SPP3401WS23RGB	SOT-23	S41W

※ Week Code : A ~ Z(1 ~ 26) ; a ~ z(27 ~ 52)

※ SPP3401WS23RGB : Tape Reel ; Pb – Free ; Halogen - Free

ABSOLUTE MAXIMUM RATINGS

(TA=25°C Unless otherwise noted)

Parameter		Symbol	Typical	Unit
Drain-Source Voltage		V _{DSS}	-30	V
Gate –Source Voltage		V _{GSS}	±12	V
Continuous Drain Current(T _J =150°C)	T _A =25°C	I _D	-4.0	A
	T _A =70°C		-3.2	
Pulsed Drain Current		I _{DM}	-15	A
Continuous Source Current(Diode Conduction)		I _S	-1.0	A
Power Dissipation	T _A =25°C	P _D	1.25	W
	T _A =70°C		0.8	
Operating Junction Temperature		T _J	-55~150	°C
Storage Temperature Range		T _{STG}	-55~150	°C
Thermal Resistance-Junction to Ambient		R _{θJA}	120	°C/W



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ELECTRICAL CHARACTERISTICS

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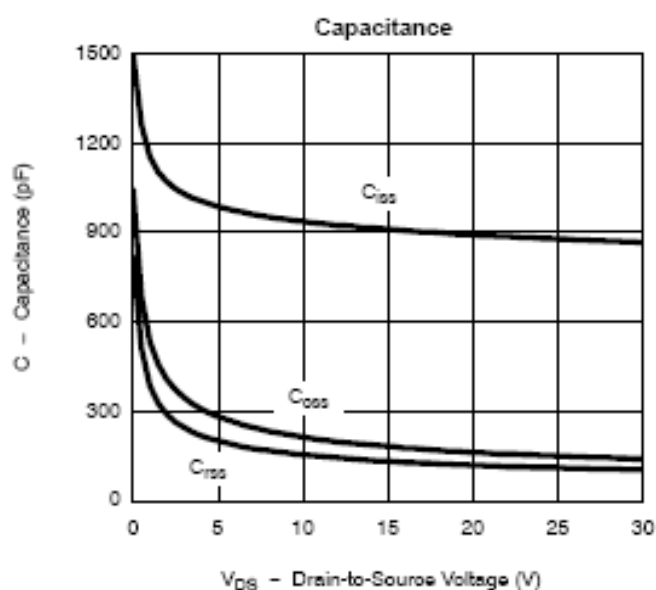
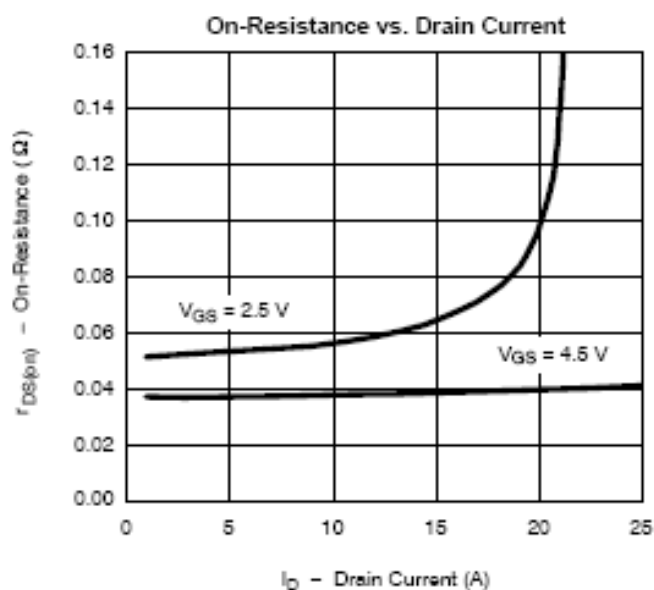
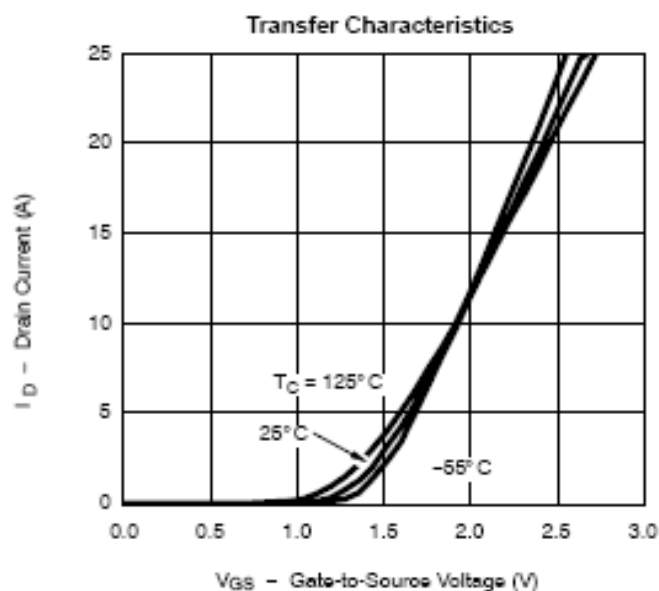
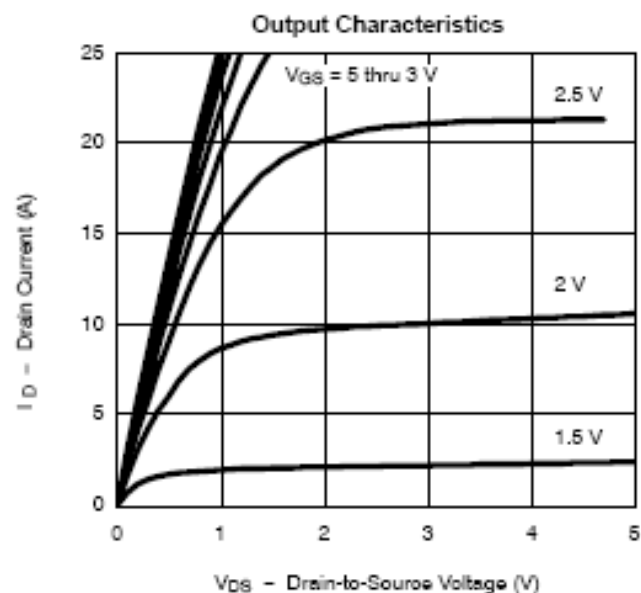
Parameter	Symbol	Conditions	Min.	Typ	Max.	Unit
Static						
Drain-Source Breakdown Voltage	V(BR)DSS	VGS=0V, ID=-250uA	-30			V
Gate Threshold Voltage	VGS(th)	VDS=VGS, ID=-250uA	-0.4		-1.0	
Gate Leakage Current	IGSS	VDS=0V, VGS=±12V			±100	nA
Zero Gate Voltage Drain Current	IDSS	VDS=-24V, VGS=0V			-1	uA
		VDS=-24V, VGS=0V TJ=55°C			-10	
On-State Drain Current	ID(on)	VDS ≤ -5V, VGS=-10V	-10			A
Drain-Source On-Resistance	RDS(on)	VGS=-10V, ID=-4.0A		0.068	0.070	Ω
		VGS=-4.5V, ID=-3.2A		0.088	0.090	
		VGS=-2.5V, ID=-1.2A		0.110	0.115	
Forward Transconductance	gfs	VDS=-5.0V, ID=-4.0A		10		S
Diode Forward Voltage	VSD	IS=-1.0A, VGS=0V		-0.8	-1.2	V
Dynamic						
Total Gate Charge	Qg	VDS=-15V, VGS=-10V ID=-4.0A		10	18	nC
Gate-Source Charge	Qgs			1.6		
Gate-Drain Charge	Qgd			3.0		
Input Capacitance	Ciss	VDS=-15V, VGS=0V f=1MHz		450		pF
Output Capacitance	Coss			95		
Reverse Transfer Capacitance	Crss			55		
Turn-On Time	td(on)	VDD=-15V, RL=15Ω ID=-1.0A, VGEN=-10V RG=6Ω		8	18	nS
	tr			8	18	
Turn-Off Time	td(off)			25	50	
	tf			25	35	



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TYPICAL CHARACTERISTICS

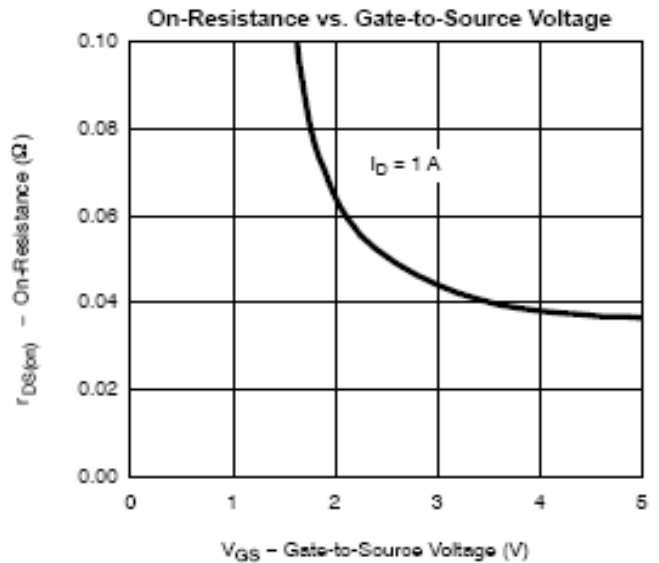
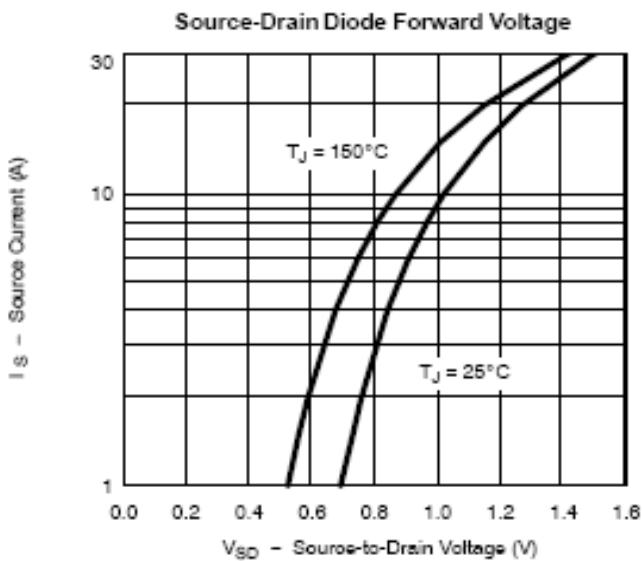
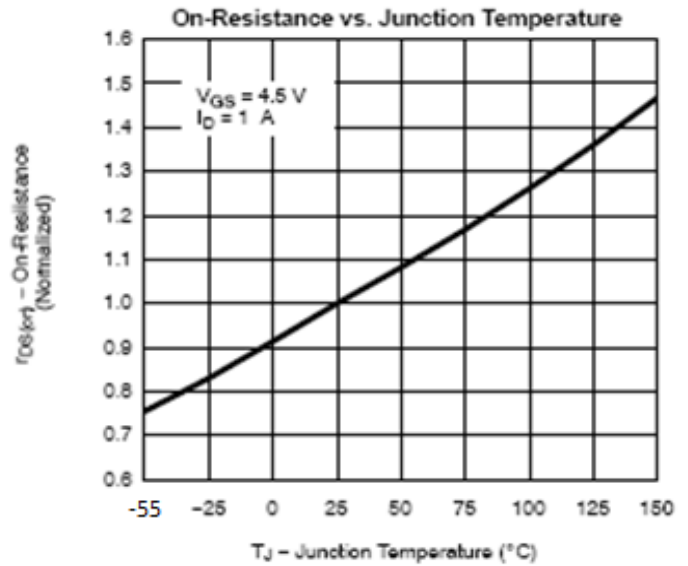
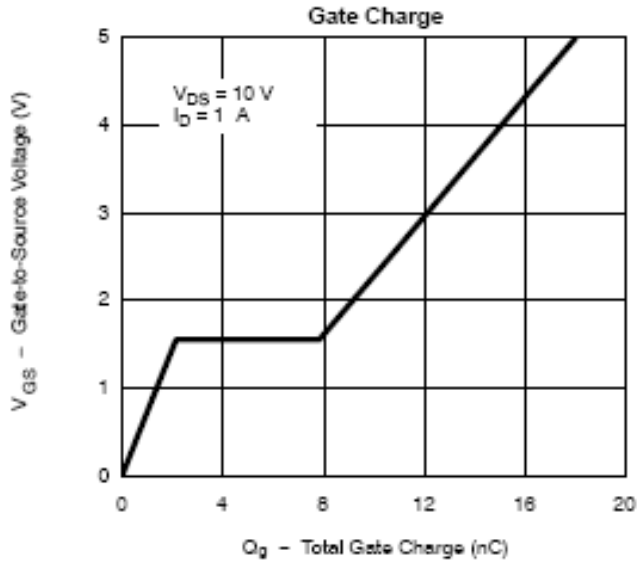




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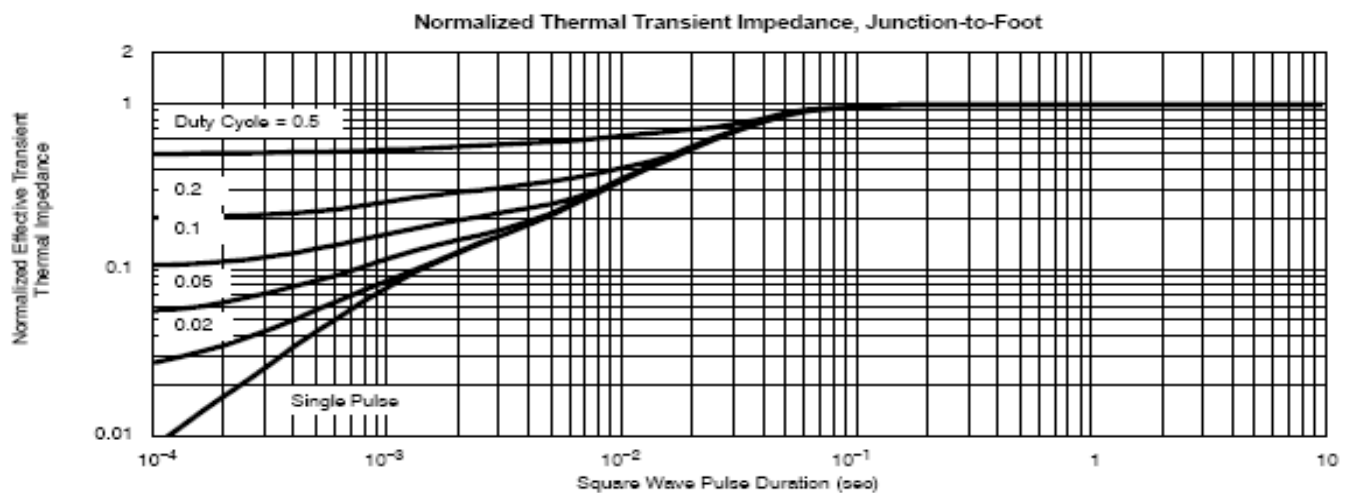
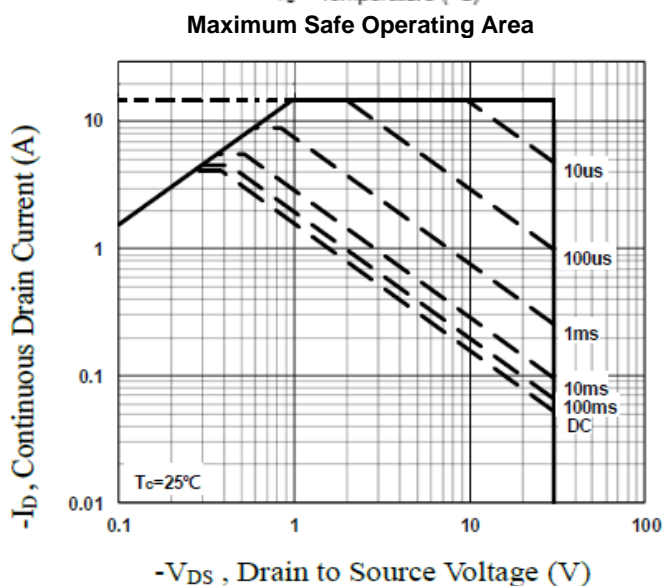
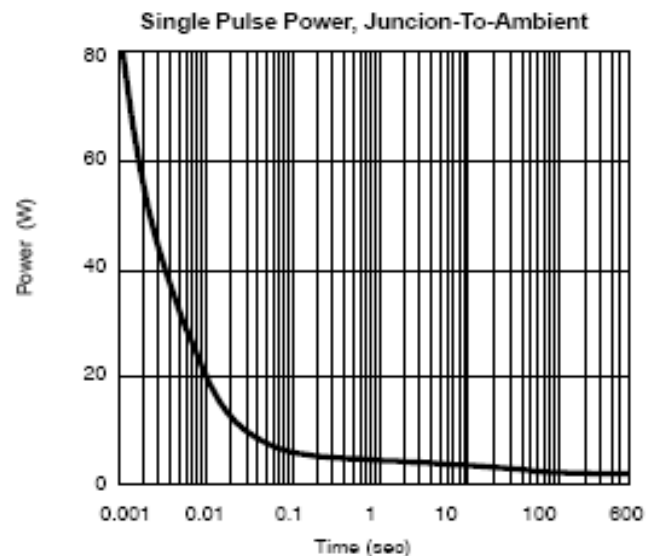
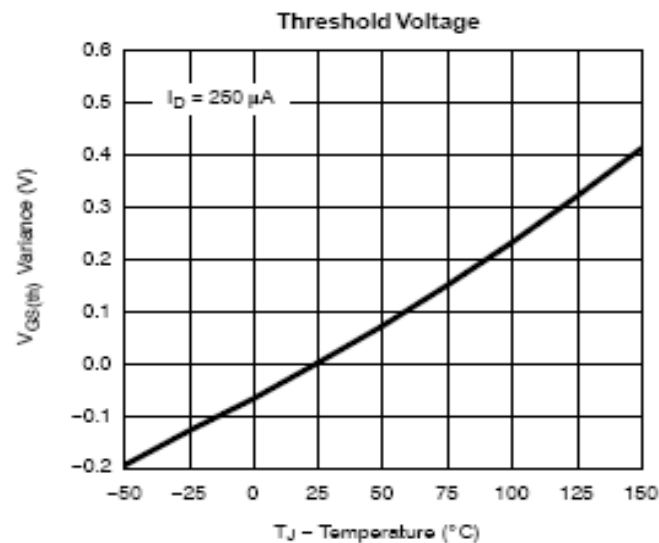




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TYPICAL CHARACTERISTICS





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