DESCRIPTION

The SPN6242 is the N-Channel logic enhancement mode power field effect transistors are produced using high cell density, DMOS trench technology.

This high density process is especially tailored to minimize on-state resistance.

These devices are particularly suited for low voltage application such as cellular phone and notebook computer power management and other battery powered circuits, and low in-line power loss are needed in a very small outline surface mount package.

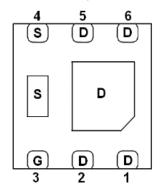
FEATURES

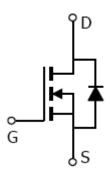
- 20V/3.3A, RDS(ON)= $19m\Omega(@VGS=4.5V)$
- 20V/2.8A, RDS(ON)= $24m\Omega$ @VGS=2.5V
- 20V/2.3A,RDS(ON)= $32m\Omega@V$ GS=1.8V
- ◆ Super high density cell design for extremely low RDS(ON)
- Exceptional on-resistance and maximum DC current capability
- ◆ UDFN2x2-6L package design

APPLICATIONS

- Power Management in Note book
- Portable Equipment
- Battery Powered System
- DC/DC Converter
- Load Switch
- DSC
- LCD Display inverter

PIN CONFIGURATION(UDFN2x2-6L)





PART MARKING

6242 YW

Y: Year Code W: Week Code

PIN DESCRIPTION		
Pin	Symbol	Description
1	D	Drain
2	D	Drain
3	G	Gate
4	S	Source
5	D	Drain
6	D	Drain

ORDERING INFORMATION

Part Number	Package	Part Marking
SPN6242UDN6RGB	UDFN2x2-6L	6242

 \times Week Code : A ~ Z(1 ~ 26); a ~ z(27 ~ 52)

ABSOULTE MAXIMUM RATINGS

(TA=25°C Unless otherwise noted)

Parameter		Symbol	Typical	Unit	
Drain-Source Voltage		Vdss	20	V	
Gate –Source Voltage		VGSS	±10	V	
Continuous Dusin Cumunt/Tr-1509C)	Tc=25°C	In	6.7	Δ.	
Continuous Drain Current(TJ=150°C)	Tc=100°C	- Id	4.2	A	
Pulsed Drain Current (*1)		Ірм	26.8	A	
Continuous Source Current(Diode Conduction)		Is	6.7	A	
Barray Dissipation	Ta=25°C	De	1.9	33 7	
Power Dissipation	Ta=70°C	PD	1.2	W	
Operating Junction Temperature		ΤJ	-55/150	°C	
Storage Temperature Range		Tstg	-55/150	°C	
Thermal Resistance-Junction to Ambient		RθJA	65	°C/W	

SPN6242 N-Channel Enhancement Mode MOSFET

ELECTRICAL CHARACTERISTICS (T.	ΓA=25°C Unless otherwise noted)
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Parameter	Symbol	Conditions	Min.	Тур	Max.	Unit
Static	l e				1	
Drain-Source Breakdown Voltage	V(BR)DSS	Vgs=0V,ID=250uA	20			.0 V
Gate Threshold Voltage	VGS(th)	VDS=VGS,ID=250uA	0.4	0.6	1.0	
Gate Leakage Current	Igss	VDS=0V,VGS=±10V			±100	nA
Zero Gate Voltage Drain Current		VDS=16V,VGS=0V, TJ=25°C			1	uA
	Idss	Vds=16V,Vgs=0V Tj=125°C			10	
Drain-Source On-Resistance		Vgs=4.5V,Id=3.3A		15	19	mΩ
	RDS(on)	Vgs=2.5V,Id=2.8A		18	24	1115.2
		Vgs=1.8V,Id=2.3A		23	32	
Forward Transconductance	gfs	Vds=10V,Id=4A		9.5		S
Diode Forward Voltage	Vsd	Is=1A,Vgs=0V,Tj=25°C			1	V
Dynamic	•					•
Total Gate Charge (*2,3)	Qg	VDS=10V,VGS=4.5V -ID=4A		5.8	8	nC
Gate-Source Charge (*2,3)	Qgs			0.6	1	
Gate-Drain Charge (*2,3)	Qgd	-ID-4A		2	4	
Input Capacitance	Ciss	VDS=10V,VGS=0V f=1MHz		600	870	pF
Output Capacitance	Coss			70	100	
Reverse Transfer Capacitance	Crss			45	65	
Turn-On Time (*2,3)	td(on)	Vdd=10V,Id=1A,Vgen=4.5V		5.0	9	
	tr			14.4	27	
	td(off)	$R_G=25\Omega$		30	55	nS
Turn-Off Time (*2,3)	tf			9.2	17	1

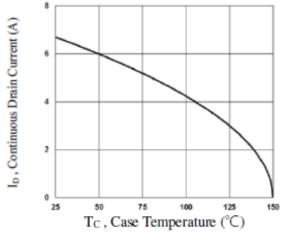
Note:

1.Repetitive Rating: Pulsed width limited by maximum junction temperature. 2.The data tested by pulsed, pulse width \leq 300us, duty cycle \leq 2%.

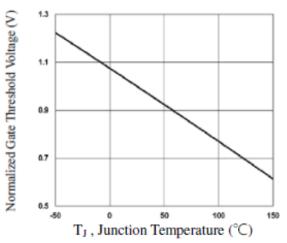
3. Essentially independent of operating temperature.

N-Channel Enhancement Mode MOSFET

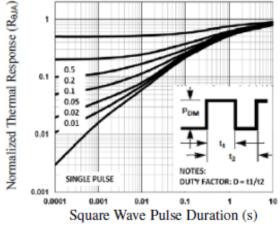
CHARACTERISTICS **TYPICAL**



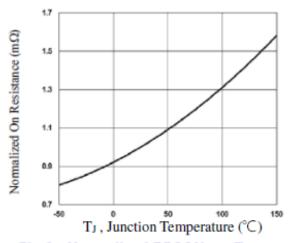
Continuous Drain Current vs. Tc



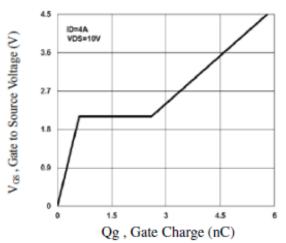
Normalized Vth vs. TJ



Normalized Transient Impedance



Normalized RDSON vs. TJ Fig.2



Gate Charge Waveform

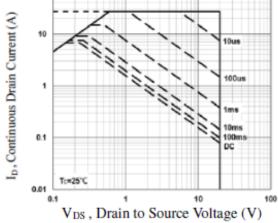


Fig.6 Maximum Safe Operation Area

TYPICAL CHARACTERISTICS

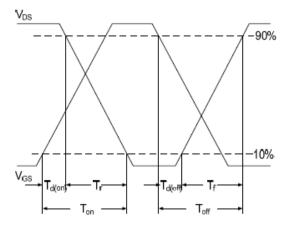


Fig.7 Switching Time Waveform

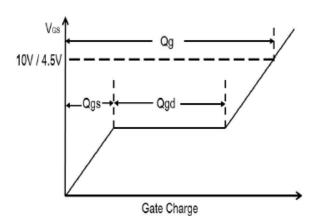


Fig.8 Gate Charge Waveform

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