



SPN6099

N-Channel Enhancement Mode MOSFET

DESCRIPTION

The SPN6099 is the N-Channel logic enhancement mode power field effect transistors are produced using high cell density , DMOS trench technology.

This high density process is especially tailored to minimize on-state resistance.

These devices are particularly suited for low voltage application , notebook computer power management and other battery powered circuits where high-side switching .

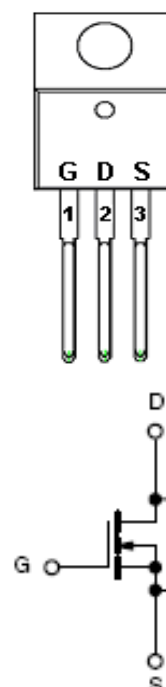
FEATURES

- ◆ 60V/80A, $R_{DS(ON)} = 4.0m\Omega @ V_{GS} = 10V$
- ◆ 60V/40A, $R_{DS(ON)} = 4.2m\Omega @ V_{GS} = 6.0V$
- ◆ 60V/10A, $R_{DS(ON)} = 4.4m\Omega @ V_{GS} = 4.5V$
- ◆ Super high density cell design for extremely low $R_{DS(ON)}$
- ◆ Exceptional on-resistance and maximum DC current capability
- ◆ TO-220-3L package design

APPLICATIONS

- DC/DC Converter
- Load Switch
- SMPS Secondary Side Synchronous Rectifier

PIN CONFIGURATION(TO-220-3L)



PART MARKING



A : Lot Code
B : Date Code
(YY/MM/DD)



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PIN DESCRIPTION

Pin	Symbol	Description
1	G	Gate
2	D	Drain
3	S	Source

ORDERING INFORMATION

Part Number	Package	Part Marking
SPN6099T220TGB	TO-220-3L	SPN6099

※ SPN6099T220TGB: Tube ; Pb – Free; Halogen – Free

ABSOLUTE MAXIMUM RATINGS

(TA=25°C Unless otherwise noted)

Parameter	Symbol	Typical	Unit
Drain-Source Voltage	V _{DSS}	60	V
Gate –Source Voltage	V _{GSS}	±20	V
Continuous Drain Current(T _J =150°C)	I _D	80	A
		80	
Pulsed Drain Current	I _{DM}	420	A
Avalanche Current	I _{AS}	75	A
Power Dissipation	P _D	62.5	W
		3.38	
Avalanche Energy with Single Pulse (T _J =25°C , L = 0.12mH , I _{AS} = 75A , V _{DD} = 80V.)	E _{AS}	380	mJ
Operating Junction Temperature	T _J	-55/150	°C
Storage Temperature Range	T _{STG}	-55/150	°C
Thermal Resistance-Junction to Ambient	R _{θJA}	2	°C/W



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ELECTRICAL CHARACTERISTICS

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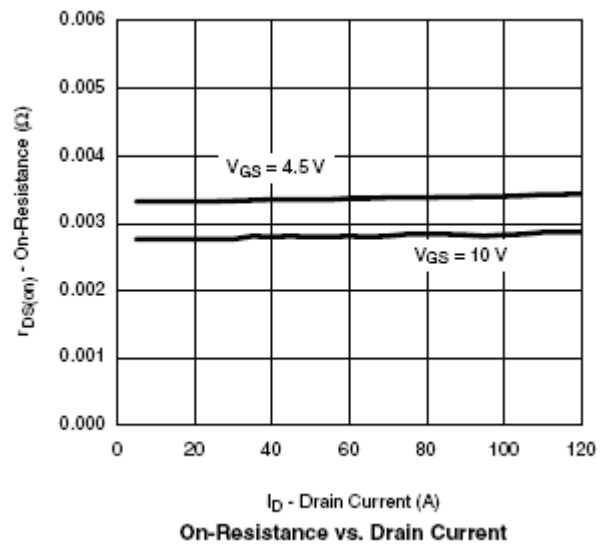
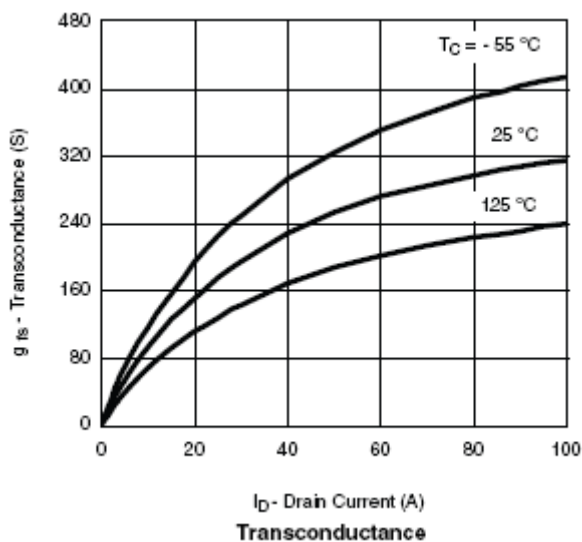
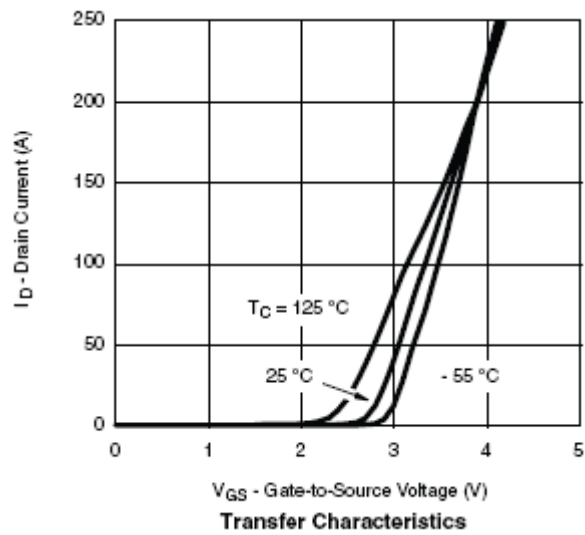
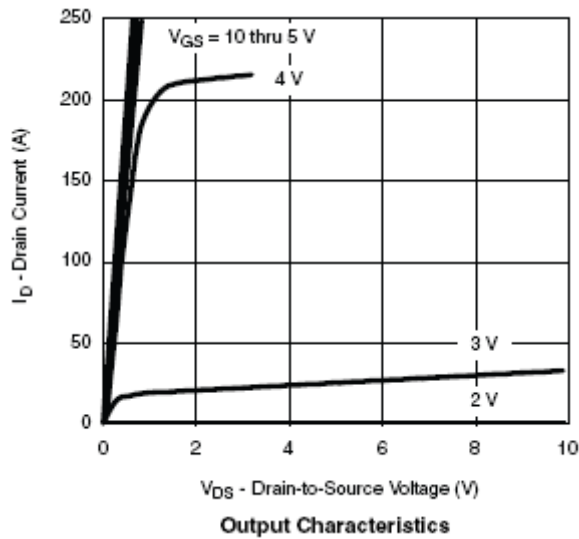
Parameter	Symbol	Conditions	Min.	Typ	Max.	Unit
Static						
Drain-Source Breakdown Voltage	V _{(BR)DSS}	V _{GS} =0V, I _D =250μA	100			V
Gate Threshold Voltage	V _{GS(th)}	V _{DS} =V _{GS} , I _D =250μA	1.0		2.5	
Gate Leakage Current	I _{GSS}	V _{DS} =0V, V _{GS} =±20V			±100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =100V, V _{GS} =0V			1	μA
		V _{DS} =100V, V _{GS} =0V T _J = 150 °C			250	
On-State Drain Current	I _{D(on)}	V _{DS} ≥10V, V _{GS} =10V	70			A
Drain-Source On-Resistance	R _{DS(on)}	V _{GS} = 10V, I _D =80A		3.6	4.0	mΩ
		V _{GS} = 6.0V, I _D =30A		3.8	4.2	
		V _{GS} = 4.5V, I _D =10A		4.0	4.4	
Forward Transconductance	g _{fs}	V _{DS} =15V, I _D =20A		60		S
Diode Forward Voltage	V _{SD}	I _S =30A, V _{GS} =0V			1.5	V
Dynamic						
Total Gate Charge	Q _g	V _{DS} =50V, V _{GS} =10V I _D = 20A		100		nC
Gate-Source Charge	Q _{gs}			28		
Gate-Drain Charge	Q _{gd}			25		
Input Capacitance	C _{iss}	V _{DS} =50V, V _{GS} =0V f=1MHz		6000		pF
Output Capacitance	C _{oss}			900		
Reverse Transfer Capacitance	C _{rss}			320		
Turn-On Time	t _{d(on)}	V _{DD} =50V, R _L =0.6Ω I _D =20A, V _{GEN} =10V R _G =1.0Ω		25	35	nS
	t _r			15	25	
Turn-Off Time	t _{d(off)}			35	55	
	t _f			8	15	



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TYPICAL CHARACTERISTICS

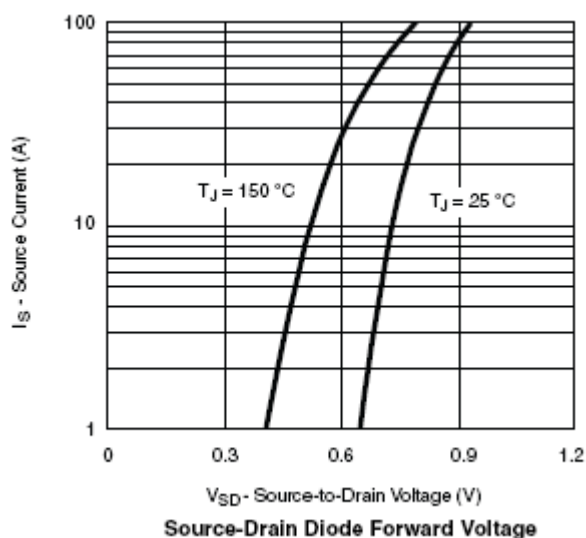
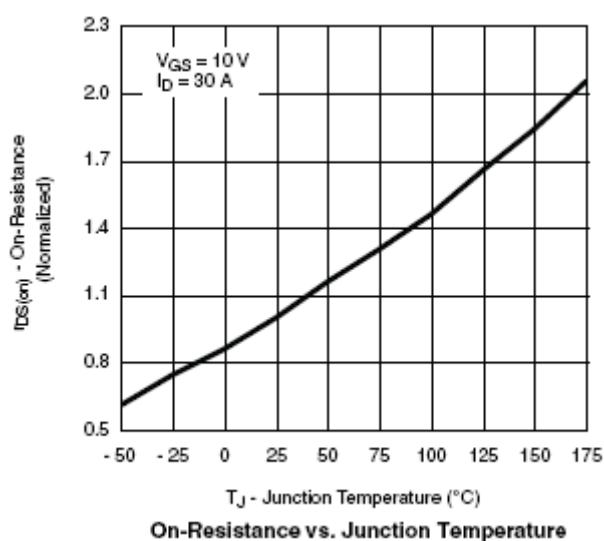
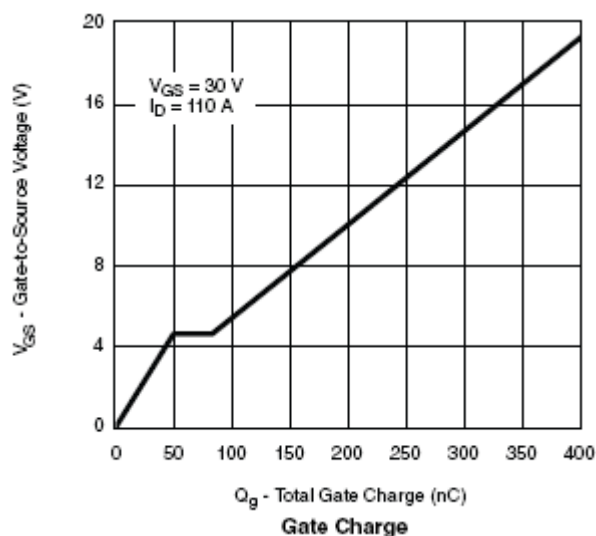
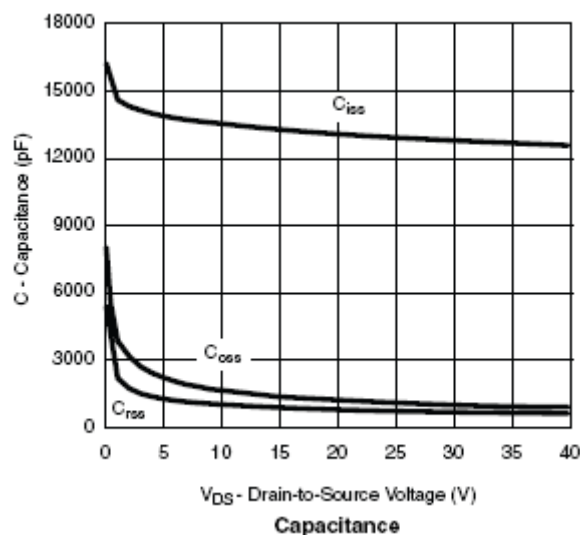




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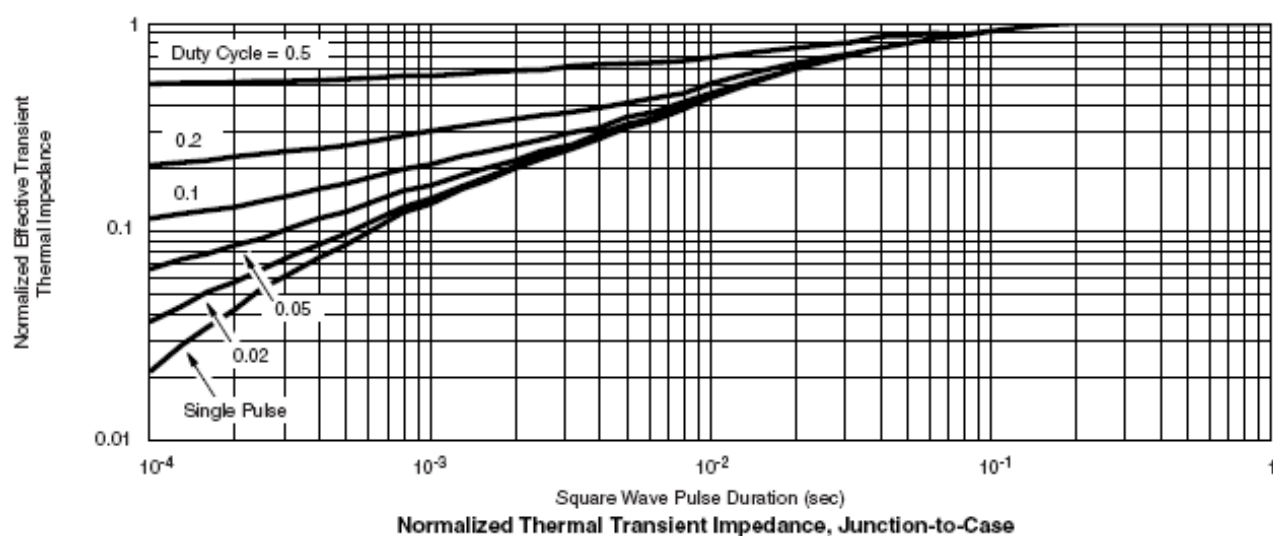
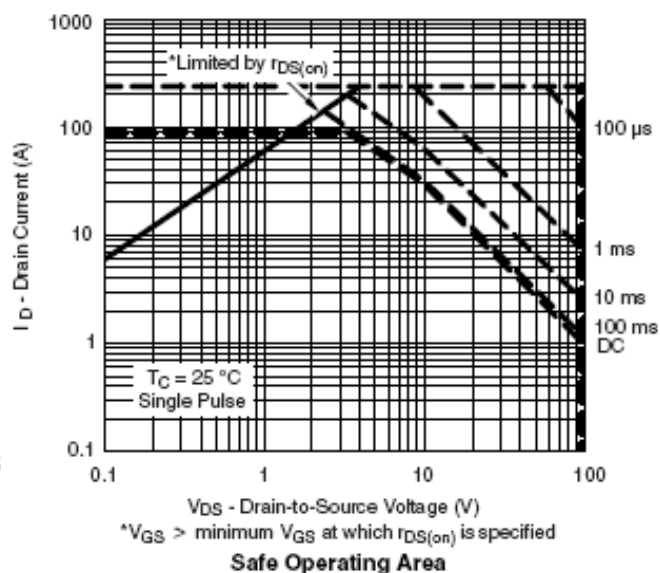
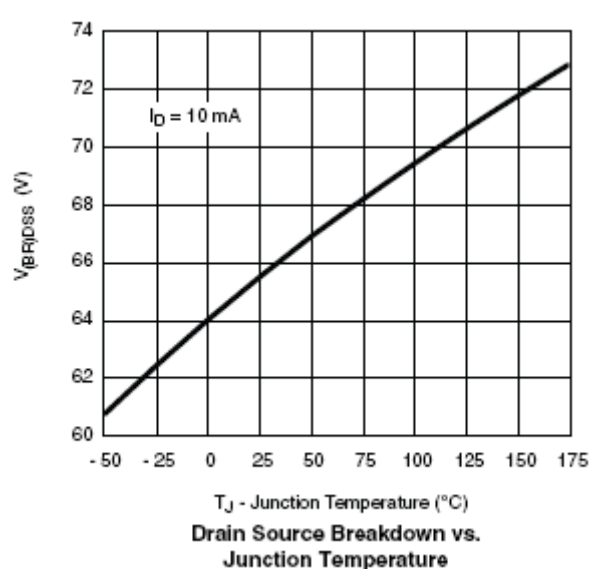




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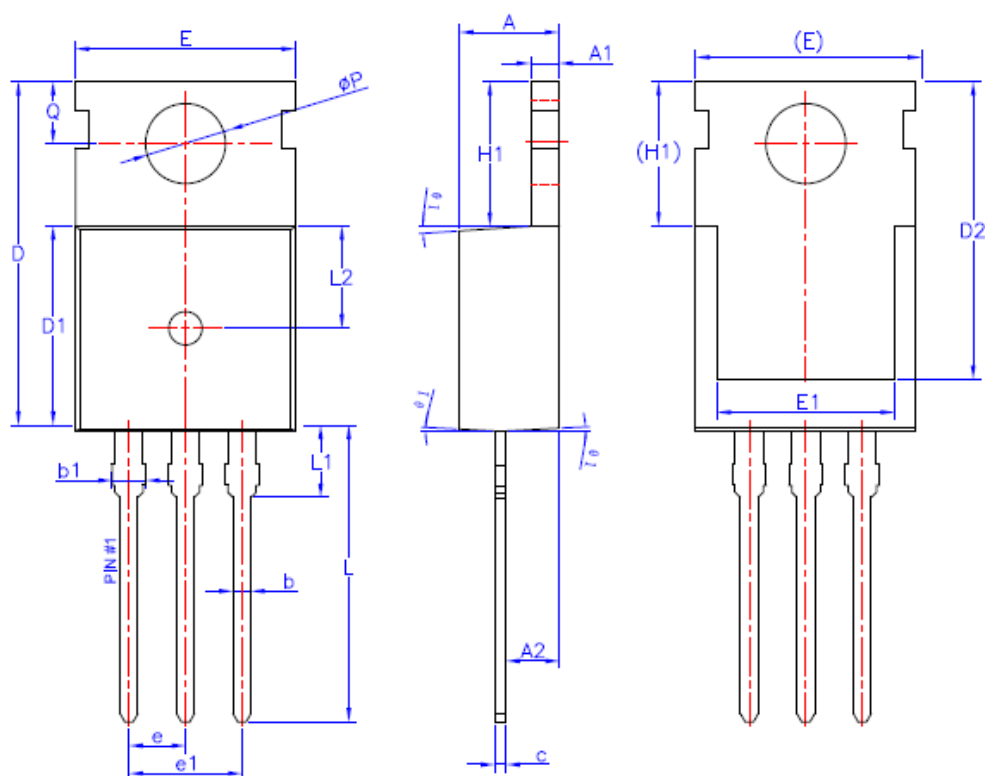




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TO-220-3L PACKAGE OUTLINE



SYMBOL	MIN	NOM	MAX
A	4.40	4.50	4.60
A1	1.27	1.30	1.33
A2	2.30	2.40	2.50
b	0.70	—	0.90
b1	1.42	—	1.57
c	0.45	0.50	0.60
D	15.30	15.70	16.10
D1	9.10	9.20	9.30
D2	13.10	—	13.70
E	9.70	9.90	10.20
E1	7.80	8.00	8.20
e	2.54BSC		
e1	5.08BSC		
H1	6.30	6.50	6.70
L	12.78	13.08	13.38
L1	—	—	3.50
L2	4.60REF		
øP	3.55	3.60	3.65
Q	2.73	—	2.87
θ 1	1°	3°	5°



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