SPN3632
N-Channel Enhancement Mode MOSFET

DESCRIPTION

The SPN3632 is the N-Channel logic enhancement mode power field effect transistors are produced using high cell density , DMOS trench technology.

This high density process is especially tailored to minimize on-state resistance.

These devices are particularly suited for low voltage application , notebook computer power management and other battery powered circuits where high-side switching .

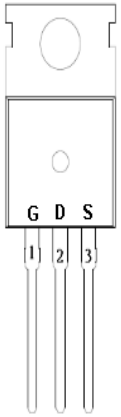
APPLICATIONS

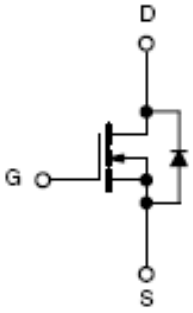
- DC/DC Converter
- Load Switch
- SMPS Secondary Side Synchronous Rectifier

FEATURES

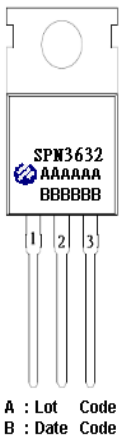
- 100V/80A,$R_{DS(ON)}$=8.8mΩ@V_{GS}=10V
- 100V/30A,$R_{DS(ON)}$=13mΩ@V_{GS}=6.0V
- 100V/10A,$R_{DS(ON)}$=10mΩ@V_{GS}=4.5V
- Super high density cell design for extremely low $R_{DS\ (ON)}$
- Exceptional on-resistance and maximum DC current capability
- TO-220-3L package design

PIN CONFIGURATION(TO-220-3L)





PART MARKING



SPN3632
N-Channel Enhancement Mode MOSFET

PIN DESCRIPTION

Pin	Symbol	Description
1	G	Gate
2	D	Drain
3	S	Source

ORDERING INFORMATION

Part Number	Package	Part Marking
SPN3632T220TGB	TO-220-3L	SPN3632

※ SPN3632T220TGB: Tube ; Pb – Free; Halogen – Free

ABSOULTE MAXIMUM RATINGS

(T_A=25℃ Unless otherwise noted)

Parameter		Symbol	Typical	Unit
Drain-Source Voltage		V_{DSS}	110	V
Gate –Source Voltage		V_{GSS}	±20	V
Continuous Drain Current(T_J=150℃)	T_A=25℃	I_D	90	A
	T_A=70℃		90	
Pulsed Drain Current		I_{DM}	240	A
Avalanche Current		I_{AS}	60	A
Power Dissipation	T_A=25℃	P_D	4.5	W
	T_A=70℃		3.38	
Avalanche Energy with Single Pulse (Tj=25℃, L = 0.12mH , I_{AS} = 75A , V_{DD} = 80V.)		E_{AS}	335	mJ
Operating Junction Temperature		T_J	-55/150	℃
Storage Temperature Range		T_{STG}	-55/150	℃
Thermal Resistance-Junction to Ambient		$R_{\theta JA}$	62.5	℃/W

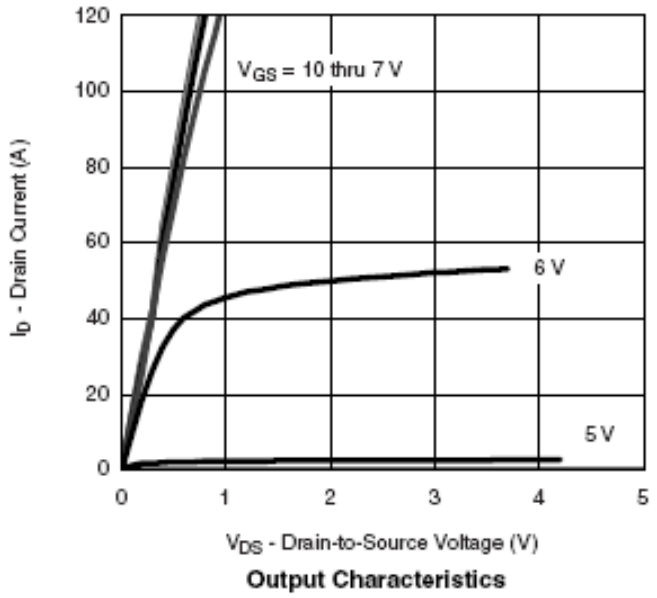
SPN3632
N-Channel Enhancement Mode MOSFET

ELECTRICAL CHARACTERISTICS

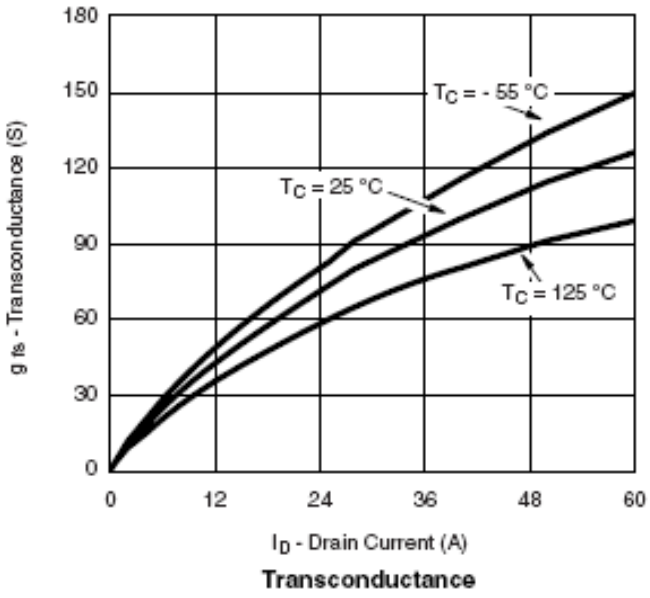
(T_A=25℃ Unless otherwise noted)

Parameter	Symbol	Conditions	Min.	Typ	Max.	Unit
Static						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS}=0V,I_D=250uA	100			V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS},I_D=250uA	1.0		3.0	
Gate Leakage Current	I_{GSS}	V_{DS}=0V,V_{GS}=±20V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=100V,V_{GS}=0V			1	uA
		V_{DS}=100V,V_{GS}=0V T_J = 150 ℃			250	
On-State Drain Current	$I_{D(on)}$	V_{DS}≥10V,V_{GS}=10V	70			A
Drain-Source On-Resistance	$R_{DS(on)}$	V_{GS}=10V,I_D=80A		7.5	8.8	mΩ
		V_{GS}=6.0V,I_D=30A		8.5	9.8	
		V_{GS}=4.5V,I_D=10A		8.2	10.0	
Forward Transconductance	gfs	V_{DS}=15V,I_D=20A		62		S
Diode Forward Voltage	V_{SD}	I_S=30A,V_{GS}=0V			1.5	V
Dynamic						
Total Gate Charge	Q_g	V_{DS}=50V,V_{GS}=10V I_D=20A		100		nC
Gate-Source Charge	Q_{gs}			35		
Gate-Drain Charge	Q_{gd}			25		
Input Capacitance	C_{iss}	V_{DS}=50V_{GS}=0V f=1MHz		6500		pF
Output Capacitance	C_{oss}			650		
Reverse Transfer Capacitance	C_{rss}			190		
Turn-On Time	$t_{d(on)}$	V_{DD}=50V,R_L=0.6Ω I_D=20A,V_{GEN}=10V R_G=1.0Ω		25		nS
	t_r			20		
Turn-Off Time	$t_{d(off)}$			30		
	t_f			10		

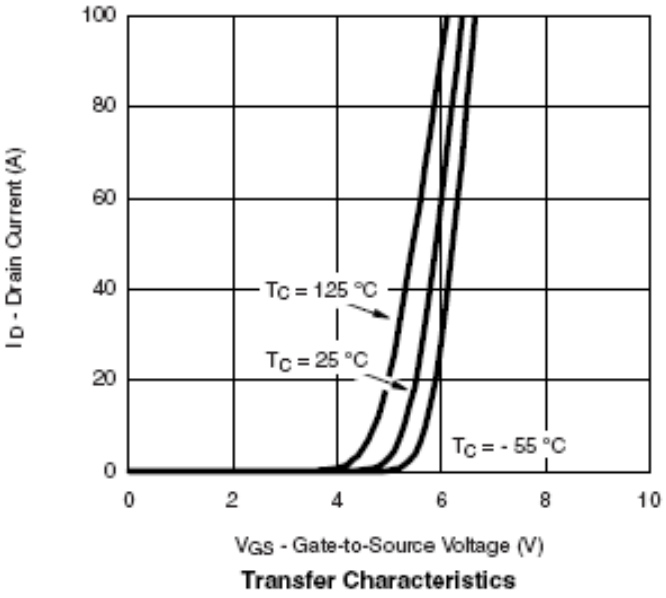
TYPICAL CHARACTERISTICS



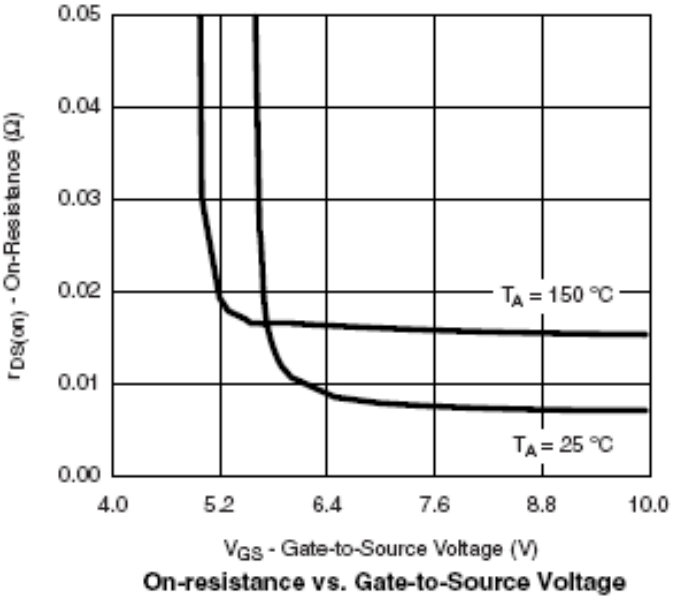
Output Characteristics



Transconductance

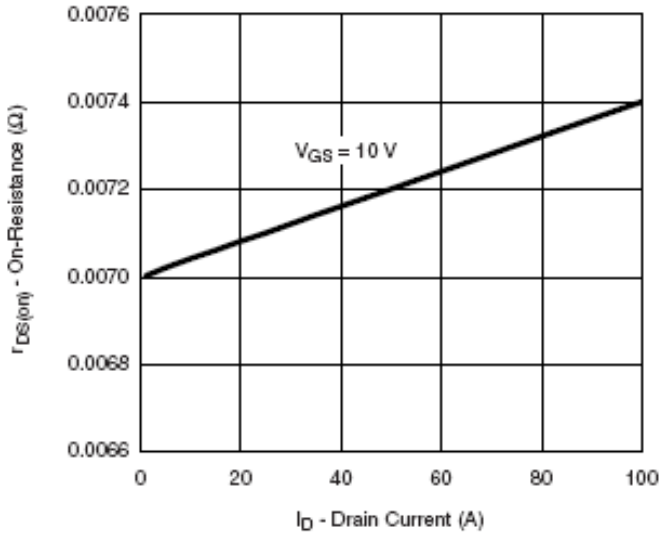


Transfer Characteristics

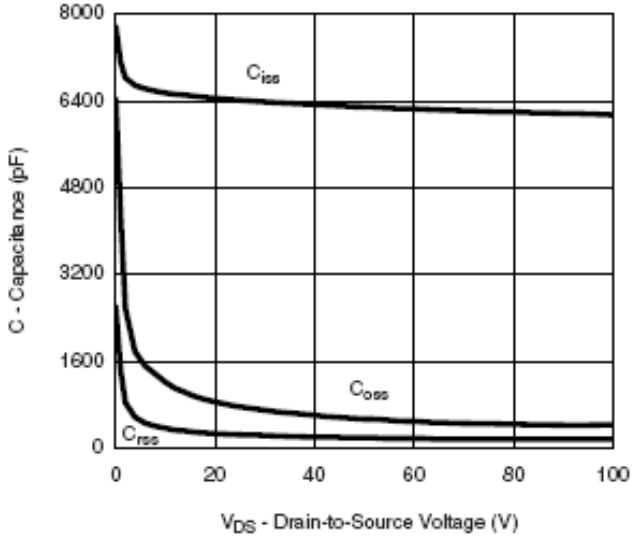


On-resistance vs. Gate-to-Source Voltage

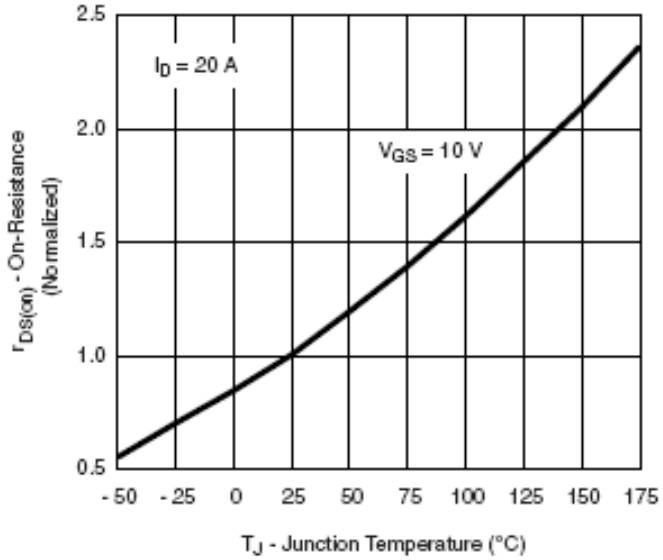
TYPICAL CHARACTERISTICS



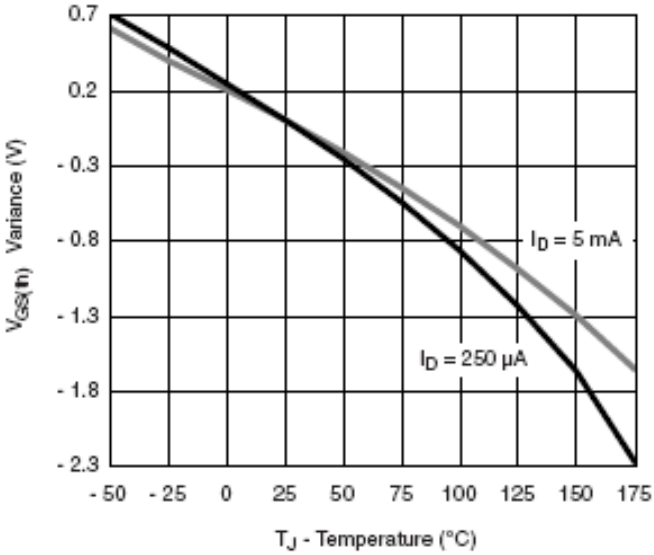
On-Resistance vs. Drain Current



Capacitance

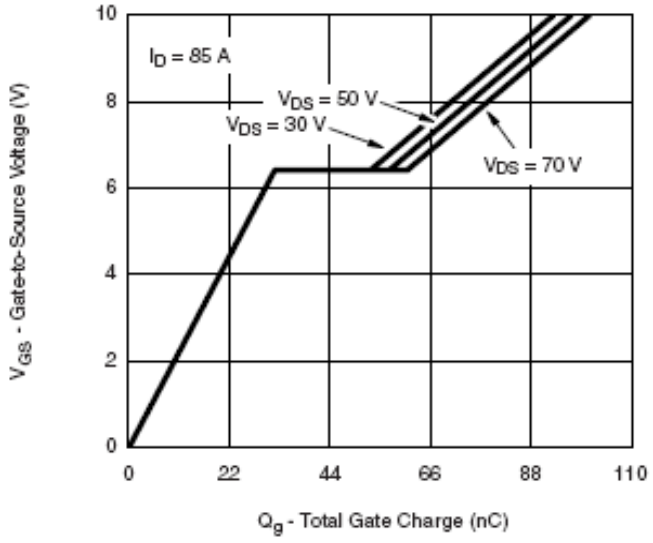


On-Resistance vs. Junction Temperature

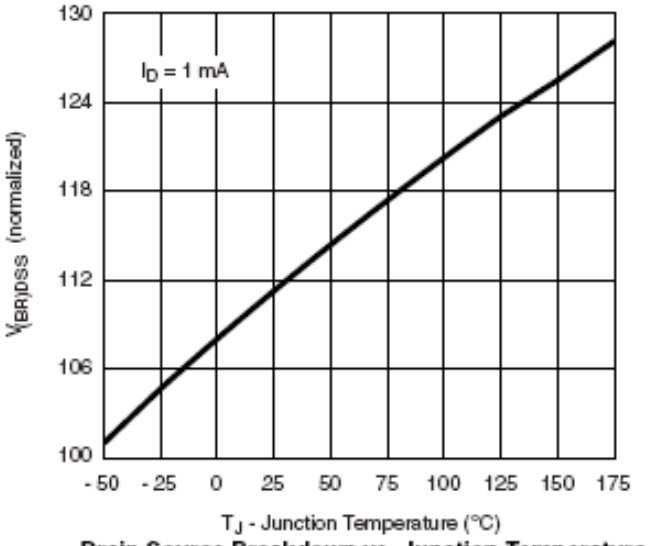


Threshold Voltage

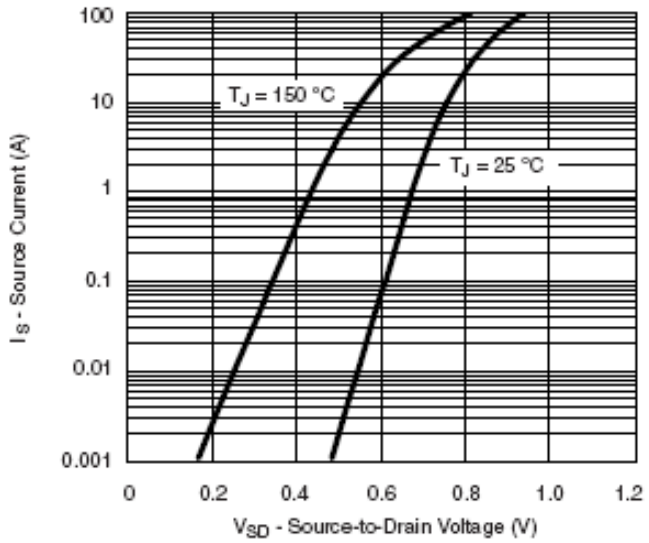
TYPICAL CHARACTERISTICS



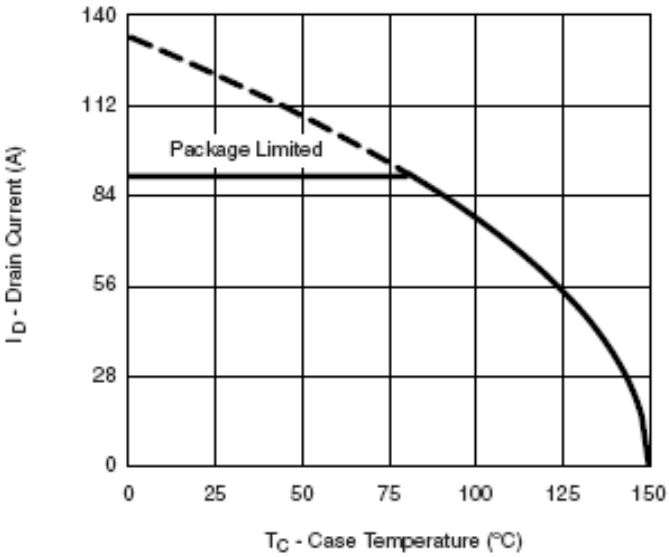
Gate Charge



Drain Source Breakdown vs. Junction Temperature

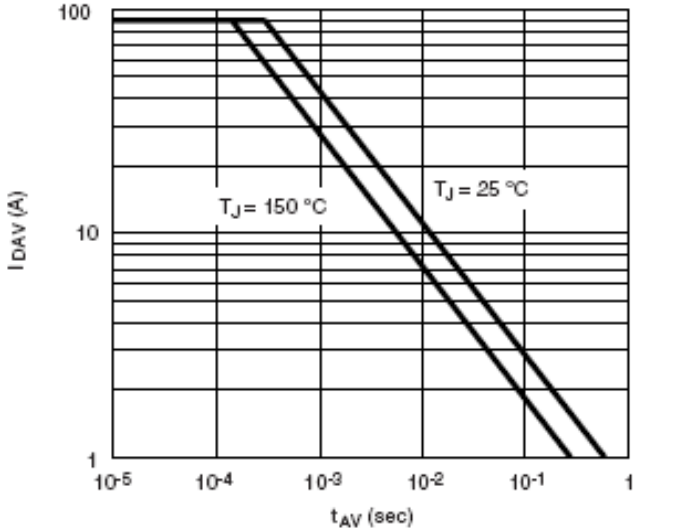


Source-Drain Diode Forward Voltage

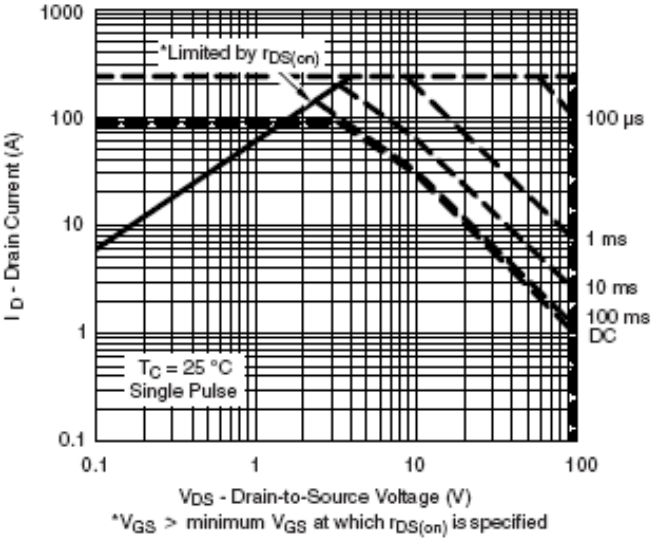


Maximum Drain Current vs. Case Temperature

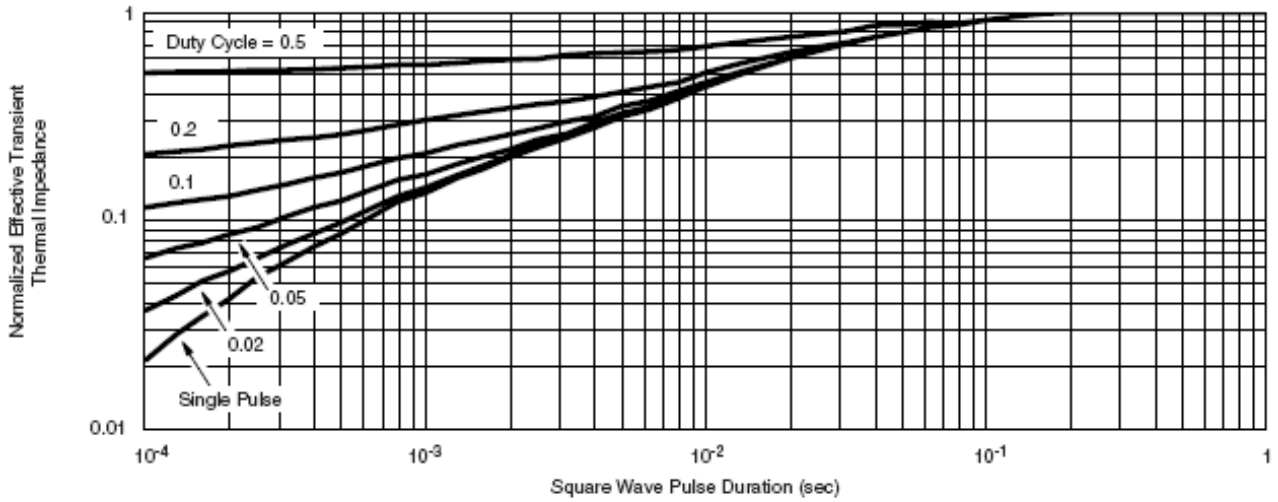
TYPICAL CHARACTERISTICS



Single Pulse Avalanche Current Capability vs. Time



Safe Operating Area



Normalized Thermal Transient Impedance, Junction-to-Case

SYNC Power Corporation
9F-5, No.3-2, Park Street
NanKang District (NKSP), Taipei, Taiwan 115
Phone: 886-2-2655-8178
Fax: 886-2-2655-8468
© http://www.syncpower.com