



SPN12T20

N-Channel Enhancement Mode MOSFET

DESCRIPTION

The SPN12T20 is the N-Channel logic enhancement mode power field effect transistor which is produced using super high cell density DMOS trench technology. The SPN12T20 has been designed specifically to improve the overall efficiency of DC/DC converters using either synchronous or conventional switching PWM controllers. It has been optimized for low gate charge, low $R_{DS(ON)}$ and fast switching speed.

FEATURES

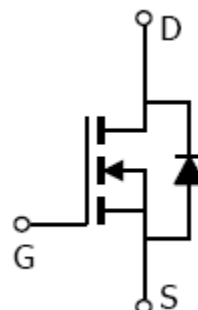
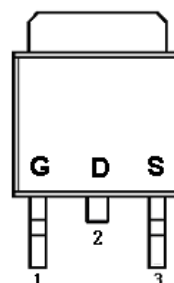
- ◆ 200V/9A, $R_{DS(ON)}=210m\Omega@V_{GS}=10V$
- ◆ High density cell design for extremely low $R_{DS(ON)}$
- ◆ Exceptional on-resistance and maximum DC current capability
- ◆ TO-252-2L package design

APPLICATIONS

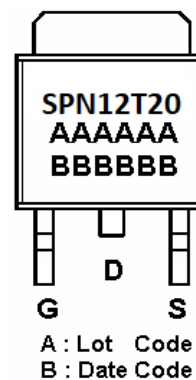
- High Frequency Small Power Switching for MB/NB/VGA
- Network DC/DC Power System
- Load Switch

PIN CONFIGURATION

TO-252-2L



PART MARKING





SPN12T20

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PIN DESCRIPTION

Pin	Symbol	Description
1	G	Gate
2	D	Drain
3	S	Source

ORDERING INFORMATION

Part Number	Package	Part Marking
SPN12T20T252RGB	TO-252-2L	SPN12T20

※ SPN12T20T252RGB : Tape Reel ; Pb – Free ; Halogen - Free

ABSOLUTE MAXIMUM RATINGS

(T_A=25°C Unless otherwise noted)

Parameter		Symbol	Typical	Unit
Drain-Source Voltage		V _{DSS}	200	V
Gate –Source Voltage		V _{GSS}	±20	V
Continuous Drain Current(T _J =150°C)	T _A =25°C	I _D	18	A
	T _A =100°C		12	
Pulsed Drain Current		I _{DM}	40	A
Avalanche Energy, Single Pulse@0.3mH, V _{dd} =25V, I _{AS} =10A		E _{AS}	15	mJ
Power Dissipation	T _A =25°C	P _D	83	W
Operating Junction Temperature		T _J	-55/150	°C
Storage Temperature Range		T _{STG}	-55/150	°C
Thermal Resistance-Junction to Ambient		R _{θJA}	60	°C/W



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ELECTRICAL CHARACTERISTICS

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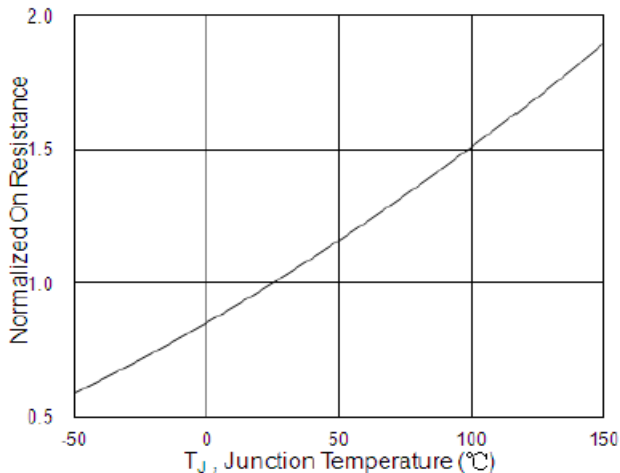
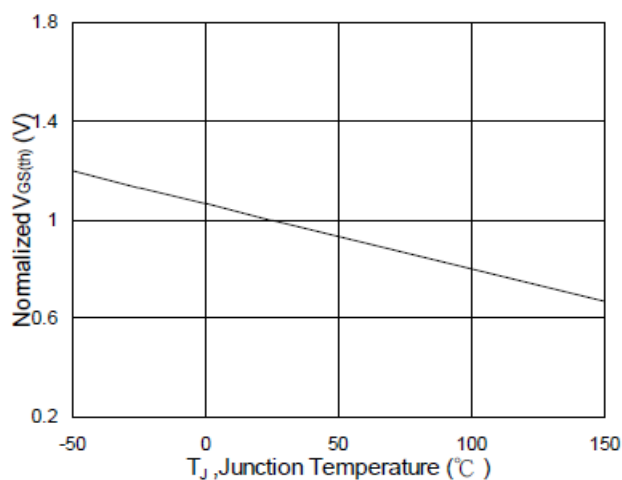
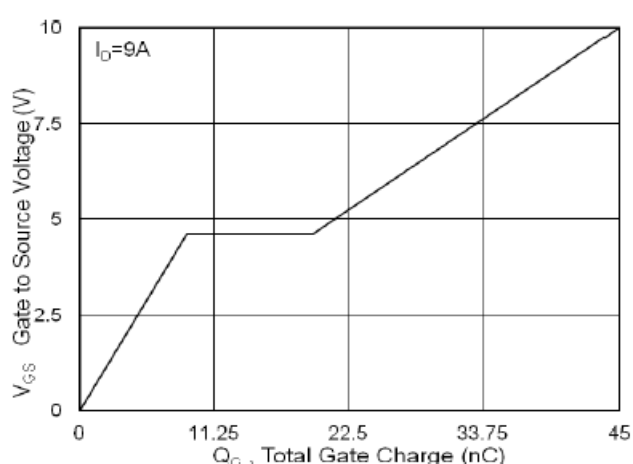
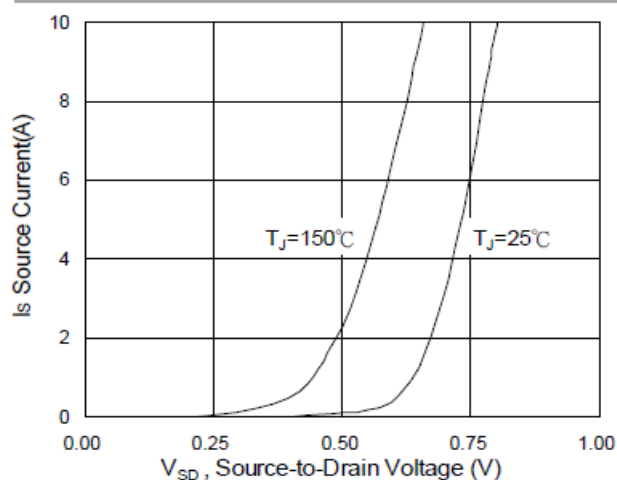
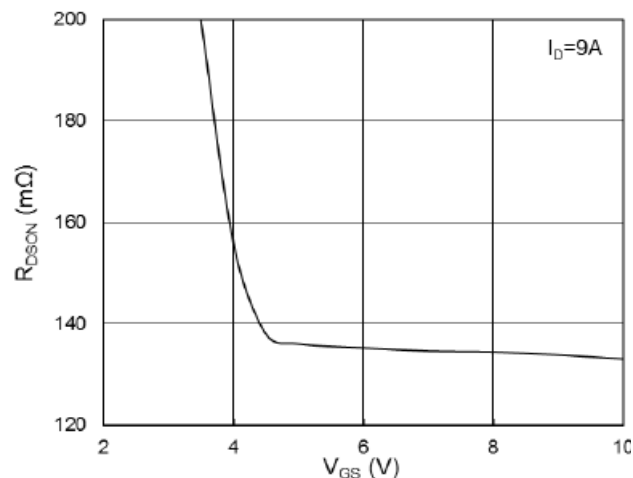
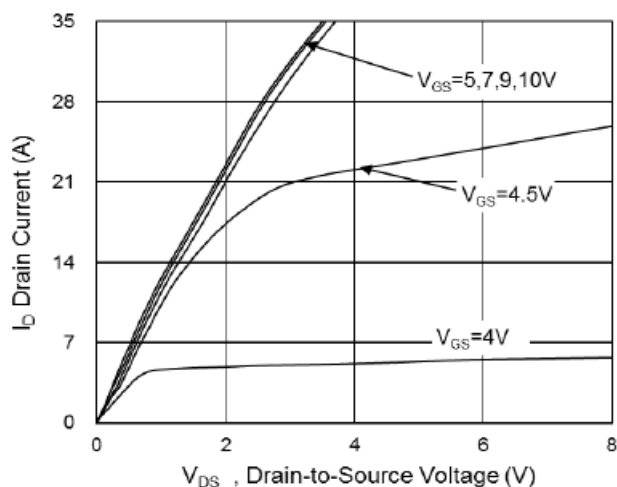
Parameter	Symbol	Conditions	Min.	Typ	Max.	Unit
Static						
Drain-Source Breakdown Voltage	V _{(BR)DSS}	V _{GS} =0V, I _D =250μA	200			V
Gate Threshold Voltage	V _{GS(th)}	V _{DS} =V _{GS} , I _D =250μA	1.2		2.5	
Gate Leakage Current	I _{GSS}	V _{DS} =0V, V _{GS} =±20V			±100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =160V, V _{GS} =0V T _J =25°C			1	μA
		V _{DS} =160V, V _{GS} =0V T _J =55°C			5	
Drain-Source On-Resistance	R _{DS(on)}	V _{GS} =10V, I _D =9A			210	mΩ
Forward Transconductance	g _{fs}	V _{DS} =5V, I _D =9A		22		S
Gate Resistance	R _g	V _{DS} =0V, V _{GS} =0V, f=1MHz		2		Ω
Diode Forward Voltage	V _{SD}	I _S =1A, V _{GS} =0V			1.2	V
Dynamic						
Total Gate Charge	Q _g	V _{DS} =80V, V _{GS} =10V I _D =9A		45		nC
Gate-Source Charge	Q _{gs}			9		
Gate-Drain Charge	Q _{gd}			10.5		
Input Capacitance	C _{iss}	V _{DS} =25V, V _{GS} =0V f=1MHz		2047		pF
Output Capacitance	C _{oss}			109		
Reverse Transfer Capacitance	C _{rss}			70		
Turn-On Time	t _{d(on)}	V _{DD} =50V, I _D =9A, V _{GEN} =10V, R _G =3.3Ω		13		nS
	t _r			8.2		
Turn-Off Time	t _{d(off)}			25		
	t _f			11		



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TYPICAL CHARACTERISTICS





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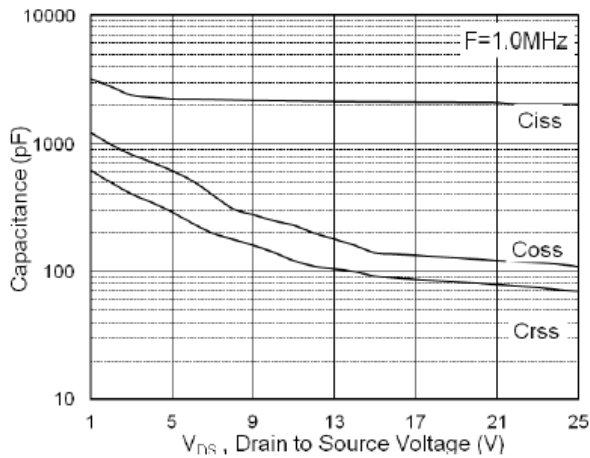


Fig.7 Capacitance

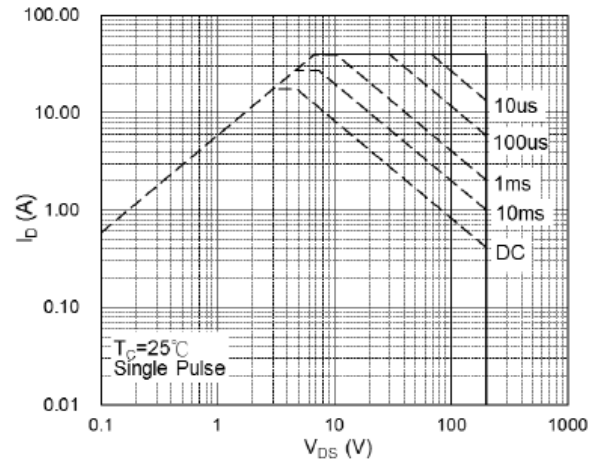


Fig.8 Safe Operating Area

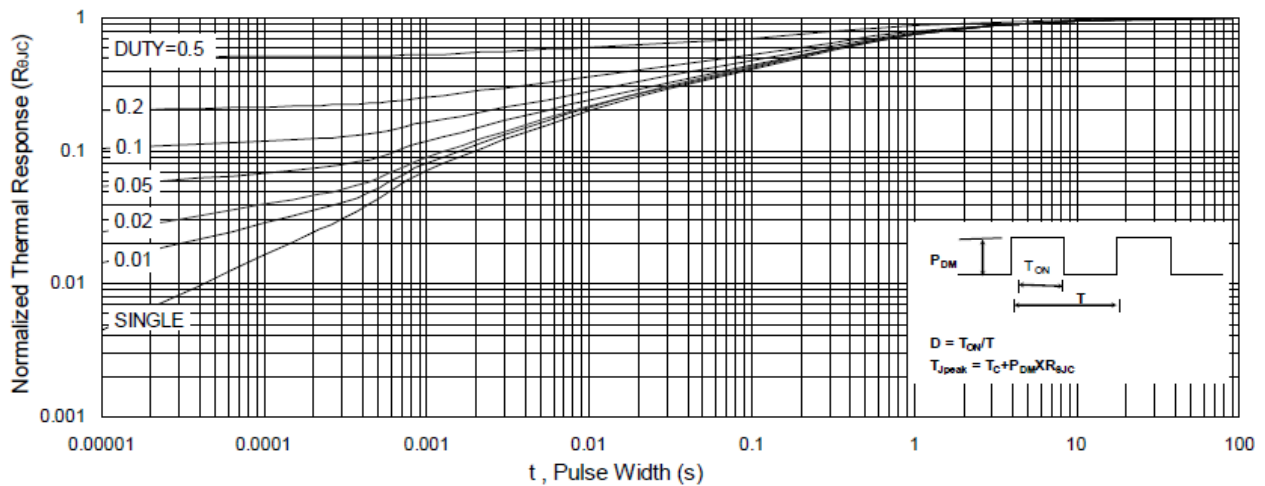


Fig.9 Normalized Maximum Transient Thermal Impedance

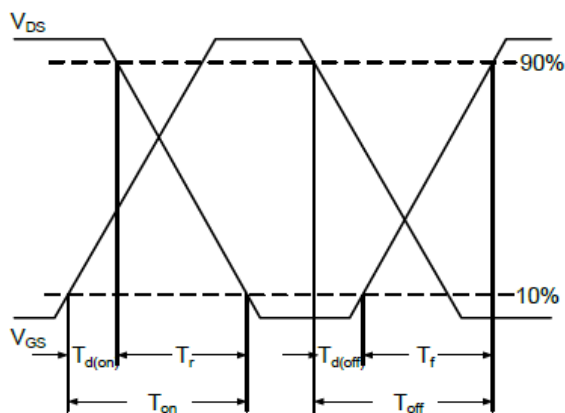


Fig.10 Switching Time Waveform

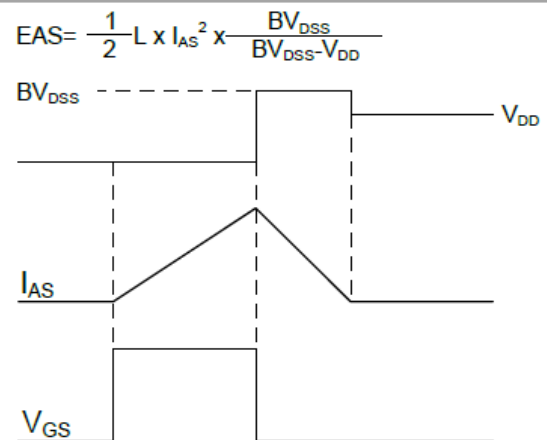


Fig.11 Unclamped Inductive Switching Waveform



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