Sunplus SPL191A2 Data Sheet

2001/06/12

Version 1.1

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256KB LCD CONTROLLER/DRIVER

1. GENERAL DESCRIPTION

The SPL191A2 is an 8-bit CMOS microprocessor containing 704 bytes working RAM, 256K bytes ROM, 12 I/Os, interrupt/wakeup controller, UART for serial communication, and automatic display controller/driver for LCD. It has one PWM driver with two audio channel outputs. Attractive sound effects can easily be generated. Its large ROM area can be used to store both program and audio data (speech duration is approx. 69 seconds at a 7KHz sampling rate using a 4-bit ADPCM). The built-in UART speeds up data transmission between two chips. Furthermore, a SLEEP (power-down) feature is also built-in to reduce power consumption. The SPL191A2 is designed with state-of-the-art technology to fulfill LCD application requirements, especially hand-held products.

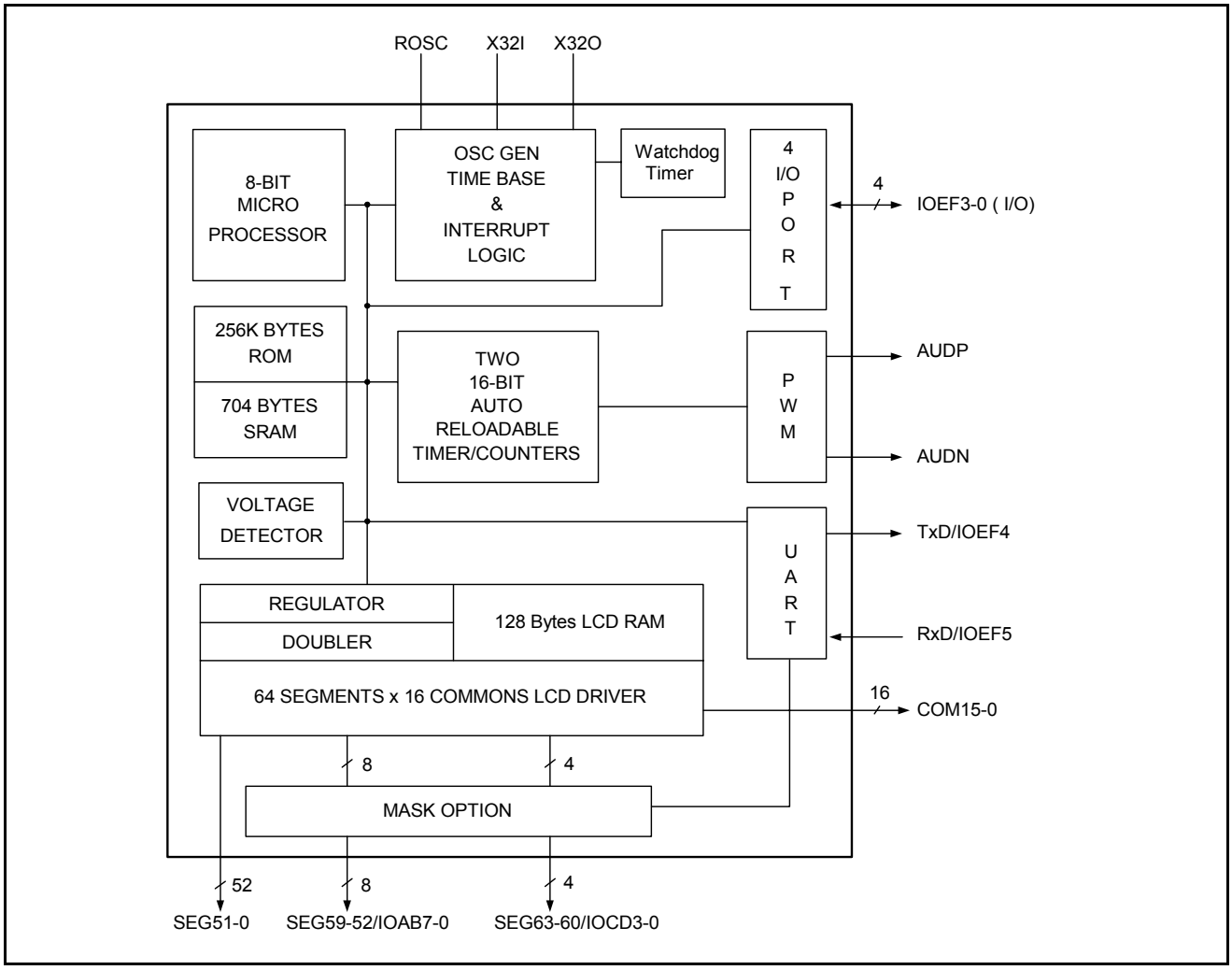
2. FEATURES

- Built-in 8-bit processor
  - **704 bytes SRAM**
  - **256K bytes ROM**
  - Max. operating speed: 3.0MHz @ 2.6V
  - CPU clock is software programmable, can be 1/2, 1/4, 1/8 or 1/16 R-oscillator clock frequency
  - Key wake-up function
  - Provides 8 interrupt sources
- Asynchronous serial interface (UART)
  - Supports bit rates up to 115.2 Kbps
- Programmable LCD driver
  - **Up to 64 segments, up to 16 commons, maximum 1024 dots**
  - 1/4 or 1/5 bias capability
  - 1/8, 1/12 or 1/16 duty
  - **128 bytes dedicated LCD RAM**
  - LCD com/seg driving strength can be adjusted to compromise the display quality and current consumption
  - Built-in voltage doubler and voltage regulator to generate VLCD for LCD driver
  - 16-level VLCD adjustable (3.3V - 4.8V)
- Power saving SLEEP mode (wake-up source: key input, 2Hz, 16Hz, and timer)
- **Low voltage detector**
  - **2.6V and 2.4V detection**
- Wide operating voltage:
  - 2.4V - 3.6V
  - 3.6V - 5.5V
- Peripherals
  - **12 I/O pins shared with LCD segments (mask option)**
  - **4 I/O pins (IOEF3 - 0)**
  - **Extra 2 general I/O pins (IOEF5 - 4) or 2 UART pins (TXD - RXD) (mask option)**
  - **Extra 2 I/O pins (IOEF7 - 6) if LCD is 1/8 or 1/12 duty (mask option)**
  - Built-in 32.768KHz oscillator circuit for real time clock function
  - Built-in R-oscillator (only one resistor is needed)
  - Internal time base generator
  - Two 16-bit reloadable timer/counters(TM0 & TM1)
  - **8-bit DAC resolution, 2-channel PWM audio output outputs (can drive speaker or buzzer directly)**
  - Watchdog Timer for reliable operation
- Low-power consumption:
  - 1mA typical @ 3V, F_{CPU} = 1.0MHz
  - <1μA typical standby current @ 3.0V

3. APPICATION FIELD

- Hand held games
- Scientific calculator
- Talking calculator, Talking clock
- Talking instrument controller
- General speech synthesizer
- Data Bank

4. BLOCK DIAGRAM



Note1: IOAB7 - 0 can be enabled by mask option from Segment 59 - 52. Each I/O(segment) can be mask optioned individually.
Note2: IOCD3 - 0 can be applied as segment 63 - 60 by mask option. Each I/O corresponds to one segment.
Note3: Common 15 - 12 can be optioned to IOEF7 - 6 when LCD driving type is selected as 1/8 duty or 1/12 duty.
Note4: TxD and RxD can be optioned to IOEF5 - 4 when UART is not used.

5. SIGNAL DESCRIPTIONS

Mnemonic	PIN No.	Type	Description
SEG3 - 0 SEG51 - 4 SEG63 - 52	1 - 4 54 - 101 37 - 48	O	LCD driver segment output SEG59 - 52 can be re-assigned as IOAB7 - 0 bi-directional I/O ports. Also, SEG60 - 63 can be re-assigned as IOCD3 - 0 bi-directional I/O port. (mask option)
COM13 - 0 COM15 - 14	18 - 5 29 - 30	O	LCD driver common output. COM15 - 14 can be re-assigned as IOEF7 - 6 bi-directional I/O port. (mask option)
IOEF3 - 0	33 - 36	I/O	Port EF is a bi-directional I/O port, can be software programmed as wake up I/O.
RxD	31	I	UART input. Can be optioned to IOEF5
TxD	32	O	UART output. Can be optioned to IOEF4
ROSC	28	I	ROSC input, connect to VDD through a resistor
RESET	22	I	System reset input, low active.
AUDP AUDN	50 51	O	PWM audio output
X32I	25	I	32.768KHz crystal input or connect to VDD through a resistor (option)
X32O	24	O	32.768KHz crystal output
TEST	23	I	Test input
VLCD	26	P	LCD voltage. Connect to VSS through a capacitor if voltage doubler is enabled.
HVLCD	21	P	LCD voltage generation. Connect to VSS through a capacitor if voltage regulator is enabled.
CPU1 CPU2	20 19	P	LCD voltage generation. Charge pump capacitor interconnection pins
VDD	27	P	Power supply voltage input
VSS	53	P	Ground reference
AVDD	49	P	Analog power
AVSS	52	P	Analog ground reference

Legend: I = Input, O = Output, P = Power

6. FUNCTIONAL DESCRIPTIONS

6.1. ROM Area

The SPL191A2 is a large ROM based micro-controller with 1024 dots LCD driver. The large ROM can be defined as program ROM, LCD fonts and audio data continuously without any limitation. To access ROM, users should program the Bank Select register, choose bank, and then access bank address to fetch data.

6.2. Map of Memory and I/Os

***I/O PORT:**

- PORT IOAB $0002
- PORT IOCD $0003
- PORT IOEF $0004
- I/O AB_CTRL $0001
- I/O CD_CTRL $0000
- I/O EF_CTRL $0006

***NMI SOURCE:**

- INT1 (from TIMER 1)

***INT SOURCE:**

- INT0 (from TIMER 0)
- INT1 (from TIMER 1)
- 2 KHz
- T2 Hz (2Hz / 1 Hz)
- T16 Hz (4Hz/8Hz/16Hz/32Hz)
- 128 Hz
- EXT INT (from IOCD0 pin)
- UART

***MEMORY MAP**

$00000 – $0003F	H/W registers , I/Os
$00040 – $000FF	WORKING SRAM (192 bytes)
$00100 – $002FF	SRAM for STACK and Data Storage (512 bytes)
$00300 – $0037F	LCD Buffer (128 bytes)
$00400 – $007FF	SUNPLUS TEST PROGRAM
$00800 – $07FFF	USER's PROGRAM DATA AREA ROM BANK #0
$08000 – $0FFFF	ROM BANK #1
$10000 – $17FFF	ROM BANK #2
$18000 – $1FFFF	ROM BANK #3
$20000 – $27FFF	ROM BANK #4
$28000 – $2FFFF	ROM BANK #5
$30000 – $37FFF	ROM BANK #6
$38000 – $3FFFF	ROM BANK #7

Note: $7FFA - $7FFF in ROM bank#0, and $FFFA - $FFFF in bank#1 - 7 are reserved for reset vectors.
$7FF2 - $7FF7 in bank#0, and $FFF2 - $FFF7 in bank#1 - 7 are reserved for SUNPLUS testing.

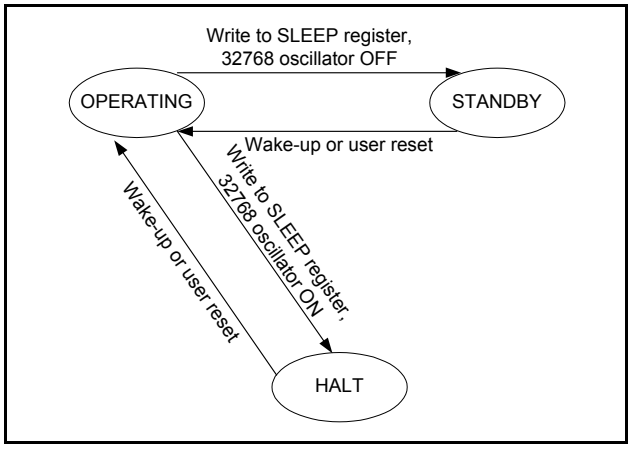
6.3. Operating States

The SPL191A2 supports three operating states: standby, halt, and operating. Following table shows the differences between the three operating states.

	Operating	Halt	Standby
CPU	ON	OFF	OFF
32768 oscillator	ON	ON	OFF
LCD driver	ON	ON/OFF	OFF

In the operating state, all modules (CPU, 32768 oscillator, timer/counter, LCD drive, etc.) are activated. The halt/standby state is entered by writing to the SLEEP register. There are four wake-up sources in SPL191A2: port IOEF wake-up, Timer0 wake-up, 4Hz/8Hz/16Hz/32Hz wake-up and 2Hz/1Hz wake-up. If any wake-up event occurs, execution of the next instruction continues in the operating state.

When in standby, all modules are shut down, and RAM and I/Os remain in their previous states. Current consumption is minimized in standby. By writing to the SLEEP register while the 32768 oscillator running, the system is in halt state. In halt state, CPU clock is halted while it waits for an event (key press, timer overflow) to generate a wake-up. The 32768 related modules (timer/counter, LCD drive, etc.) may remain active in the halt state. The following figure is the SPL191A2 state diagram.



SPL191A2 State Diagram

6.4. Speech and Melody

Since the SPL191A2 provides large ROM and wide range of CPU operating speed, it is most appropriate for speech and melody synthesis. For speech synthesis, SPL191A2 provides several timer interrupts for precise sampling frequency. Users can record or synthesize the sound and digitize it into the ROM. The sound then can be played back in the sequence assigned by the users' programs. Several algorithms are recommended for high fidelity and good compression of sound: such as PCM and ADPCM.

For melody synthesis, the SPL191A2 provides a dual tone mode. Once in the dual tone mode, users need only program the tone frequency of each channel by writing to the timer/counter TM0 and TM1, and set the envelope of each channel. The hardware will toggle the tone wave automatically.

6.5. LCD Controller/Driver

SPL191A2 contains a 1024-dot LCD driver. Programmers can set the LCD configuration (bias, duty, voltage doubler) by writing to LCD control register ($20). Once the LCD configuration is initialized, the desired pattern can be displayed by filling the LCD buffer with appropriate data. The LCD driver can also operate during sleep by keeping 32768 oscillator running. The LCD driver in SPL191A2 is designed to fit most LCD specifications. It can either be programmed as 1/4 or 1/5 bias and the duty is also programmable as 1/8, 1/12, or 1/16 duty.

6.6. Voltage Doubler/Regulator

The SPL191A2 also contains a built-in voltage doubler and a voltage regulator. The voltage regulator provides a reference voltage (HVLCD) for the voltage doubler to generate VLCD (by charge-pumping). Users can get desired VLCD by changing the output reference voltage (writing to register) of the voltage regulator. By enabling the voltage doubler and regulator, users can get a stable VLCD that will not be affected by VDD. The three possible configurations of voltage doubler and regulator are shown in the following table:

Regulator	Doubler	VLCD
OFF	OFF	VDD (not regulated)
OFF	ON	2*VDD (not regulated)
ON	OFF	N/A
ON	ON	3.3V - 4.8V adjustable

6.7. PWM Output

Internally, the SPL191A2 has one pair of PWM outputs with two sound channels. Each channel can be set to play speech or tone individually. SPL191A2 uses Pulse Width Modulation that could directly drive speaker or buzzer without any buffer or amplification circuit.

6.8. Asynchronous Serial Interface (UART)

The SPL191A2 supports a 1-channel UART for serial communications. It supports bit rates up to 115.2kbps. UART operation is controlled by UART command registers. Configurations such as Tx/Rx interrupt, parity check, parity even/odd and clock source can be set in command registers. Two interrupts are generated by Rx and Tx. The Rx or Tx interrupt activates when a byte is received or transmitted. By reading the status register, users can tell whether the interrupt is generated by Rx or Tx. Framing, overrun and parity errors are detected as each byte is received. All error status can be read from status register.

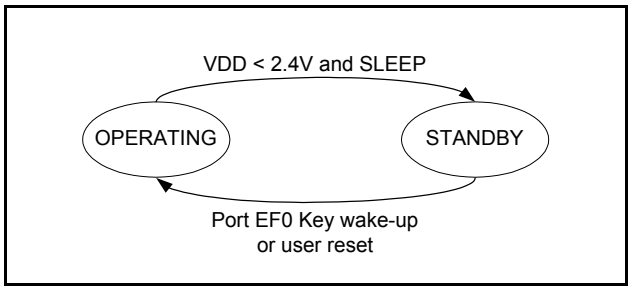
The UART supports clock auto calibration. If this clocking scheme is selected, standard baud rates from 1.2kbps to 115.2kbps are available. The baud rate is selected by writing to baud rate control registers. The supported standard baud rates and their minimum R-oscillator clock frequency required are shown in the following table:

Baud Rate(bps)	Min. Frosc(Hz)
1200	24000
2400	48000
4800	96000
9600	192000
19200	384000
38400	768000
51200	1024000
57600	1152000
102400	2048000
115200	2304000

If the auto calibration clocking scheme is not selected, users can get desired baud rates by writing appropriate values to prescaler registers. Non-standard baud rates can be obtained this way. When using the non-calibration mode, one should be aware that the frequency of R-oscillator may alter due to manufacturing process variations, supply voltage, operating temperature and tolerance of external R components used.

6.9. Low Voltage Detection

The SPL191A2 provides a 2.6V/2.4V voltage detector to detect a low voltage event. Users can turn on 2.6V detection and read bit1 of the port periodically to monitor if VDD is lower than 2.6V. In addition, if 2.4V detection is turned on and VDD drops below 2.4V, after a SLEEP command is issued, system will shut down all activities (LCD bias, LCD display, 32768 oscillator) and enters standby to reduce current consumption. This low voltage power-down can be awakened by a PEF0 key change or RESET. Users can use this feature to implement the low battery check/battery change function.



State Diagram of Low Voltage Power Down

6.10. Watchdog Timer (WDT)

An on chip watchdog timer is available in the SPL191A. The WDT is designed for recovering the system from abnormal operation. If the system is stalled, the WDT will generate a system reset to restart system after 1 second. If WDT is enabled, the WDT should be cleared every 0.5 seconds to avoid accidental reset. The WDT can be cleared by writing to the register. Note that the WDT only works when 32768 Hz clock is available.

6.11. Mask Options

6.11.1. 32768 oscillator

1). X'TAL

2). R-oscillator

6.11.2. Watchdog timer

1). Enable

2). Disable

6.11.3. TxD/RxD select

1). TxD as UART transmit output, RxD as UART receive input

2). TxD as I/O port EF4, RxD as I/O port EF5

6.11.4. Port EF bit7 - 0 with 600K, Pull-Low

Each bit can be optioned to Enable/Disable individually.

6.11.5. I/O and LCD driver

There are some examples shown as below:

Dots	Segment	Common	Input/Output	Input/Output	Input/Output
1024	64	16	4 IOEF3 - 0	-	-
960	60	16	4 IOEF3 - 0	4 IOCD3 - 0	-
832	52	16	4 IOEF3 - 0	4 IOCD3 - 0	8 IOAB7 - 0
768	64	12	8 IOEF3 - 0	-	-

Each input/output port, IOAB7 - 0 and IOCD3 - 0, can be optioned to LCD segments independently, and LCD commons (COM15 - 12) can be optioned to IOEF7 - 6 when LCD mode is 1/8 duty or 1/12 duty. If UART is not used, 2 more I/O ports (TxD/IOEF4, RxD/IOEF5) can be used.

7. ELECTRICAL SPECIFICATIONS

7.1. Absolute Maximum Ratings

Characteristics	Symbol	Ratings
DC Supply Voltage	V_+	< 7.0V
Input Voltage Range	V_{IN}	-0.5V to V+ + 0.5V
Operating Temperature	T_A	0℃ to +60℃
Storage Temperature	T_{STO}	-50℃ to +150℃

Note: Stresses beyond those given in the Absolute Maximum Rating table may cause operational errors or damage to the device. For normal operational conditions see AC/DC Electrical Characteristics.

7.2. DC Characteristics

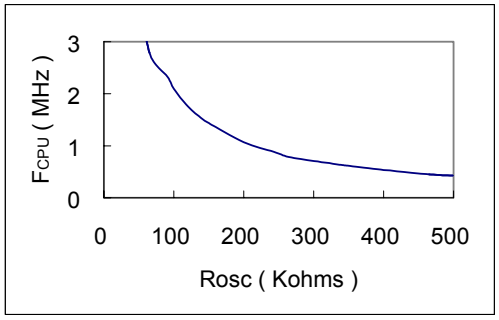
Characteristics	Symbol	Limit			Unit	Test Condition
		Min.	Typ.	Max.		
Operating Voltage	VDD	2.4	-	3.6	V	For 2-battery
		3.6	-	5.5	V	For 3-battery
Operating Current	I_{OP}	-	1.0	-	mA	F_{CPU} = 1.0MHz @ 3.0V, no load
Standby Current	I_{STBY}	-	1.0	2.0	μA	VDD = 3.0V, 32768Hz OFF
Audio Output Current	I_{OH}	-	-15	-	mA	VDD = 3.0V, V_{OH} = 2.5V
		-	-30	-	mA	VDD = 3.0V, V_{OH} = 2.0V
Audio Output Current	I_{OL}	-	25	-	mA	VDD = 3.0V, V_{OL} = 0.5V
		-	50	-	mA	VDD = 3.0V, V_{OL} = 1.0V
VLCD Variation	V_{LCD_VAR}	-	±0.2	-	V	VDD = 2.6V - 5.0V, V_{LCD} = 4.5V LCD bias strength = $04 No LCD panel applied
Low Voltage Detection Level	V_{LV26}	2.45	2.60	2.75	V	
Input High Level	V_{IH}	2.0	-	-	V	VDD = 3.0V
Input Low Level	V_{IL}	-	-	0.8	V	VDD = 3.0V
Output High Current (I/O)	I_{OH}	-	-1.0	-	mA	VDD = 3.0V, V_{OH} = 2.4V
Output Sink Current (I/O)	I_{OL}	-	6.0	-	mA	VDD = 3.0V, V_{OL} = 0.8V
OSC Resistor	R_{OSC}	-	200K	-	ohm	F_{OSC2} = 2.0MHz @ 3.0V
CPU Clock	F_{CPU}	-	-	3.0	MHz	F_{CPU} = F_{OSC2}/2 @ 2.6V

Note1: VLCD variation is subject to change due to the variation of process, temperature, supply voltage and loadings.

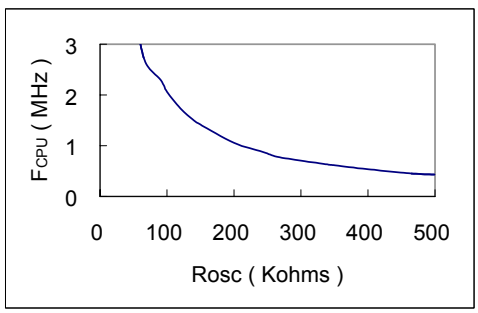
Note2: When voltage regulator and voltage doubler are enabled, VDD should be lower than VLCD to prevent forward biasing the p-n junction of I/O output PMOS.

7.3. The Relationship Between the R_{OSC} and The F_{CPU}

7.3.1. VDD = 3.0V , T_A = 25℃

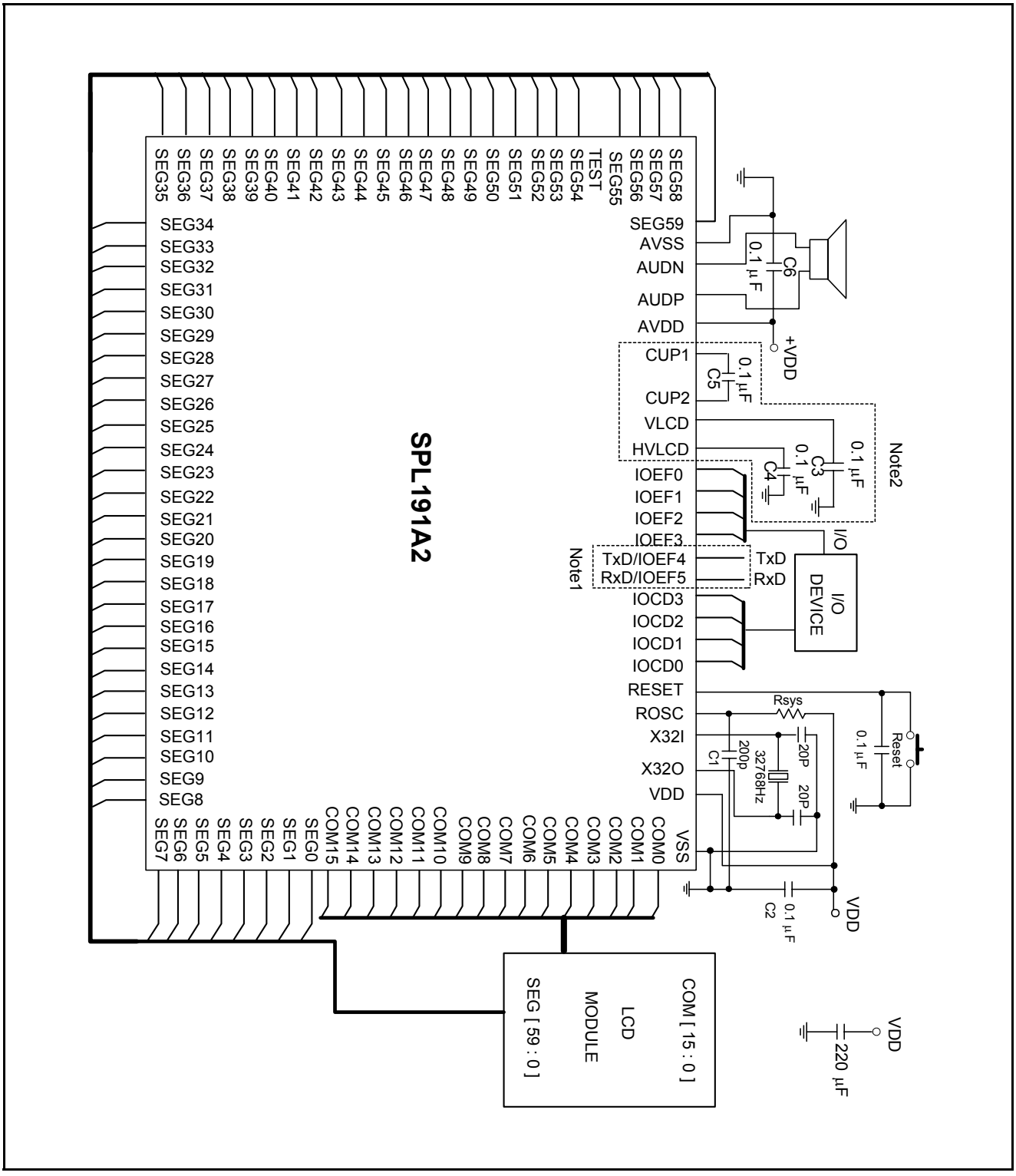


7.3.2. VDD = 5.0V , T_A = 25℃



8. APPLICATION CIRCUITS

8.1.1. 960 Points LCD Driver, 60 Segments × 16 Commons



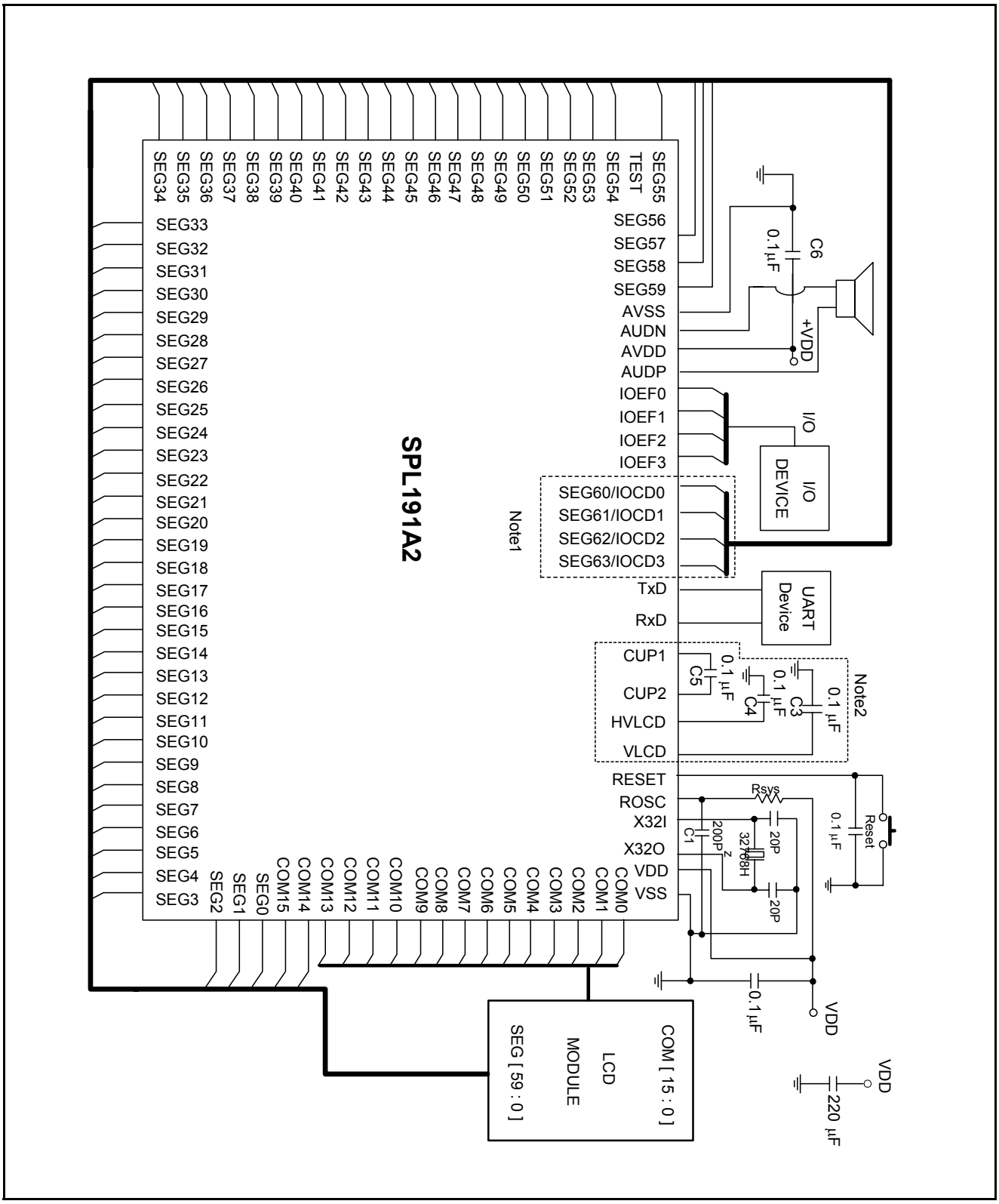
Note1: IOEF4, IOEF5 are shared with TxD, RxD(UART), if UART is not used, these two pins can be used as I/O ports

Note2: These capacitors must be connected if voltage doubler and voltage regulator are used.

Note3: Wire route path from capacitors (C6 - 1) to chip should be as close as possible.

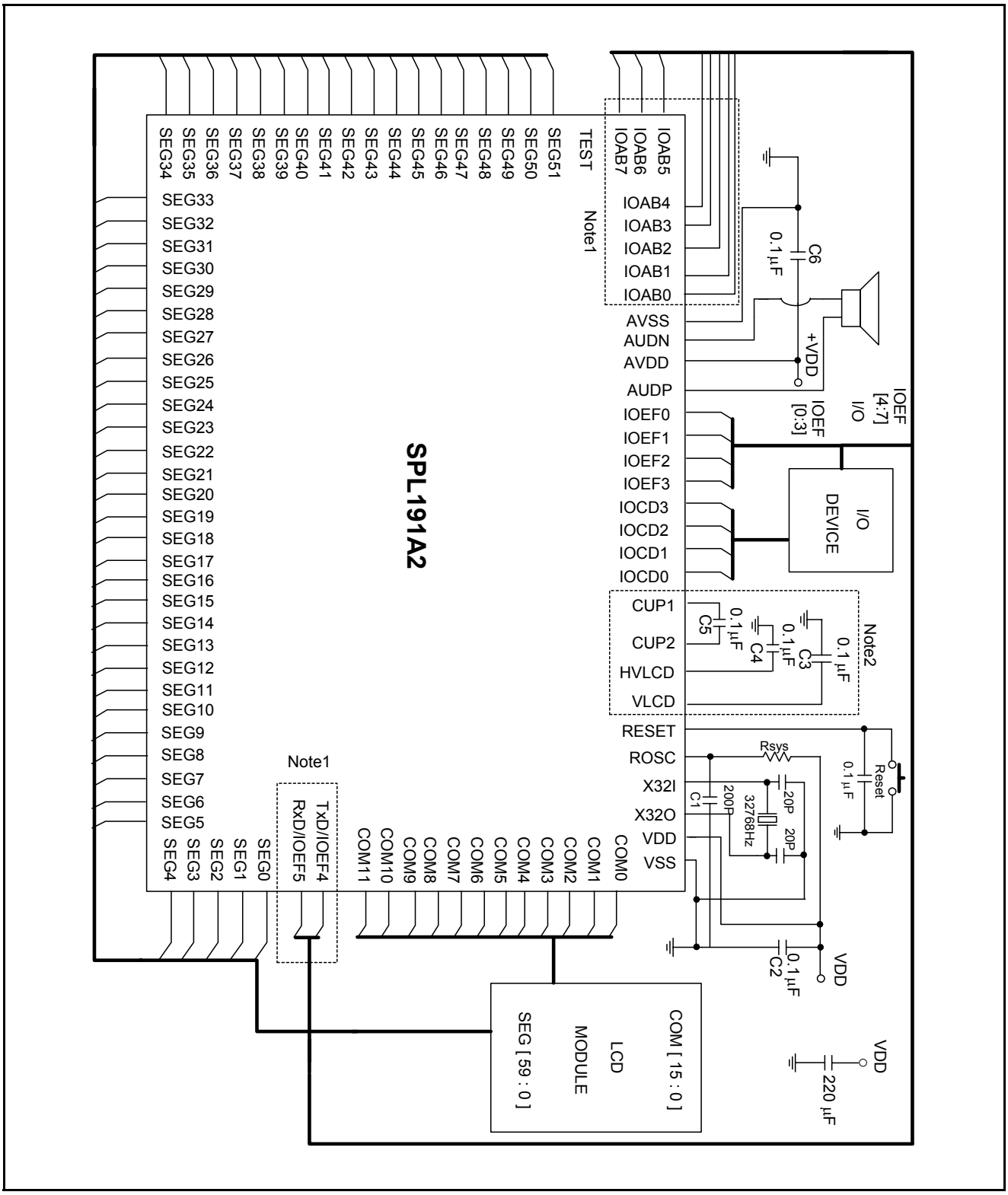
Note4: If voltage doubler and voltage regulator are not used, VLCD should be connected to VDD.

8.2. 1024 Points LCD Driver, 64 Segments × 16 Commons



Note1: IOCD3 - 0 can be mask-option for segment 63 - 60.
Note2: These capacitors must be connected if voltage doubler and voltage regulator are used.
Note3: Wire route path from capacitors (C6 - 1) to chip should be as close as possible.
Note4: If voltage doubler and voltage regulator are not used, VLCD should be connected to VDD.

8.3. LCD in 1/8 Duty or 1/12 Duty, IOAB7 - 0, IOCD3 - 0, IOEF5 - 0



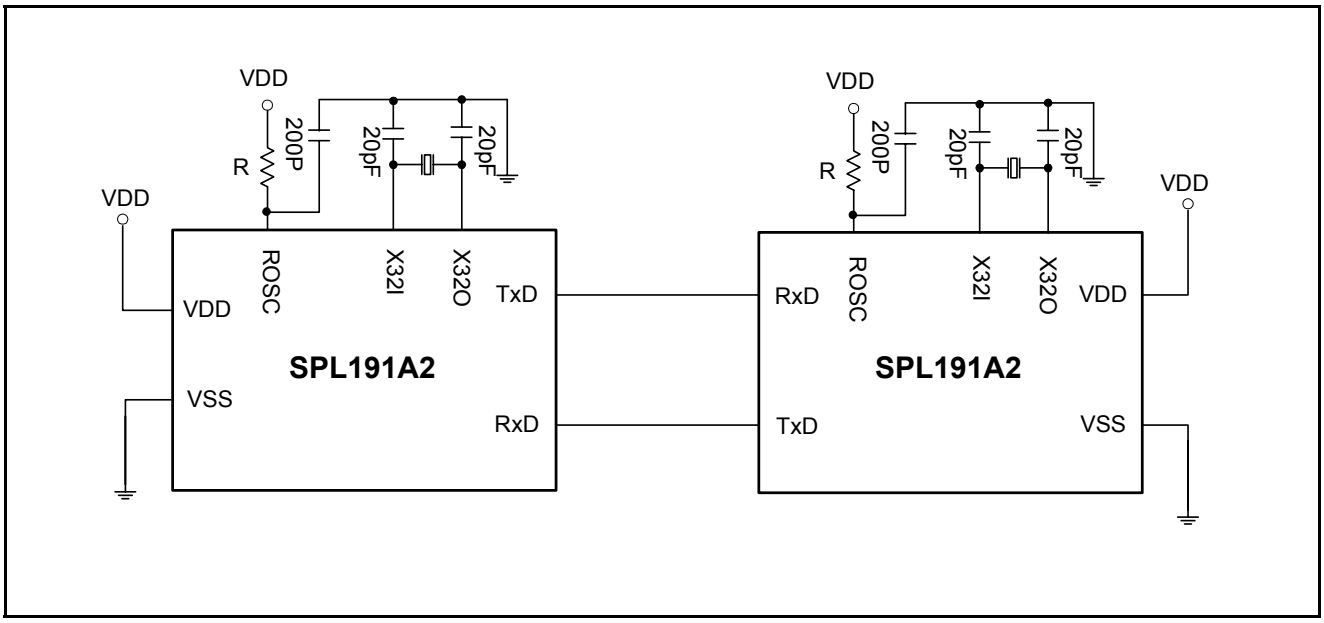
Note1: SEG59 - 52 can be mask-option for IOAB7 - 0.
TxD and RxD can be used for IOEF4, IOEF5 when UART is not used.

Note2: These capacitors must be connected if voltage doubler and voltage regulator are used.

Note3: Wire route path from capacitors (C6 - 1) to chip should be as close as possible.

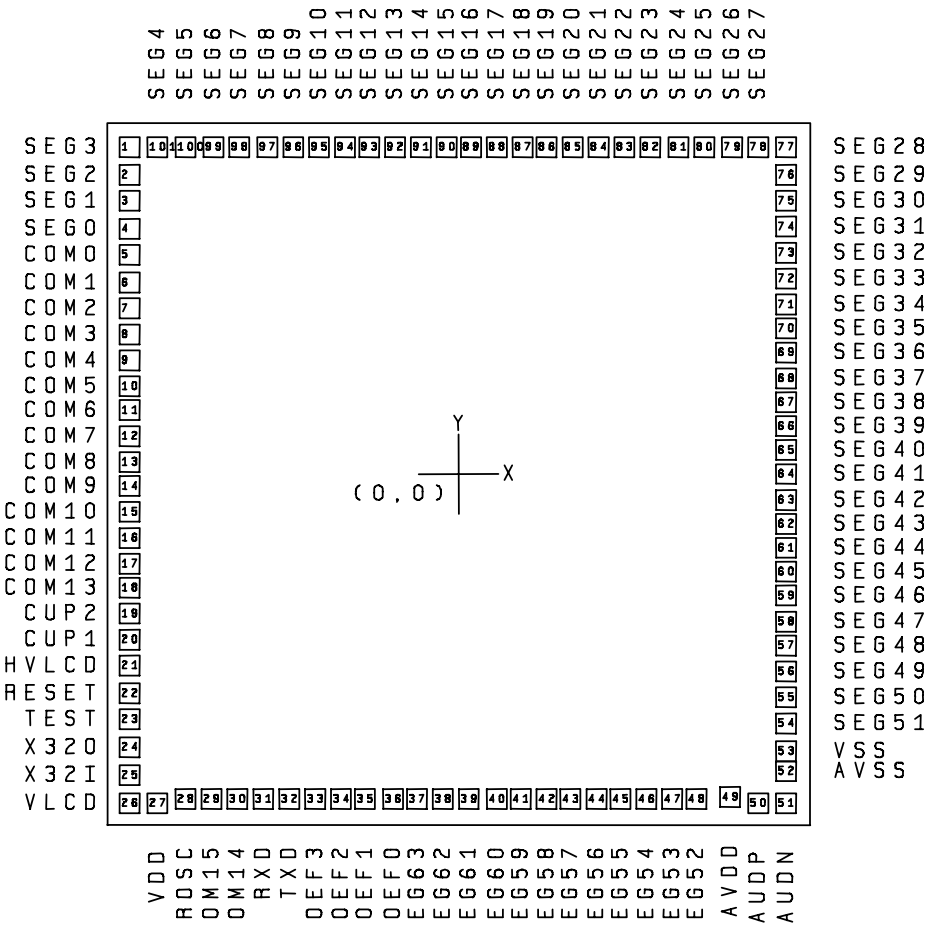
Note4: If voltage doubler and voltage regulator are not used, VLCD should be connected to VDD.

8.4. Serial Communications Between Two SPL191A2s



9. PACKAGE/PAD LOCATIONS

9.1. PAD Assignment



Chip Size: 3630μm x 3630μm

This IC substrate should be connected to VSS

Note1: chip size included scribe line.

Note2: The 0.1μF capacitor between VDD and VSS should be placed to IC as close as possbile.

9.2. Ordering Information

Product Number	Package Type
SPL191A2-nnnnV-C	Chip form

Note1: Code number (nnnnV) is assigned for customer.

Note2: Code number (nnnn = 0000 - 9999); version (V = A - Z).

9.3. PAD Locations

PAD No.	PAD Name	X	Y	PAD No.	PAD Name	X	Y
1	SEG3	-1646	1645	44	SEG56	690	-1627
2	SEG2	-1646	1505	45	SEG55	815	-1627
3	SEG1	-1646	1368	46	SEG54	941	-1627
4	SEG0	-1646	1231	47	SEG53	1066	-1627
5	COM0	-1646	1096	48	SEG52	1192	-1627
6	COM1	-1646	962	49	AVDD	1364	-1621
7	COM2	-1646	830	50	AUDP	1497	-1646
8	COM3	-1646	698	51	AUDN	1645	-1646
9	COM4	-1646	571	52	AVSS	1645	-1492
10	COM5	-1646	444	53	VSS	1645	-1386
11	COM6	-1646	317	54	SEG51	1645	-1254
12	COM7	-1646	190	55	SEG50	1645	-1122
13	COM8	-1646	63	56	SEG49	1645	-993
14	COM9	-1646	-64	57	SEG48	1645	-863
15	COM10	-1646	-191	58	SEG47	1645	-736
16	COM11	-1646	-318	59	SEG46	1645	-614
17	COM12	-1646	-445	60	SEG45	1645	-492
18	COM13	-1646	-572	61	SEG44	1645	-370
19	CUP2	-1646	-699	62	SEG43	1645	-248
20	CUP1	-1646	-831	63	SEG42	1645	-126
21	HVLCD	-1646	-963	64	SEG41	1645	-4
22	RESET	-1646	-1098	65	SEG40	1645	118
23	TEST	-1646	-1232	66	SEG39	1645	240
24	X32O	-1646	-1369	67	SEG38	1645	362
25	X32I	-1646	-1506	68	SEG37	1645	484
26	VLCD	-1646	-1646	69	SEG36	1645	606
27	VDD	-1506	-1646	70	SEG35	1645	728
28	ROSC	-1365	-1627	71	SEG34	1645	855
29	COM15	-1239	-1627	72	SEG33	1645	982
30	COM14	-1106	-1627	73	SEG32	1645	1111
31	RXD	-981	-1627	74	SEG31	1645	1241
32	TXD	-848	-1627	75	SEG30	1645	1373
33	IOEF3	-723	-1627	76	SEG29	1645	1505
34	IOEF2	-590	-1627	77	SEG28	1645	1645
35	IOEF1	-465	-1627	78	SEG27	1505	1645
36	IOEF0	-332	-1627	79	SEG26	1368	1645
37	SEG63	-207	-1627	80	SEG25	1231	1645
38	SEG62	-78	-1627	81	SEG24	1096	1645
39	SEG61	47	-1627	82	SEG23	962	1645
40	SEG60	189	-1627	83	SEG22	830	1645
41	SEG59	314	-1627	84	SEG21	698	1645
42	SEG58	439	-1627	85	SEG20	571	1645
43	SEG57	564	-1627	86	SEG19	444	1645

PAD No.	PAD Name	X	Y	PAD No.	PAD Name	X	Y
87	SEG18	317	1645	95	SEG10	-699	1645
88	SEG17	190	1645	96	SEG9	-831	1645
89	SEG16	63	1645	97	SEG8	-963	1645
90	SEG15	-64	1645	98	SEG7	-1098	1645
91	SEG14	-191	1645	99	SEG6	-1232	1645
92	SEG13	-318	1645	100	SEG5	-1369	1645
93	SEG12	-445	1645	101	SEG4	-1506	1645
94	SEG11	-572	1645				

10. DISCLAIMER

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11. REVISION HISTORY

Date	Revision #	Description	Page
JAN. 11, 2000	0.1	Original	
JUN. 20, 2000	0.2	1. Modify "*7.2 DC Characteristics*" 2. Modify "*7.3 The relationship between the R_{OSC} and the F_{CPU}*" 3. Modify Grammar 4. Modify Note1 in the "*8. Application Circuits*"	
OCT. 17, 2000	1.0	1. Delete "*PRELIMINARY*" 2. Correct Wide operating voltage: 2.4V - 3.4V -> 2.4V - 3.6V	
JUN. 12, 2001	1.1	1. Add Low Voltage Detection Level in the *"7.2 DC Charactertics*" 2. Correct chip size 3. Add "*11. REVISION HISTORY*" 3. Renew to a new document format	8 13 17