

### DESCRIPTION

The SPE1212 are designed by TVS device that is to protect sensitive electronics from damage or latch-up due to ESD. They are designed for use in applications where board space is at a premium. SPE1212 will protect up to two lines, and may be used on lines where the signal polarities swing above and below ground.

SPE1212 offer desirable characteristics for board level protection including fast response time, low operating and clamping voltage, and no device degradation.

SPE1212 may be used to meet the immunity requirements of IEC 61000-4-2, level 4. The small SOT-523 package makes them ideal for use in portable electronics such as cell phones, PDA's, notebook computers, and digital cameras.

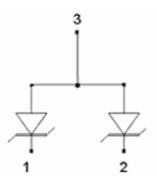
## APPLICATIONS

- Cellular Handsets and Accessories
- Cordless Phone
- ♦ PDA
- Notebooks and Handhelds
- Portable Instrumentation
- Digital Cameras
- MP3 Player

### FEATURES

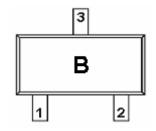
- Transient protection for data lines to IEC 61000-4-2 (ESD) ±15kV (air), ±8kV (contact) IEC 61000-4-4 (EFT) 40A (5/50ns)
- Protects two I/O lines
- Working voltage: 12V
- Low leakage current
- Low operating and clamping voltages

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PIN CONFIGURATION (SOT-523 / SC-89)

### PART MARKING





### **ORDERING INFORMATION**

| Part Number  | Package | Part Marking |
|--------------|---------|--------------|
| SPE1212S52RG | SOT-523 | В            |

※ SPE1212S52RG : Tape Reel ; Pb − Free

## ABSOULTE MAXIMUM RATINGS

(TA=25°C Unless otherwise noted)

| Parameter  | Symbol | Typical     | Unit |
|--|--------|-------------|------|
| Peak Pulse Power ( $tp = 8/20 \ \mu s$ )           | Ppk    | 250         | W    |
| Maximum Peak Pulse Current ( $tp = 8/20 \ \mu s$ ) | Ірр    | 8           | А    |
| ESD per ICE 61000 – 4 – 2 (Air )                   | Vpp    | ±15         | KV   |
| ESD per ICE 61000 – 4 – 2 (Contact )               | Vpp    | $\pm 8$     | KV   |
| Operating Junction Temperature                     | TJ     | -55 ~ 150   | °C   |
| Storage Temperature Range                          | Tstg   | -55 ~ 150   | °C   |
| Lead Soldering Temperature                         | TL     | 260 (10sec) | °C   |

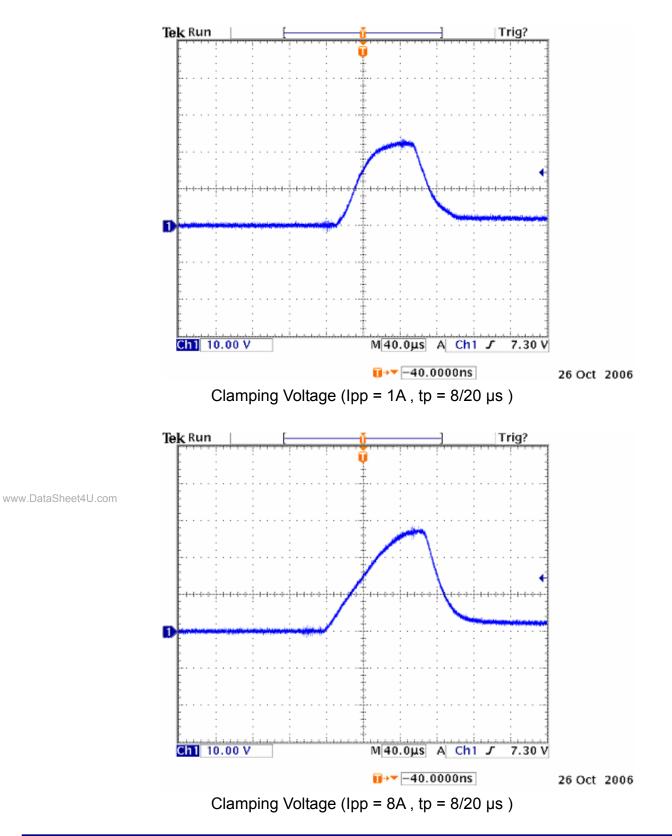
## **ELECTRICAL CHARACTERISTICS**

(TA=25 C Unless otherwise noted)

| Parameter                   | Symbol | Conditions                                      | Min. | Тур | Max. | Unit |
|-----------------------------|--------|---|------|-----|------|------|
| Reverse Stand – Off Voltage | Vrwm   |   |      |     | 12   | V    |
| Reverse Breakdown Voltage   | VBR    | It = 1mA  | 13.3 |     |      | V    |
| Reverse Leakage Current     | Ir     | $V_{RWM} = 12V$ , $T=25^{\circ}C$               |      |     | 1    | μΑ   |
| Clamping Voltage            | Vc     | Ipp = 1A , tp = $8/20 \ \mu s$                  |      |     | 19   | V    |
| Clamping Voltage            | Vc     | Ipp = 8A , tp = $8/20 \ \mu s$                  |      |     | 25   | V    |
| Junction Capacitance        | Сј     | Between I/O Pin and GND $V_R = 0V$ , $f = 1MHz$ |      | 16  | 20   | pF   |



## TYPICAL CHARACTERISTICS



2006/11/26 Ver.1

# SPE1212 2-Line ESD Protection Array

## TYPICAL CHARACTERISTICS

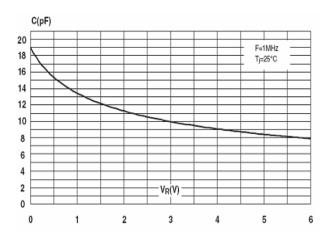


Fig 1 : Junction Capacitance V.S Reverse Voltage Applied

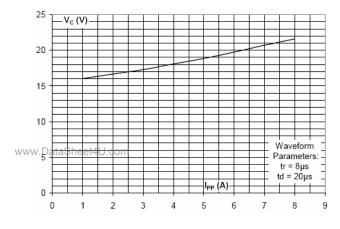


Fig 3 : Clamp Voltage V.S Peak Pulse Current

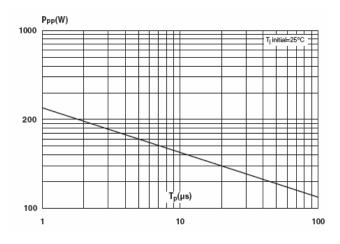


Fig 2 : Peak Plus Power V.S Exponential Plus Duration

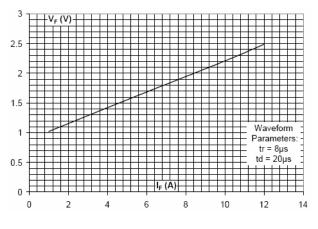


Fig 4 : Forward Voltage V.S Forward Current

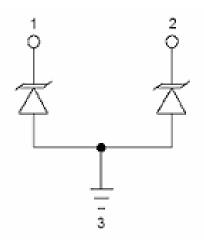


## APPLICATION NOTE

### **Device Connection for Protection of Two Data Lines**

SPE1212 is designed to protect up to two data lines. The device is connected as follows:

1. The TVS protection of two I/O lines is achieved by connecting pins 1 and 2 to the data lines. Pin 3 is connected to ground. The ground connection should be made directly to the ground plane for best results. The path length is kept as short as possible to reduce the effects of parasitic inductance.



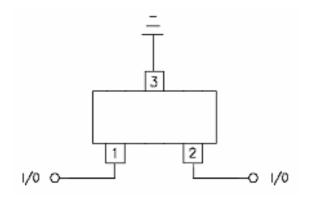
## **Circuit Board Layout Recommendations for Suppression of ESD**

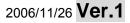
Good circuit board layout is critical for the suppression of ESD induced transients. The following guidelines are recommended:

1. Place the TVS near the input terminals or connectors to restrict transient coupling.

<sup>www</sup>2.<sup>D</sup>Minimize the path length between the TVS and the protected line.

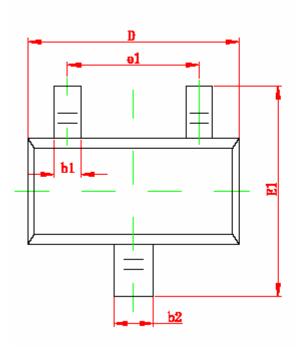
- 3. Minimize all conductive loops including power and ground loops.
- 4. The ESD transient return path to ground should be kept as short as possible.
- 5. Never run critical signals near board edges.
- 6. Use ground planes whenever possible.

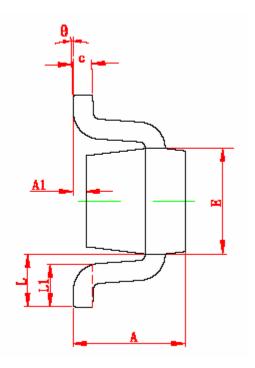


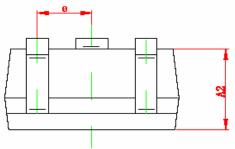




## SOT-523 PACKAGE OUTLINE







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| Symbol | Dimensions In Millimeters |       | Dimensions In Inches |       |  |
|--------|---------------------------|-------|----------------------|-------|--|
|        | Min                       | Max   | Min                  | Max   |  |
| A      | 0.700                     | 0.900 | 0.028                | 0.035 |  |
| A1     | 0.000                     | 0.100 | 0.000                | 0.004 |  |
| A2     | 0.700                     | 0.800 | 0.028                | 0.031 |  |
| b1     | 0.150                     | 0.250 | 0.006                | 0.010 |  |
| b2     | 0.250                     | 0.325 | 0.010                | 0.013 |  |
| С      | 0.100                     | 0.200 | 0.004                | 0.008 |  |
| D      | 1.500                     | 1.700 | 0.059                | 0.067 |  |
| E      | 0.750                     | 0.850 | 0.030                | 0.033 |  |
| E1     | 1.450                     | 1.750 | 0.057                | 0.069 |  |
| е      | 0.500 TYP                 |       | 0.020 TYP            |       |  |
| e1     | 0.900                     | 1.100 | 0.035                | 0.043 |  |
| L      | 0.550 REF                 |       | 0.022 REF            |       |  |
| L1     | 0.280                     | 0.440 | 0.011                | 0.017 |  |
| θ      | 0°                        | 4°    | 0°                   | 4°    |  |



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