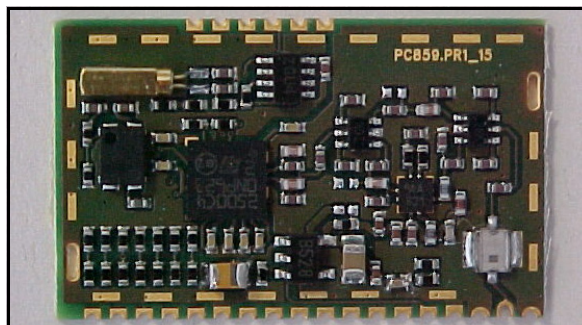




Features

- Bluetooth™ specification compliant V2.0
- Output power class 1 (20 dBm max)
- Transmission rate up to 721 Kbps in BR
- Point-to-point, point-to-multi-point (up to 7 slaves) and scatternet capability
- Asynchronous Connection Oriented (ACL) logical transport link
- Synchronous Connection Oriented link: 2 simultaneous SCO channels capability
- Pitch-Period Error Concealment (PPEC) improves speech quality in the vicinity of interference like e.g. WLAN
- Extended SCO (eSCO) links
- Packet types supported:
 - ACL: DM1, DM3, DM5, DH1, DH3, DH5
 - SCO: HV1, HV3 and DV
 - eSCO: EV3, EV4, EV5
- Adaptive Frequency Hopping (AFH): hopping kernel, channel assessment as master and as slave
- Efficient and flexible support for WLAN coexistence in collocated scenario
- Communication interfaces:
 - Fast UART up to 4 Mbit/s
 - SPI interface
 - PCM interface
- Memory organization:
 - On chip RAM, including provision for patches
 - On chip ROM, preloaded with FW up to HCI
- 3.3 V single supply voltage
- No external oscillator required
- Integrated voltage regulator with Inhibit function.
- Module size: 17 x 29 mm



Description

SPBT2563C1, class 1 radio module is highly integrated for easy implementation in embedded applications. Class 1 module enables wireless communication with other Bluetooth enabled devices up to 100 m away. The SPBT2563C1 integrates on a unique FR4 PCB support: BT 2.0 radio, 32.768 kHz and 26 MHz oscillators, Vreg as well as PA function. The antenna has not been included in order to grant a degree of freedom to the user in selecting the most suitable design and placement between external and integrated antenna that could be SMA aerial or a low cost antenna trace designed on PCB. The module is based on the ST Bluetooth Transceiver STLC2500C and can be interfaced by the host processor by means of a UART or SPI line (selectable by a pin) for HCI transport, and PCM for voice. SPBT2563C1 module implements an add-on feature perfectly fitting in systems equipped with host processor capable to manage upper and lower Bluetooth stack layers, including profiles. ST Bluetooth SPBT2563 series is specifically targeting all those applications requiring Bluetooth devices integrating up to HCI level. Conformance testing through Bluetooth qualification program enables a fast time to market after system integration, by ensuring a high degree of compliance and interoperability.

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1 Certifications

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- BQB qualified component, listed as STLC2563: BQB ID B012391

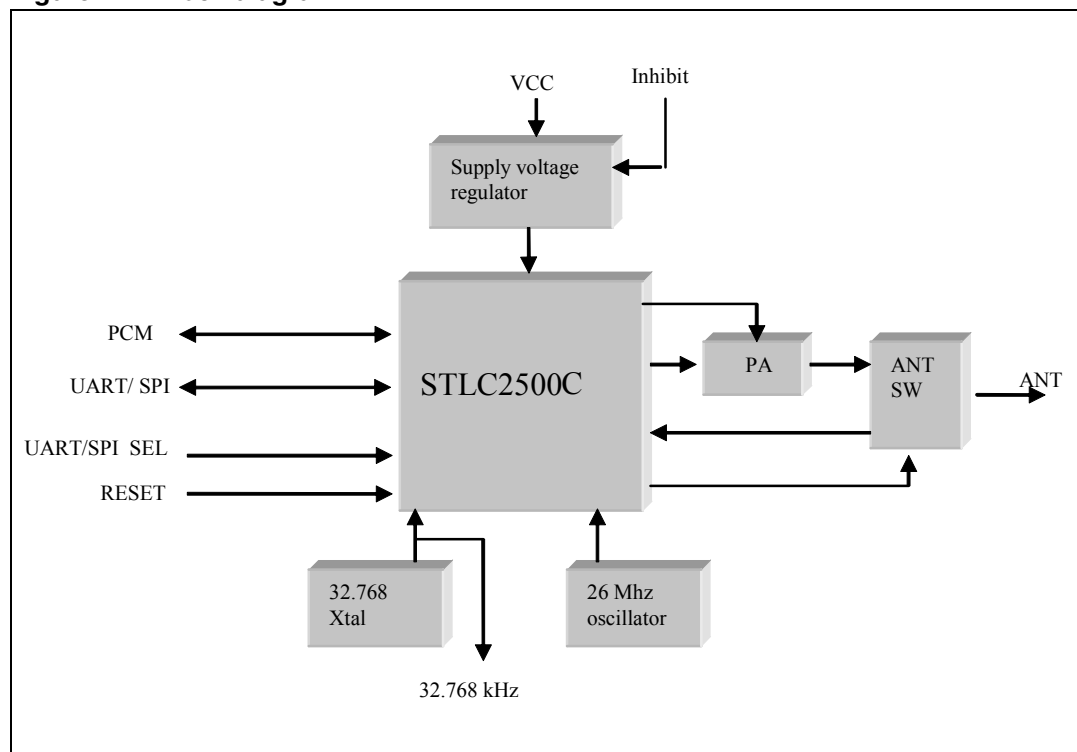
1.1 RoHS compliance

ST modules are RoHS complaint and being based on ST devices comply with ECOPACK® norms implemented by ST.

2 Block diagram

Figure 1. Block diagram

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3 Maximum ratings

3.1 Absolute maximum ratings

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Table 1. Absolute maximum ratings

Symbol	Parameter	Values		Unit
		Min	Max	
V_{CC}	Module supply voltage		4	V
V_{IN}	Input voltage on any digital pin	$V_{SS} - 0.3$	$V_{CC} + 0.3$	V
T_{STG}	Storage temperature	-40	+85	°C
H	Humidity (Not condensing)	0	95	%
T_{sold}	Soldering temperature < 10s		250	°C

3.2 Operating ranges

Operating ranges define the limits for functional operation and parametrics characteristics of the module.

Functionality outside these limits is not implied

Table 2. Operating ranges

Symbol	Parameter	Conditions	Values			Unit
			Min	Typ	Max	
V_{CC}	Module supply voltage	$-20^{\circ}\text{C} < T < 70^{\circ}\text{C}$	3.1	3.3	3.6	V
T_{STG}	Operating ambient temperature		-20		+70	°C
I_{TXBR}	Total supply current in Tx BR	Basic rate, DH1 173kbps (master/slave)		46		mA
I_{RX}	Total supply current in Rx BR	Basic rate, DH1 173kbps (master/slave)		33		mA
$I_{disable}$	Module disabled current.	Enable = L		1		μA

4 DC I/O specification

($V_{dd} = 3.3V$, $T = 25^{\circ}C$, unless otherwise specified)

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Table 3. DC input / output specification

Symbol	Parameter	Conditions	Values			Unit
			Min	Typ	Max	
VIL	Low level input voltage				1.1	V
VIH	High level input voltage		2.15		2.85	V
VOL	Low level output voltage				0.15	V
VOH	High level output voltage		2.55			V
LP_CKH	32.768kHz out high level output voltage		2.4			V
LP_CKL	32.768kHz out low level output voltage				0.3	V
INH_L	Inhibit signal low level				0.15	V
INH_H	Inhibit signal high level		2		V _{cc}	V
I _{inh}	Inhibit input current	V _{inh} = 3.3V		38	55	μA

5 Bluetooth section

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$T_A = 25\text{ }^{\circ}\text{C}$, $V_{CC} = 3.3\text{ V}$ (parameters are given at antenna pin)

Table 4. Bluetooth parameters

Symbol	Parameter	Conditions	Values			Unit
			Min	Typ	Max	
$P_{\text{out-BR}}$	Output power	Basic rate		+16.5	18	dBm
RX_{sensBR}	Sensitivity	Basic rate, clean Tx		-82		dBm
RX_{max}	Max useable input level			10		dBm
Freq	Frequency range		2402		2480	MHz
ΔF	Initial CF tolerance		-75		+75	kHz
$ \Delta f\text{-p1} $	CFD 1 slot packet			15	25	kHz
$ \Delta f\text{-p3} $	CFD 3 slot packet			15	40	kHz
$ \Delta f\text{-p5} $	CFD 5 slot packet			15	40	kHz
$ \Delta f/50\mu\text{s} $	CFD rate				20	kHz/ μs
Hop	Hopping			1600		hops/sec
SYS_CK	System clock			26		MHz
	System clock precision	25 $^{\circ}\text{C}$	-10		+10	ppm
	System clock stability	-20 $^{\circ}\text{C}$ to 70 $^{\circ}\text{C}$	-20		+20	ppm
LP_CK	Low power clock			32.768		kHz
	Low power clock accuracy		-200		+200	ppm
Z	Antenna port impedance	Tx and Rx		50		Ω

Note: Details about Bluetooth features are available at www.st.com, out of the STLC2500C data sheet.

6 Pin settings

Table 5. Pin description

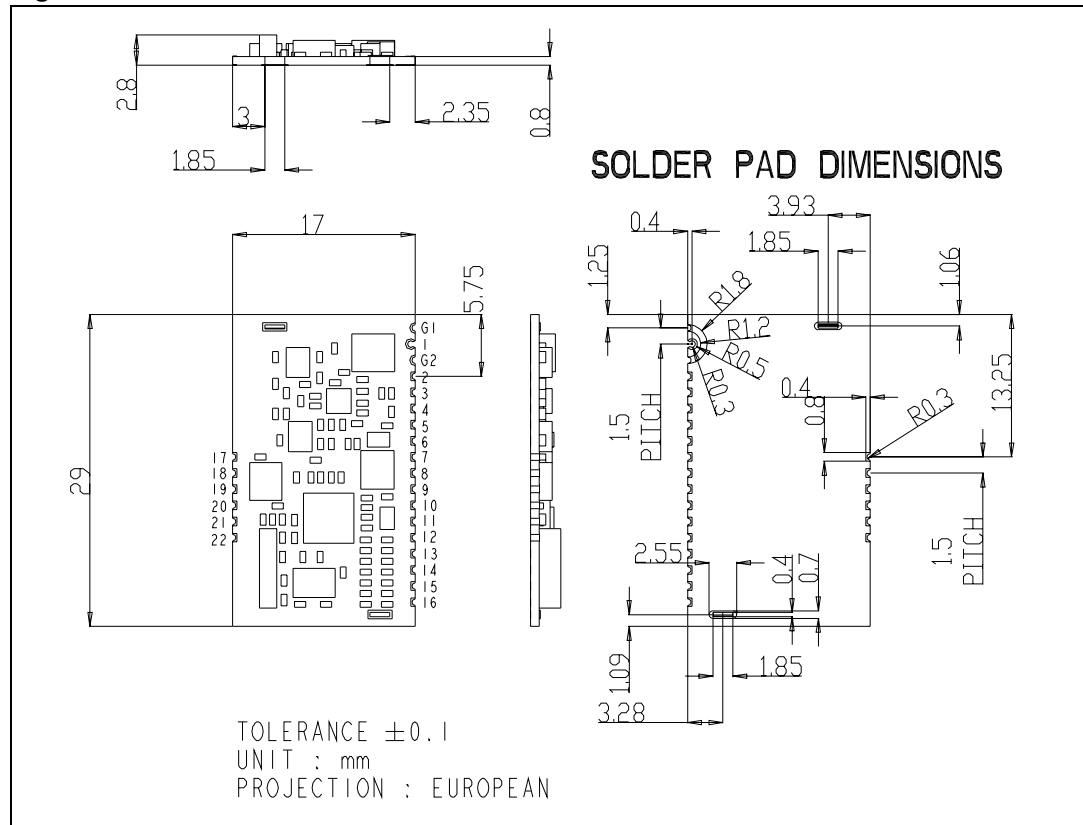
Pin N°	Name	I/O	Description
Power / GND/enable			
12	VCC	-	DC power input 3.3 ± 0.3 V
2	GND	-	
11	GND	-	
3	Inhibit	I	Module inhibit pin , active low. To be connected to V _{CC} for module enabling ; if left open or connected to GND the module is disabled
UART / SPI Interface / Selection			
8	TXD	O	UART serial data output / SPI data out
5	RXD	I	UART serial data input / SPI data in
7	CTS	I	UART clear to send / SPI CK
6	RTS	O	UART request to send / SPI CSN
17	UART / SPI	I	UART / SPI selection When connected to VCC UART is selected When connected to GND or left open , SPI is selected
PCM interface			
15	PCMIN	I	PCM data in
14	PCMOUT	O	PCM data output (tri-state capability)
13	PCMSYNC	I	PCM sync signal
16	PCMBCLK	I	PCM bit clock
RF interface			
1	ANT	I/O	Antenna interface, 50 Ω impedance
G1	ANT_GND	-	Antenna Ground
G2	ANT_GND	-	Antenna Ground
System control and clock interface			
4	RESET_N	I	Reset (active low)
9	BT_WAKEUP	I	Wake-up signal to Bluetooth
10	HOST_WAKEUP	O	Wake-up signal to host
18	NC1		Spare signal (pin G7 of STLC2500C)
19	LP_CK_OUT	O	LP clock out The 32.768 kHz low power clock is available at this pin
WLAN/BT coexistence			
20	BT_PRIORITY	O	WLAN/BT coexistence function
21	WL_ACTIVE	I	WLAN/BT coexistence function
22	RF REQ1	O	pin E6 of STLC2500C

7 Mechanical dimensions

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In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com

Figure 2. Mechanical dimensions



8 Application

8.1 Low-power improvements

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In low power modes, due to the oscillators continuously running, the module current is roughly 2.5 mA (measured at pin 12).

This current consumption can be drastically improved by switching off the two oscillators during low power phases.

This can be done by means of Inhibit function (pin 3) which act directly on the internal power supply regulator ; in this mode the module is no more powered and the current consumption becomes $< 1 \mu\text{A}$ instead of 2.5mA .

8.2 Low power clock startup time

Due to 32.768 Khz oscillator stabilization , when the module is powered on or when enabled (Inhibit from Low to High state) a waiting time of at least 500ms must be observed (Reset signal could be kept Low for the waiting1 time or given after it).

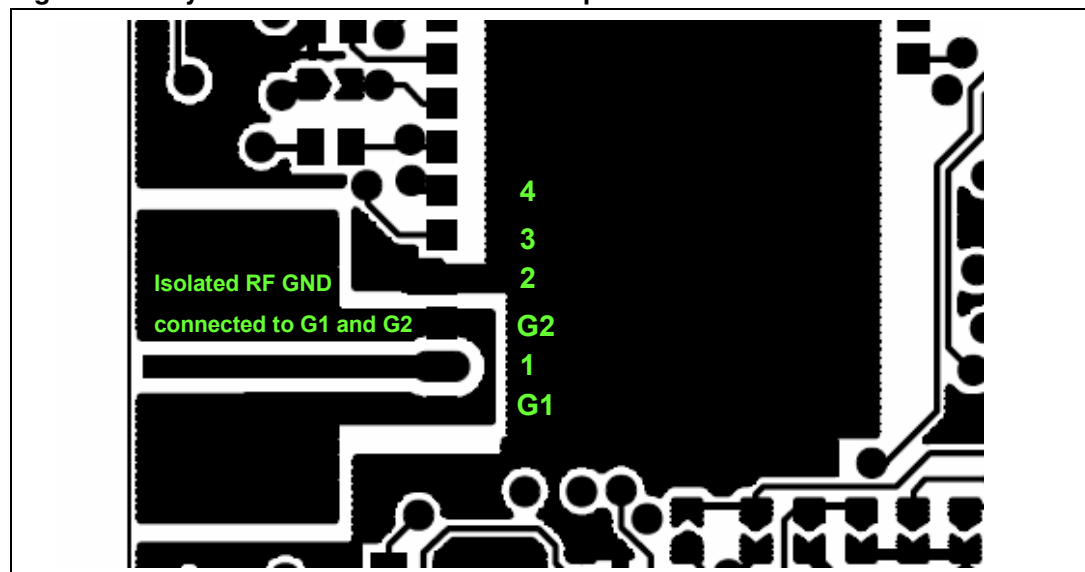
8.3 PCB layout of the antenna output

The microstrip track connected to the antenna (pin 1) should respect a characteristic impedance of $50\ \Omega$. It should be verified particularly if some variations in the final project: dielectric material, tolerances, layout changes.

The RF ground island around the antenna is connected only to G1 and G2 pins of the module. This ground island is isolated from other grounds. The ground plane at lower PCB layer should also be isolated from other grounds.

Vias every 5 millimeters should connect together RF ground islands of each layer.

Figure 3. Layout of the RF track to antenna pin of SPBT2563C1



9 Ordering information scheme

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Table 6. Ordering information scheme

	SPBT	2563	C1
Bluetooth modules			
V 2.0 compliant			
Class 1			

10 Revision history

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Table 7. Document revision history

Date	Revision	Changes
14-Nov-2007	1	First release

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