SPXXHC93
SPXXHC161
SPXXHC163
SPXXHC177
SPXXHC193

Features

- Utilizes SPI's Selective Oxidation, Silicon-Gate CMOS Process.
- Speed, function and pin-out compatible to 74LS series Logic.
- High Noise Immunity.
- Low quiescent power consumption.
- Wide power supply range.
- Operates over V_{CC} range of 2.0 to 6.0 Volts.
- Symmetric current drive.
- All Inputs are fully buffered.
- All devices have Input Protection diodes to V_{CC} and ground.
- All devices have Logic Input voltage levels consistent with CMOS.

All devices contain diodes to protect inputs against damage due to high static voltages or electric fields; however, it is advised that precautions be taken not to exceed the maximum recommended input voltages. All unused inputs must be connected to an appropriate logic voltage level (either V_{CC} or GND).

54/74 Series Binary Counters

Ordering Information

Plastic DIP, Industrial Temp Range	Ceramic DIP, Industrial Temp Range	Ceramic DIP, Military Temp Range
SP74HCXXXN	SP74HCXXXJ	SP54HCXXXJ

Absolute Maximum Ratings

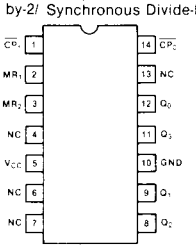
	Parameter	Min	Max	Units
V_{CC}	DC Supply Voltage	−0.5	+7.0	V
V_I, V_O	Input or Output Voltage	−0.5	V_{CC} +0.5	V
I_L	DC Current Per Pin Any Input or Output	—	25	mA
I_{CC}	DC Current Drain, V_{CC} or GND	—	50	mA
T_S	Storage Temperature	−65	+150	°C
P_D	Power Dissipation (Note 1)	—	500	mW
T_L	Lead Temperature (1/16" from mounting surface for 10 sec)	—	+300	°C

Note 1: Derate at 12mW/°C over +45 to +85°C for Plastic "N" Package.

Recommended Operating Conditions

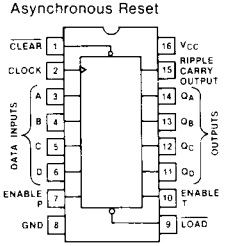
		SP74HCXXX		SP54HCXXX		
	Parameter	Min	Max	Min	Max	Units
V_{CC}	DC Supply Voltage Range	2.0	6.0	2.0	6.0	V
V_I, V_O	Input Voltage, Output Voltage	0	V_{CC}	0	V_{CC}	V
T_A	Operating Temperature Range	−40	+85	−55	+125	°C

SPXXHC93
4-Bit Binary Counter, Divide-by-2/ Synchronous Divide-by-8



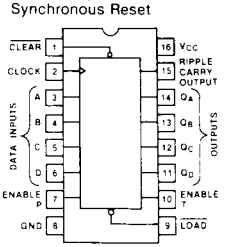
14 PIN DIP
TOP VIEW

SPXXHC161
4-Bit Binary Counter Asynchronous Reset



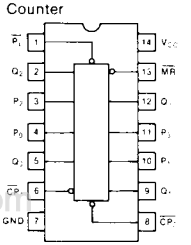
16 PIN DIP
TOP VIEW

SPXXHC163
4-Bit Binary Counter Synchronous Reset



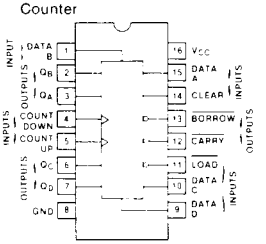
16 PIN DIP
TOP VIEW

SPXXHC177
Presettable Binary Counter



14 PIN DIP
TOP VIEW

SPXXHC193
4-Bit Binary Up/Down Counter



16 PIN DIP
TOP VIEW

DC Electrical Characteristics

Symbol	Parameter	Conditions	V_{CC}	Typ T = 25 °C	Guaranteed Limits SP74HC −40 to +85 °C	Guaranteed Limits SP54HC −55 to +125 °C	Units
V_{IH}	Minimum High Level Input Voltage	V_O = 0.1V or V_{CC} − 0.1V $I_O \leq 20\ \mu A$	2.0V		1.5	1.5	V
			4.5V		3.15	3.15	
			6.0V		4.2	4.2	
V_{IL}	Maximum Low Level Input Voltage	V_O = 0.1V or V_{CC} − 0.1V $I_O \leq 20\ \mu A$	2.0V		0.3	0.3	V
			4.5V		0.9	0.9	
			6.0V		1.2	1.2	
V_{OH}	Minimum High Level Output Voltage	$I_{OH} = 20\ \mu A$ $V_I = V_{CC}$ or GND	2.0V	2.0	1.9	1.9	V
			4.5V	4.5	4.4	4.4	
			6.0V	6.0	5.9	5.9	
		I_{OH} = * $V_I = V_{CC}$ or GND	4.5V		3.7	3.7	V
			6.0V		5.2	5.2	
V_{OL}	Maximum Low Level Output Voltage	$I_{OL} = 20\ \mu A$ $V_I = V_{CC}$ or GND	2.0V	0	0.1	0.1	V
			4.5V	0	0.1	0.1	
			6.0V	0	0.1	0.1	
		I_{OL} = * $V_I = V_{CC}$ or GND	4.5V	0.1	0.3	0.4	V
			6.0V		0.3	0.4	
I_{IN}	Input Leakage Current	$V_I = V_{CC}$ or GND V_{CC} = 2.0 to 6.0V			±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	$V_I = V_{CC}$ or GND, $I_O = 0\ \mu A$, $T_A = 25\,°C$	5.0V	0.1	2.0	2.0	μA
		$T_A = 85\,°C$	5.0V		20.0	20.0	
		$T_A = 125\,°C$	5.0V			40.0	

* 4ma STD outputs 6ma Bus-Drivers

AC Electrical Characteristics (V_{CC} = 5.0V, $t_r = t_f$ = 6ns, T_A = 25 °C, unless otherwise specified)

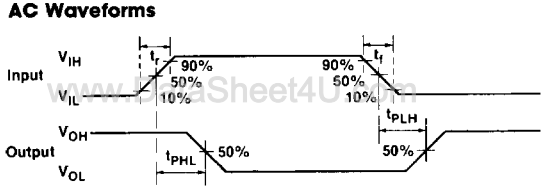
Device Type	Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
93	t_{PHL}, t_{PLH}	$\overline{C}_{P0}$ to Q_0	C_L = 15pF C_L = 50pF	19 21		ns
	t_{PHL}, t_{PLH}	$\overline{C}_{P1}$ to Q_1	C_L = 15pF C_L = 50pF	21 23		ns
	t_{PHL}, t_{PLH}	$\overline{C}_{P0}$ to Q_3	C_L = 15pF C_L = 50pF	37 40		ns
	t_{PHL}	M_R to Q_0	C_L = 15pF C_L = 50pF	25 27		ns
	t_{PHL}	M_R to Q_1	C_L = 15pF C_L = 50pF	24 26		ns
	t_{PHL}	M_{R1} to Q_2	C_L = 15pF C_L = 50pF	24 26		ns
	t_{PHL}	M_R to Q_3	C_L = 15pF C_L = 50pF	24 26		ns
	f_{max}	$\overline{C}_{P0}$ to $\overline{C}_{P1}$		30		MHz
	t_w	Minimum Clock Pulse Width		10		ns
	t_w	Minimum Reset Low Pulse Width		9		ns
161	t_{PHL}, t_{PLH}	Clock to Q_0	C_L = 15pF C_L = 50pF	17 20		ns
	t_{PHL}, t_{PLH}	Clock to Q_1	C_L = 15pF C_L = 50pF	18 21		ns
	t_{PHL}, t_{PLH}	Clock to Q_2	C_L = 15pF C_L = 50pF	19 22		ns
	t_{PHL}, t_{PLH}	Clock to Q_3	C_L = 15pF C_L = 50pF	21 24		ns
	t_{PHL}, t_{PLH}	Clock to T_C	C_L = 15pF C_L = 50pF	28 33		ns
	t_{PHL}, t_{PLH}	Set to T_C	C_L = 15pF C_L = 50pF	18 21		ns
	f_{max}	Max Clock Frequency		40		MHz
	t_w	Minimum Clock Pulse Width		8		ns

CONTINUED ON NEXT PAGE

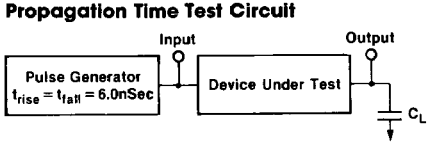
AC Electrical Characteristics (V_{CC} = 5.0V, $t_r = t_f$ = 6ns, T_A = 25°C, unless otherwise specified) CONTINUED

Device Type	Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
163	t_{PHL}, t_{PLH}	Clock to Output $\overline{PE}$ = High	C_L = 15pF C_L = 50pF	23 26		ns
	t_{PHL}, t_{PLH}	Clock to Output $\overline{PE}$ = High	C_L = 15pF C_L = 50pF	23 26		ns
	t_{PHL}, t_{PLH}	Clock to TC	C_L = 15pF C_L = 50pF	35 40		ns
	t_{PHL}, t_{PLH}	CET to TC	C_L = 15pF C_L = 50pF	30 35		ns
	f_{max}	Maximum Clock Frequency		40		Mhz
	t_w	Minimum Clock Width		8		ns
177	t_{PHL}, t_{PLH}	C_{P1} to Q_A	C_L = 15pF C_L = 50pF	22 25		ns
	t_{PHL}, t_{PLH}	C_{P2} to Q_B	C_L = 15pF C_L = 50pF	31 35		ns
	t_{PHL}, t_{PLH}	C_{P2} to Q_C	C_L = 15pF C_L = 50pF	26 28		ns
	t_{PHL}, t_{PLH}	C_{P2} to Q_D	C_L = 15pF C_L = 50pF	28 30		ns
	t_{PHL}, t_{PLH}	D_A to Q_A	C_L = 15pF C_L = 50pF	22 24		ns
	t_{PHL}, t_{PLH}	D_B to Q_B	C_L = 15pF C_L = 50pF	27 31		ns
	t_{PHL}, t_{PLH}	D_C to Q_C	C_L = 15pF C_L = 50pF	24 26		ns
	t_{PHL}, t_{PLH}	D_D to Q_D	C_L = 15pF C_L = 50pF	25 27		ns
	t_{PHL}, t_{PLH}	CLR to Q_A	C_L = 15pF C_L = 50pF	25 27		ns
	t_{PHL}, t_{PLH}	CLR to Q_B	C_L = 15pF C_L = 50pF	29 31		ns
	t_{PHL}, t_{PLH}	CLR to Q_C	C_L = 15pF C_L = 50pF	27 29		ns
	t_{PHL}, t_{PLH}	CLR to Q_D	C_L = 15pF C_L = 50pF	28 30		ns
	f_{max}			45		MHz
	t_w			10		ns
193	t_{PHL}, t_{PLH}	C_{PU} to $\overline{T}_{CU}$	C_L = 15pF C_L = 50pF	25 28		ns
	t_{PHL}, t_{PLH}	C_{PD} to $\overline{T}_{CD}$	C_L = 15pF C_L = 50pF	25 28		ns
	t_{PHL}, t_{PLH}	C_{PU} or C_{PD} to Q_n	C_L = 15pF C_L = 50pF	28 31		ns
	t_{PHL}, t_{PLH}	$\overline{P}_L$ to Q_n	C_L = 15pF C_L = 50pF	16 19		ns
	t_{PHL}	M_R to Output	C_L = 15pF C_L = 50pF	13 16		ns
	f_{max}	Maximum Clock Frequency		40		MHz
	t_w	Minimum Clock Pulse Width		10		ns

AC Waveforms



Propagation Time Test Circuit



Includes Oscilloscope probe and test fixture capacitance C_L = 15pF unless otherwise specified.

Mode Select—Function Tables

HC161

Operating Mode	Inputs						Outputs	
	$\overline{MR}$	CP	CEP	CET	$\overline{PE}$	D_n	Q_n	TC
Reset (Clear)	L	X	X	X	X	X	L	L
Parallel Load	H	↑	X	X	l	l	L	L
	H	↑	X	X	l	h	H	(b)
Count	H	↑	h	h	h(d)	X	count	(b)
Hold (do nothing)	H	X	l(c)	X	h(d)	X	q_n	(b)
	H	X	X	l(c)	h(d)	X	q_n	L

HC163

Operating Mode	Inputs						Outputs	
	$\overline{SR}$	CP	CEP	CET	$\overline{PE}$	D_n	Q_n	TC
Reset (Clear)	l	↑	X	X	X	X	L	L
Parallel Load	h(d)	↑	X	X	l	l	L	L
	h(d)	↑	X	X	l	h	H	(b)
Count	h(d)	↑	h	h	h(d)	X	count	(b)
Hold (do nothing)	h(d)	X	l(c)	X	h(d)	X	q_n	(b)
	h(d)	X	X	l(c)	h(d)	X	q_n	L

HC193

Operating Mode	Inputs								Outputs					
	MR	$\overline{PL}$	CP_U	CP_D	D_0,	D_1,	D_2,	D_3	Q_0,	Q_1,	Q_2,	Q_3	$\overline{TC}_U$	$\overline{TC}_D$
Reset (clear)	H	X	X	L	X	X	X	X	L	L	L	L	H	L
	H	X	X	H	X	X	X	X	L	L	L	L	H	H
Parallel Load	L	L	X	L	L	L	L	L	L	L	L	L	H	L
	L	L	X	H	L	L	L	L	L	L	L	L	H	H
	L	L	L	X	H	H	H	H	H	H	H	H	L	H
	L	L	H	X	H	H	H	H	H	H	H	H	H	H
Count up	L	H	↑	H	X	X	X	X	Count up				H(b)	H
Count down	L	H	H	↑	X	X	X	X	Count down				H	H(c)

HC93

Reset Inputs		Outputs			
MR_1	MR_2	Q_0	Q_1	Q_2	Q_3
H	H	L	L	L	L
L	H	Count			
H	L	Count			
H	L	Count			

HC177

Inputs			
$\overline{MR}$	PL	$\overline{CP}$	Response
L	X	X	Q_n forced LOW
H	L	X	$P_n \rightarrow Q_n$
H	H	⌐	Count Up

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

Truth Table

Count	Output Q_0	Q_1	Q_2	Q_3
0	L	L	L	L
1	H	L	L	L
2	L	H	L	L
3	H	H	L	L
4	L	L	H	L
5	H	L	H	L
6	L	H	H	L
7	H	H	H	L
8	L	L	L	H
9	H	L	L	H
10	L	H	L	H
11	H	H	L	H
12	L	L	H	H
13	H	L	H	H
14	L	H	H	H
15	H	H	H	H

H = HIGH voltage level steady state.
L = LOW voltage level steady state.
h = HIGH voltage level one setup time prior to the LOW-to-HIGH clock transition.
l = LOW voltage level one setup time prior to the LOW-to-HIGH clock transition
X = Don't care
q = Lower case letters indicate the state of the referenced output prior to the LOW-to-HIGH clock transition.
↑ = LOW-to-HIGH clock transition.