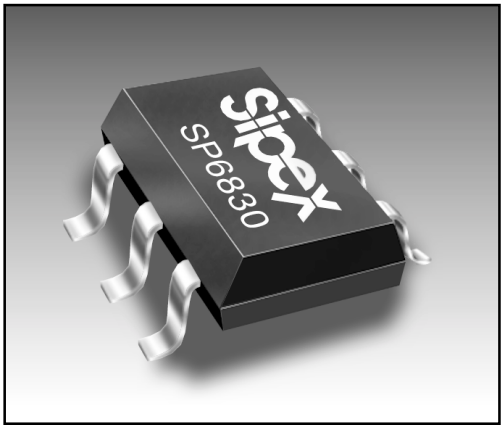
Low Power Voltage Inverters With Shutdown

FEATURES

- 99.9% Voltage Conversion Efficiency
- +1.15V to +5.3V Input Voltage Range
- Inverts Input Supply Voltage
- 70µA Supply Current for the SP6830
- 200µA Supply Current for the SP6831
- 35kHz Operating Frequency for the SP6830
- 120kHz Operating Frequency for the SP6831
- <1µA Shutdown Current
- 6-pin SOT23-6 Package
- Ideal for +3.6V Lithium Ion Battery Applications
- Reverse +3.6V Lithium Ion Battery Protection
- 25mA Output Current
- 19Ω Output Resistance



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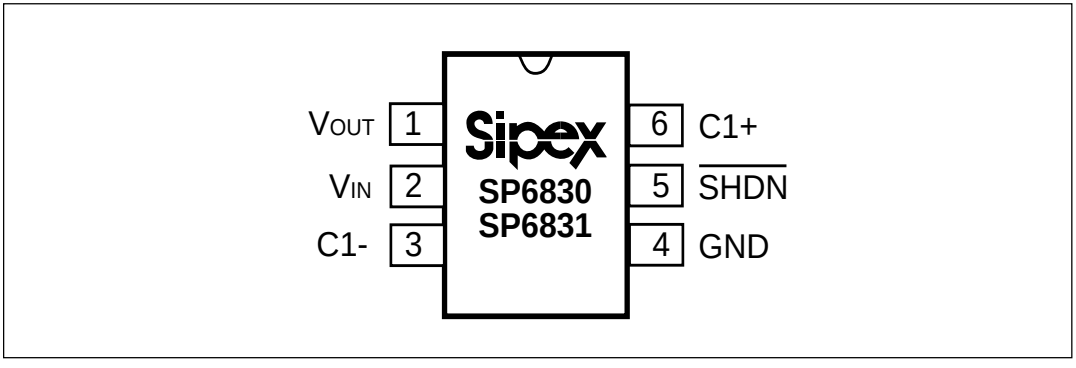
APPLICATIONS

- Small LCD Negative Bias Voltage
- Power Amplifier Negative Bias Voltage
- +5V to -5V Voltage Conversion

DESCRIPTION

The SP6830/6831 devices are CMOS Charge Pump Voltage Inverters that can be implemented into designs which require a negative voltage from a battery voltage source as low as +1.15V or a power supply rail voltage as high as +5.3V. The SP6830/6831 devices are ideal for both battery-powered and board level voltage conversion applications with a typical operating current of 70µA for the SP6830 and 200µA for the SP6831. These devices combine an ultra-low shutdown current of <1µA with high efficiency (>95% over most of its load-current range) which are ideal for designs using batteries such as cell phones, PDAs, medical instruments, and other portable equipment. The SP6830/6831 devices are available in a space-saving 6-pin SOT23-6 Package.

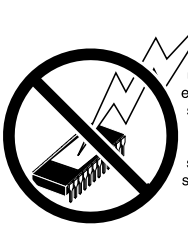


ABSOLUTE MAXIMUM RATINGS

These are stress ratings only and functional operation of the device at these ratings or any other above those indicated in the operation sections of the specifications below is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

V_{IN}.....-0.3V to +5.6V
V_{OUT}.....-5.6V to +0.3V
I_{OUT}.....50mA
Storage Temperature.....-65°C to +150°C
Lead Temperature (Soldering).....300°C

Power Dissipation Per Package
6-pin SOT (derate 4.35mW/°C above +70°C).....400mW



CAUTION:
ESD (ElectroStatic Discharge) sensitive device. Permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. Personnel should be properly grounded prior to handling this device. The protective foam should be discharged to the destination socket before devices are removed.

SPECIFICATIONS

V_{IN} = +5V, C1=C2=C3=3.3µF for the **SP6830**, C1=C2=C3=1µF for the **SP6831**, and T_{AMB}=-40°C to +85°C unless otherwise noted. Typical values are taken specifically at T_{AMB}=+25°C.

PARAMETER	MIN.	TYP.	MAX.	UNITS	CONDITIONS
Supply Voltage Range, V_{DD}	1.15		5.3	V	R_L = 1kΩ
Supply Current, I_{VIN}		70 200	150 400	µA	**SP6830** **SP6831**
Guaranteed Start-up Voltage			1.8	V	R_L = 1kΩ, NOTE1
Shutdown Input Voltage HIGH LOW	1.5		 V_{IN} 0.5	V	 V_{IN} = V_{MIN} to V_{MAX} V_{IN} = V_{MIN} to V_{MAX}
Shutdown Supply Current		0.1	1.0	µA	SHDN = GND, V_{IN} = 5V, NOTE 2
Oscillator Frequency, f_{OSC}	24.5 70	35 120	56.3 200	kHz	**SP6830** **SP6831**
Output Resistance		19	45	Ω	I_{OUT} = 5mA to 25mA, NOTE 3
Voltage Conversion Efficiency	95	99.9		%	R_L = open
Power Efficiency (Ideal)		98		%	R_L = 1kΩ, NOTE 4
Power Efficiency (Actual)		96		%	R_L = 1kΩ, NOTE 5

Note 1: Minimum V_{IN} required for $V_O = -V_{IN} + 0.2V$.

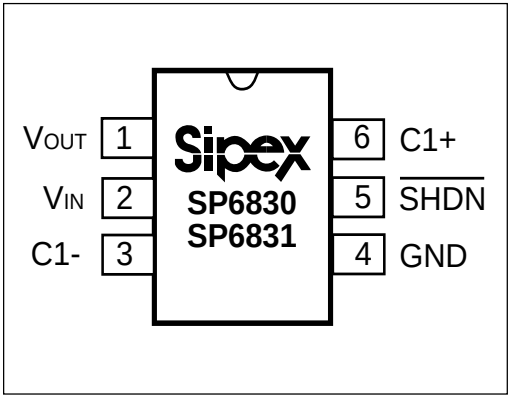
Note 2: During the shutdown mode, V_{IN} is disconnected from V_{OUT}.

Note 3: Capacitors are approximately 20% of the output impedance where ESR = $\frac{1}{f_{OSC} \times C}$.

Note 4: Power Efficiency (Ideal) = $\frac{V_{OUT} \times I_{OUT}}{-V_{IN} \times (-V_{IN}/R_L)}$

Note 5: Power Efficiency (Actual) = $\frac{V_{OUT} \times I_{OUT}}{V_{IN} \times I_{IN}}$

PINOUT



PIN ASSIGNMENTS

Pin 1— V_{OUT} — Inverting charge pump output.

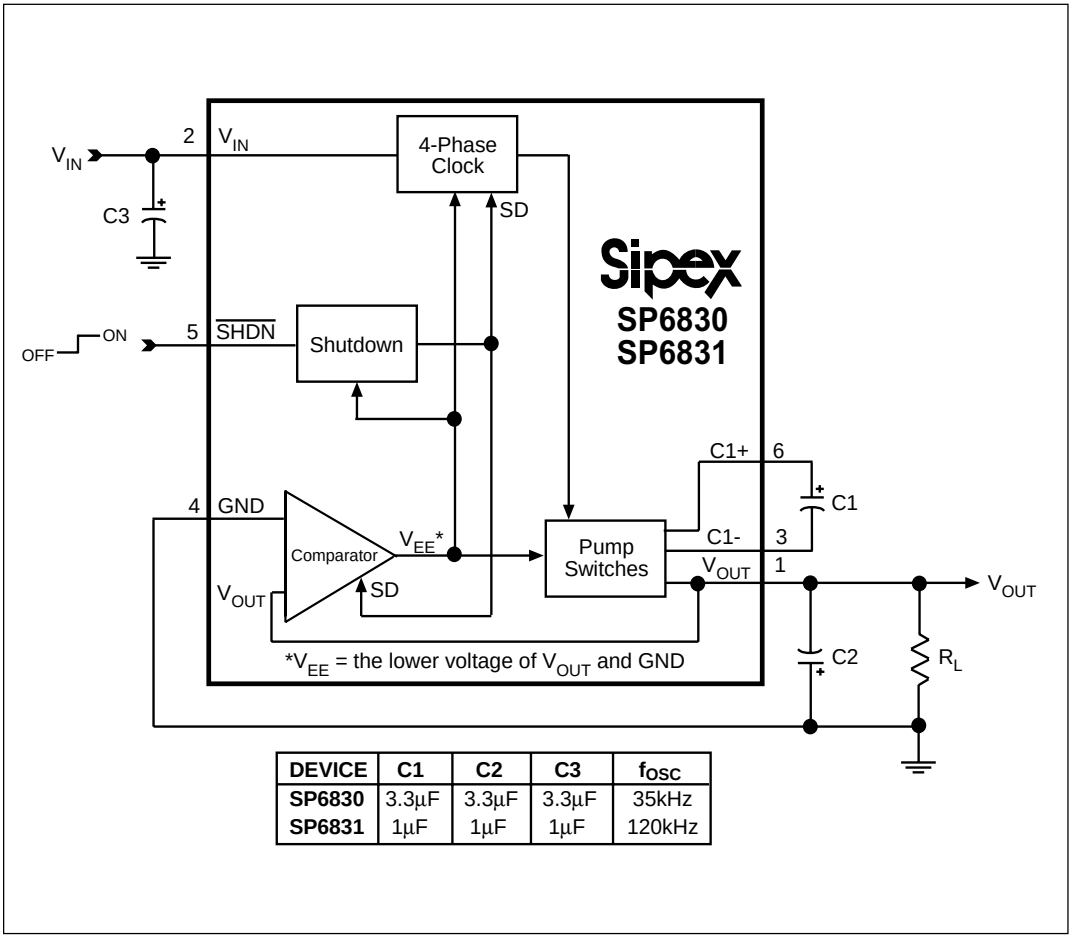
Pin 2 — V_{IN} — Input to the positive power supply.

Pin 3 — C1- — Negative terminal to the charge pump capacitor.

Pin 4 — GND — Ground reference.

Pin 5 — $\overline{SHDN}$ — Active LOW Shutdown input.

Pin 6 — C1+ — Positive terminal to the charge pump capacitor.



DEVICE	C1	C2	C3	f_{OSC}
SP6830	3.3µF	3.3µF	3.3µF	35kHz
SP6831	1µF	1µF	1µF	120kHz

Figure 1. Voltage Inverter Circuit for the SP6830/6831

TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = +5.0V, C1 = C2 = C3 = 3.3µF for **SP6830**, C1 = C2 = C3 = 1µF for **SP6831**, and T_{AMB} = 25°C unless otherwise noted. The **SP6830/6831** devices use the circuit found in *Figure 17* when obtaining the following typical performance characteristics (unless otherwise noted).

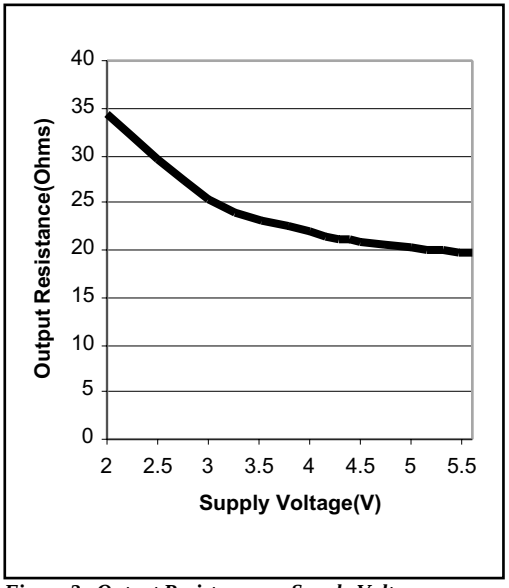


Figure 2. Output Resistance vs. Supply Voltage

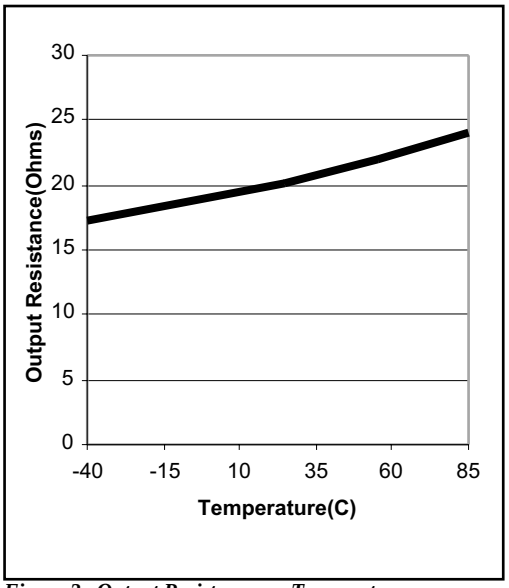


Figure 3. Output Resistance vs. Temperature

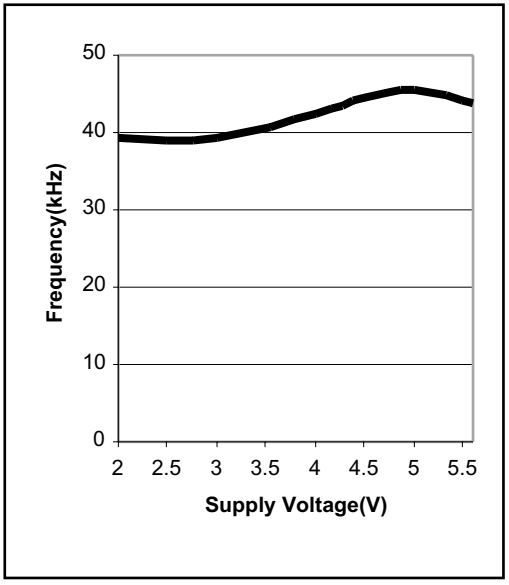


Figure 4. Charge Pump Frequency vs. Supply Voltage for the SP6830

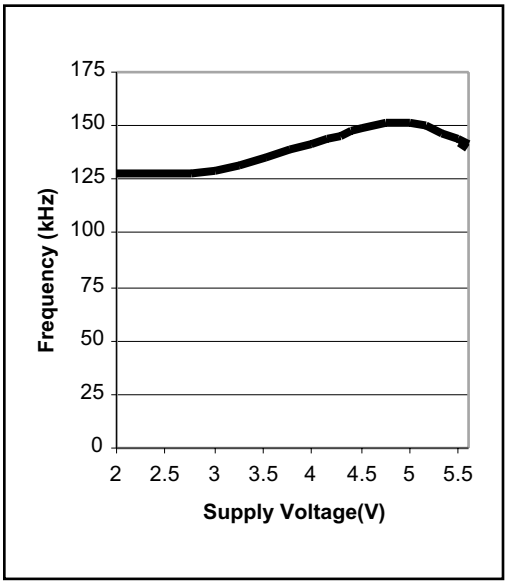


Figure 5. Charge Pump Frequency vs. Supply Voltage for the SP6831

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

V_{IN} = +5.0V, C1 = C2 = C3 = 3.3µF for **SP6830**, C1 = C2 = C3 = 1µF for **SP6831**, and T_{AMB} = 25°C unless otherwise noted. The **SP6830/6831** devices use the circuit found in *Figure 17* when obtaining the following typical performance characteristics (unless otherwise noted).

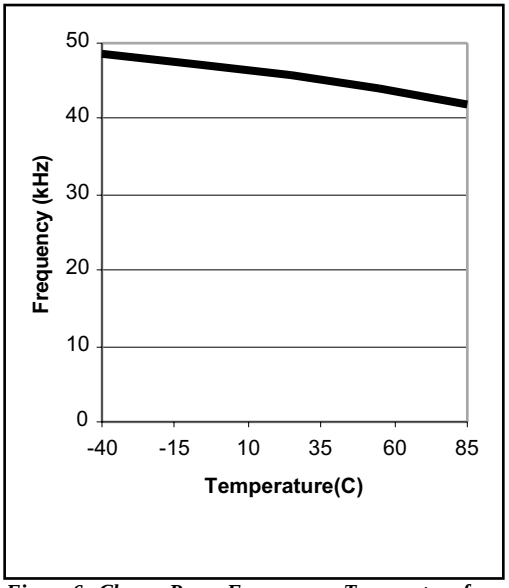


Figure 6. Charge Pump Freqency vs. Temperature for the SP6830

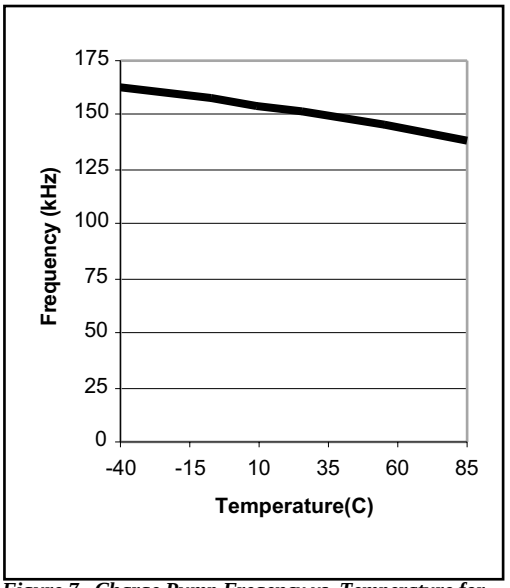


Figure 7. Charge Pump Freqency vs. Temperature for the SP6831

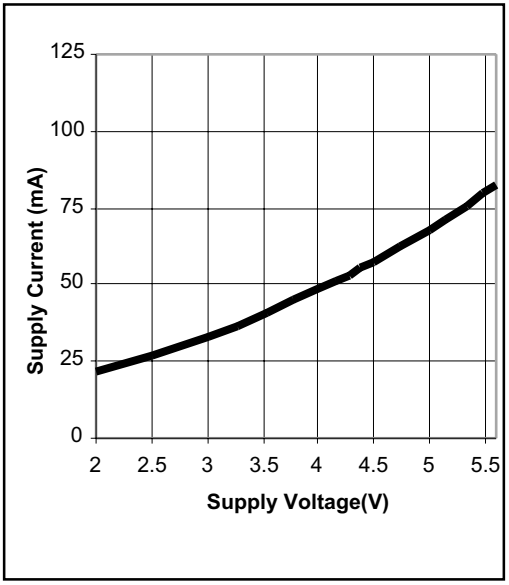


Figure 8. Supply Current vs. Supply Voltage for the SP6830

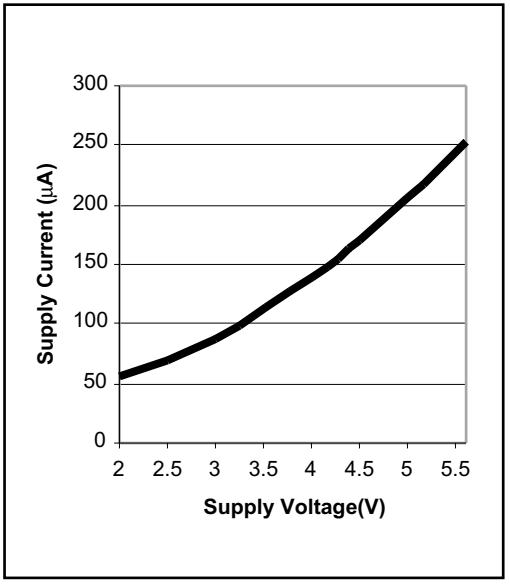


Figure 9. Supply Current vs. Supply Voltage for the SP6831

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

V_{IN} = +5.0V, C1 = C2 = C3 = 3.3µF for **SP6830**, C1 = C2 = C3 = 1µF for **SP6831**, and T_{AMB} = 25°C unless otherwise noted. The **SP6830/6831** devices use the circuit found in when obtaining the following typical performance characteristics (unless otherwise noted).

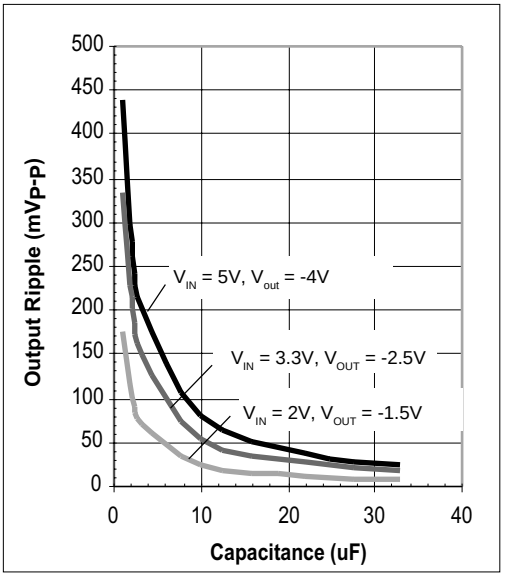


Figure 10. Output Voltage Ripple vs. Capacitance for the SP6830

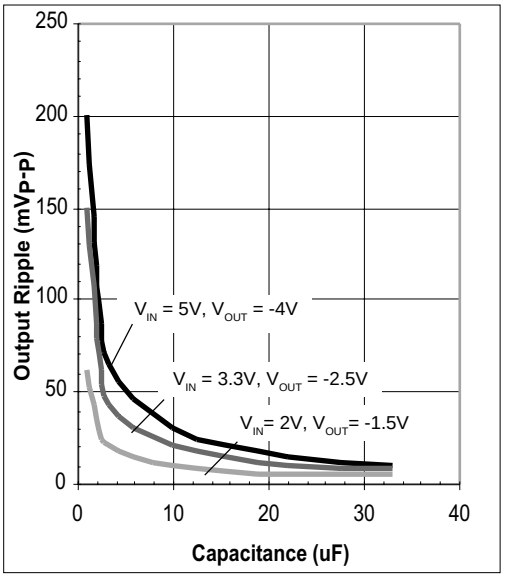


Figure 11. Output Voltage Ripple vs. Capacitance for the SP6831

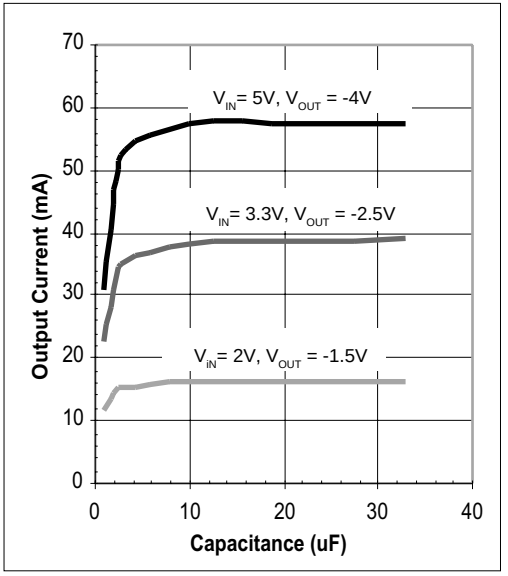


Figure 12. Output Current vs. Capacitance for the SP6830

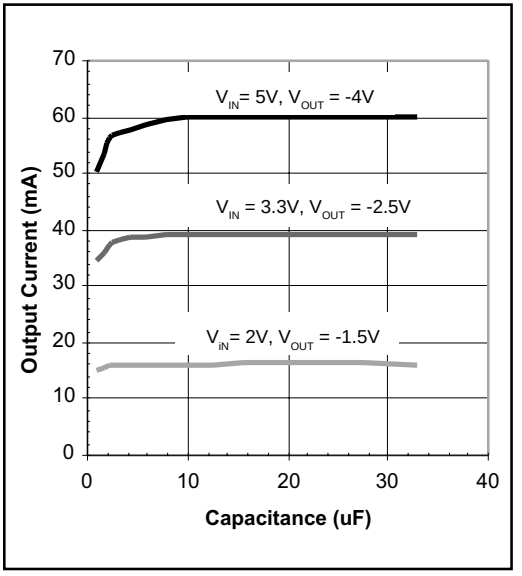


Figure 13. Output Current vs. Supply Voltage for the SP6831

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

V_{IN} = +5.0V, C1 = C2 = C3 = 3.3µF for **SP6830**, C1 = C2 = C3 = 1µF for **SP6831**, and T_{AMB} = 25°C unless otherwise noted. The **SP6830/6831** devices use the circuit found in when obtaining the following typical performance characteristics (unless otherwise noted).

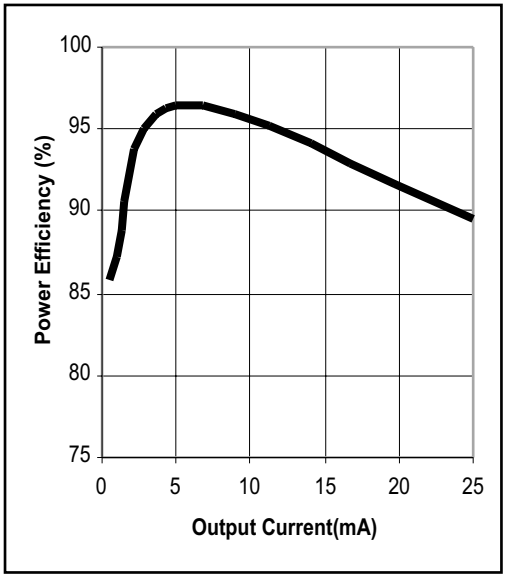


Figure 14. Power Efficiency vs. Output Current

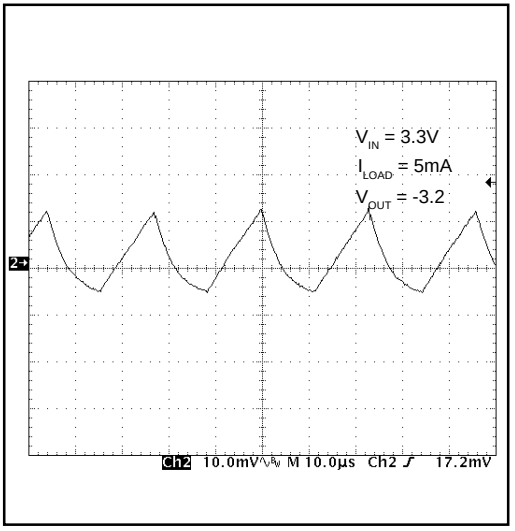


Figure 15. Output Noise and Ripple for the SP6830

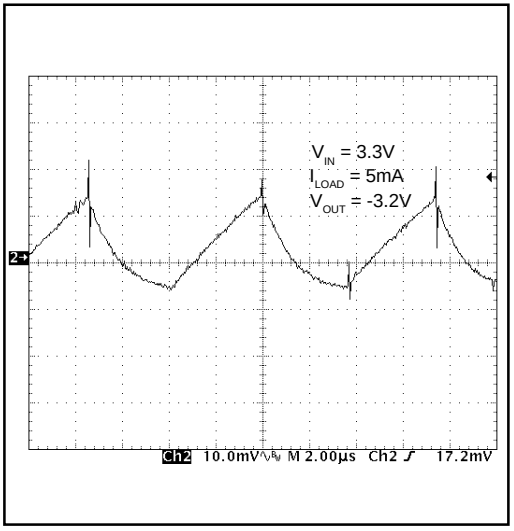


Figure 16. Output Noise and Ripple for the SP6831

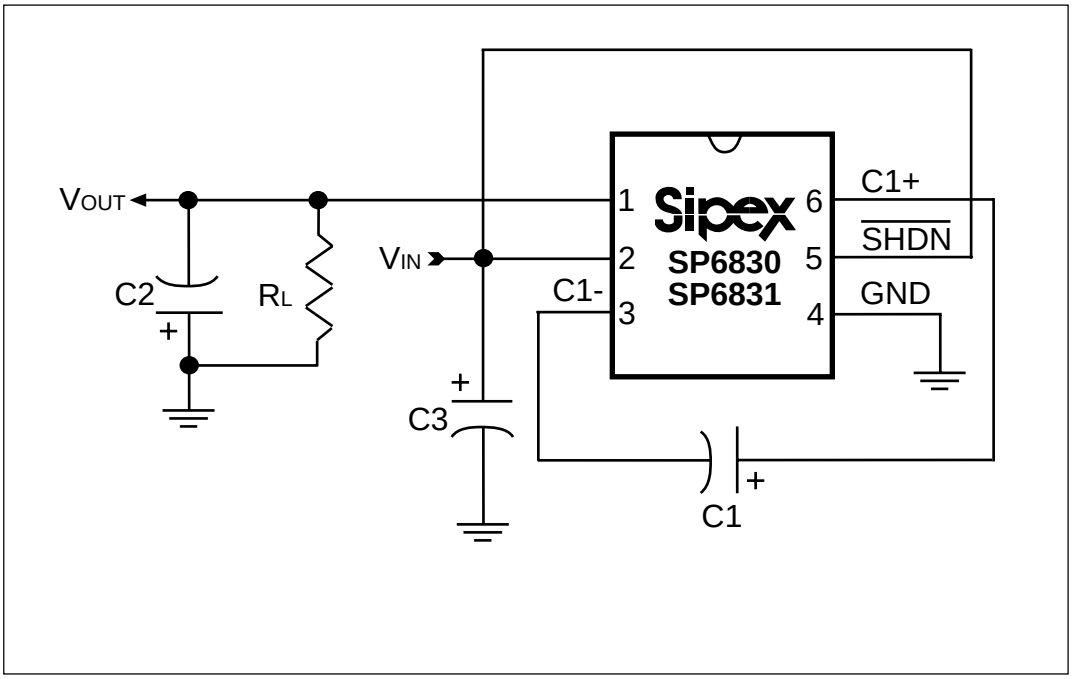


Figure 17: SP6830/6831 Connected as a Voltage Inverter in its Typical Operating Circuit; this Circuit Was Used to Obtain the Typical Performance Characteristics Found in Figures 2 Through 16 (unless otherwise noted)

DESCRIPTION

The SP6830/6831 devices are CMOS Charge Pump Voltage Converters that can be used to invert a +1.15V to +5.3V input voltage. These devices are ideal for designs involving battery-powered and/or board level voltage conversion applications.

The typical operating frequency of the SP6830 is 35kHz. The typical operating frequency of the SP6831 is 120kHz. The SP6830 has a typical operating current of 70µA and the SP6831 operates at 200µA. Both devices can output 25mA with a voltage drop of 500mV. The devices are ideal for LCD panel bias applications, cellular phones, pagers, PDAs, medical instruments, and other portable battery-powered equipment. The SP6830/6831 devices combine a high efficiency (>95% over most of its load-current range) with a low quiescent current.

THEORY OF OPERATION

The SP6830/6831 devices should theoretically produce an inverted input voltage. In real world applications, there are small voltage drops at the output that reduce efficiency. The circuit of an ideal voltage inverter can be found in *Figure 18.* The voltage inverters require two external capacitors to store the charge. A description of the two phases follows:

Phase 1

In the first phase of the clock cycle, switches S2 and S4 are opened and S1 and S3 closed. This connects the flying capacitor, C1, from V_{IN} to ground. C1 charges up to the input voltage applied at V_{IN}.

Phase 2

In the second phase of the clock cycle, switches S1 and S3 are opened and S2 and S4 are closed. This connects the flying capacitor, C1, in parallel with the output capacitor, C2. The charge stored in C1 is now transferred to C2. Simultaneously, the negative side of C2 is connected to V_{OUT} and the positive side is connected to ground. With the voltage across C2 smaller than the voltage across C1, the charge flows from C1 to C2 until the voltage at the V_{OUT} equals $-V_{IN}$.

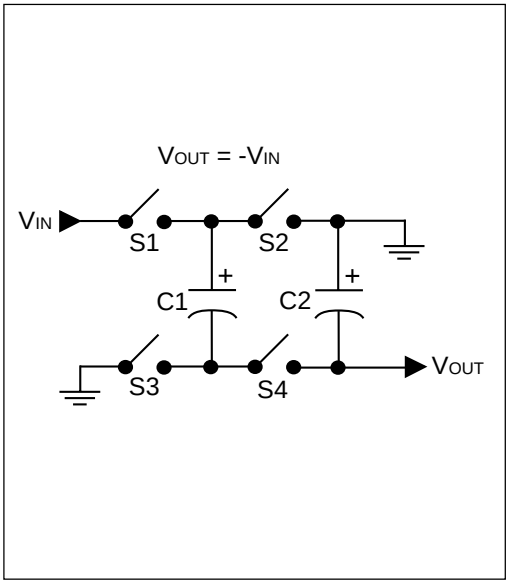


Figure 18. Circuit for an Ideal Voltage Inverter

Charge-Pump Output

The output of the SP6830/6831 devices is not regulated and therefore is dependent on the output resistance and the amount of load current. As the load current increases, losses may slightly increase at the output and the voltage may become slightly more positive. The loss at the negative output, V_{LOSS}, equals the current draw, I_{OUT}, from V_{OUT} times the negative converter's source resistance, R_S:

$$\mathbf{V_{LOSS} = I_{OUT} \times R_S.}$$

The actual inverted output voltage at V_{OUT} will equal the inverted voltage difference of V_{IN} and V_{LOSS}:

$$\mathbf{V_{OUT} = -(V_{IN} - V_{LOSS}).}$$

Efficiency

Theoretically, the total power loss of a switched capacitor voltage converter can be summed up as follows:

$$\mathbf{\sum P_{LOSS} = P_{INT} + P_{CAP} + P_{CONV},}$$

where P_{LOSS} is the total power loss, P_{INT} is the total internal loss in the IC including any losses in the MOSFET switches, P_{CAP} is the resistive loss of the charge pump capacitors, and P_{CONV} is the total

conversion loss during charge transfer between the flying and output capacitors. These are the three theoretical factors that may effect the power efficiency of the SP6830/6831 devices in designs.

Any internal losses come from the IC's on board circuitry. Losses in the IC can be induced by the input voltage, the frequency of the oscillator, and the ambient temperature. The most influential internal loss in the IC may be found in the power-on resistance of the internal MOSFET switches.

Any of the losses with the charge pump capacitors will be induced by the capacitor's ESR. The affects of the ESR losses and the output resistance can be found in the following equation:

$$I_{OUT}^2 \times R_{OUT} = P_{CAP} + P_{CONV}$$

and

$$R_{OUT} \approx 4 \times (2 \times R_{SWITCHES} + ESR_{C1}) + ESR_{C2} + \frac{1}{f_{OSC} \times C1},$$

where I_{OUT} it the output current, R_{OUT} is the circuit's output resistance, $R_{SWITCHES}$ is the internal resistance of the MOSFET switches, ESR_{C1} and ESR_{C2} are the ESR of their respective capacitors, and f_{OSC} is the oscillator frequency. This term with f_{OSC} is derived from an ideal switched-capacitor circuit as seen in *Figure 19*.

Any losses due to the conversion process will happen during the charge transfer between the flying capacitor, C1, and the output capacitor, C2, when there is a voltage difference between them. P_{CONV} can be determined by the following equation:

$$P_{CONV} = f_{OSC} \times [\ {}^1/_2 \times C1 \times (V_{IN}^2 - V_{OUT}^2) + {}^1/_2 \times C2 \times (V_{RIPPLE}^2 - 2V_{OUT}V_{RIPPLE})\ ].$$

Actual Efficiency

To determine the actual efficiency of the SP6830/6831 device operation, a designer can use the following equation:

$$\text{Efficiency (actual)} = \frac{P_{OUT}}{P_{IN}} \times 100\%,$$

where

$$P_{OUT} = V_{OUT} \times I_{OUT}$$

and

$$P_{IN} = V_{IN} \times I_{IN}$$

where P_{OUT} is the power output, V_{OUT} is the output voltage, I_{OUT} is the output current, P_{IN} is the power from the supply driving the SP6830/6831 devices, V_{IN} is the supply input voltage, and I_{IN} is the supply input current.

Ideal Efficiency

The ideal efficiency is not the true power efficiency because it does not involve the input power which includes the input current losses in the charge pump. The ideal efficiency can be determined with the following equation:

$$\text{Efficiency (ideal)} = \frac{P_{OUT}}{P_{OUT(IDEAL)}} \times 100\%,$$

where

$$P_{OUT(IDEAL)} = -V_{IN} \times \frac{-V_{IN}}{R_L},$$

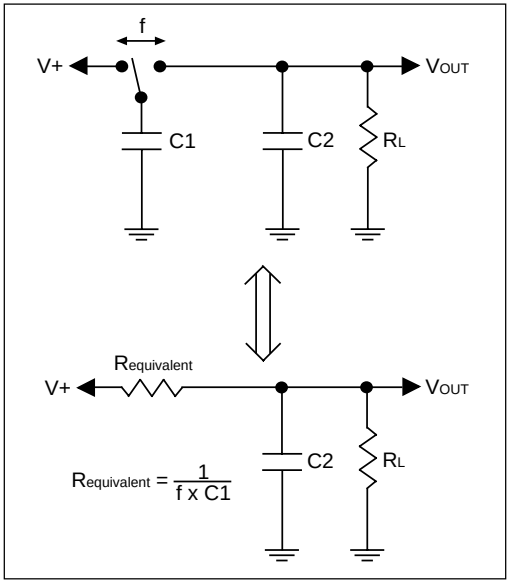


Figure 19. Equivalent Circuit for an Ideal Switched Capacitor

and P_{OUT} is the the power output. Both efficiencies are provided to designers for comparison.

APPLICATION INFORMATION

For the following applications, C1 = C2 = C3 = 3.3µF for the SP6830 and C1 = C2 = C3 = 1.0µF for the SP6831.

Capacitor Selection

Low ESR capacitors are needed to obtain low output resistance. Refer to *Table 1* for some suggested low ESR capacitors. The output resistance of the SP6830/6831 devices is a function of the ESR of C1 and C2. This output resistance can be determined by the equation previously provided in the **Efficiency** section:

$$R_{OUT} \approx 4 \times (2 \times R_{SWITCHES} + ESR_{C1}) + ESR_{C2} + \frac{1}{f_{OSC} \times C1},$$

where R_{OUT} is the circuit's output resistance, $R_{SWITCHES}$ is the internal resistance of the MOSFET switches, ESR_{C1} and ESR_{C2} are the ESR of their respective capacitors, and f_{OSC} is the oscillator frequency. This term with f_{OSC} is derived from an ideal switched-capacitor circuit as seen in *Figure 19*.

Minimizing the ESR of C1 and C2 will minimize the total output resistance and will improve the efficiency.

Flying Capacitor

Decreasing flying capacitor, C1, values will increase the output resistance of the SP6830/6831 devices while increasing C1 will reduce the output resistance. There is a point where increasing C1 will have a negligible effect on the output resistance due to the the domination of the output resistance by the internal MOSFET switch resistance and the total capacitor ESR.

Output Capacitor

Increasing output capacitor, C2, values will decrease the output ripple voltage. Reducing the ESR of C2 will reduce both output ripple voltage and output resistance. If higher output ripple can be tolerated in designs, smaller capacitance values for C2 should be used with light loads. The following equation can be used to calculate the peak-to-peak ripple voltage:

$$V_{RIPPLE} = 2 \times I_{OUT} \times ESR_{C2} + \frac{I_{OUT}}{f_{OSC} \times C2}.$$

Input Bypass Capacitor

The bypass capacitor at the input voltage will reduce AC impedance and the impact of any of the SP6830/6831 device's switching noise. It is recommended that for heavy loads a bypass capacitor approximately equal to the flying capacitor, C1, be used. For light loads, the value of the bypass capacitor can be reduced.

SIPEX PART NUMBER	MANUFACTURER/ TELEPHONE #	PART NUMBER	CAPACITANCE / VOLTAGE	MAX ESR @ 100kHz	CAPACITOR SIZE/TYPE
SP6830	KEMET / 864-963-6300	T494B335*020	3.3µF / 20V	1.5Ω	Case B / Tantalum
SP6830	SPRAGUE / 207-324-4140	595D335X0035	3.3µF / 35V	2.0Ω	Case C / Tantalum
SP6830	TDK / 847-803-6100	C3216X5R1A335K	3.3µF / 10V	0.04Ω	1206 / X5R
SP6831	AVX / 843-448-9411	0805ZC105K	1µF / 10V	0.04Ω	0805 / X7R
SP6831	KEMET/ 864-963-6300	C0805C105KRAC	1µF / 10V	0.05Ω	0805 / X7R
SP6831	TDK / 847-803-6100	C2012X5R1A105K	1µF / 10V	0.05Ω	0805 / X5R

Table 1. Suggested Low ESR Surface Mount Capacitors

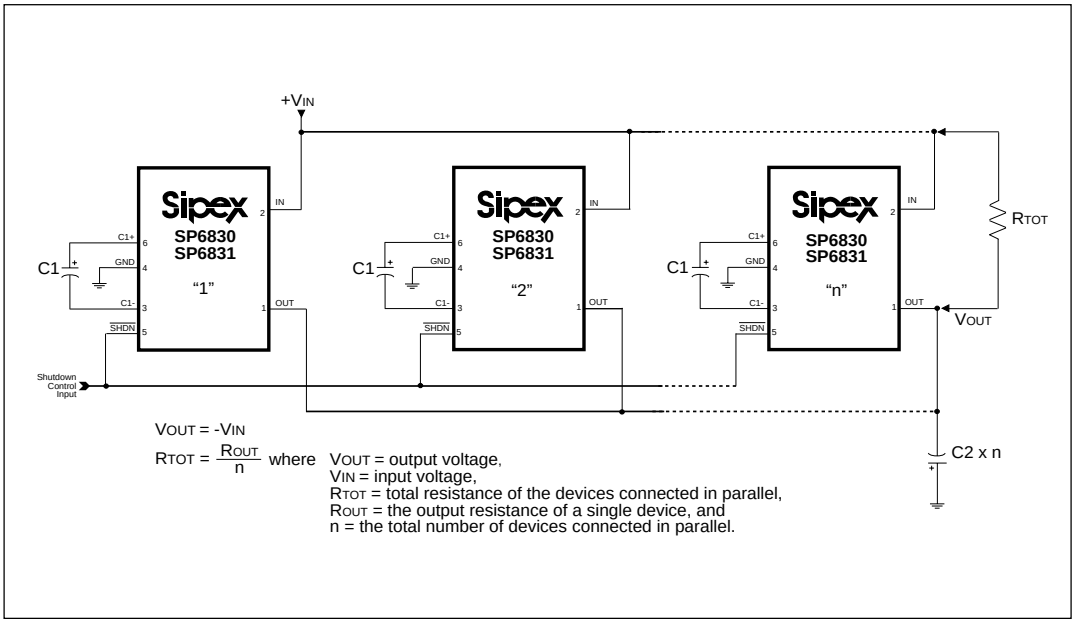


Figure 20. SP6830/6831 Devices Connected in Parallel to Reduce Total Output Resistance

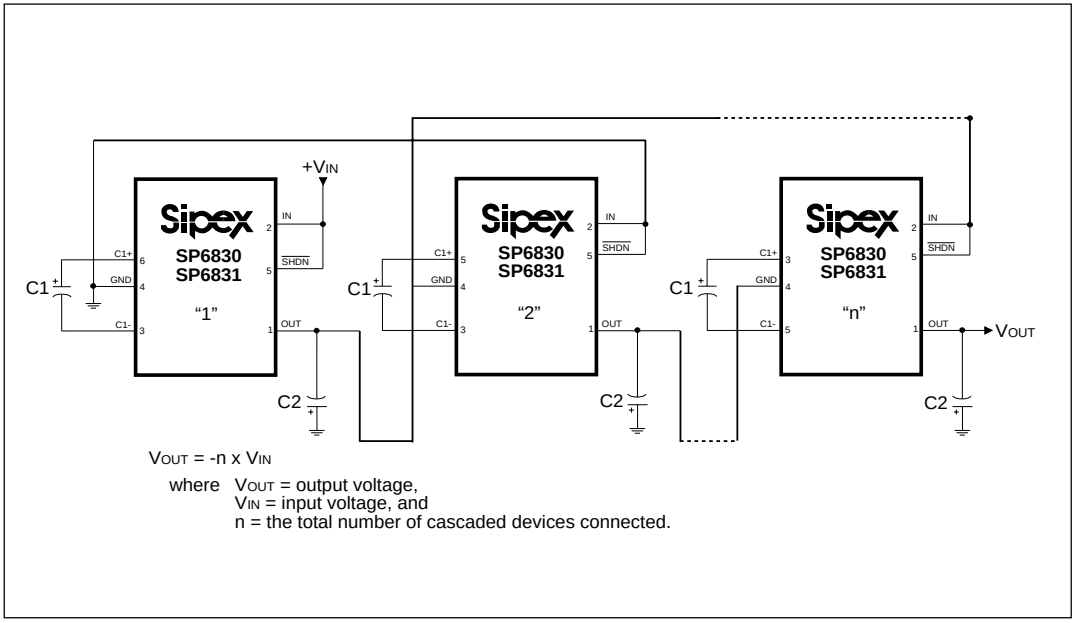


Figure 21. SP6830/6831 Devices Cascaded to Increase Output Voltage

When loading the SP6830/6831 devices from IN to OUT, the input current remains constant (disregarding any spikes due to internal switching). Implementing a 0.1µF bypass capacitor should be sufficient.

When loading the SP6830/6831 devices from OUT to GND, the current from the supply will switch from twice that of I_{OUT} and zero amperes. Designers should implement a large bypass capacitor (C3 = C1) if the supply has a high AC impedance.

Voltage Inverter

A designer can find the most common application for the SP6830/6831 devices in *Figure 17* as a voltage inverter. The only external components needed are 3 capacitors: the flying capacitor, C1, the output capacitor, C2, and the bypass capacitor, C3 (if necessary). This circuit is used to obtain the Typical Performance Characteristics found in *Figures 2* to *16* (unless otherwise noted).

Connecting in Parallel

A designer can parallel a number of SP6830/6831 devices to reduce the output resistance for specific designs. All devices will need their own flying capacitor, C1, but a single output capacitor will serve all of the devices connected in parallel by increasing the capacitance of C2 by a factor of n where n equals the total number of devices connected. This connection can be found in *Figure 20*.

Cascading Devices

A designer can cascade SP6830/6831 devices to produce a larger inverted voltage output. Refer to *Figure 21* for this circuit connection. With two cascaded devices, the unloaded output voltage is decreased by the output resistance of the first device multiplied by the quiescent current of the second device connected. The total output resistance is greatly increased when more than two devices are cascaded.

Driving Excessive Loads

The output should never be pulled above ground. A designer should implement a Schottky diode (1N5817) from OUT to GND when driving heavy loads where a higher supply is sourcing current into OUT. Refer to *Figure 22* for this circuit connection.

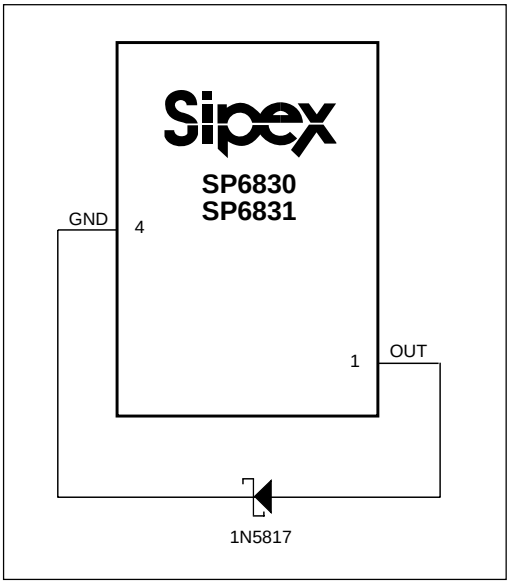


Figure 22. Protection for Heavy Loads

Combining a Doubler and Inverter Circuit

A designer can connect a SP6830/6831 device in a combination doubler/inverter circuit as seen in *Figure 23*. The doubler uses C3 and C4 while the inverter uses capacitors C1 and C2. Loading either output decreases both output voltages to GND because both the doubler and the inverter circuits use the charge pump. Designers should not allow the total current output from the doubler and the inverter to exceed 40mA.

Implementing Shutdown

The SP6830/6831 devices are enabled when the $\overline{SHDN}$ input pin is driven HIGH and disabled when driven LOW. This input must be tied to V_{IN} or GND to minimize any noise effects due to the internal switching of these devices. The $\overline{SHDN}$ input cannot be driven 0.5V above V_{IN} without the possibility of introducing significant current flows.

Layout and Grounding

Designers should make an effort to minimize noise by paying special attention to the circuit layout with the SP6830/6831 devices. External components should be connected in close proximity to the device and a ground plane should be implemented. This will keep electrical traces short minimizing parasitic inductance and capacitance.

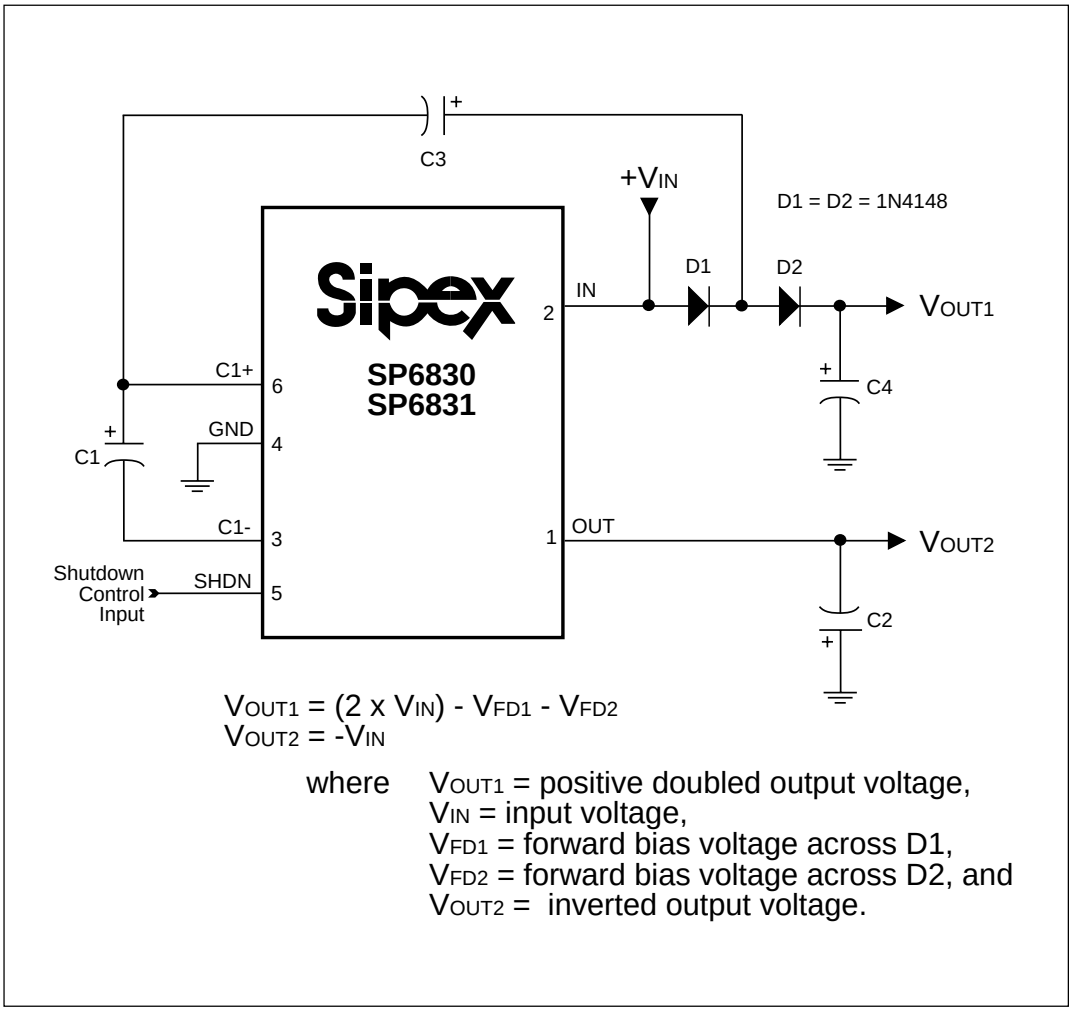
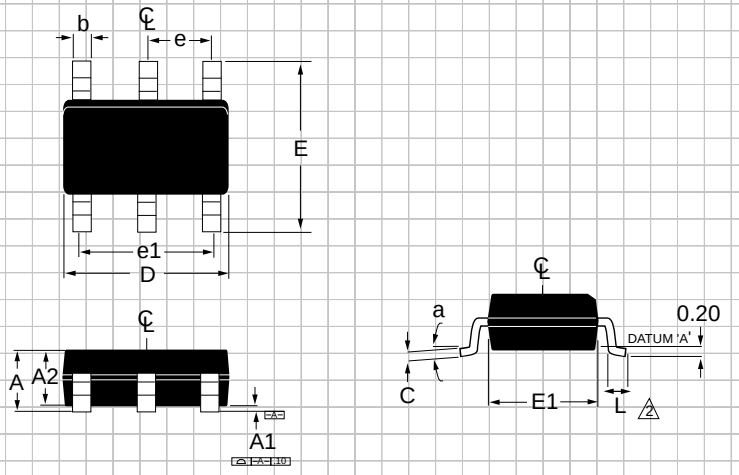


Figure 23. SP6830/6831 Device Connected in a Doubler/Inverter Combination Circuit

PACKAGE: SOT23-6



SYMBOL	MIN	MAX
A	0.90	1.45
A1	0.00	0.15
A2	0.90	1.30
b	0.25	0.50
C	0.09	0.20
D	2.80	3.10
E	2.60	3.00
E1	1.50	1.75
L	0.35	0.55
e	0.95ref	
e1	1.90ref	
a	0°	10°

ORDERING INFORMATION

Model	Temperature Range	Package Type
SP6830EK .	-40˚C to +85˚C	SOT23-6
SP6830EK/TR	-40˚C to +85˚C	SOT23-6
SP6831EK .	-40˚C to +85˚C	SOT23-6
SP6831EK/TR	-40˚C to +85˚C	SOT23-6

Please consult the factory for pricing and availability on a Tape-On-Reel option.

Available in lead free packaging. To order, add "-L" suffix to the part number.
Example: SP6660EU/TR=Tape & Reel. SP6660EU-L/TR = lead free.

SIGNAL PROCESSING EXCELLENCE

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