

DESCRIPTION

The fundamental of SP6026F synchronous rectifier (SR) driver IC is based on our U.S. patented methods that utilize the principle of "prediction" logic circuit. The IC deliberates previous cycle timing to control the SR in present cycle by "predictive" algorithm that makes adjustments to the turn-off time, in order to achieve maximum efficiency and avoid cross-conduction at the same time. Specially, SP6026F is designed for Resonance. It also maintains the MOSFET's body diode conduction at minimum level. The SP6026F is capable to adapt in almost all existing Resonance converters with few adjustments considered necessary.

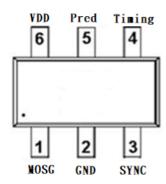
FEATURES

- Offers efficiency improvement over Schottky Diode.
- Low Standby Power to meet DOE Lot 6 requirement.
- Drives all Power MOSFET.
- Automatic detection DCM & CCM
- In DCM the current detection method is applied
- In CCM the prediction method is applied
- Minimum MOSFET body diode conduction.
- Operating frequency up to 200 KHz.
- Synchronize to transformer secondary voltage waveform.
- Minimum on time 1.8us (typical).
- External timing pin to adjust the falling slope

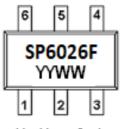
APPLICATIONS

- Switching Mode Power Supply
- Storage area network power supplies
- Telecommunication converters
- Embedded systems
- Industrial & commercial systems using high current processors
- Power converters to meet Lot 6 requirement

PIN CONFIGURATION (SOT-23-6L)



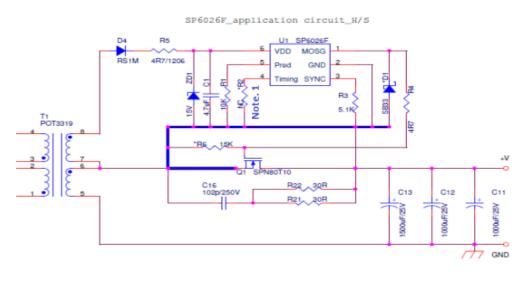
PART MARKING

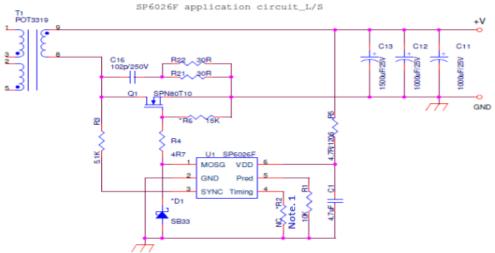


Y: Year Code W: Week Code



TYPICAL APPLCATION CIRCUIT





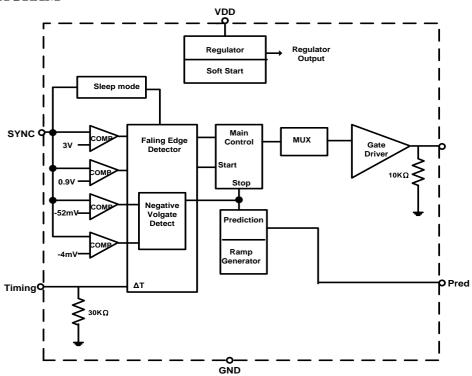
PIN DESCRIPTION

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Pin	Symbol	Description
1	MOSG	MOSFET gate drive.
2	GND	Ground connection.
3	SYNC	Synchronized signal from the VDS of SR MOSFET.
4	Timing	Discontinuous current filter timing adjustment resistor connection.
5	Pred	Capacitor to store previous cycle timing for SR MOSFET.
6	Vdd	DC supply voltage.

Note 1

^{*}The timing pin has an internal resistor of 30 K Ω , as shown in the block diagram Typically, the timing pin is NC pin. If a sharper falling edge of SYNC is required, an external resistor can be added.

BLOCK DIAGRAM



ORDERING INFORMATION

Part Number	Package	Part Marking		
SP6026FS26RGB	SOT-23-6L	SP6026F		

[※] SP6026FS26RGB: Tape Reel; Pb − Free; Halogen - Free

ABSOULTE MAXIMUM RATINGS (TA=25°C, unless otherwise specified.)

The following ratings designate persistent limits beyond which damage to the device may occur.

Symbol	Parameter	Value	Unit
V_{dd}	DC Supply Voltage	20	V
I_{OUT}	Peak Source Current (Pulsed)	1.0	A
	Peak Sink Current (Pulsed)	1.5	A
P_D	Power Dissipation @ $T_A=85^{\circ}C$ (*)	0.3	W
T_{J}	Operating Junction Temperature Range	-40 to125	$^{\circ}\mathbb{C}$
T_{STG}	Storage Temperature Range	-40 to 150	$^{\circ}\mathbb{C}$
T_{LEAD}	Lead Soldering Temperature for 5 sec.	260	

THERMAL RESISTANCE

Symbol	Parameter	Value	Unit
Rөjc	Thermal Resistance Junction – Case (*)	110	°C/W

^(*) The power dissipation and thermal resistance are evaluated under copper board mounted with free air conditions.

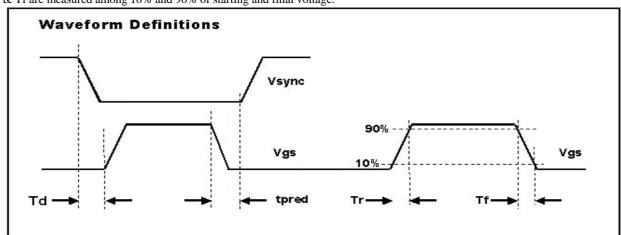


ELECTRICAL CHARACTERISTICS

 $(T_A=25^{\circ}\text{C}, V_{dd}=12\text{V}, \text{Freq.}=50 \text{ KHz}, \text{Duty Cycle}=50\%, \text{unless otherwise specified.})$

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
SUPPLY INP	UT					
Idd	Supply current	No load & Sleep mode		0.15		mA
		V _{SYNC} =0V, Vdd on		3		mA
Vdd	Supply voltage	Idd peak < 1A	4.2		18	V
Vdd on	Enable voltage			3.8		V
Vdd hysteresis	Enable voltage			0.25	0.5	V
SYNC REFE	RENCE (SYNC)	•				
Vshth	SYNC high threshold			3.0		V
Vslth	SYNC low threshold			0.9		V
Vsync	SYNC clamp voltage	Isync=3mA	Vdd+1.0			V
Vsync Sleep	SYNC sleep voltage	Pulse width >60 uS Vsync	3.5			V
Isync	SYNC input current				15	mA
REFERENCE	Voltage (V_Pred)					
V Pred				1.25		V
Control Circu	itry Section for Current detection	mode				
Vfwd	Vgnd-Vsync forward voltage			52		mV
, 1, v a	Vgnd-Vsync turn-off voltage			4		mV
TBon	Turn-on blanking time			1.8		uS
TDoff	Turn-off total delay	Vsync=Vgnd, CLOAD=4.7nF, RG=0Ω, VGS=2V		60		nS
MOSFET GA	TE DRIVER (MOSG)					
Voh	Output high voltage	Io = -200mA		10.8		V
Vol	Output low voltage	Io = 200mA		0.2		V
Vcl	Maximum Gate clamped voltage	Vdd=18V		15		V
Ton-max	MOSG maximum on time	Prediction mode		25		uS
Ton-min	MOSG minimum on time			1.8		uS
Td	Turn-on Propagation delay	No load,R_Pred=10KΩ		100		nS
Tpred	Dead time(prediction mode) in CCM	No load,R_Pred=10KΩ		750		nS
Tr	Rise time	Load = 1nF(*)		13		nS
Tf	Fall time	Load = 1nF(*)		7		nS

(*) Tr & Tf are measured among 10% and 90% of starting and final voltage.





TYPICAL CHARACTERISTICS (TA=25°C, unless otherwise specified.)

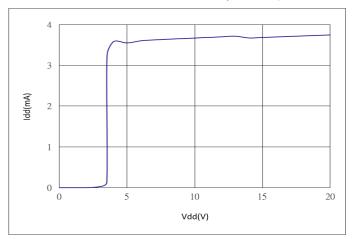


Figure 1: Supply Current vs Supply Voltage

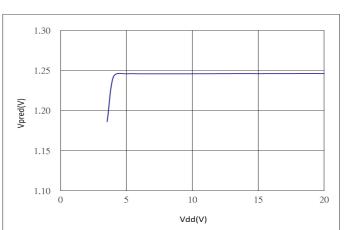


Figure 3: Pred Voltage vs Supply Voltage

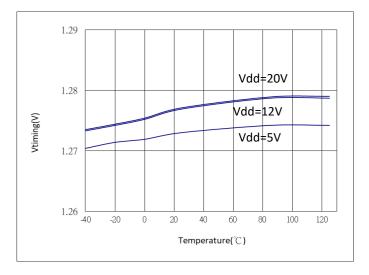


Figure 5: Timing Voltage vs Temperature

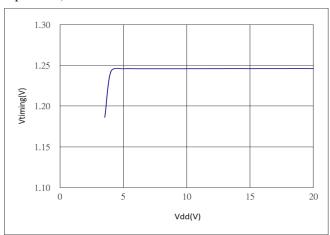


Figure 2: Timing Voltage vs Supply Voltage

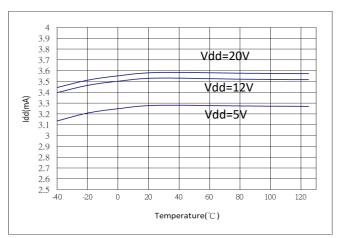


Figure 4: Supply Voltage vs Temperature

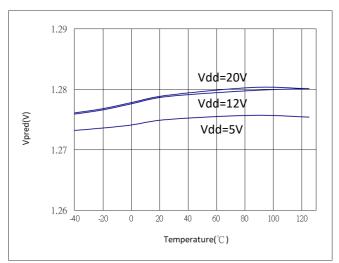
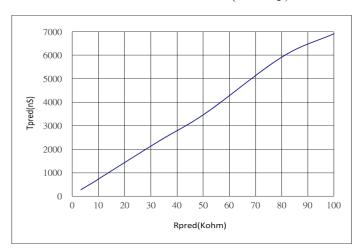


Figure 6: Pred Voltage vs Temperature

TYPICAL CHARACTERISTICS (TA=25°C, unless otherwise specified.)



500 450 400 350 250 250 150 150 0 1000 2000 3000 4000 5000 6000 7000 8000 9000 10000 C Load(pF)

Figure 7: Tpred vs Rpred

Figure 8: Output Rising Time vs Load Capacitor

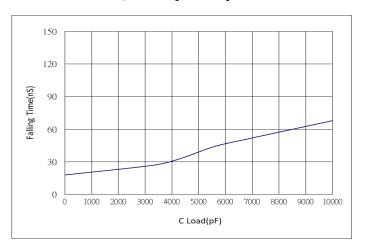


Figure 9 : Output Falling Time vs Load Capacitor



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