



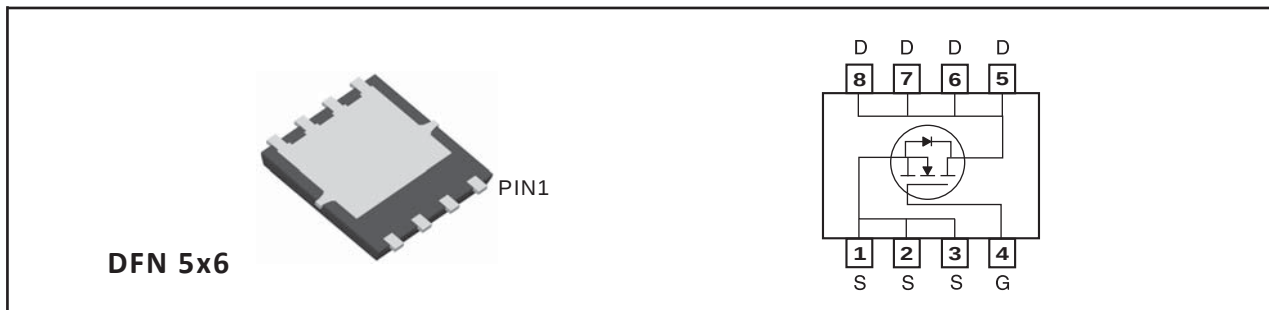
N-Channel Logic Level Enhancement Mode Field Effect Transistor

PRODUCT SUMMARY

V _{DSS}	I _D	R _{DS(ON)} (mΩ) Max
100V	48A	19 @ V _{GS} =10V

FEATURES

- Super high dense cell design for low R_{DS(ON)}.
- Rugged and reliable.
- Surface Mount Package.



ABSOLUTE MAXIMUM RATINGS (T_C=25°C unless otherwise noted)

Symbol	Parameter		Limit	Units
V _{DS}	Drain-Source Voltage		100	V
V _{GS}	Gate-Source Voltage		±20	V
I _D	Drain Current-Continuous ^c	Tc=25°C	48	A
		Tc=70°C	38.4	A
I _{DM}	-Pulsed ^{a c}		98	A
E _{AS}	Single Pulse Avalanche Energy ^d		132	mJ
P _D	Maximum Power Dissipation	Tc=25°C	83	W
		Tc=70°C	53	W
T _J , T _{STG}	Operating Junction and Storage Temperature Range		-55 to 150	°C

THERMAL CHARACTERISTICS

R _{θJC}	Thermal Resistance, Junction-to-Case	1.5	°C/W
------------------	--------------------------------------	-----	------

SP4510DG

Ver 1.0

ELECTRICAL CHARACTERISTICS (T_C=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
OFF CHARACTERISTICS						
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V , I _D =250uA	100			V
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} =80V , V _{GS} =0V			1	uA
I _{GSS}	Gate-Body leakage current	V _{GS} = ±20V , V _{DS} =0V			±100	nA
ON CHARACTERISTICS						
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =250uA	2.5	3.5	4.5	V
R _{DS(ON)}	Drain-Source On-State Resistance	V _{GS} =10V , I _D =24A		15	19	m ohm
g _{FS}	Forward Transconductance	V _{DS} =10V , I _D =24A		45		S
DYNAMIC CHARACTERISTICS ^b						
C _{ISS}	Input Capacitance	V _{DS} =25V, V _{GS} =0V f=1.0MHz		1460		pF
C _{OSS}	Output Capacitance			570		pF
C _{RSS}	Reverse Transfer Capacitance			65		pF
SWITCHING CHARACTERISTICS ^b						
t _{D(ON)}	Turn-On DelayTime	V _{DD} =50V I _D =1A V _{GS} =10V R _{GEN} = 2.5 ohm		10		ns
t _r	Rise Time			12		ns
t _{D(OFF)}	Turn-Off DelayTime			16		ns
t _f	Fall Time			7		ns
Q _g	Total Gate Charge	V _{DS} =50V, I _D =24A, V _{GS} =10V		25		nC
Q _{gs}	Gate-Source Charge	V _{DS} =50V, I _D =24A, V _{GS} =10V		8.4		nC
Q _{gd}	Gate-Drain Charge			7.8		nC
DRAIN-SOURCE DIODE CHARACTERISTICS						
V _{SD}	Diode Forward Voltage	V _{GS} =0V, I _S =8A		0.82	1.3	V
Notes						
a.Pulse Test:Pulse Width ≤ 10us, Duty Cycle ≤ 1%.						
b.Guaranteed by design, not subject to production testing.						
c.Drain current limited by maximum junction temperature.						
d.Starting T _J =25°C, L=0.5mH, V _{DD} = 50V.(See Figure13)						
e.Mounted on FR4 Board of 1 inch ² , 2oz.						

Dec,08,2016

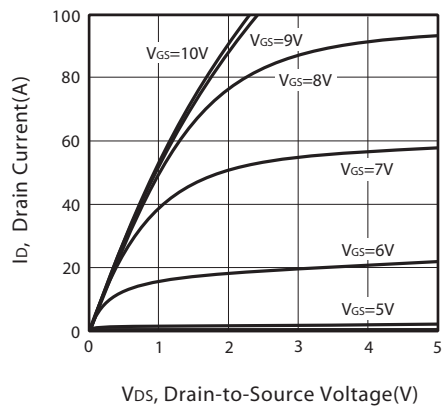


Figure 1. Output Characteristics

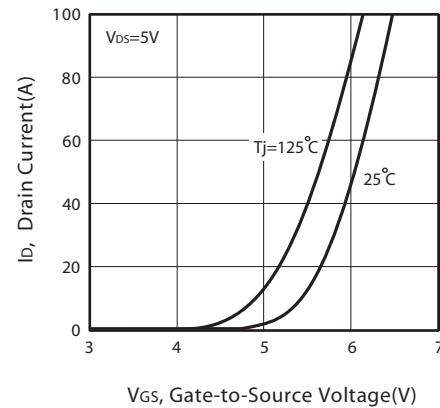


Figure 2. Transfer Characteristics

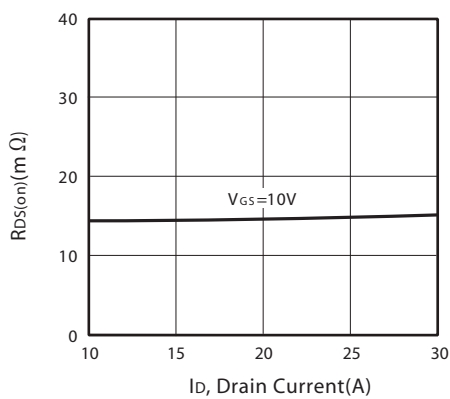


Figure 3. On-Resistance vs. Drain Current and Gate Voltage

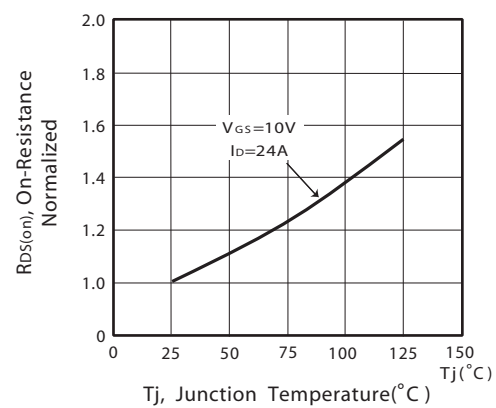


Figure 4. On-Resistance Variation with Drain Current and Temperature

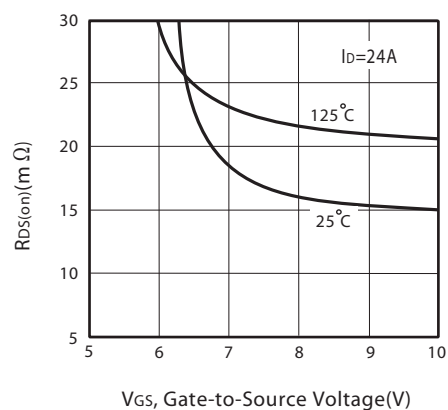


Figure 5. On-Resistance vs. Gate-Source Voltage

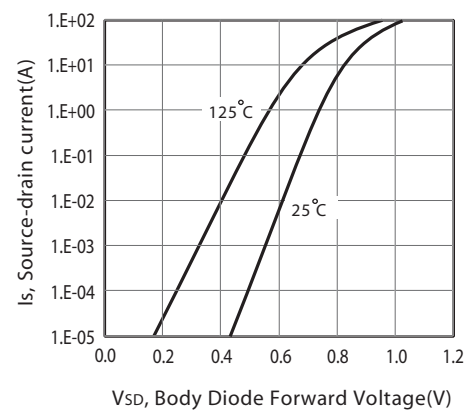


Figure 6. Body Diode Forward Voltage Variation with Source Current

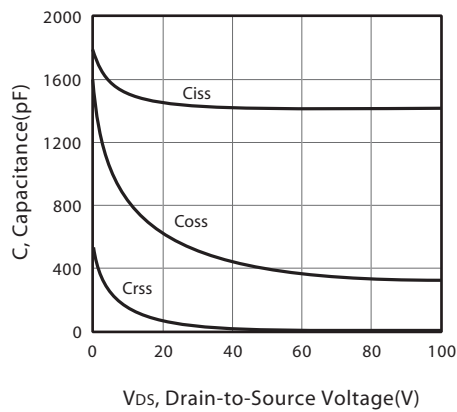


Figure 7. Capacitance

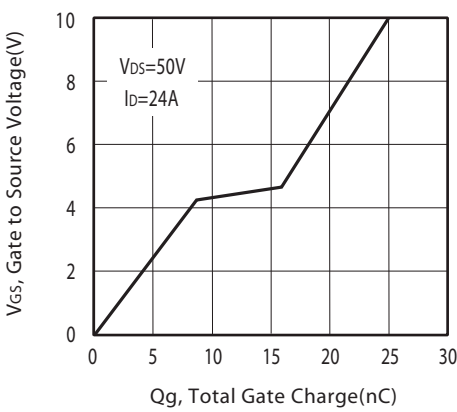


Figure 8. Gate Charge

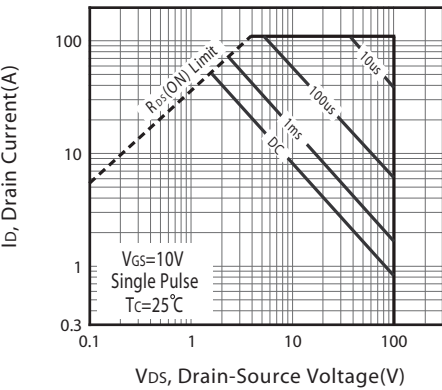
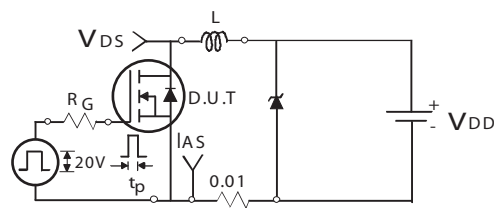
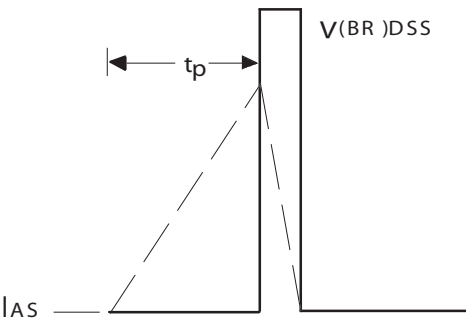


Figure 9. Maximum Safe Operating Area



Unclamped Inductive Test Circuit

Figure 13a.



Unclamped Inductive Waveforms

Figure 13b.

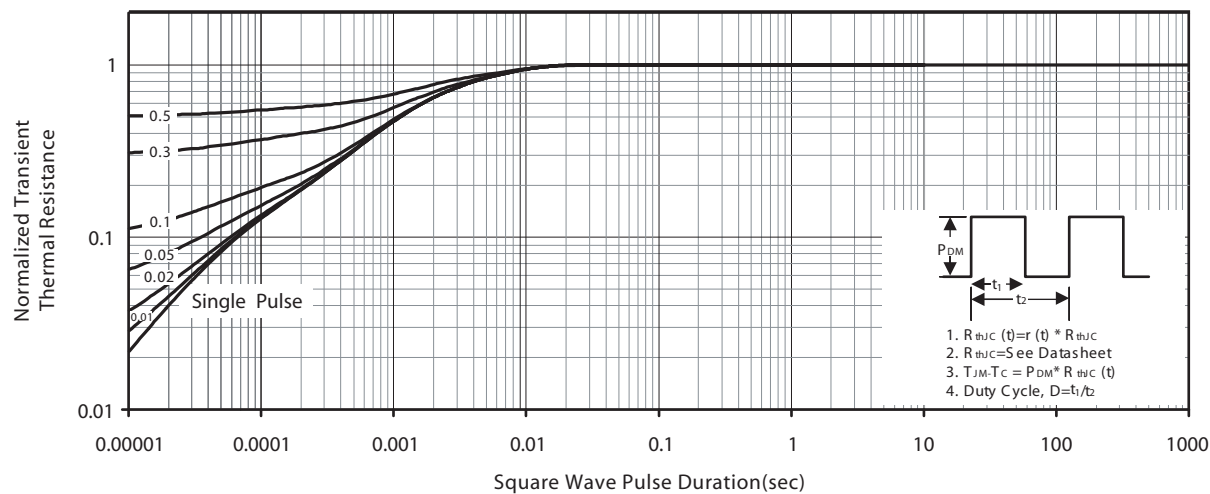
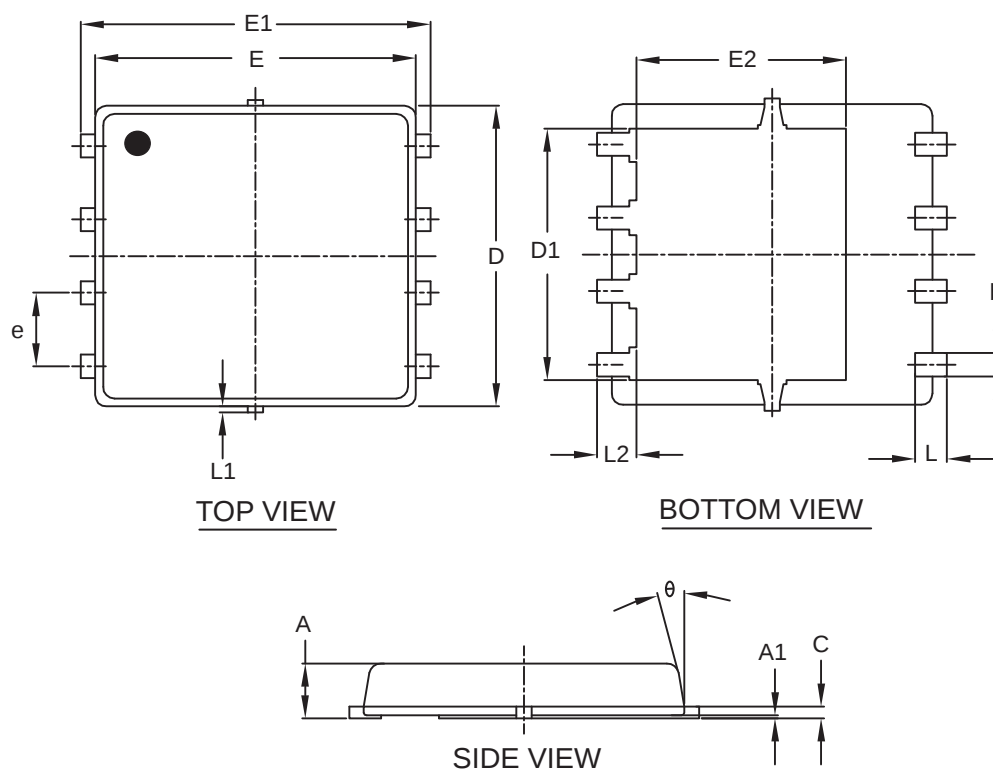


Figure 14. Normalized Thermal Transient Impedance Curve

PACKAGE OUTLINE DIMENSIONS

DFN 5x6-8L



SYMBOLS	MILLIMETERS		
	MIN	NOM	MAX
A	0.85	0.95	1.00
A1	0.00	—	0.05
b	0.30	0.40	0.50
c	0.15	0.20	0.25
D	5.20 BSC		
D1	4.35 BSC		
E	5.55 BSC		
E1	6.05 BSC		
E2	3.62 BSC		
e	1.27 BSC		
L	0.45	0.55	0.65
L1	0.00	—	0.15
L2	0.68 REF		
θ	0°	—	10°

TOP MARKING DEFINITION

