OPTICAL ID IMAGE Decoder [2nd generation]

- two_wire_interface version

1. General Description

SN9P701 is the second generation of OID decoder. It is designed for implementing SONiX newly developed D.H.R.T. Technology (Data Hiding & Retrieving Technology), which integrates the solution that includes CMOS sensor interface, image pattern recognizing engine, voltage regulator, RC oscillator and retrieved index output interface.

2. Feature of SN9P701

- Support dot pattern format : OID_Code_v2
- Core voltage operation range : 3.0V ~ 3.6V (Reference design)
- Regulator input : 3.6V ~5.0V (Reference design)
- Low power dissipation : 5mA (typ)
- Shot down current : <10uA
- Embedded 16 bit-DSP for sensor control and image pattern recognition
- Light source timing control
- Built-in voltage regulator
- Built-in 16Mhz RC type oscillator (not recommended in RF/IR version)
- Built-in low battery detection
- Bi-directions communication in two wire serial interface
- Output Optical_ID in two_wire_serial_interface
  (Please refer to two_wire_interface_v2.pdf)
- 48 pin LQFP package.

3. Feature of OID_Code_V2

OID_Code_V2 is the 2nd generation of dot pattern used in OID system.

- Dimension of single dot pattern : 1.3mm x 1.3mm
- Number of index : 65,536（can extend to 262,144）
- Low visual artifact
- Low visual fixed pattern noise
- Suggested paper type :art coated paper, mid-grade paper*

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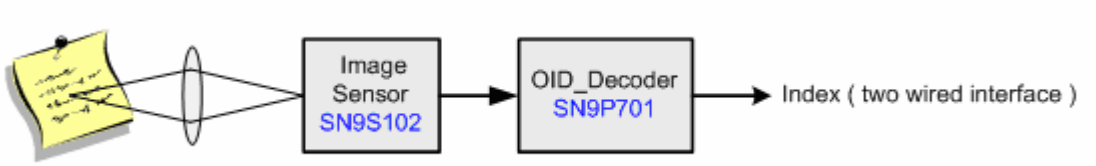
4. Specification of 2nd generation OID decoding system

The 2nd generation OID decoding system is a low cost active detection module that provides a non-platform positioning engine for implementing Optical ID system, which reads the dot pattern on printed media by optically acquiring the surface image and translates the dot pattern into digits. The acquiring module includes the SONiX CMOS Image Sensor, an Image Decoder and a set of optical components (a lens, two light sources, housing & case) to provide a complete and compact Optical ID sensing engine. This sensing engine is a small stand alone module. It has no platform and requires no cable (wireless version) enabling it to be highly flexible and mobile.



- Supported dot pattern format: OID_Code_v2
- Hit rate : 98% (typ)
- Error rate : < 0.1% (typ)
- Illumination range of environment : 0 ~ 10,000 Lux
- Maximum scan speed : 3cm/sec
- Response time: 100ms(typ), controlled by internal firmware automatically.
  It can be also configured to 50ms via two wire interface.
  (please refer to AN9P701_01 for detail setting)
- Tilt sensing range : – 45° ~ +45° (typ)／ – 30° ~ +30° (guaranteed)
- Sensing distance between paper and tip of pen (@ tilt angle= 0°) : 0 ~ 2.0mm
- Support dot pattern printed by office-use 1200dpi laser printer for verification purpose
  (ex: Epson:N2120, HP 4000 series...)
- System power dissipation
  operating current (off／on paper) : 3mA／6mA (typ)
  shot down current : < 30uA (typ)
- Low battery detection
- Supply voltage : 3.6V ~5.0V (Reference design)
- Bi-directions communication via two_wire_interface_v2
- Output Optical Index via two_wire_interface_v2
- Selectable OSC type : RC type or X'tal type.

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5. Comparison table of OID_Decoding_System v2 & v1

ITEMS		OID_Decoding_System V2	OID_Decoding_System V1
Lens module		Version_2	Version_1
OID Decoder		SN9P701-001	SN9P700
Sensor		SN9S102C	SN9S100C／SN9S102C
Graphic Code (Dot Pattern)	**Version**	OID_Code_V2.0	OID_Code_V1.0
	Indexes	0~ 65,535	0~ 4,096
	Graphic Code Size	~ 1.3mm x 1.3mm	~ 0.5mm x 0.42mm
	Visual Artifact	~ 25% of (OID_Code_V1)	Low
Paper type	**Art coated paper**	Yes	Yes
	Mid- grade paper	Yes (ex: A4 grade paper for printer)	NA
	Low grade paper	TBD	NA
Verified by Office-use laser printer		Yes, (ex:Epson, EPL-N2120)	NA
***Hit Rate (typical)**		98%	—
***Error Rate (typical)**		< 0.1%	< 1%
***Illumination range of environment**		0 ~ 10,000 Lux	0 ~ 3,000 Lux
***Tilt angle (typical)**		–45°~ +45°	–40°~ +40°
***Sensing range between paper and tip of pen (@ tilt angle= 0°)**		0 ~ 2.0mm	0 ~ 1.0mm
***System operating current (off page)**		3mA	13mA
***System operating current (on page)**		6mA	15mA
Shot down current		< 10uA	< 10uA
Linear regulator		Built in	NA
RC OSC／Crystal OSC		Built in／Built in	NA／Built in
Low battery detection		Built in	NA
Package		LQFP 48 pin	LQFP 32 pin
Package (None-RoHS／RoHS)		SN9P701／SN9P701G	SN9P700A／SN9P700AG

Note: *Please check SONiX for detail test conditions

6. Pin Assignment

LQFP 48	PIN NAME	Type	Description
1	KEY1	I	KEY1 input（internal pull down）, connect to ground if no used
2	GPIO0	B	General purpose I/O
3	GPIO1	B	General purpose I/O
4	GPIO2	B	General purpose I/O
5	VDD3	P	Digital VDD, 3.3V
6	GND	P	Digital ground
7	GPIO3	B	General purpose I/O
8	ADIO2	B	ADIO2/ADO_SDIO/IR_TRAN/RF_TRAN
9	ADIO0	B	ADIO0/ADO_CLK
10	VSSD_OSC	P	GND for oscillator
11	RC_BIAS	P	RC oscillator bias, using an external “R” to set frequency. Recommended “R” = 29KΩ±1% for 16MHz ±10% frequency.
12	VDD_OSC	P	VDD for oscillator, 3.3V
13	XIN	I	Crystal OSC input
14	XOUT	B	Crystal OSC output
15	XTAL_SEL	I	OSC type selection (1:Crystal, 0:RC)
16	VDD3	P	Digital VDD, 3.3V
17	GND	P	GND for I/O and core
18	TAVSS	P	Reserved, please connect to digital GND
19	DN	B	Reserved, please connect 5KΩ to digital GND
20	DP	B	Reserved, please connect 5KΩ to digital VDD, 3.3V
21	TAVDD	P	Reserved, please connect to digital VDD, 3.3V
22	VRO_S	O	Regulator 3.3 v switch output, controlled by internal firmware
23	VRO_P	O	Regulator 3.3 v output, controlled by REG_EN
24	GND_A	P	Analog ground
25	REG_IN	P	Regulator input , 3.6V~5V
26	REG_EN	I	Regulator enable
27	PWR_CTL	O	Output for power control
28	VDD5D	P	Digital VDD, 3.6V~5V, please do not connect to VRO_P
29	ADIO1	B	ADIO1/ADO_SCK
30	USB_DET	I	Reserved, please connect to ground

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31	KEY0	I	KEY0 input（internal pull down）
32	BAT_SW	O	Switch for battery voltage detection
33	BAT_DET	I	Low voltage detection input. Voltage applied to pin BAT_DET is compared with internal threshold level (VDD3)／3 and reports result via two wire interface every 10 sec.
34	RST	B	Chip reset（internal pull down）
35	TEST	I	Test pin for IC test, please connect to ground
36	KEY2	I	KEY2 input（internal pull down）, connect to ground if not used
37	VDD	I	Digital VDD, 3.3V
38	GND	P	Digital ground
39	SEN_CMD	B	Sensor control interface, connect to SN9S102C directly
40	SEN_CLK	O	Sensor clock, connect to SN9S102C directly
41	SEN_D0	I	Sensor image data input, connect to SN9S102C directly
42	SEN_D1	I	Sensor image data input, connect to SN9S102C directly
43	OP_GND	P	Analog ground
44	IRED1	O	Output for IRED_1 control
45	IRED_FEB1	I	Voltage feedback for IRED1 control
46	IRED_FEB0	I	Voltage feedback for IRED0 control
47	IRED0	O	Output for IRED_0 control
48	OP_VDD	P	Analog VDD, 3.3V

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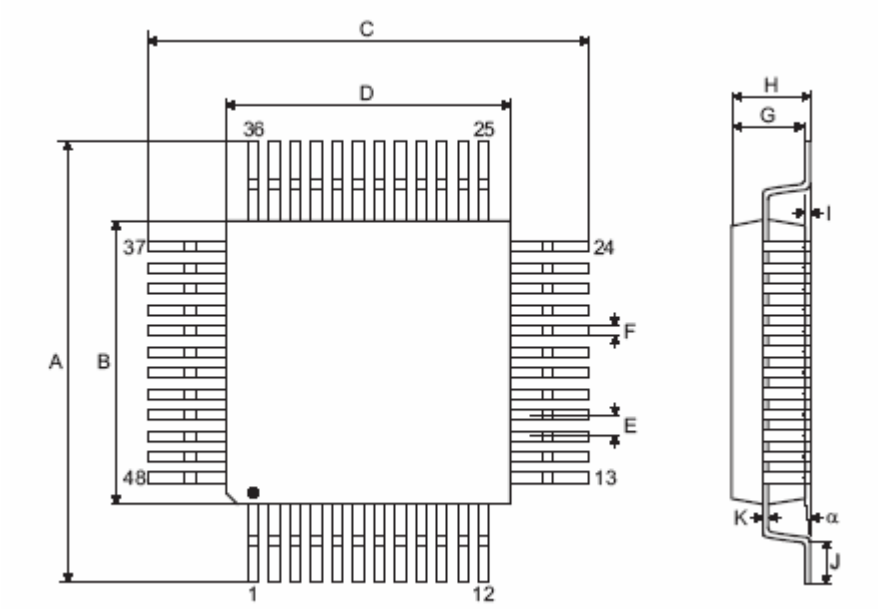
7. Package Information



Symbol	Dimensions in mm		
	Min.	Nom.	Max.
A	8.9	—	9.1
B	6.9	—	7.1
C	8.9	—	9.1
D	6.9	—	7.1
E	—	0.5	—
F	—	0.2	—
G	1.35	—	1.45
H	—	—	1.6
I	—	0.1	—
J	0.45	—	0.75
K	0.1	—	0.2
α	0°	—	7°

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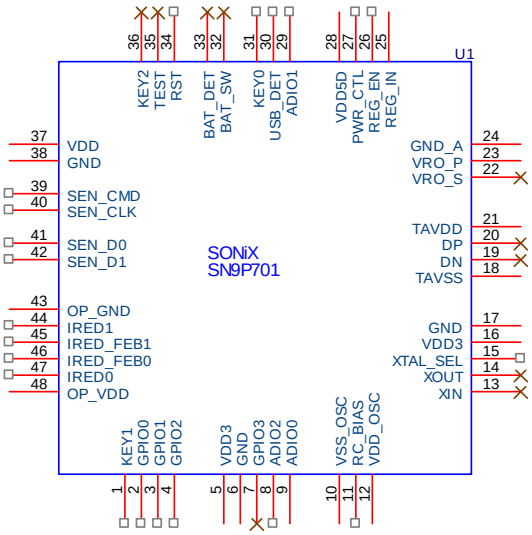
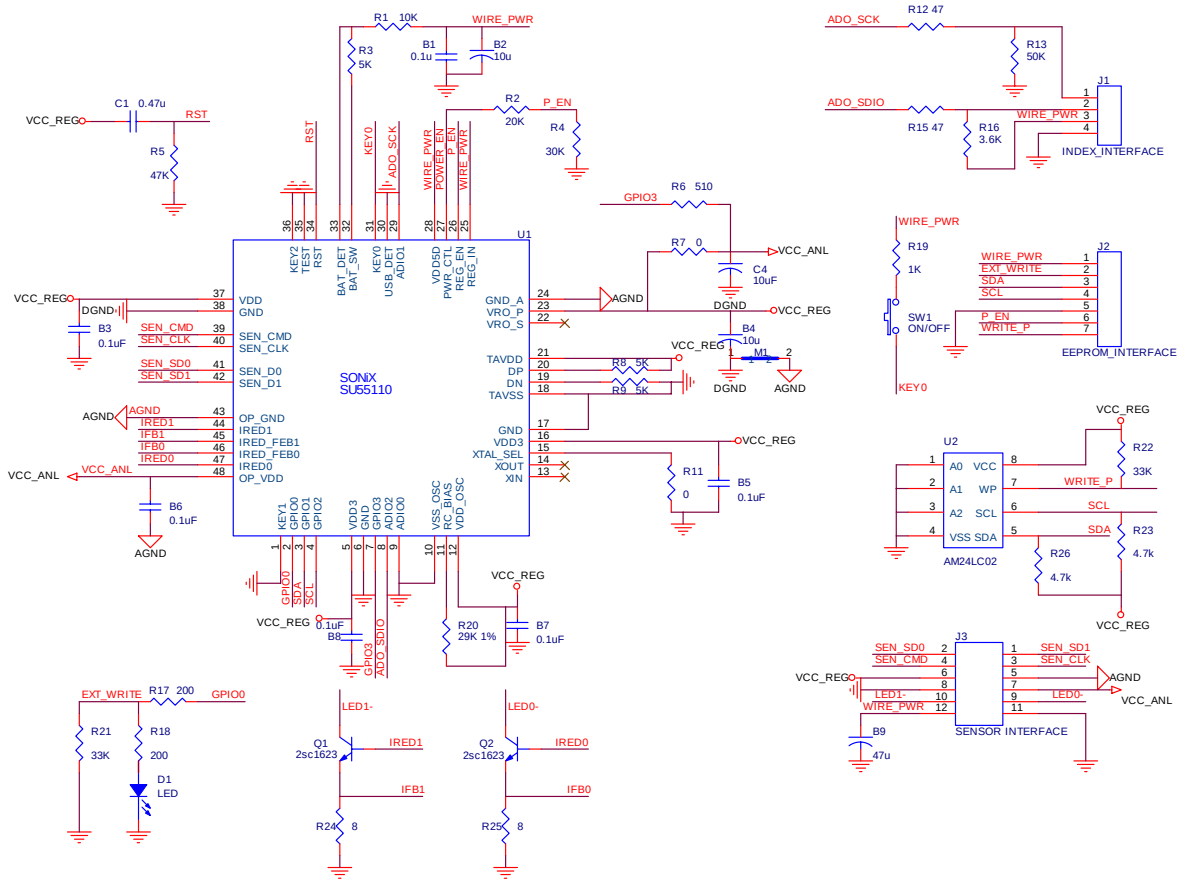
8. Reference Design (for reference purposes only)





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